

MOSFET - Power, Single N-Channel, STD Gate, SO8FL

40 V, 4.7 mΩ, 66 A

NVMFWS004N04XM

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5x6 mm) for Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	40	V
Gate-to-Source Voltage	DC V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation	$T_C = 25^\circ\text{C}$ P_D	38	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$ I_{DM}	332	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	32	A
Single Pulse Avalanche Energy ($I_{PK} = 32 \text{ A}$)	E_{AS}	68	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

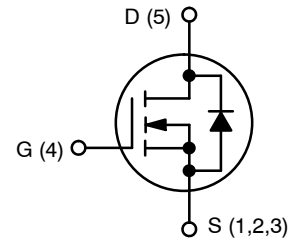
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

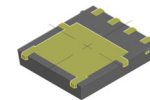
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	3.9	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	42	

1. Surface-mounted on FR4 board using 650 mm², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

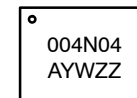
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	4.7 mΩ @ 10 V	66 A



N-CHANNEL MOSFET



DFNW5 (SO-8FL)
CASE 507BA



004N04 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
NVMFWS004N04XMT1G	DFN5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFWS004N04XM

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	40	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D = 1 mA, Referenced to 25°C	–	15	–	mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, T _J = 25°C	–	–	10	μA
		V _{DS} = 40 V, T _J = 125°C	–	–	100	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A, T _J = 25°C	–	4.1	4.7	mΩ
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 30 μA, T _J = 25°C	2.5	–	3.5	V
Gate Threshold Voltage Temperature Coefficient	ΔV _{GS(TH)} /ΔT _J	V _{GS} = V _{DS} , I _D = 30 μA	–	–7.29	–	mV/°C
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 10 A	–	45.5	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	669	–	pF
Output Capacitance	C _{OSS}		–	431	–	
Reverse Transfer Capacitance	C _{RSS}		–	9.4	–	
Total Gate Charge	Q _{G(TOT)}	V _{DD} = 32 V, I _D = 30 A, V _{GS} = 10 V	–	10.6	–	nC
Threshold Gate Charge	Q _{G(TH)}		–	2.0	–	
Gate-to-Source Charge	Q _{GS}		–	3.2	–	
Gate-to-Drain Charge	Q _{GD}		–	2.1	–	
Gate-Resistance	R _G	f = 1 MHz	–	1.6	–	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(ON)}	Resistive Load, V _{GS} = 0/10 V, V _{DD} = 32 V, I _D = 30 A, R _G = 0 Ω	–	11.9	–	ns
Rise Time	t _r		–	4.0	–	
Turn-Off Delay Time	t _{d(OFF)}		–	17.2	–	
Fall Time	t _f		–	3.6	–	

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V, T _J = 25°C	–	0.8	1.2	V
		I _S = 10 A, V _{GS} = 0 V, T _J = 125°C	–	0.7	–	
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 30 A, di/dt = 100 A/μs, V _{DD} = 32 V	–	28	–	ns
Charge Time	t _a		–	11	–	
Discharge Time	t _b		–	17	–	
Reverse Recovery Charge	Q _{RR}		–	9.5	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

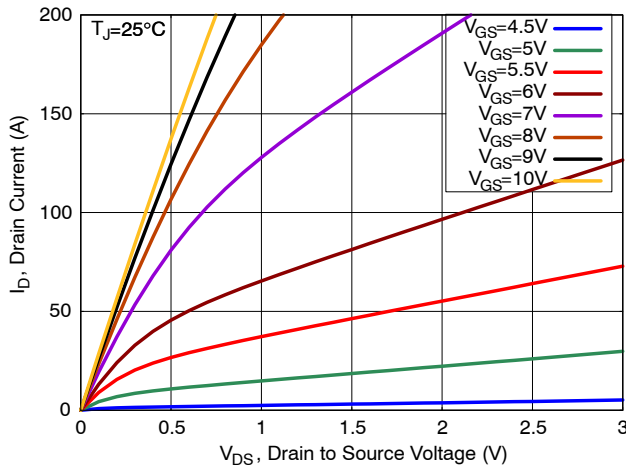


Figure 1. On-Region Characteristics

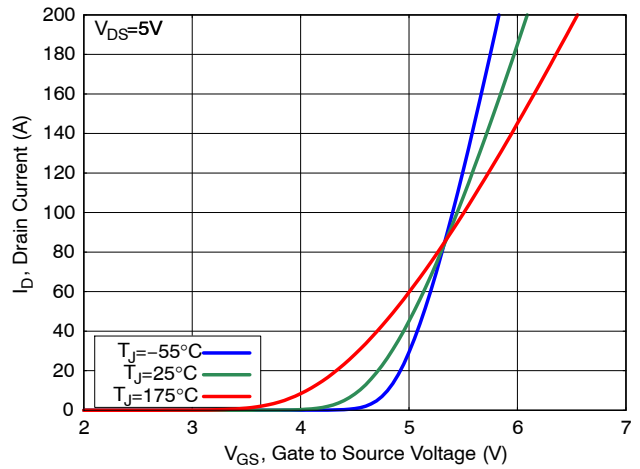


Figure 2. Transfer Characteristics

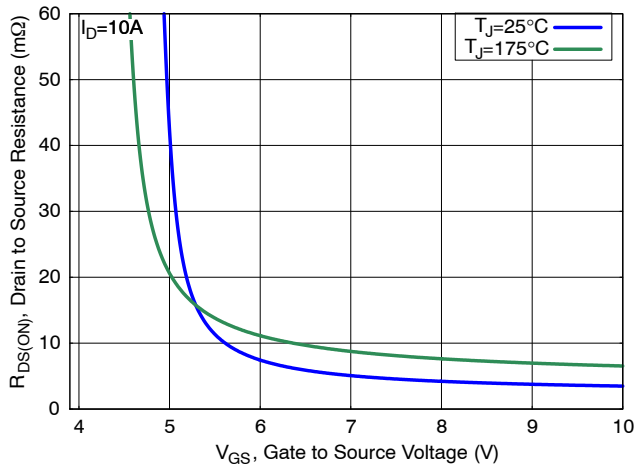


Figure 3. On-Resistance vs. Gate Voltage

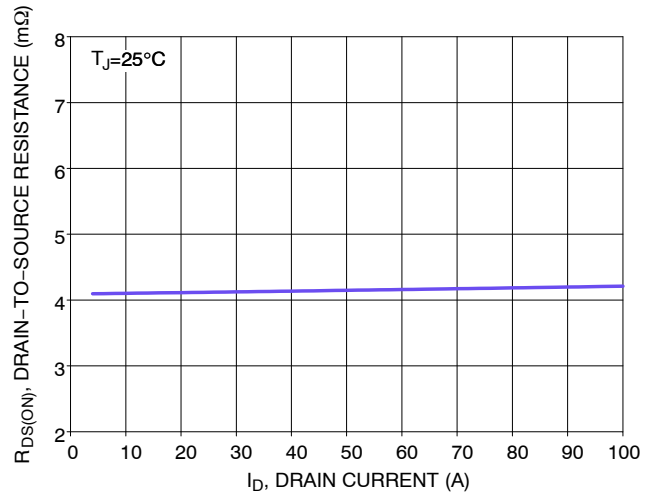


Figure 4. On-Resistance vs. Drain Current

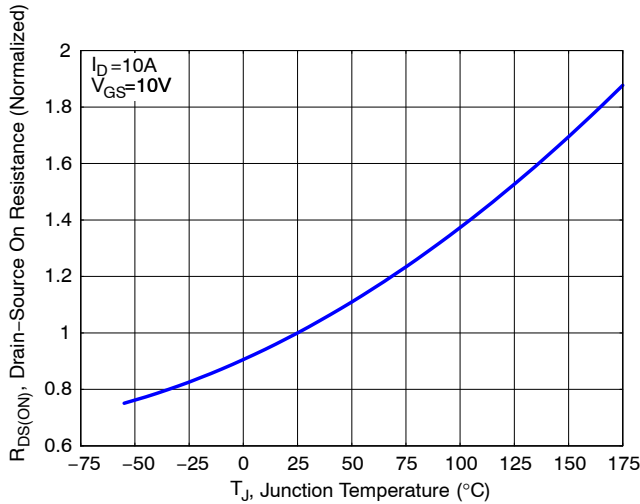


Figure 5. Normalized On-Resistance vs. Junction Temperature

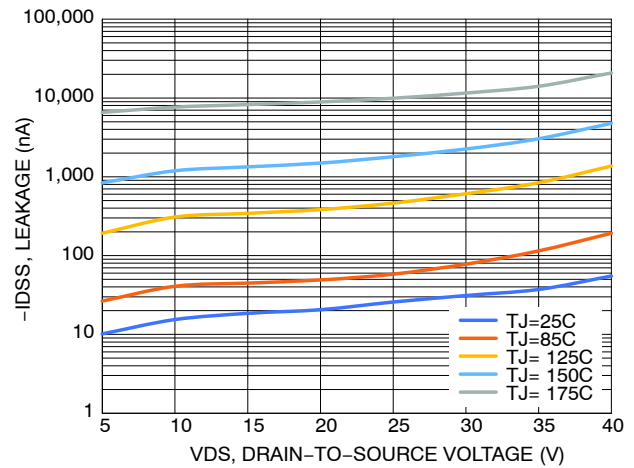


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

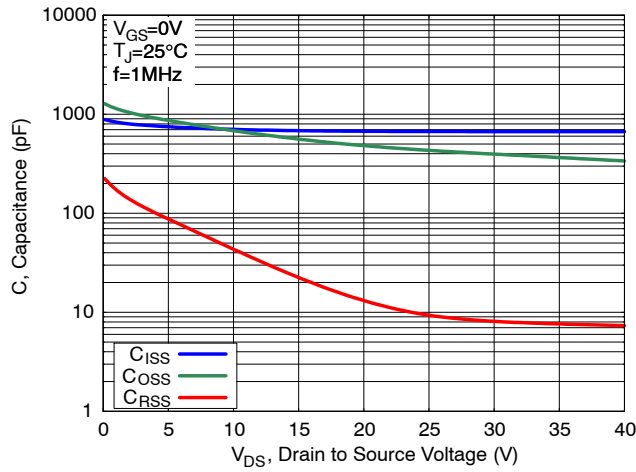


Figure 7. Capacitance Characteristics

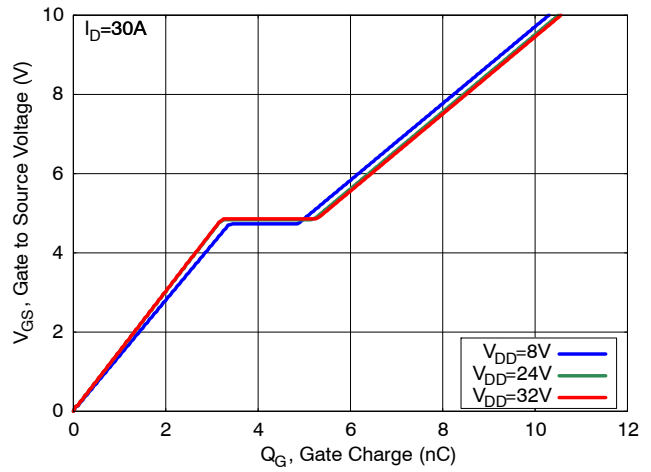


Figure 8. Gate Charge Characteristics

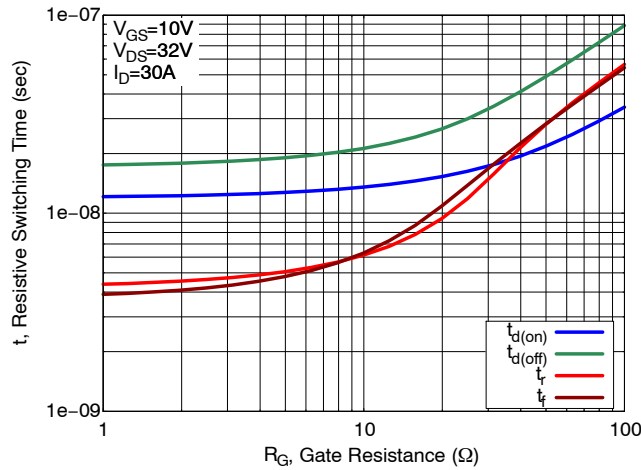


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

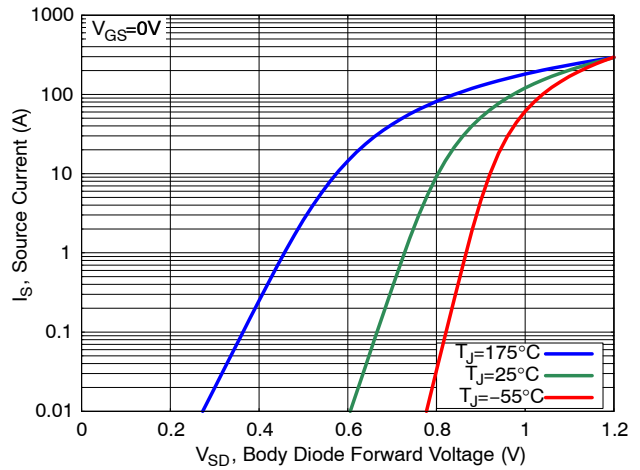


Figure 10. Diode Forward Characteristics

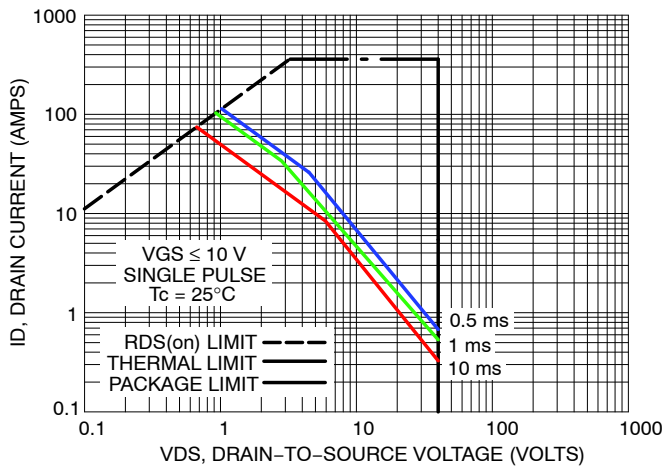


Figure 11. Safe Operating Area (SOA)

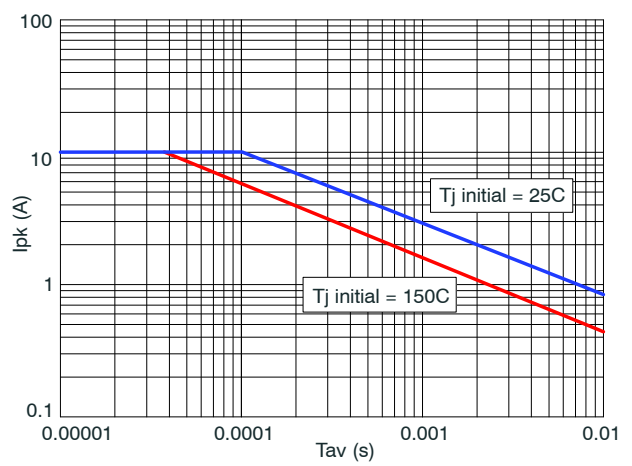


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

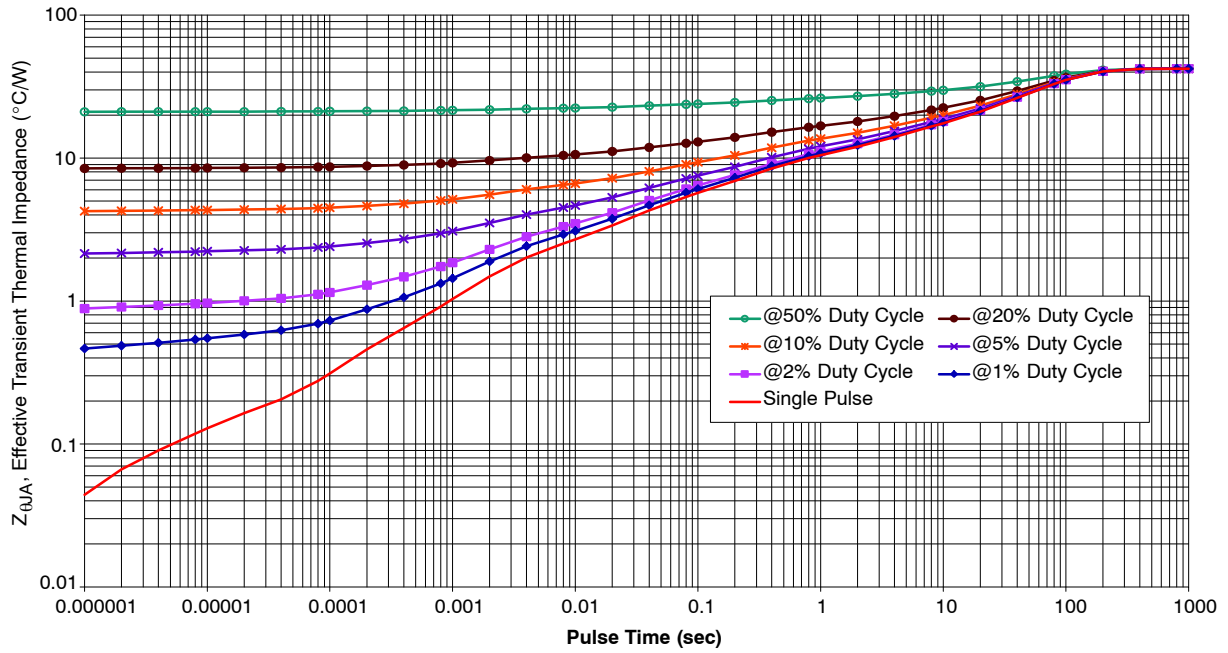


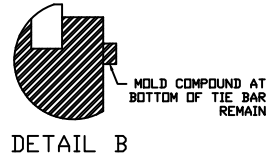
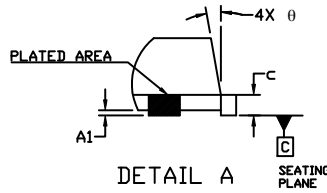
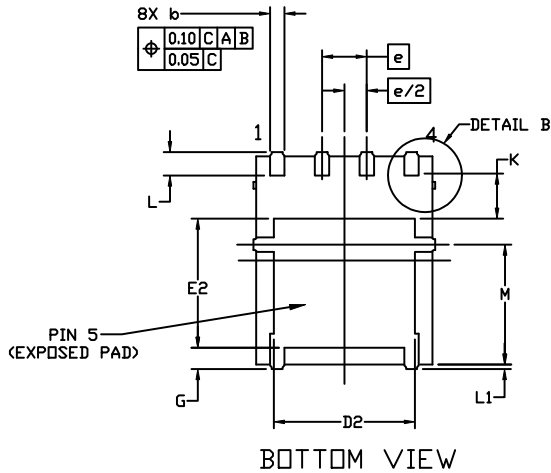
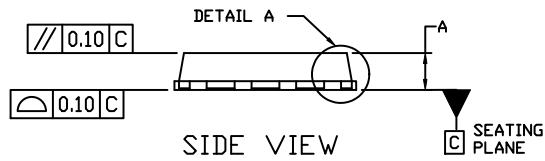
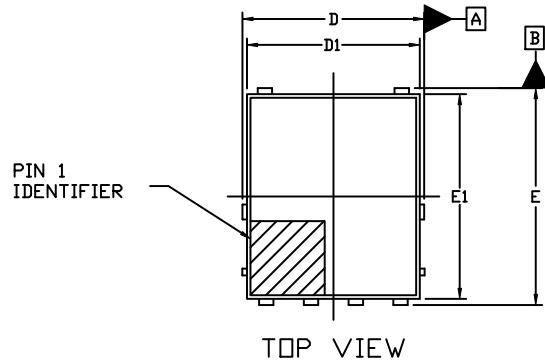
Figure 13. Transient Thermal Response

PACKAGE DIMENSIONS

DFNW5 5x6 (FULL-CUT SO8FL WF)

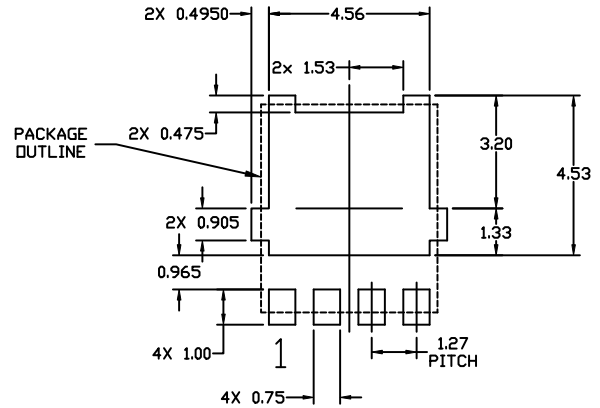
CASE 507BA

ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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[STU7N60DM2](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPB45P03P4L11ATMA2](#) [BXP4N65F](#) [BXP2N20L](#) [BXP2N65D](#) [SLF10N65ABV2](#)
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[SSM10N954L,EFF\(S](#) [2SK3878\(STA1,E,S\)](#) [TPN6R303NC,LQ\(S](#) [AP3N5R0MT](#) [AP6NA3R2MT](#) [AP3C023AMT](#) [AP6242](#) [HSBB3909](#)
[HSBA3204](#) [HSBA0903](#)