

# MOSFET - Power, Single N-Channel, DFN5/DFNW5 40 V, 4.5 mΩ, 78 A

## NVMFS5C460NL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5C460NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	40	V
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	A
		T <sub>C</sub> = 100°C		
Power Dissipation $R_{\theta JC}$ (Note 1)		T <sub>C</sub> = 25°C	P <sub>D</sub>	W
		T <sub>C</sub> = 100°C		
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	A
		T <sub>A</sub> = 100°C		
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	W
		T <sub>A</sub> = 100°C		
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 µs	I <sub>DM</sub>	396	A
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)		I <sub>S</sub>	56	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 5 A)		E <sub>AS</sub>	107	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C

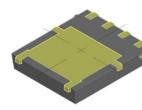
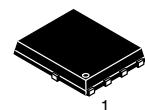
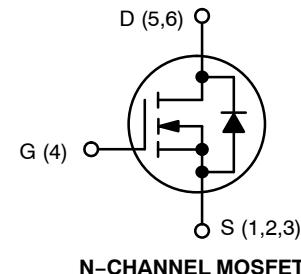
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	R <sub>θJC</sub>	3.0	°C/W
Junction-to-Ambient – Steady State (Note 2)	R <sub>θJA</sub>	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

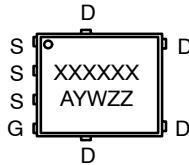
V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
40 V	4.5 mΩ @ 10 V	78 A
	7.2 mΩ @ 4.5 V	



DFN5 (SO-8FL)  
CASE 488AA

DFNW5  
(FULL-CUT SO8FL WF)  
CASE 507BA

### MARKING DIAGRAM



XXXXXX = 5C460L  
(NVMFS5C460NL) or  
460LWF  
(NVMFS5C460NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFS5C460NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				21		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25 °C			10	μA
			T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 40 μA		1.2		2.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.1		mV/°C
Drain-to-Source On Resistance	R <sub>DSON</sub>	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 35 A		5.8	7.2	mΩ
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 35 A		3.7	4.5	
Forward Transconductance	g <sub>F</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 35 A			72		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		1300		pF
Output Capacitance	C <sub>OSS</sub>			530		
Reverse Transfer Capacitance	C <sub>rss</sub>			25		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 35 A		23		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 35 A		11		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			2.5		
Gate-to-Source Charge	Q <sub>GS</sub>			4.7		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.0		
Plateau Voltage	V <sub>GP</sub>			3.3		V

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V, I <sub>D</sub> = 35 A, R <sub>G</sub> = 1 Ω		9.2		ns
Rise Time	t <sub>r</sub>			3.4		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			17		
Fall Time	t <sub>f</sub>			4.4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 35 A	T <sub>J</sub> = 25°C		0.86	1.2	V
			T <sub>J</sub> = 125°C		0.75		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 35 A			29		ns
Charge Time	t <sub>a</sub>				14		
Discharge Time	t <sub>b</sub>				14		
Reverse Recovery Charge	Q <sub>RR</sub>				12		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

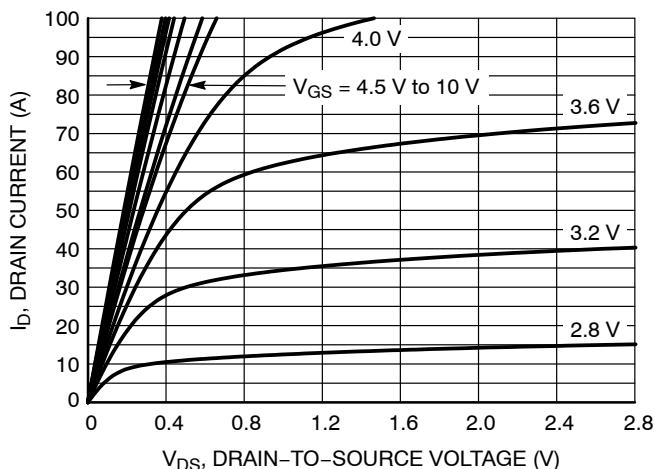


Figure 1. On-Region Characteristics

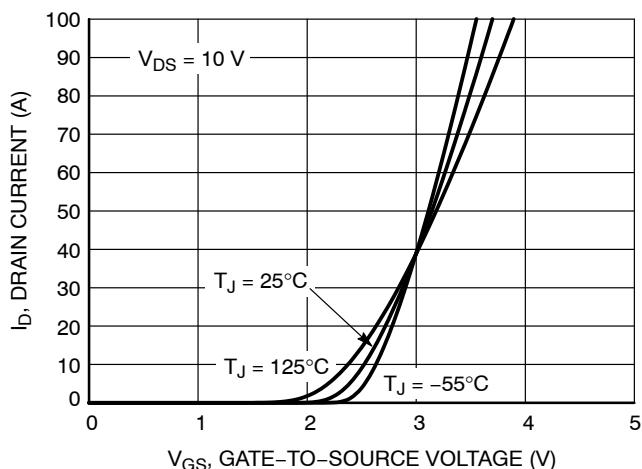


Figure 2. Transfer Characteristics

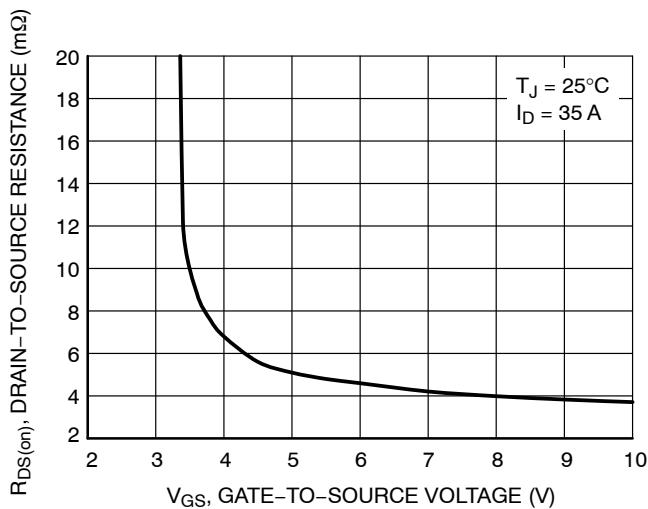


Figure 3. On-Resistance vs. Gate-to-Source Voltage

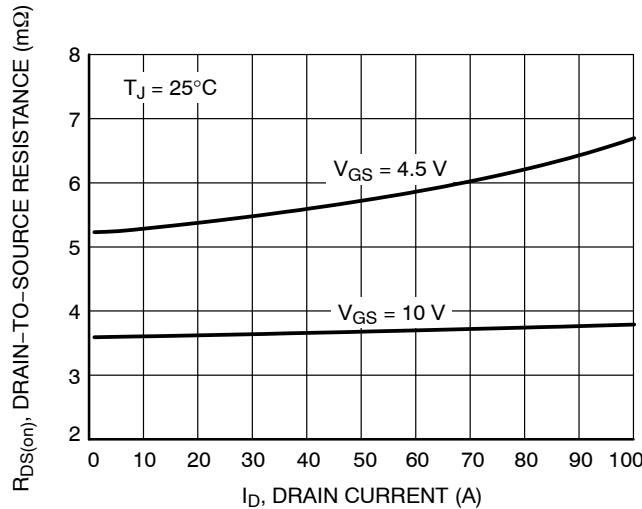


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

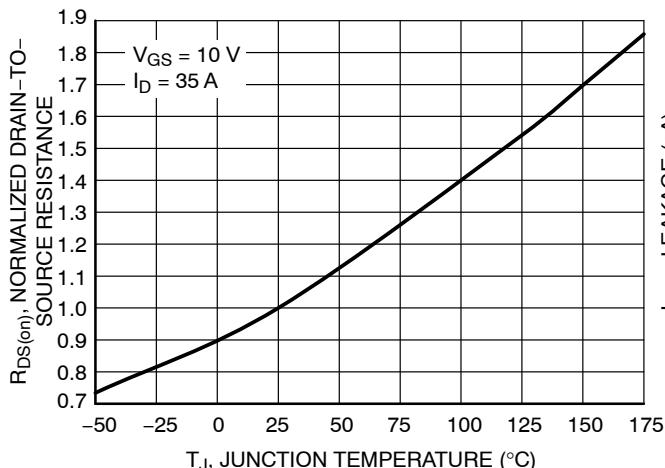


Figure 5. On-Resistance Variation with Temperature

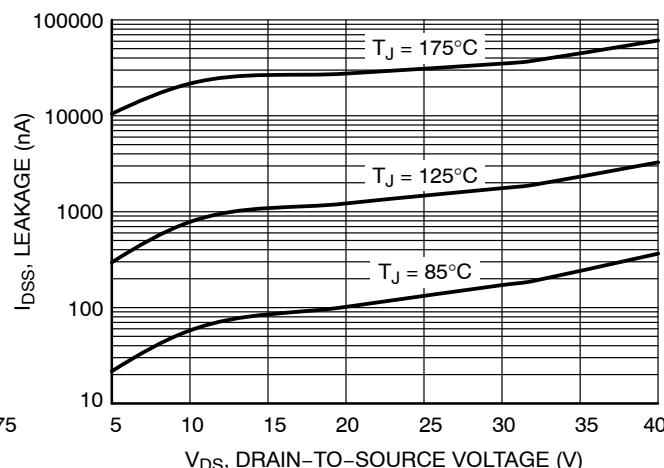


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

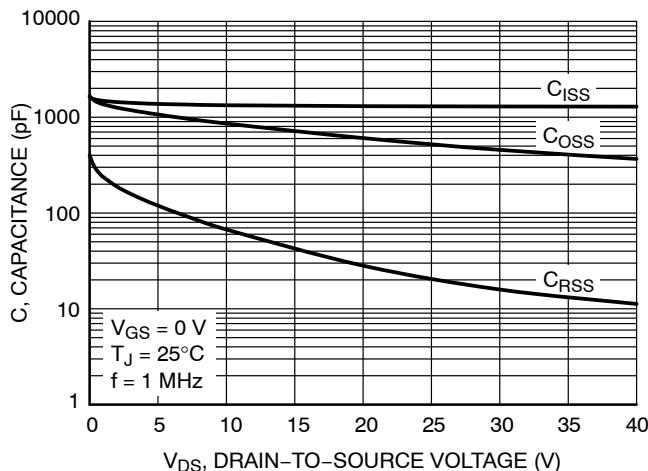


Figure 7. Capacitance Variation

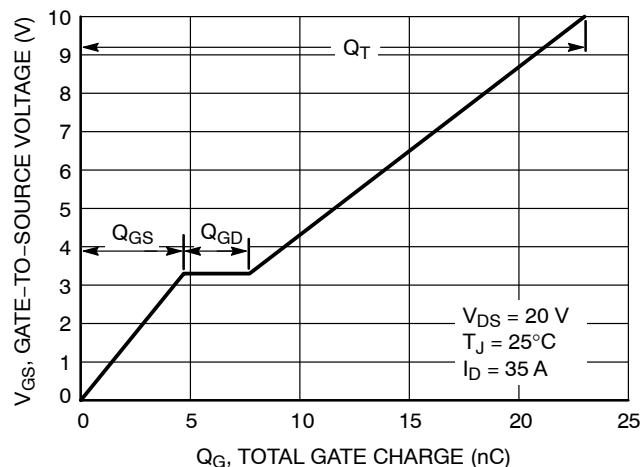


Figure 8. Gate-to-Source vs. Total Charge

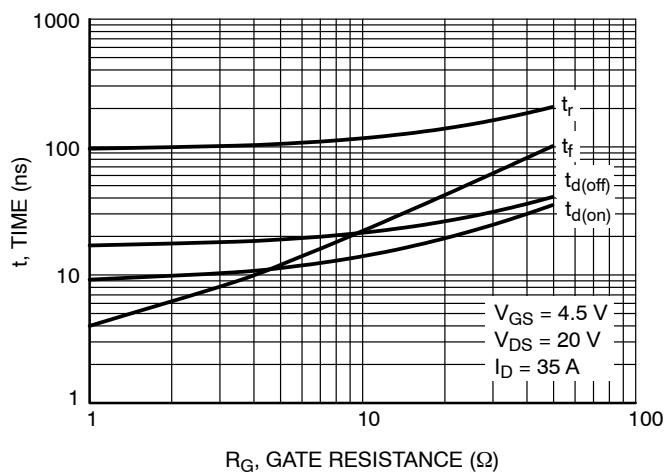


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

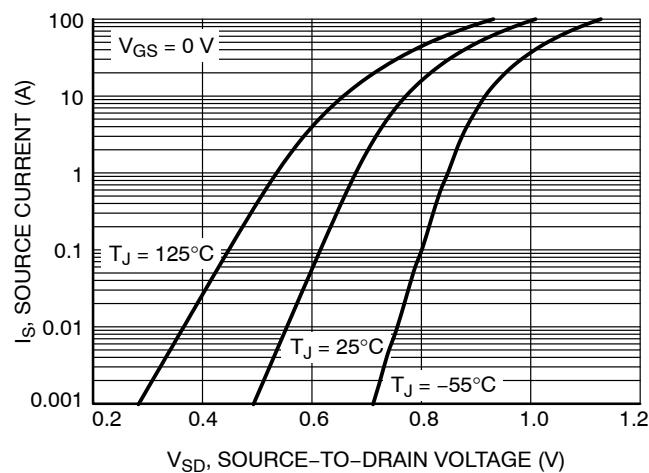


Figure 10. Diode Forward Voltage vs. Current

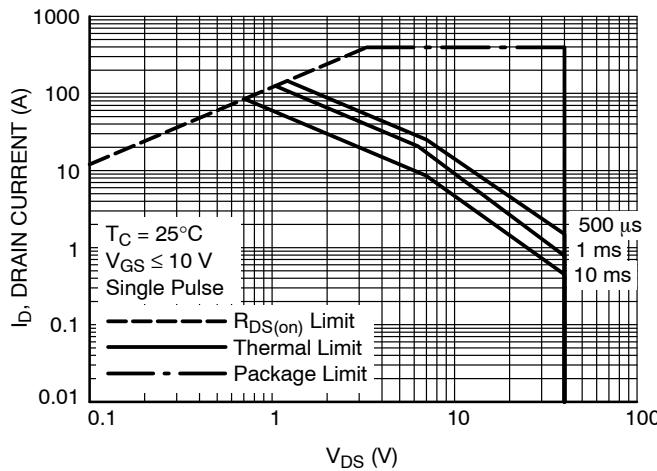


Figure 11. Safe Operating Area

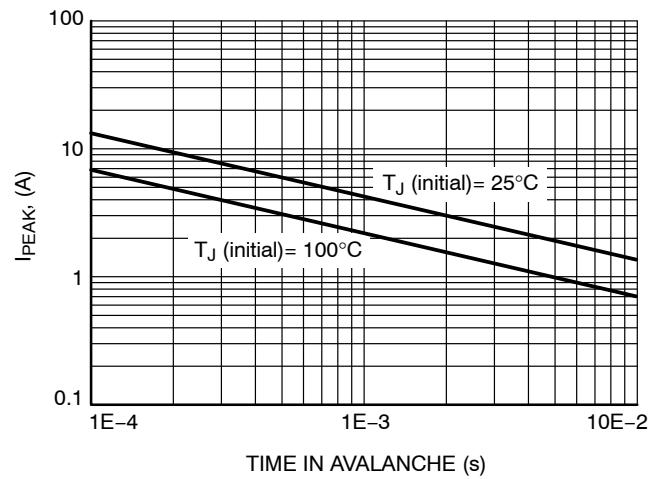


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFS5C460NL

## TYPICAL CHARACTERISTICS

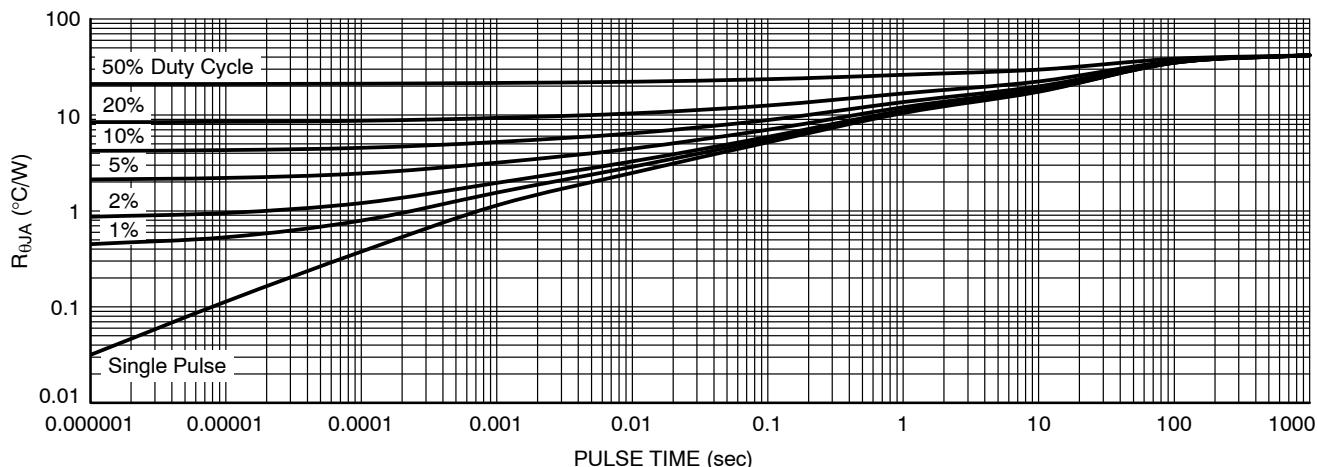


Figure 13. Thermal Characteristics

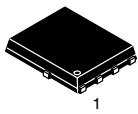
## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5C460NLT1G	5C460L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C460NLWFT1G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C460NLT3G	5C460L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C460NLWFT3G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C460NLAFT1G	5C460L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C460NLAFT1G-YE	5C460L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C460NLWFAFT1G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C460NLWFAFT3G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C460NLWFET1G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C460NLWFET3G	460LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

**onsemi**<sup>TM</sup>



SCALE 2:1

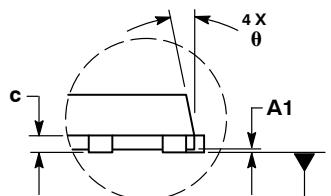
**DFN5 5x6, 1.27P  
(SO-8FL)**  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018

NOTES:

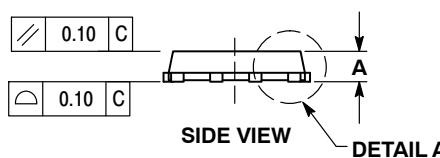
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
$\theta$	0°	---	12°

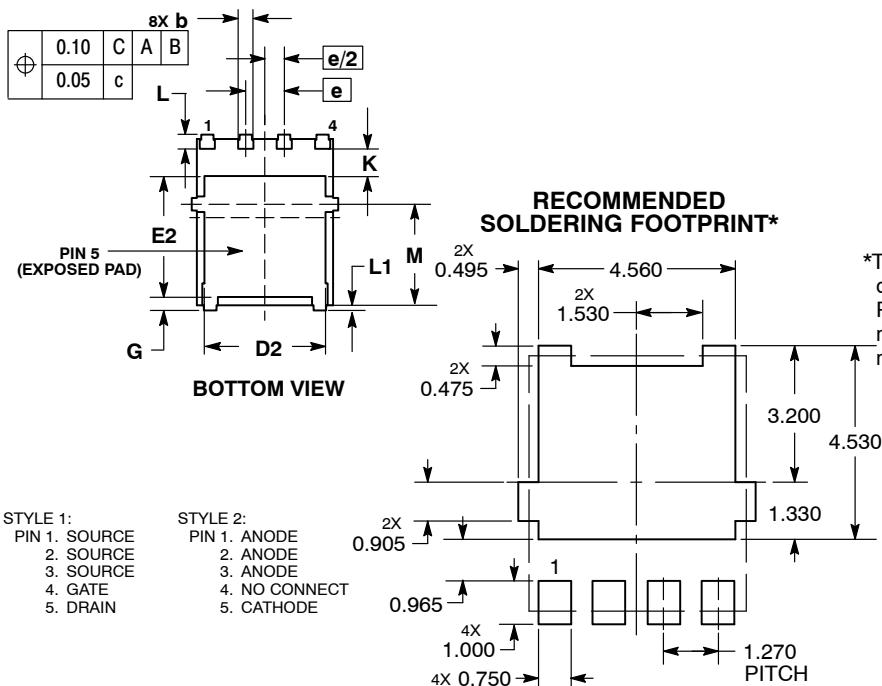


DETAIL A

SEATING PLANE



DETAIL A



STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

DIMENSIONS: MILLIMETERS

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



XXXXXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

ZZ = Lot Traceability

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

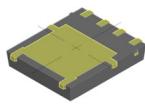
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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

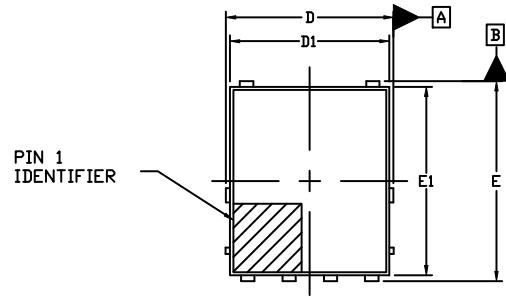
## PACKAGE DIMENSIONS

ON Semiconductor®

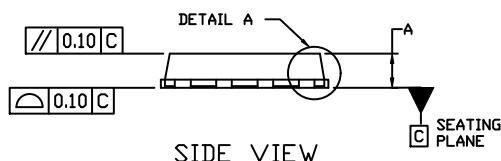


DFNW5 5x6  
CASE 507BE  
ISSUE O

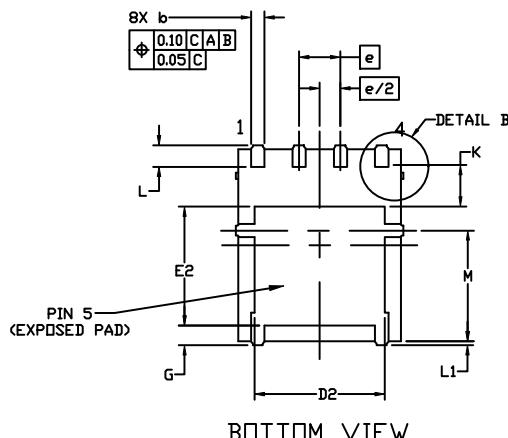
DATE 23 APR 2021



TOP VIEW

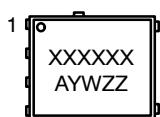


SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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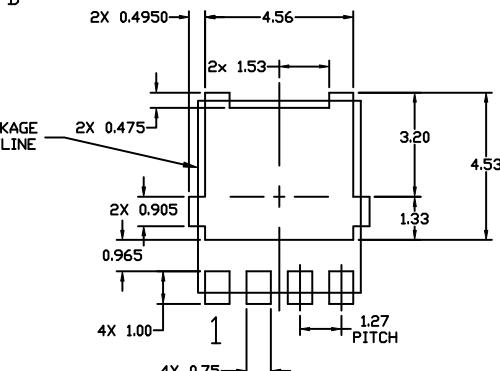
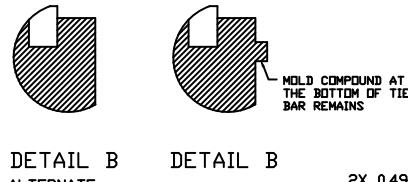
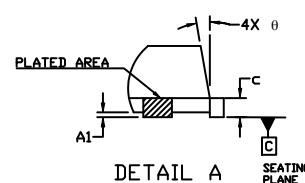
DESCRIPTION: DFNW5 5x6

PAGE 1 OF 1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27	BSC	
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150	REF	
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED  
MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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