

MOSFET - Power, Single N-Channel, DFN5/DFNW5 40 V, 3.7 mΩ, 87 A

NVMFS5C456NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C456NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	40	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	I _D	87
		T _C = 100°C		61
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	55
		T _C = 100°C		27
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	22
		T _A = 100°C		16
Power Dissipation R _{θJA} (Notes 1 & 2)		T _A = 25°C	P _D	3.6
		T _A = 100°C		1.8
Pulsed Drain Current	T _A = 25°C, t _p = 10 µs	I _{DM}	520	A
Operating Junction and Storage Temperature		T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)		I _S	61	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 5 A)		E _{AS}	202	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

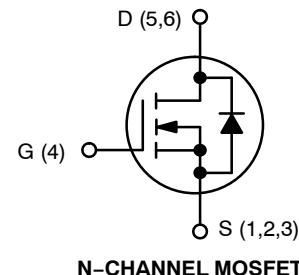
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	R _{θJC}	2.7	°C/W
Junction-to-Ambient – Steady State (Note 2)	R _{θJA}	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

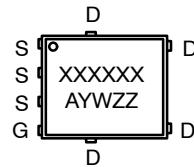
V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
40 V	3.7 mΩ @ 10 V	87 A
	6.0 mΩ @ 4.5 V	



DFN5 (SO-8FL)
CASE 488AA

DFNW5
(FULL-CUT SO8FL WF)
CASE 507BA

MARKING DIAGRAM



XXXXXX = 5C456L
(NVMFS5C456NL) or
456LWF
(NVMFS5C456NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS5C456NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C			10	μA
			T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 50 μA		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.1		mV/°C
Drain-to-Source On Resistance	R _{DSS(on)}	V _{GS} = 4.5 V	I _D = 20 A		4.8	6.0	mΩ
		V _{GS} = 10 V	I _D = 20 A		3.1	3.7	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 40 A			80		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		1600		pF
Output Capacitance	C _{OSS}			590		
Reverse Transfer Capacitance	C _{rss}			21		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 40 A		18		nC
Total Gate Charge	Q _{G(TOT)}			8.2		
Threshold Gate Charge	Q _{G(TH)}			2		
Gate-to-Source Charge	Q _{GS}			3.8		
Gate-to-Drain Charge	Q _{GD}			2.1		
Plateau Voltage	V _{GP}			3.2		
						V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 40 A, R _G = 1 Ω		9.3		ns
Rise Time	t _r			100		
Turn-Off Delay Time	t _{d(OFF)}			17		
Fall Time	t _f			4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 40 A	T _J = 25°C		0.86	1.2	V
			T _J = 125°C		0.75		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 40 A			29		ns
Charge Time	t _a				14		
Discharge Time	t _b				15		
Reverse Recovery Charge	Q _{RR}				20		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

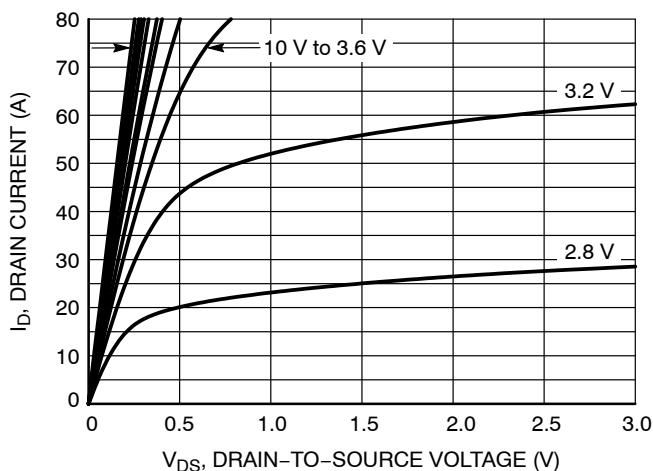


Figure 1. On-Region Characteristics

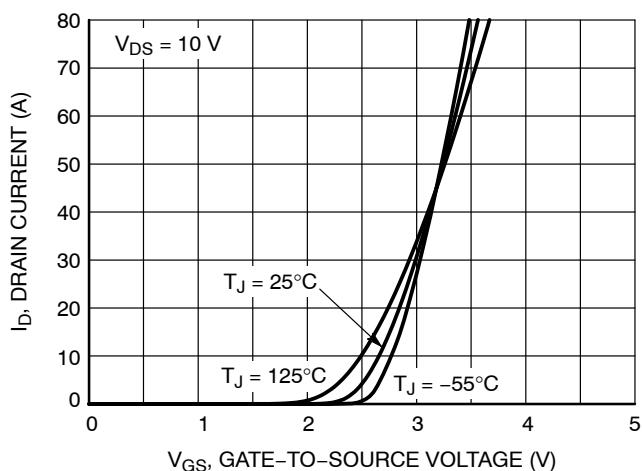


Figure 2. Transfer Characteristics

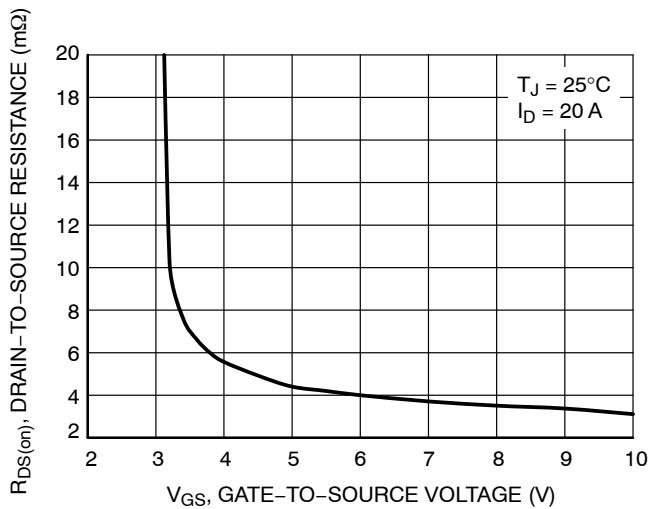


Figure 3. On-Resistance vs. Gate-to-Source Voltage

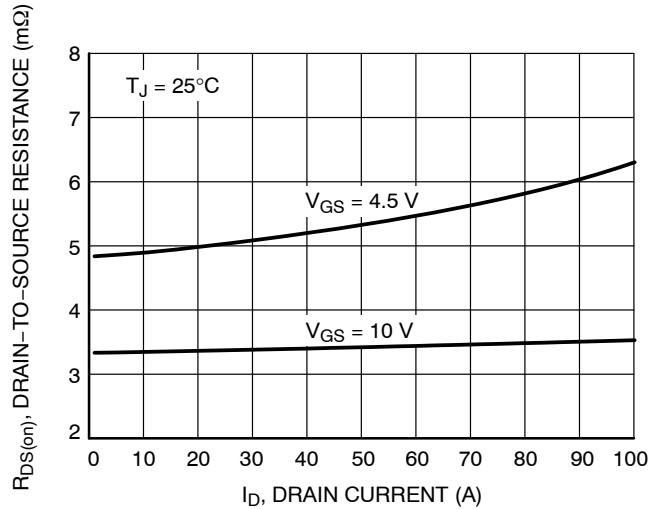


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

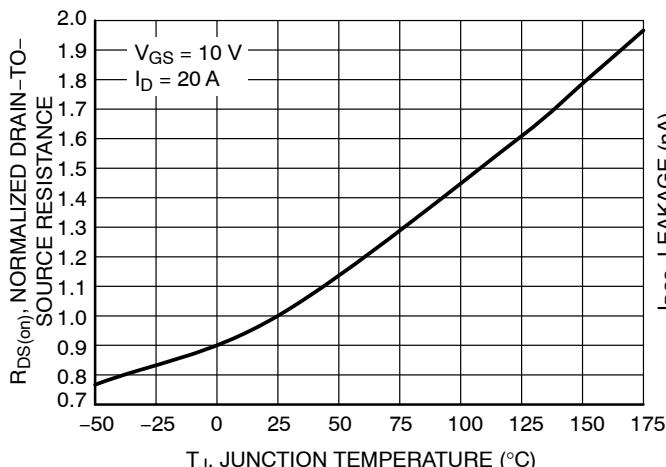


Figure 5. On-Resistance Variation with Temperature

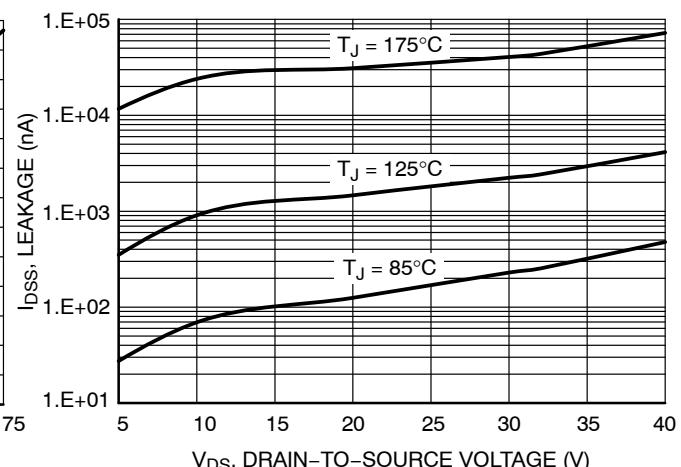
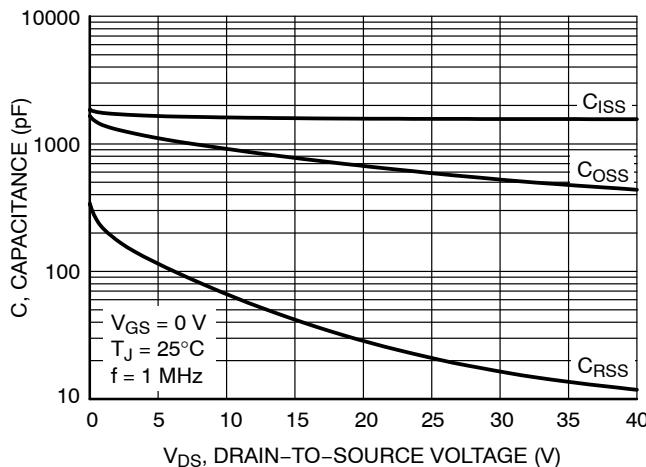
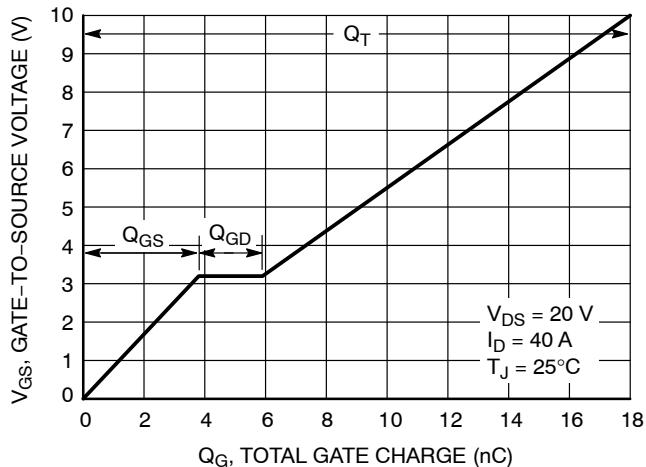
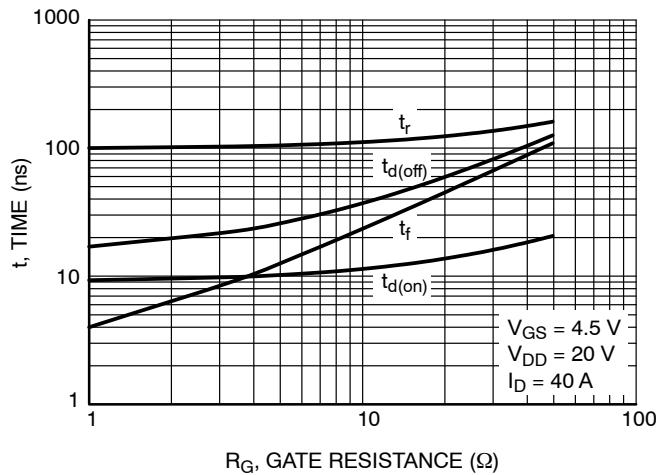
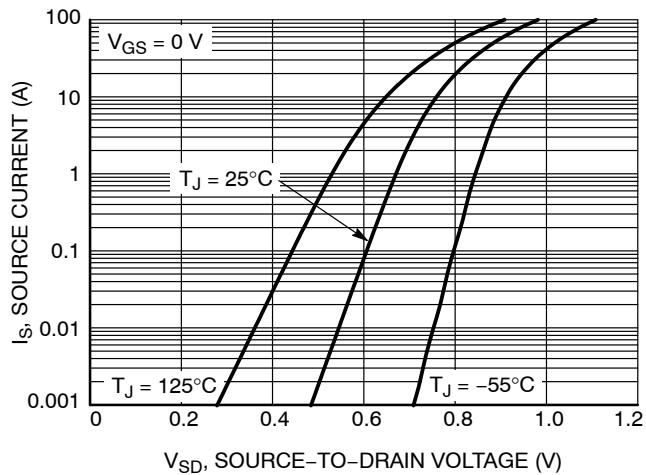
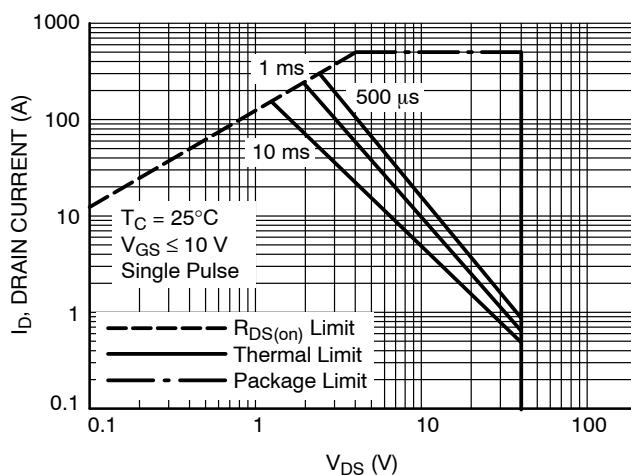
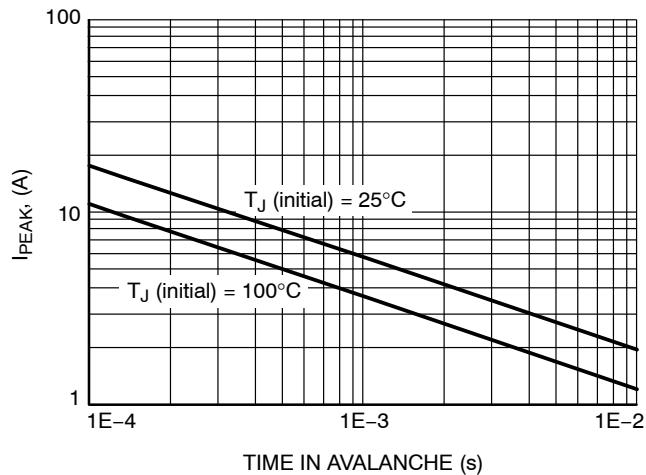


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

Figure 11. Safe Operating Area

Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

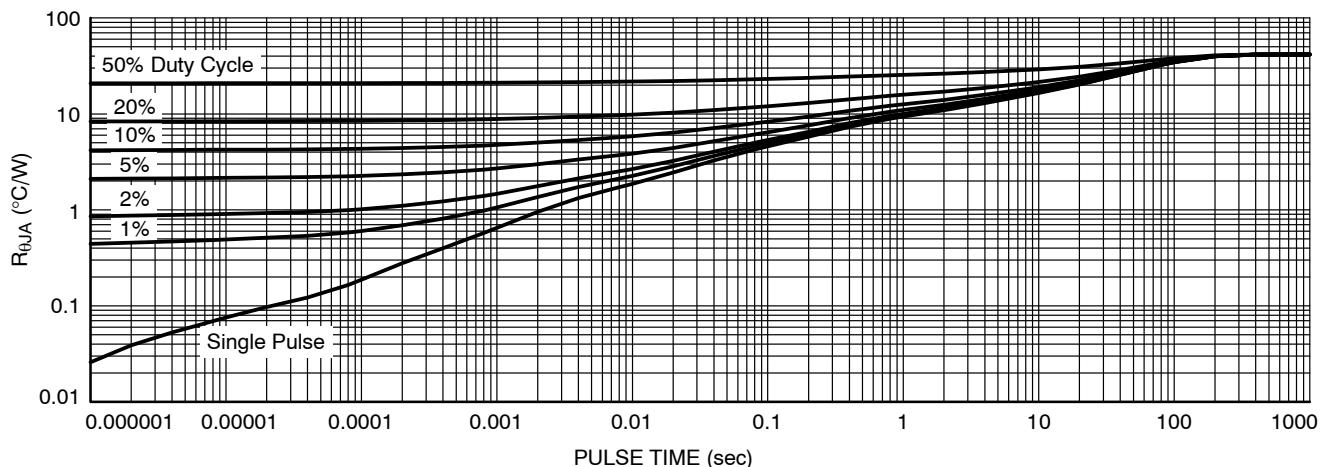


Figure 13. Thermal Characteristics

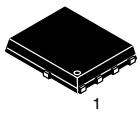
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C456NLT1G	5C456L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C456NLWFT1G	456LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C456NLT3G	5C456L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C456NLWFT3G	456LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C456NLAFT1G	5C456L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C456NLAFT1G-YE	5C456L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C456NLWFAFT1G	456LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C456NLWFET1G	456LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C456NLWFET3G	456LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemiTM



SCALE 2:1

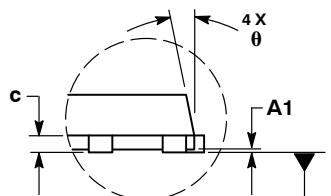
**DFN5 5x6, 1.27P
(SO-8FL)**
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:

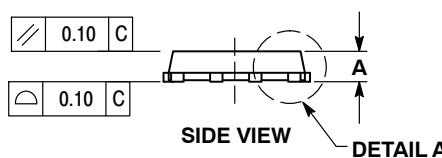
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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

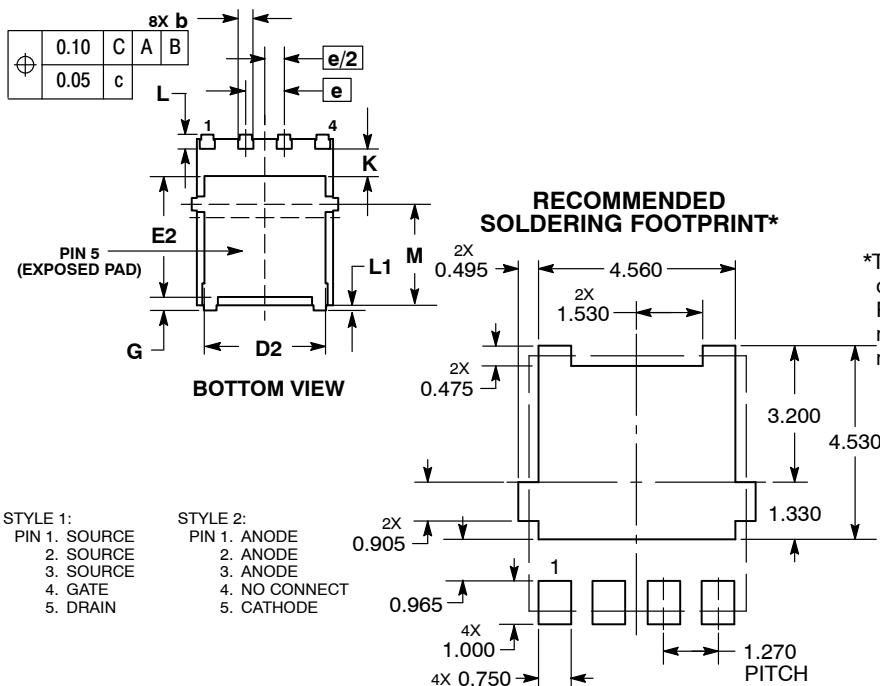


DETAIL A

SEATING PLANE



DETAIL A

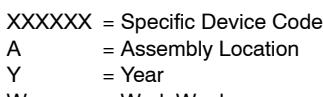


STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

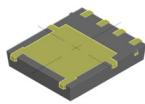
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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

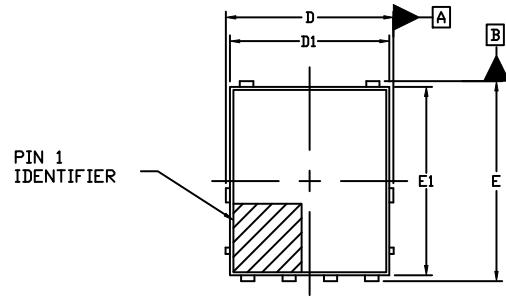
PACKAGE DIMENSIONS

ON Semiconductor®

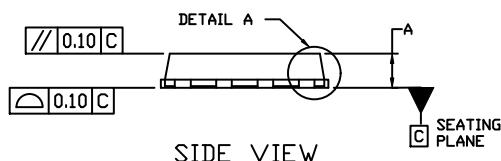


DFNW5 5x6
CASE 507BE
ISSUE O

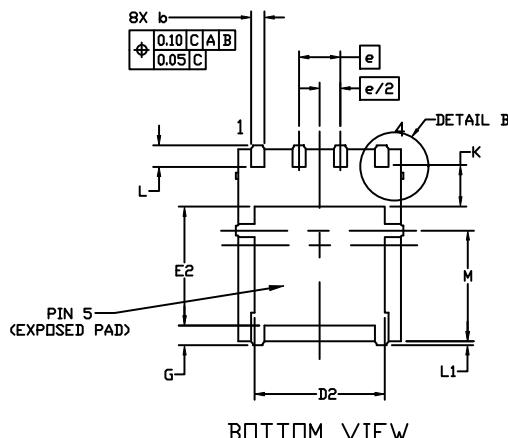
DATE 23 APR 2021



TOP VIEW

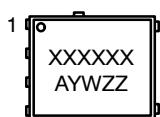


SIDE VIEW



BOTTOM VIEW

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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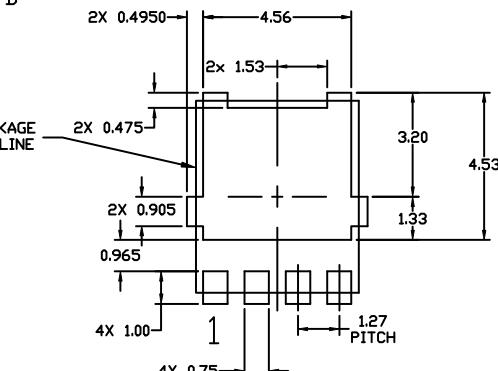
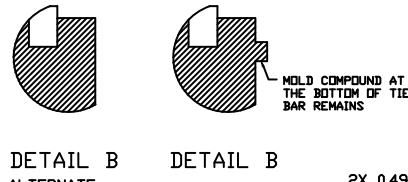
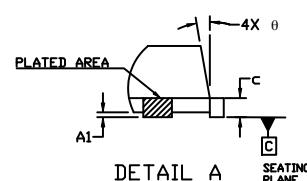
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PAGE 1 OF 1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27	BSC	
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150	REF	
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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