Power MOSFET

60 V, 15 m Ω , 37 A, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	V
Continuous Drain			I _D	36	Α
Current R _{θJC} (Notes 1, 2, 3)	State	T _C = 100°C		21	
Power Dissipation		T _C = 25°C	P_{D}	37	W
R _{θJC} (Notes 1, 2)		T _C = 100°C		12	
Continuous Drain	Steady State	T _A = 25°C	I _D	12	Α
Current R _{0JA} (Notes 1, 2, 3)	State	T _A = 100°C		8.4	
Power Dissipation		T _A = 25°C	P_{D}	3.8	W
R _{θJA} (Notes 1 & 2)		T _A = 100°C		1.9	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	185	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	–55 to + 175	°C
Source Current (Body Diode)			Is	31	Α
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _{L(pk)} = 1.6 A)			E _{AS}	65	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{ heta JC}$	4.1	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	39	

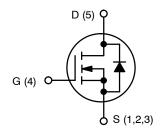
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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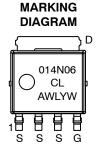
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	15 mΩ @ 10 V	07.4
	21.5 m Ω @ 4.5 V	37 A



N-CHANNEL MOSFET



LFPAK4 CASE 760AB



014N06CL = Specific Device Code A = Assembly Location

WL = Wafer Lot
 Y = Year
 W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J				26		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 \text{ V}, T_{J} = 25 ^{\circ} \text{ C}$				10	μΑ
		$V_{DS} = 60 \text{ V}$	T _J = 125°C			250	1
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)					-		
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 25 μΑ	1.2		2.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A		12.5	15	mΩ
		V _{GS} = 4.5 V	I _D = 10 A		17.9	21.5	1
Forward Transconductance	9FS	V _{DS} = 15 V, I _D	= 15 A		43		S
CHARGES, CAPACITANCES & GATE RESIS	TANCE				•	•	
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			620		pF
Output Capacitance	C _{OSS}				340		
Reverse Transfer Capacitance	C _{RSS}				7.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 10 A			4.5		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 10 A			9.7		1
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 10 A			1.3		1
Gate-to-Source Charge	Q _{GS}				2.1		1
Gate-to-Drain Charge	Q_{GD}				1.0		1
Plateau Voltage	V_{GP}				3.1		V
SWITCHING CHARACTERISTICS (Note 5)					•	•	
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 10 \text{ V}, V_{DS}$	s = 48 V,		7.0		ns
Rise Time	t _r	$I_D = 10 \text{ A}, R_G = 1.0 \Omega$			13		7
Turn-Off Delay Time	t _{d(OFF)}				25		1
Fall Time	t _f				6.0		1
DRAIN-SOURCE DIODE CHARACTERISTIC	s					•	
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 V$,	T _J = 25°C		0.85	1.2	V
		I _S = 10 A	T _J = 125°C		0.72		1
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dIS/dt} = 20 \text{ A/}\mu\text{s,}$			23.8		ns
Charge Time	t _a	I _S = 10 A	4		11.9		
Discharge Time	t _b				11.8		1
Reverse Recovery Charge	Q _{RR}				11.6		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

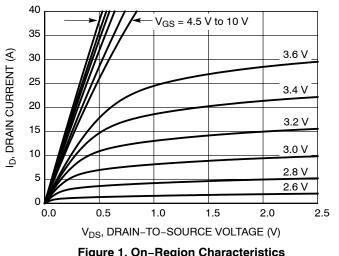
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

30

25

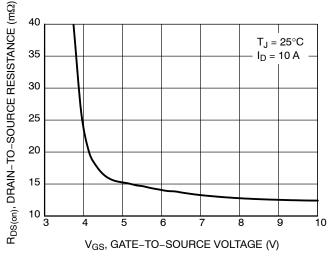
 $V_{DS} = 10 V$



ID, DRAIN CURRENT (A) 20 15 10 T_J = 25°C 5 $T_{\rm J} = 125^{\circ}$ -55°C 0 0 2 6

Figure 1. On-Region Characteristics

V_{GS}, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics



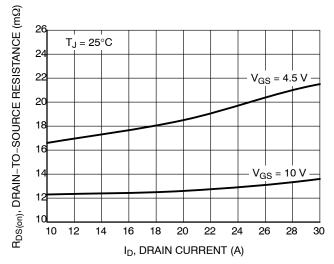
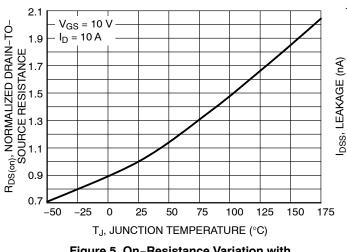


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**



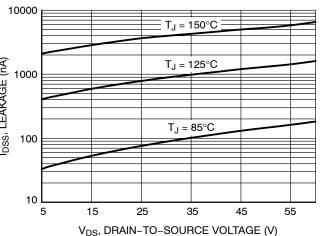


Figure 5. On-Resistance Variation with **Temperature**

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

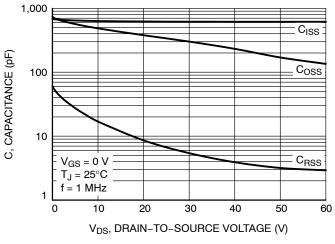


Figure 7. Capacitance Variation

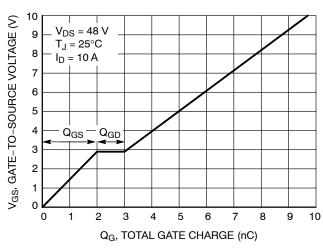


Figure 8. Gate-to-Source vs. Total Charge

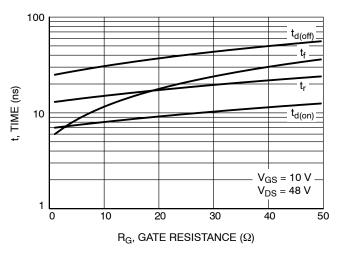


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

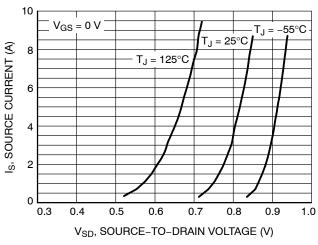


Figure 10. Diode Forward Voltage vs. Current

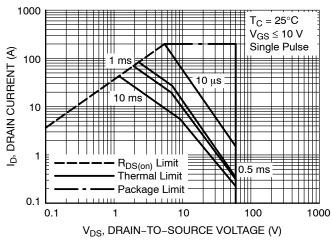


Figure 11. Maximum Rated Forward Biased Safe Operating Area

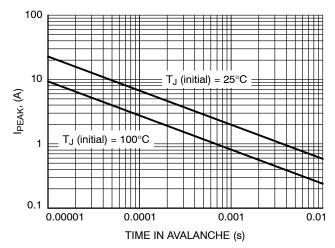


Figure 12. $I_{\mbox{\scriptsize PEAK}}$ vs. Time in Avalanche

TYPICAL CHARACTERISTICS

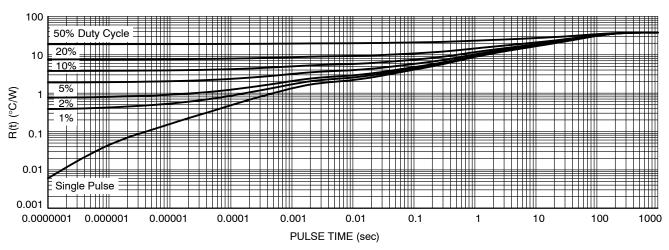
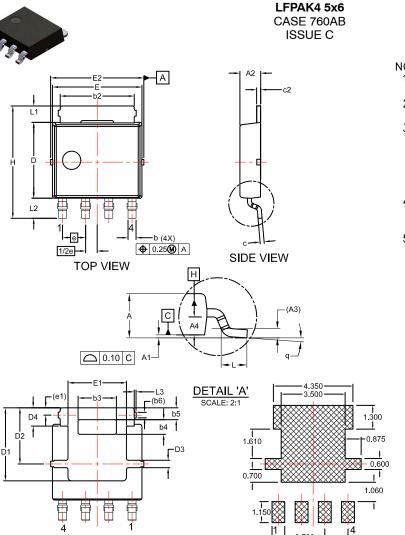


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMYS014N06CLTWG	014N06CL	LFPAK4 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



DATE 19 NOV 2019

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
- 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

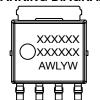
L	UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX	
Α	1.10	1.20	1.30	
A1	0.00	0.08	0.15	
A2	1.10	1.15	1.20	
А3	().25 REF		
A4	0.45	0.50	0.55	
b	0.40	0.45	0.50	
b2	3.80	4.10	4.40	
b3	2.00	2.10	2.20	
b4	0.70	0.80	0.90	
b5	0.55	0.65	0.75	
b6	(0.31 REI		
С	0.19	0.22	0.25	
c2	0.19	0.22	0.25	
D	4.05	4.15	4.25	
D1	3.80	4.00	4.20	
D2	3.00	3.10	3.20	
D3	0.30	0.40	0.50	
D4	0.90	1.00	1.10	
Е	4.80	4.90	5.00	
E1	3.10	3.20	3.30	
E2	5.00	5.15	5.30	
е		1,27 BS0)	
1/2e		0.635 BS		
e1	0.40 REF			
Ι	6.00	6.15	6.30	
L	0.40	0.65	0.85	
L1	0.80	0.90	1.00	
L2	0.90	1.10	1.30	
L3	0.00	0.10	0.20	
q	0°	4°	8°	

RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

BOTTOM VIEW



XXXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot Y = Year

Y = Year W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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