

# MOSFET - Power, Single N-Channel, DUAL COOL<sup>®</sup> 40 V, 0.78 mΩ, 310 A

## NTMFSC0D8N04XM

### Features

- Dual Sided Cooling Package
- Latest 40 V Power MOSFET Technology for Motor Drive Applications
- Extreme Lower On-Resistance to Minimize Conduction Losses
- Lower Gate Charge to Minimize Gate Driving and Switching Losses
- Soft Body Diode Reverse Recovery
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

### Applications

- Motor Drive
- ORing FET
- Battery Protection

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	40	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current (Note 2)	T <sub>C</sub> = 25°C	I <sub>D</sub>	310 A
	T <sub>C</sub> = 100°C		219
Power Dissipation (Note 2)	T <sub>C</sub> = 25°C	P <sub>D</sub>	135 W
Pulsed Drain Current	T <sub>C</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	1463 A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Continuous Source-Drain Current (Body Diode)	I <sub>S</sub>	150	A
Single Pulse Avalanche Energy (I <sub>PK</sub> = 69 A)	E <sub>AS</sub>	248	mJ
Lead Temperature Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	150	°C

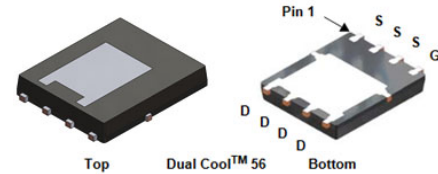
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

### THERMAL CHARACTERISTICS

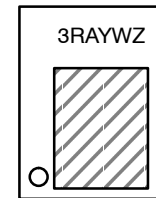
Symbol	Parameter	Max	Unit
R <sub>θJC</sub>	Junction-to-Case (Bottom) – Steady State (Note 2)	1.1	°C/W
R <sub>θJC</sub>	Junction-to-Case (Top) – Steady State (Note 2)	1.7	
R <sub>θJA</sub>	Junction-to-Ambient – Steady State (Notes 1, 2)	39	

V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
40 V	0.78 mΩ @ 10 V	310 A



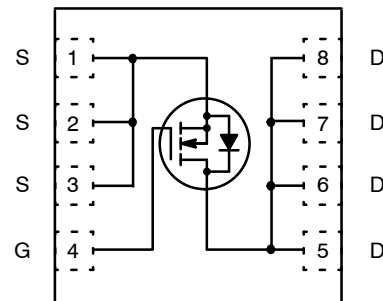
DFN8 5x6  
CASE 506EG

### MARKING DIAGRAM



- 3R = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

### N-Channel MOSFET



### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# NTMFSC0D8N04XM

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	I <sub>D</sub> = 1 mA, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 25°C			10	μA
		V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

## ON CHARACTERISTICS (Note 3)

Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		0.63	0.78	mΩ
		V <sub>GS</sub> = 7 V, I <sub>D</sub> = 50 A		0.86	1.25	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 180 μA	2.5	3.0	3.5	V
Gate Threshold Voltage Temperature Coefficient	ΔV <sub>GS(TH)</sub> /ΔT <sub>J</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 180 μA		-7		mV/°C
Forward Trans-conductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 A		244		S

## CHARGES & CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, f = 1 MHz		4651		pF	
Output Capacitance	C <sub>OSS</sub>			3319			
Reverse Transfer Capacitance	C <sub>RSS</sub>			69			
Output Charge	Q <sub>OSS</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 20 V, I <sub>D</sub> = 50 A		100		nC	
Total Gate Charge	Q <sub>G(TOT)</sub>			72			
Threshold Gate Charge	Q <sub>G(TH)</sub>			14			
Gate-to-Source Charge	Q <sub>GS</sub>			21			
Gate-to-Drain Charge	Q <sub>GD</sub>			13			
Gate Plateau Voltage	V <sub>GP</sub>			4.5			V
Gate Resistance	R <sub>G</sub>		f = 1 MHz		0.65		1.2

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	Resistive Load V <sub>GS</sub> = 0/10 V, V <sub>DD</sub> = 20 V, I <sub>D</sub> = 50 A, R <sub>G</sub> = 2.5 Ω		28		ns
Rise Time	t <sub>r</sub>			10		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			45		
Fall Time	t <sub>f</sub>			9.5		

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A, T <sub>J</sub> = 25°C		0.81	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A, T <sub>J</sub> = 125°C		0.66	1.0	
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 50 A, V <sub>DD</sub> = 50 V		69		ns
Charge Time	t <sub>a</sub>			36		
Discharge Time	t <sub>b</sub>			33		
Reverse Recovery Charge	Q <sub>RR</sub>			144		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

# NTMFSC0D8N04XM

## TYPICAL CHARACTERISTICS

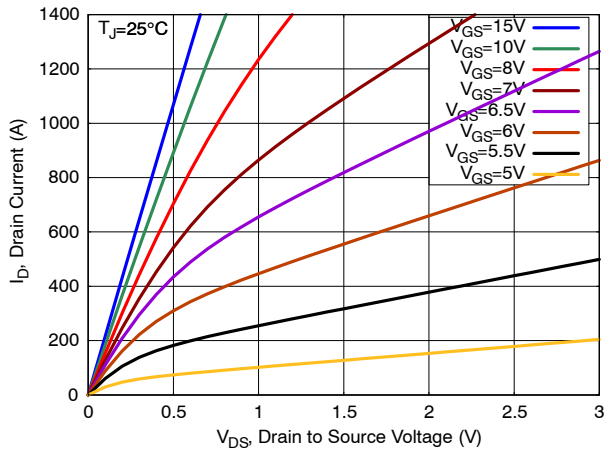


Figure 1. On-Region Characteristics

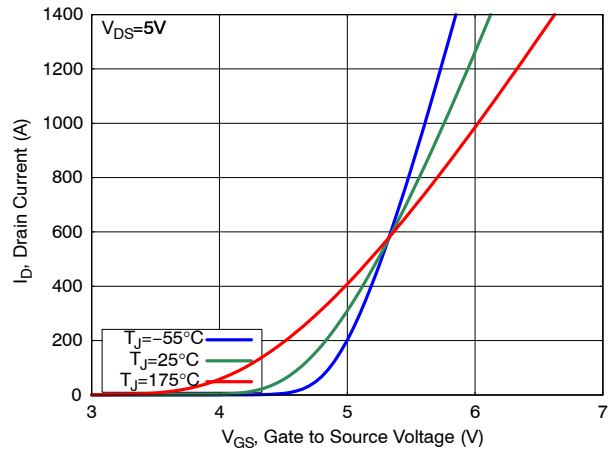


Figure 2. Transfer Characteristics

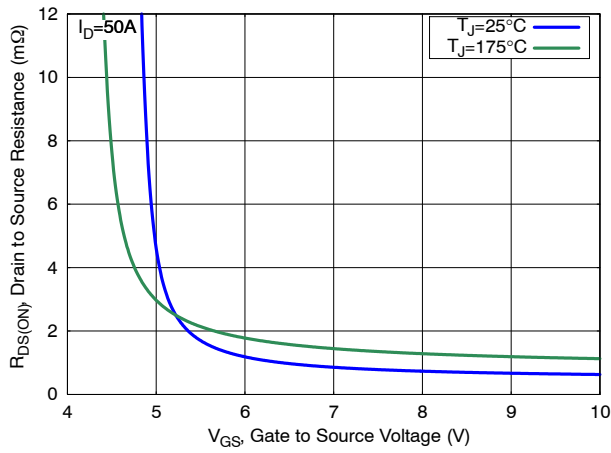


Figure 3. On-Resistance vs. Gate Voltage

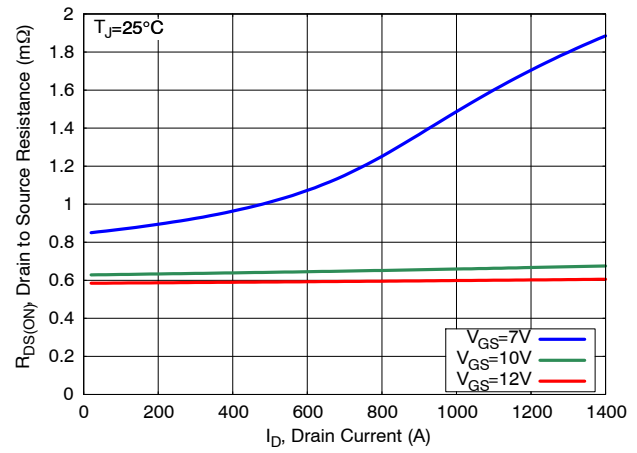


Figure 4. On-Resistance vs. Drain Current

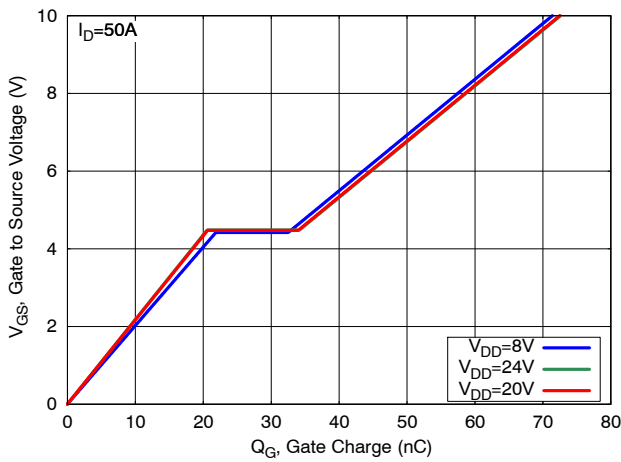


Figure 5. Gate Charge Characteristics

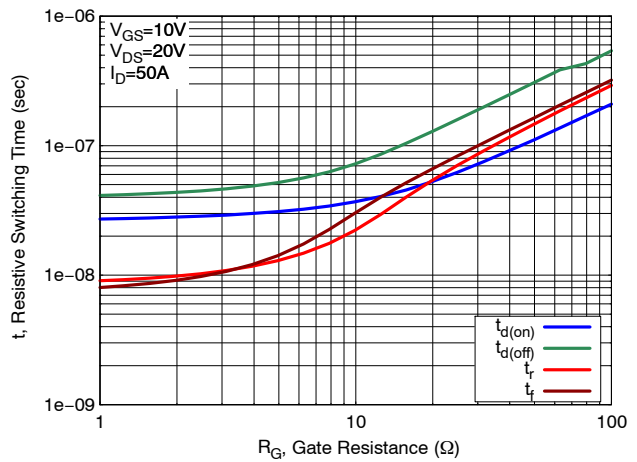


Figure 6. Resistive Switching Time Variation vs. Gate Resistance

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## TYPICAL CHARACTERISTICS

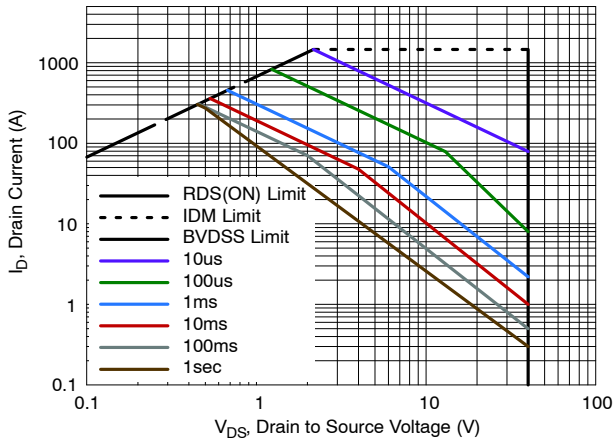


Figure 7. Safe Operating Area (SOA)

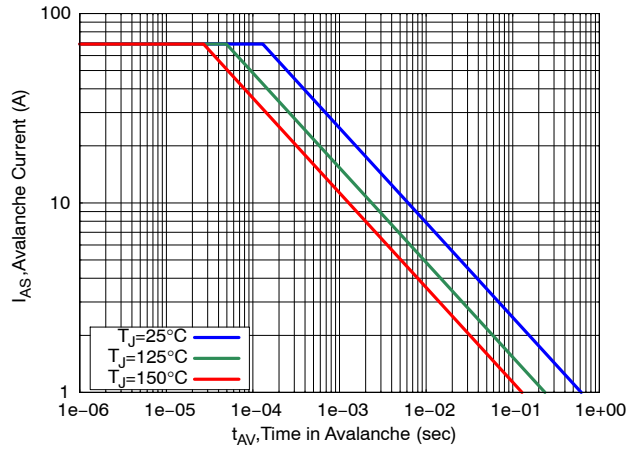


Figure 8. Avalanche Current vs Pulse Time (UIS)

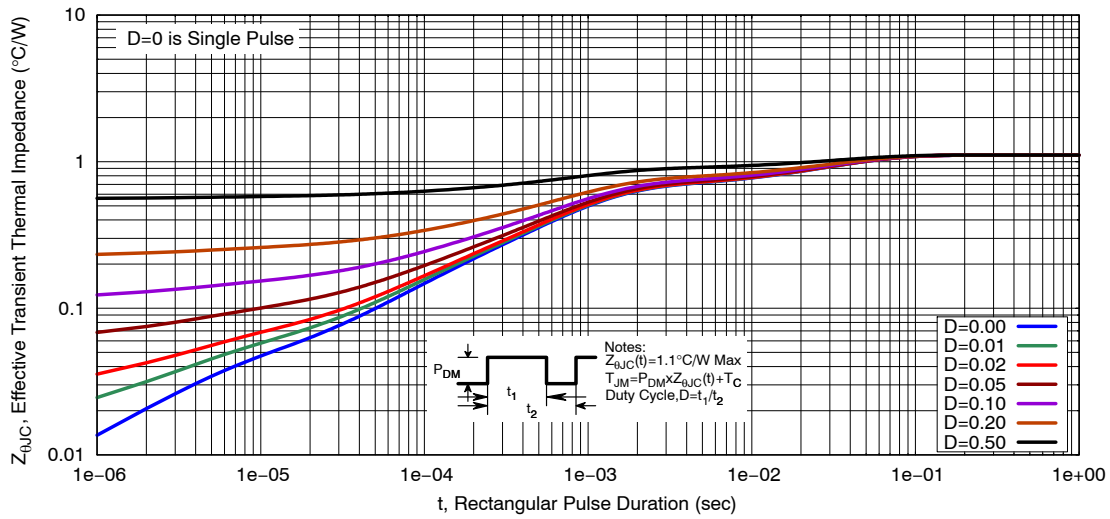


Figure 9. Transient Thermal Response

### ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NTMFSC0D8N04XMTWG	3R	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

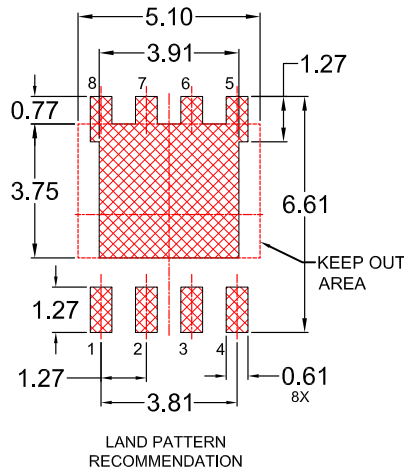
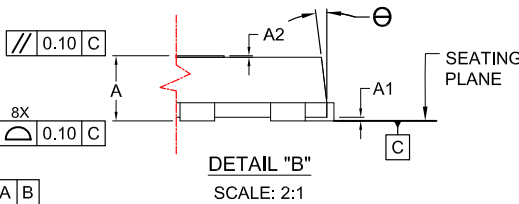
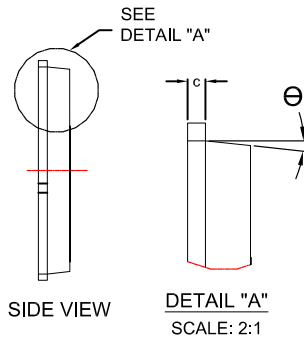
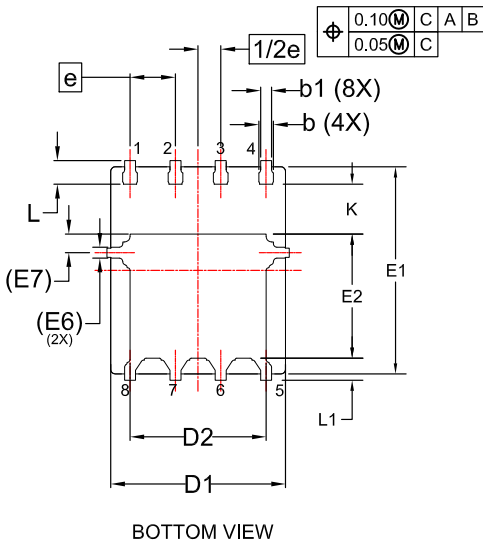
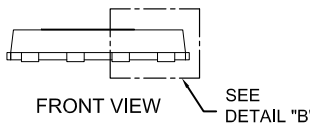
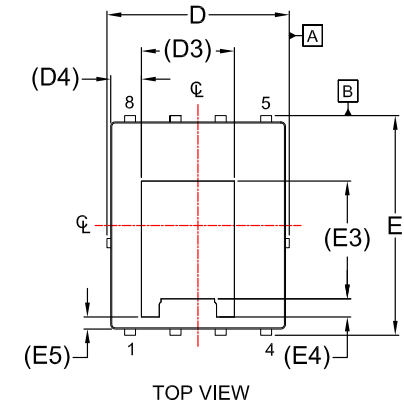
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

### DFN8 5.1x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

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onsemi Website: [www.onsemi.com](http://www.onsemi.com)

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[IRFS350](#) [VN1206L](#) [NDP4060](#) [IPS70R2K0CEAKMA1](#) [AON6932A](#) [2N4352](#) [TS19452CS RL](#) [TK31J60W5,S1VQ\(O](#) [TK16J60W,S1VQ\(O](#)  
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[RQ7L055BGTCR](#) [SLF10N65ABV2](#)