ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at www.onsemi.com

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/ or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application,

12-Bit Binary Counter

The MC14040B 12-stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	٧
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range -55 to +125		°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	ô

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



ON Semiconductor®

http://onsemi.com







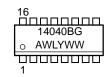
SOIC-16 D SUFFIX CASE 751B SOEIAJ-16 F SUFFIX CASE 966

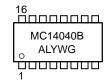
TSSOP-16 DT SUFFIX CASE 948F

PIN ASSIGNMENT

Q12 [1●	16] V _{DD}
Q6 [2	15	Q11
Q5 [3	14	Q10
Q7 [4	13] Q8
Q4 [5	12] Q9
Q3 [6	11	R
Q2 [7	10] C
V _{SS} [8	9] Q1

MARKING DIAGRAMS





SOIC-16

SOEIAJ-16



= Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

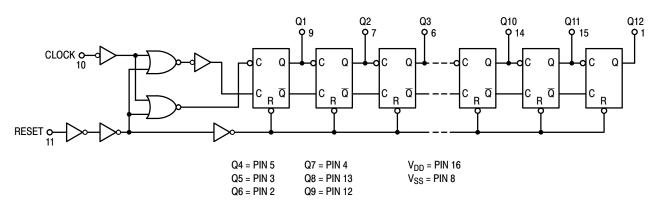
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

TRUTH TABLE

Clock Reset		Output State
	0	No Change
\ \	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14040BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14040BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14040BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14040BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14040BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14040BDTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
MC14040BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

				-55	5° C		25°C		125	5°C	
Characteristic		Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage ($V_O = 4.5 \text{ or } 0.5 \text{ Vdc}$) ($V_O = 9.0 \text{ or } 1.0 \text{ Vdc}$) ($V_O = 13.5 \text{ or } 1.5 \text{ Vdc}$)	"0" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25	1 1	3.5 7.0 11	- - -	Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	Source	I _{OH}	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2	- - -	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	- - -	-1.7 -0.36 -0.9 -2.4	- - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	-	±0.1	-	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	-	_	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Note (Dynamic plus Quiesce Per Package) (C _L = 50 pF on all output buffers switching)	nt,	I _T	5.0 10 15			$I_{T} = (0$.42 μA/kHz) .85 μA/kHz) .43 μA/kHz)	f + I _{DD}			μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

^{3.} The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $T_{TLH}, T_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $T_{TLH}, T_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $T_{TLH}, T_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t _{TLH} , t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15	- - -	260 115 80	520 230 160	ns
Clock to Q12 t_{PHL} , t_{PLH} = (1.7 ns/pF) C_L + 2415 ns t_{PHL} , t_{PLH} = (0.66 ns/pF) C_L + 867 ns t_{PHL} , t_{PLH} = (0.5 ns/pF) C_L + 475 ns		5.0 10 15	- - -	1625 720 500	3250 1440 1000	ns
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 485 \text{ ns}$ $t_{PHL} = (0.86 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	t _{PHL}	5.0 10 15	- - -	370 155 115	740 310 230	ns
Clock Pulse Width	t _{WH}	5.0 10 15	385 150 115	140 55 38	- - -	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	- - -	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15		No Limit		ns
Reset Pulse Width	t _{WH}	5.0 10 15	960 360 270	320 120 80	- - -	ns
Reset Removal Time	t _{rem}	5.0 10 15	130 50 30	65 25 15	- - -	ns

- 5. The formulas given are for the typical characteristics only at 25°C.
 6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

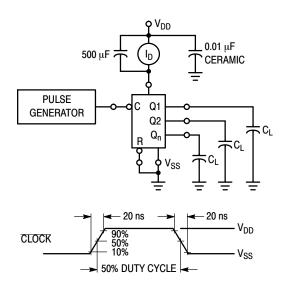


Figure 1. Power Dissipation Test Circuit and Waveform

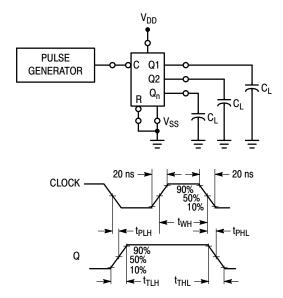


Figure 2. Switching Time Test Circuit and Waveforms

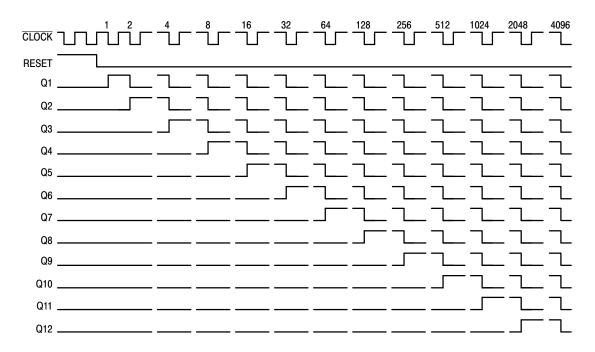


Figure 3. Timing Diagram

APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting

outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

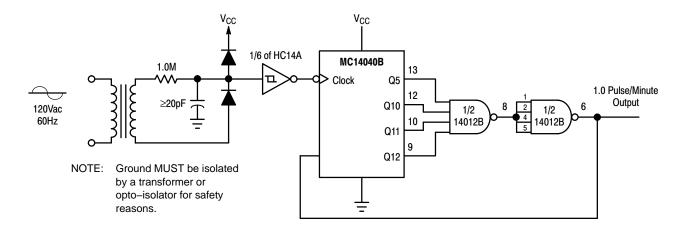
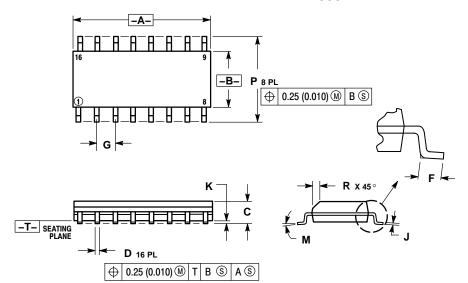


Figure 4. Time-Base Generator

PACKAGE DIMENSIONS

SOIC-16 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE K



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

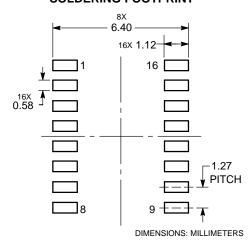
 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTEINSION.
 - PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- MAXIMUM MOLD PHO HUSION 0.15 (0.006) PER SIDE DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

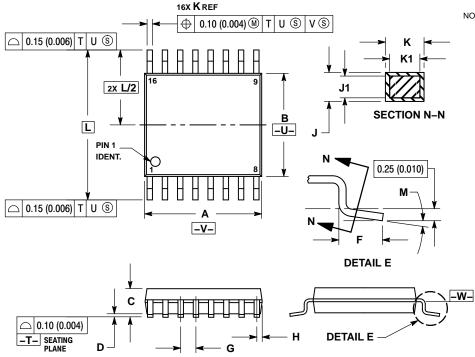
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-16 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948F **ISSUE B**

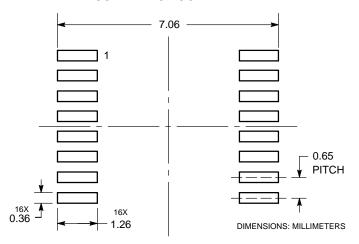


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08
 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
C		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.18	0.28	0.007	0.011
L	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
Κ	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252	BSC
М	0°	8 °	0°	8 °

SOLDERING FOOTPRINT*

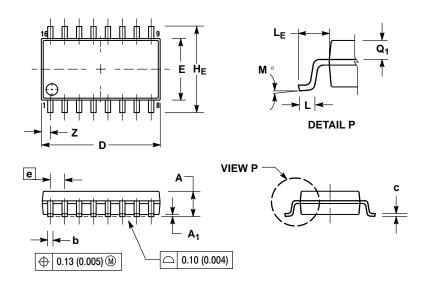


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOEIAJ-16 F SUFFIX

PLASTIC EIAJ SOIC PACKAGE CASE 966 ISSUE A



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10°
Q ₁	0.70	0.90	0.028	0.035
Z	-	0.78		0.031

ON Semiconductor and the unare registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent–Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal inju

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81–3–5817–1050 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Counter ICs category:

Click to view products by ON Semiconductor manufacturer:

Other Similar products are found below:

CD4018BE CD4033BE CD4060BE NLV14040BDR2G NLV14017BDG TC74VHC4040F(E,K,F 74VHC163FT 74VHC161FT(BJ)

74VHC163FT(BJ) 74HC393D.652 74HC4040D.653 74HCT4040D.653 74HC191D.652 HEF4060BT.653 HEF4518BT.652 74HC160D,652

74HC390DB,118 74HC163PW.112 74HC191PW.112 74HC390PW.112 74HC393DB.118 74HC4024D.652 74HCT193DB.112

74HCT390DB.112 74HC193PW.112 74HC390D.652 74HC4017PW.112 74HC4020DB.112 74HC4020PW.112 74HC4040DB.112

74HC4040PW.112 74HC4060DB.112 74HC4520D.112 74HCT393DB.112 74HCT6323AD.112 74LV393D.112 74LV393PW.112

74LV4060D.112 74LV4060DB.112 74LV4060PW.112 74LVC161D.112 74LVC161PW.112 XD74LS90 XD74LS93 CD4017BE

XD74LS161 XD74LS192 XD74LS193 CD4060BE XD4553