

# 8-Input Data Selector/ Multiplexer with 3-State Outputs

## High-Performance Silicon-Gate CMOS

### MC74HC251A

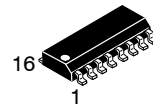
The MC74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the  $\bar{Y}$  outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

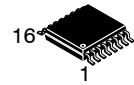
The HC251 is similar in function to the HC251 which does not have 3-state outputs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOIC-16  
D SUFFIX  
CASE 751B

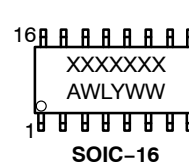


TSSOP-16  
DT SUFFIX  
CASE 948F

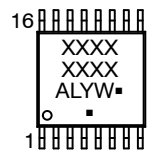


QFN16  
MN SUFFIX  
CASE 485AW

#### MARKING DIAGRAMS



SOIC-16



TSSOP-16



QFN16

XXXXXXX = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

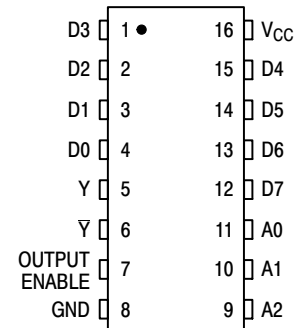
Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

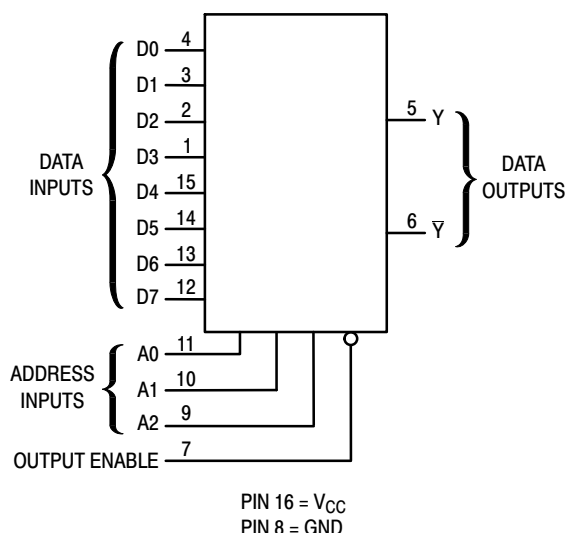
#### PIN ASSIGNMENT



#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

# MC74HC251A



**Figure 1. Logic Diagram**

**FUNCTION TABLE**

| Inputs |    |    |                | Outputs |            |
|--------|----|----|----------------|---------|------------|
| A2     | A1 | A0 | Output Enabled | Y       | $\bar{Y}$  |
| X      | X  | X  | H              | Z       | $\bar{Z}$  |
| L      | L  | L  | L              | D0      | $\bar{D0}$ |
| L      | L  | H  | L              | D1      | $\bar{D1}$ |
| L      | H  | L  | L              | D2      | $\bar{D2}$ |
| L      | H  | H  | L              | D3      | $\bar{D3}$ |
| H      | L  | L  | L              | D4      | $\bar{D4}$ |
| H      | L  | H  | L              | D5      | $\bar{D5}$ |
| H      | H  | L  | L              | D6      | $\bar{D6}$ |
| H      | H  | H  | L              | D7      | $\bar{D7}$ |

Z = high impedance

D0, D1, ..., D7 = the level of the respective D input.

## MAXIMUM RATINGS

| Symbol           | Parameter                                                                           | Value                           | Unit |
|------------------|-------------------------------------------------------------------------------------|---------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage                                                                   | −0.5 to +6.5                    | V    |
| V <sub>IN</sub>  | DC Input Voltage                                                                    | −0.5 to V <sub>CC</sub> +0.5    | V    |
| V <sub>OUT</sub> | DC Output Voltage                                                                   | −0.5 to V <sub>CC</sub> +0.5    | V    |
| I <sub>IN</sub>  | DC Input Diode Current, per Pin                                                     | ±20                             | mA   |
| I <sub>OUT</sub> | DC Input Diode Current, Per Pin                                                     | ±25                             | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                     | ±50                             | mA   |
| I <sub>IK</sub>  | Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )     | ±20                             | mA   |
| I <sub>OK</sub>  | Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> )  | ±20                             | mA   |
| T <sub>STG</sub> | Storage Temperature Range                                                           | −65 to +150                     | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 secs                                        | 260                             | °C   |
| T <sub>J</sub>   | Junction Temperature Under Bias                                                     | +150                            | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Note 1)<br><div>SOIC−16<br/>QFN16<br/>TSSOP−16</div>            | <div>126<br/>118<br/>159</div>  | °C/W |
| P <sub>D</sub>   | Power Dissipation in Still Air at 25°C<br><div>SOIC−16<br/>QFN16<br/>TSSOP−16</div> | <div>995<br/>1062<br/>787</div> | mW   |
| MSL              | Moisture Sensitivity                                                                | Level 1                         | –    |
| F <sub>R</sub>   | Flammability Rating<br>Oxygen Index: 28 to 34                                       | UL 94 V−0 @ 0.125 in            | –    |
| V <sub>ESD</sub> | ESD Withstand Voltage (Note 2)<br>Human Body Model<br>Charged Device Model          | <div>2000<br/>N/A</div>         | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

# MC74HC251A

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                                                                                 | Min         | Max                | Unit |
|-------------------|-----------------------------------------------------------------------------------------------------------|-------------|--------------------|------|
| $V_{CC}$          | DC Supply Voltage                                                                                         | 2.0         | 6.0                | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Note 3)                                                                 | 0           | $V_{CC}$           | V    |
| $T_A$             | Operating Temperature, All Package Types                                                                  | -55         | +125               | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>$V_{CC} = 2.0\text{ V}$<br>$V_{CC} = 4.5\text{ V}$<br>$V_{CC} = 6.0\text{ V}$ | 0<br>0<br>0 | 1000<br>500<br>400 | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol   | Parameter                                      | Test Conditions                                                                                | $V_{CC}$<br>V     | Guaranteed Limit   |                    |                    | Unit |
|----------|------------------------------------------------|------------------------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
|          |                                                |                                                                                                |                   | - 55 to<br>25°C    | ≤ 85°C             | ≤ 125°C            |      |
| $V_{IH}$ | Minimum High-Level Input Voltage               | $V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$  | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| $V_{IL}$ | Maximum Low-Level Input Voltage                | $V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$  | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| $V_{OH}$ | Minimum High-Level Output Voltage              | $V_{in} = V_{IH}$ or $V_{IL}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$                        | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|          |                                                | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0\text{ mA}$<br>$ I_{out}  \leq 5.2\text{ mA}$ | 4.5<br>6.0        | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| $V_{OL}$ | Maximum Low-Level Output Voltage               | $V_{in} = V_{IH}$ or $V_{IL}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$                        | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|          |                                                | $V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0\text{ mA}$<br>$ I_{out}  \leq 5.2\text{ mA}$ | 4.5<br>6.0        | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| $I_{in}$ | Maximum Input Leakage Current                  | $V_{in} = V_{CC}$ or GND                                                                       | 6.0               | ± 0.1              | ± 1.0              | ± 1.0              | μA   |
| $I_{OZ}$ | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>$V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{out} = V_{CC}$ or GND   | 6.0               | ± 0.5              | ± 5.0              | ± 10               | μA   |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$I_{out} = 0\text{ }\mu\text{A}$                                   | 6.0               | 8                  | 80                 | 160                | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

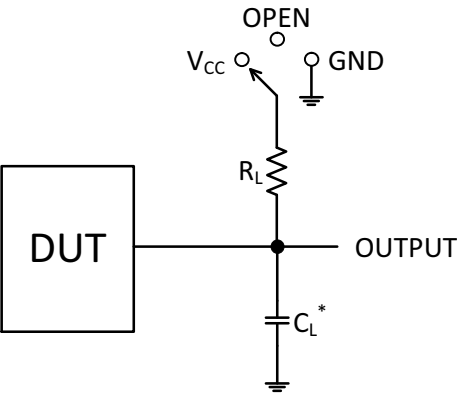
# MC74HC251A

## AC ELECTRICAL CHARACTERISTICS

| Symbol                                 | Parameter                                                                        | V <sub>CC</sub><br>V | Guaranteed Limit |                 |                 | Unit |
|----------------------------------------|----------------------------------------------------------------------------------|----------------------|------------------|-----------------|-----------------|------|
|                                        |                                                                                  |                      | – 55 to 25°C     | ≤ 85°C          | ≤ 125°C         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input D to Output Y or $\bar{Y}$<br>(Figures 2, 3, 4) | 2.0<br>4.5<br>6.0    | 185<br>37<br>31  | 230<br>46<br>39 | 280<br>56<br>48 | ns   |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A to Output Y or $\bar{Y}$<br>(Figures 2, 5)    | 2.0<br>4.5<br>6.0    | 205<br>41<br>35  | 255<br>51<br>43 | 310<br>62<br>53 | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 5, 7)           | 2.0<br>4.5<br>6.0    | 195<br>39<br>33  | 245<br>49<br>42 | 295<br>59<br>50 | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 2, 6)           | 2.0<br>4.5<br>6.0    | 145<br>29<br>25  | 180<br>36<br>31 | 220<br>44<br>38 | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Output $\bar{Y}$<br>(Figures 2, 6)   | 2.0<br>4.5<br>6.0    | 220<br>44<br>37  | 275<br>55<br>47 | 330<br>66<br>56 | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Output $\bar{Y}$<br>(Figures 2, 6)   | 2.0<br>4.5<br>6.0    | 150<br>30<br>26  | 190<br>38<br>33 | 225<br>45<br>38 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 2, 3, 4)                  | 2.0<br>4.5<br>6.0    | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                        | –                    | 10               | 10              | 10              | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State)       | –                    | 15               | 15              | 15              | pF   |

|                 |                                             |                                         |    |
|-----------------|---------------------------------------------|-----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package) | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                             | 36                                      |    |

MC74HC251A



\*C<sub>L</sub> Includes probe and jig capacitance

| Test                                | Switch Position | C <sub>L</sub> | R <sub>L</sub> |
|-------------------------------------|-----------------|----------------|----------------|
| t <sub>PLH</sub> / t <sub>PHL</sub> | Open            | 50 pF          | 1 kΩ           |
| t <sub>PLZ</sub> / t <sub>PZL</sub> | V <sub>CC</sub> |                |                |
| t <sub>PHZ</sub> / t <sub>PZH</sub> | GND             |                |                |

Figure 2. Test Circuit

SWITCHING WAVEFORMS

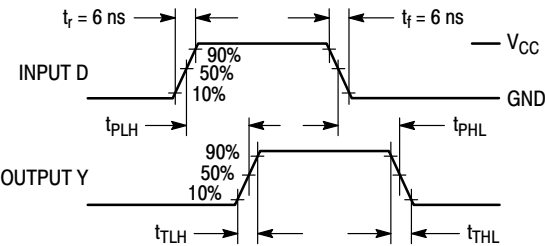


Figure 3.

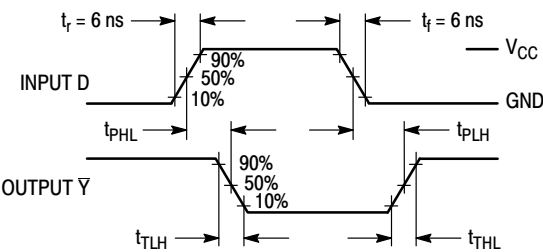


Figure 4.

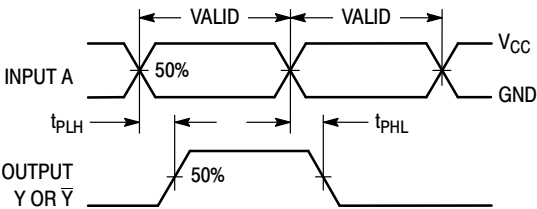


Figure 5.

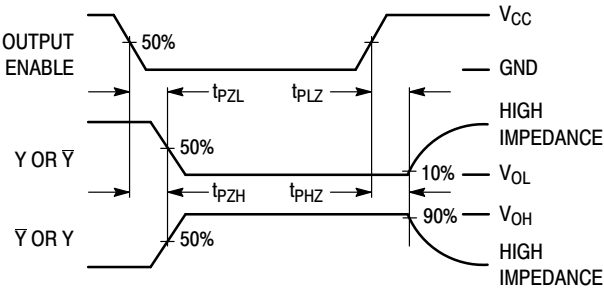


Figure 6.

# MC74HC251A

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0, A1, A2 (Pins 1, 2, 3)**

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

### CONTROL INPUTS

**CS1, CS2, CS3 (Pins 6, 4, 5)**

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the

Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic low.

### OUTPUTS

**Y0 – Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)**

Active-high Decoded outputs. These outputs assume a high level when addressed and the chip is selected. These outputs remain low when not addressed or the chip is not selected.

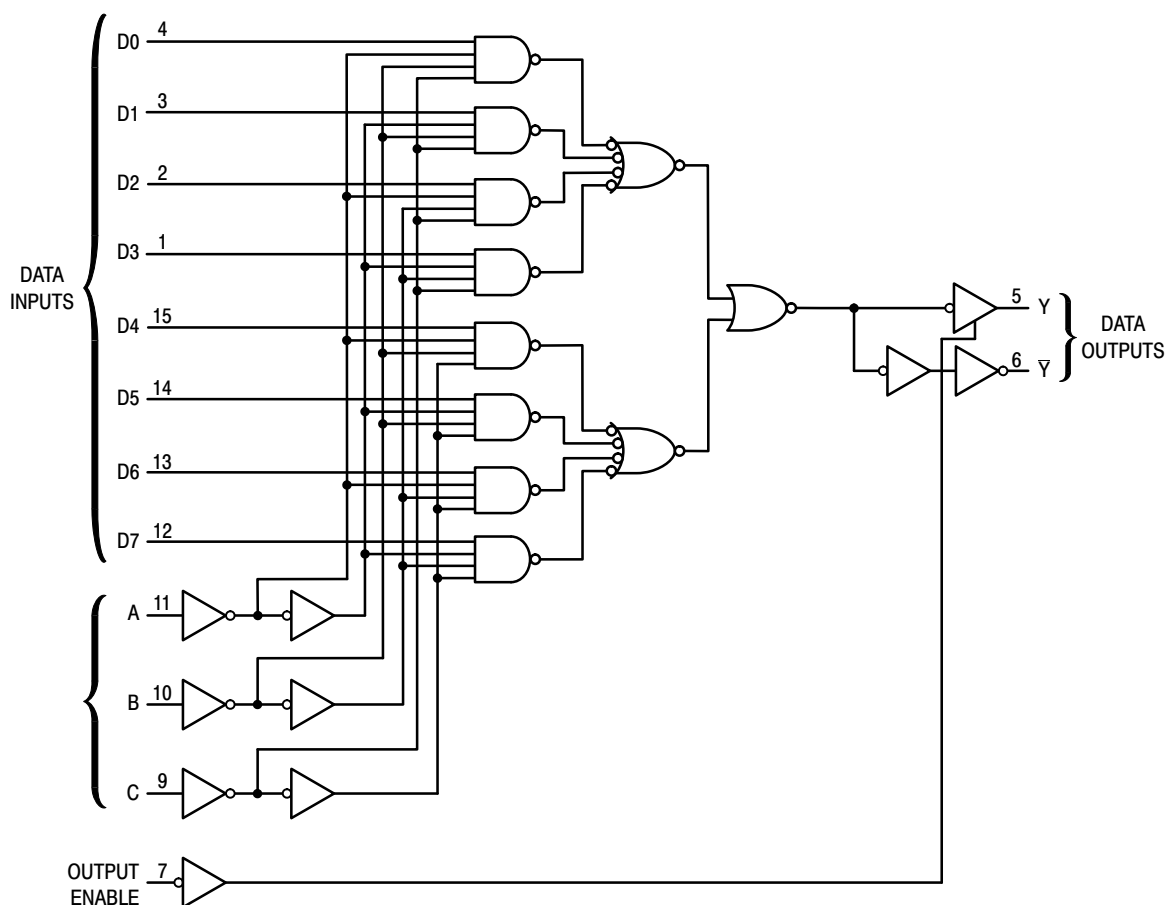


Figure 7. Expanded Logic Diagram

## ORDERING INFORMATION

| Device            | Marking    | Package  | Shipping†                |
|-------------------|------------|----------|--------------------------|
| MC74HC251ADG      | HC251AG    | SOIC-16  | 48 Units / Rail          |
| MC74HC251ADR2G    | HC251AG    | SOIC-16  | 2500 Units / Tape & Reel |
| MC74HC251ADR2G-Q* | HC251AG    | SOIC-16  | 2500 Units / Tape & Reel |
| MC74HC251ADTG     | HC<br>251A | TSSOP-16 | 96 Units / Rail          |
| MC74HC251ADTR2G   | HC<br>251A | TSSOP-16 | 2500 Units / Tape & Reel |

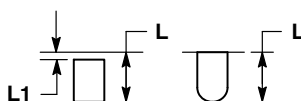
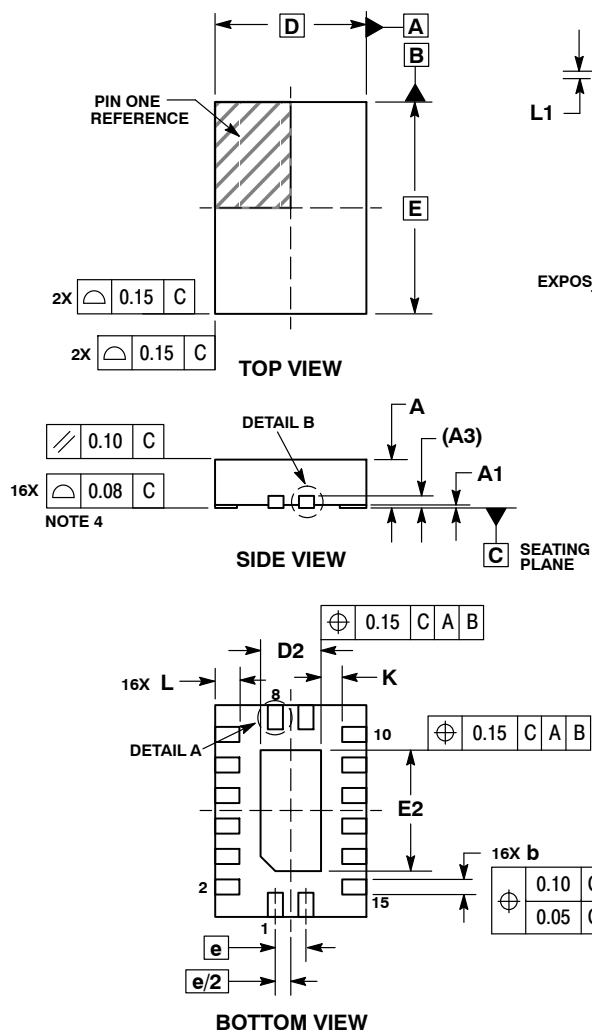
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

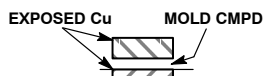
# MC74HC251A

## PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P  
CASE 485AW  
ISSUE O



**DETAIL A**  
ALTERNATE TERMINAL  
CONSTRUCTIONS



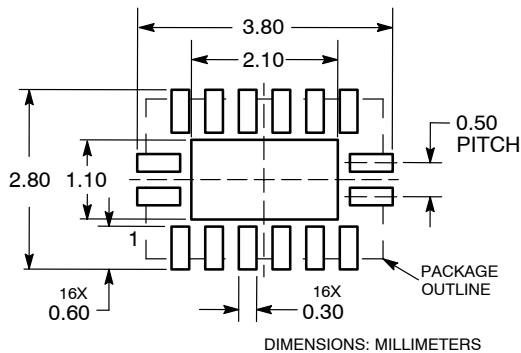
**DETAIL B**  
ALTERNATE  
CONSTRUCTIONS

### NOTES:

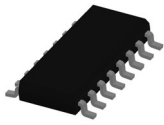
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20        | REF  |
| b   | 0.20        | 0.30 |
| D   | 2.50        | BSC  |
| D2  | 0.85        | 1.15 |
| E   | 3.50        | BSC  |
| E2  | 1.85        | 2.15 |
| e   | 0.50        | BSC  |
| K   | 0.20        | ---  |
| L   | 0.35        | 0.45 |
| L1  | ---         | 0.15 |

### RECOMMENDED SOLDERING FOOTPRINT\*



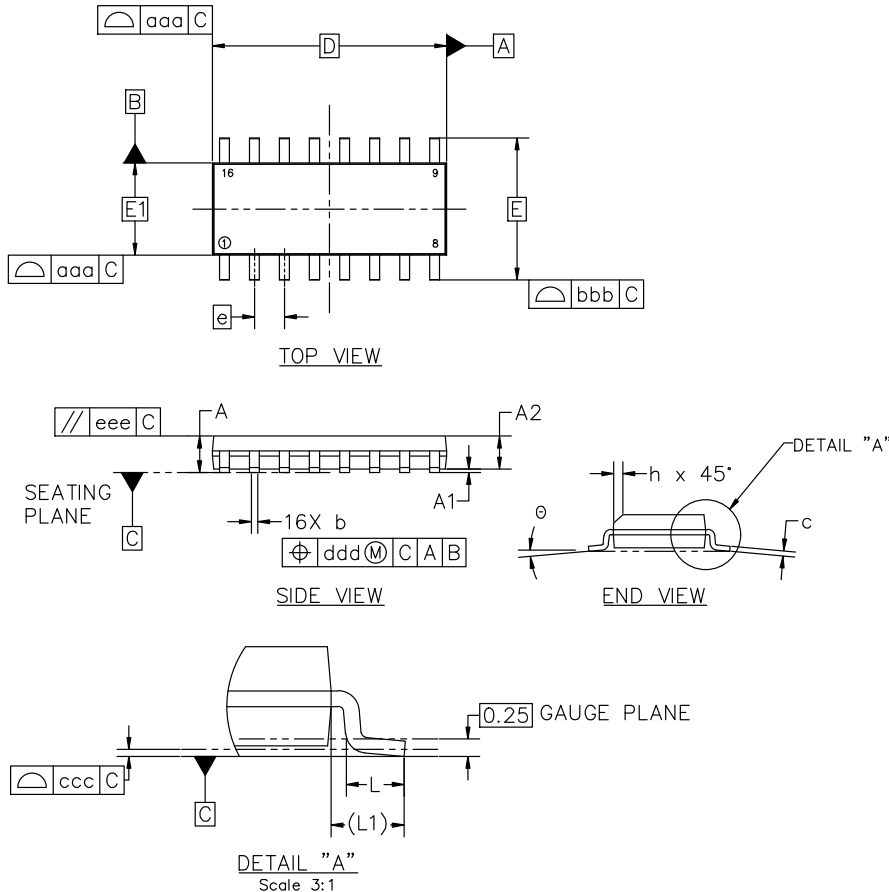
\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

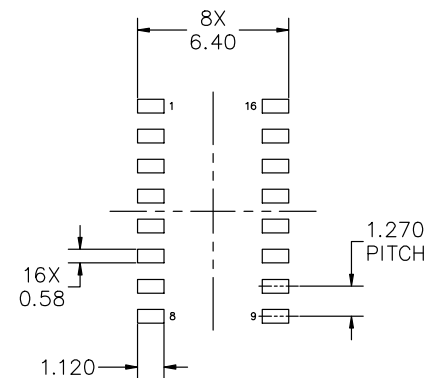
DATE 18 OCT 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS                    |          |      |      |
|--------------------------------|----------|------|------|
| DIM                            | MIN      | NOM  | MAX  |
| A                              | 1.35     | 1.55 | 1.75 |
| A1                             | 0.10     | 0.18 | 0.25 |
| A2                             | 1.25     | 1.37 | 1.50 |
| b                              | 0.35     | 0.42 | 0.49 |
| c                              | 0.19     | 0.22 | 0.25 |
| D                              | 9.90 BSC |      |      |
| E                              | 6.00 BSC |      |      |
| E1                             | 3.90 BSC |      |      |
| e                              | 1.27 BSC |      |      |
| h                              | 0.25     | ---  | 0.50 |
| L                              | 0.40     | 0.83 | 1.25 |
| L1                             | 1.05 REF |      |      |
| θ                              | 0°       | ---  | 7°   |
| TOLERANCE OF FORM AND POSITION |          |      |      |
| aaa                            | 0.10     |      |      |
| bbb                            | 0.20     |      |      |
| ccc                            | 0.10     |      |      |
| ddd                            | 0.25     |      |      |
| eee                            | 0.10     |      |      |



\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE onsemi SOLDERING  
AND MOUNTING TECHNIQUES REFERENCE  
MANUAL, SOLDERM/D

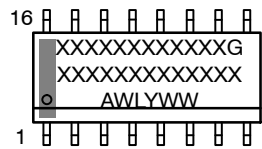
|                         |                                     |                                                                                                                                                                                     |
|-------------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42566B</b>                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-16 9.90X3.90X1.37 1.27P</b> | <b>PAGE 1 OF 2</b>                                                                                                                                                                  |

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SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

DATE 18 OCT 2024

GENERIC  
MARKING DIAGRAM\*

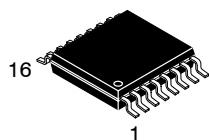


XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

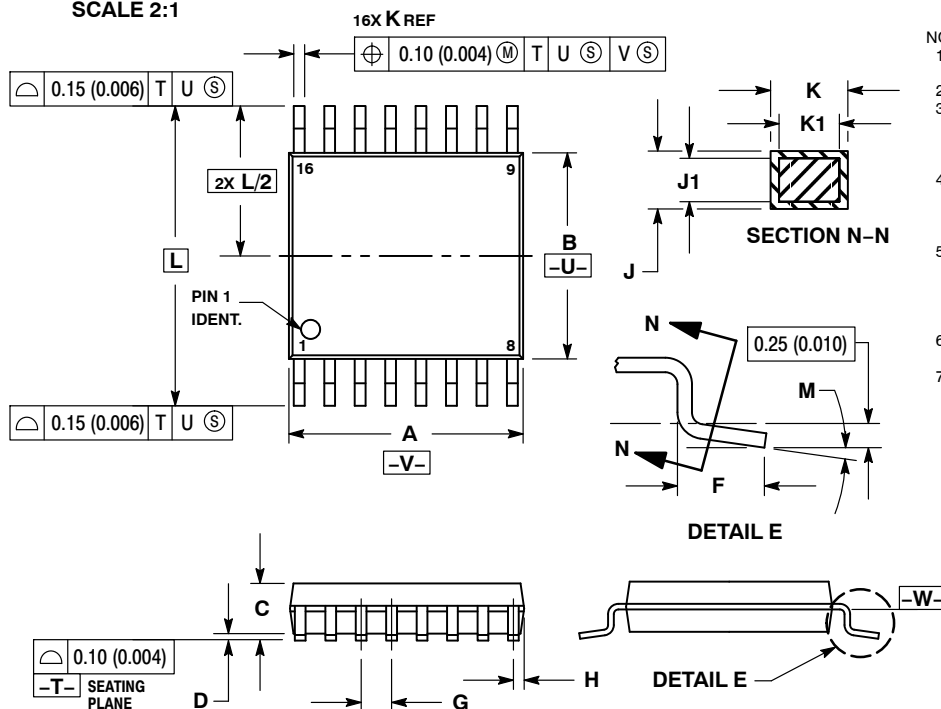
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER<br>4. NO CONNECTION<br>5. EMITTER<br>6. BASE<br>7. COLLECTOR<br>8. COLLECTOR<br>9. BASE<br>10. EMITTER<br>11. NO CONNECTION<br>12. EMITTER<br>13. BASE<br>14. COLLECTOR<br>15. EMITTER<br>16. COLLECTOR                           | STYLE 2:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION<br>4. CATHODE<br>5. CATHODE<br>6. NO CONNECTION<br>7. ANODE<br>8. CATHODE<br>9. CATHODE<br>10. ANODE<br>11. NO CONNECTION<br>12. CATHODE<br>13. CATHODE<br>14. NO CONNECTION<br>15. ANODE<br>16. CATHODE | STYLE 3:<br>PIN 1. COLLECTOR, DYE #1<br>2. BASE, #1<br>3. EMITTER, #1<br>4. COLLECTOR, #1<br>5. COLLECTOR, #2<br>6. BASE, #2<br>7. EMITTER, #2<br>8. COLLECTOR, #2<br>9. COLLECTOR, #3<br>10. BASE, #3<br>11. EMITTER, #3<br>12. COLLECTOR, #3<br>13. COLLECTOR, #4<br>14. BASE, #4<br>15. EMITTER, #4<br>16. COLLECTOR, #4                                                                                         | STYLE 4:<br>PIN 1. COLLECTOR, DYE #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #3<br>6. COLLECTOR, #3<br>7. COLLECTOR, #4<br>8. COLLECTOR, #4<br>9. BASE, #4<br>10. EMITTER, #4<br>11. BASE, #3<br>12. EMITTER, #3<br>13. BASE, #2<br>14. EMITTER, #2<br>15. BASE, #1<br>16. EMITTER, #1 |
| STYLE 5:<br>PIN 1. DRAIN, DYE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. DRAIN, #3<br>6. DRAIN, #3<br>7. DRAIN, #4<br>8. DRAIN, #4<br>9. GATE, #4<br>10. SOURCE, #4<br>11. GATE, #3<br>12. SOURCE, #3<br>13. GATE, #2<br>14. SOURCE, #2<br>15. GATE, #1<br>16. SOURCE, #1 | STYLE 6:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE<br>7. CATHODE<br>8. CATHODE<br>9. ANODE<br>10. ANODE<br>11. ANODE<br>12. ANODE<br>13. ANODE<br>14. ANODE<br>15. ANODE<br>16. ANODE                                 | STYLE 7:<br>PIN 1. SOURCE N-CH<br>2. COMMON DRAIN (OUTPUT)<br>3. COMMON DRAIN (OUTPUT)<br>4. GATE P-CH<br>5. COMMON DRAIN (OUTPUT)<br>6. COMMON DRAIN (OUTPUT)<br>7. COMMON DRAIN (OUTPUT)<br>8. SOURCE P-CH<br>9. SOURCE P-CH<br>10. COMMON DRAIN (OUTPUT)<br>11. COMMON DRAIN (OUTPUT)<br>12. COMMON DRAIN (OUTPUT)<br>13. GATE N-CH<br>14. COMMON DRAIN (OUTPUT)<br>15. COMMON DRAIN (OUTPUT)<br>16. SOURCE N-CH |                                                                                                                                                                                                                                                                                                                             |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                              |                                                                                                                                                                                     |
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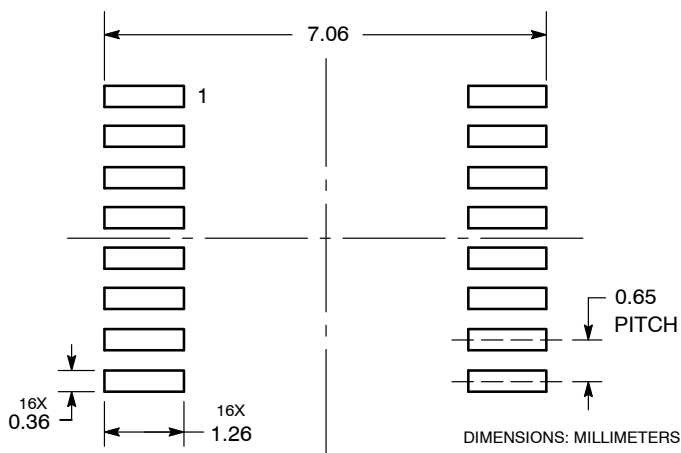

**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006

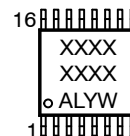

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                    |                                                                                                                                                                                  |
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| <b>DESCRIPTION:</b>     | <b>TSSOP-16</b>    | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

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[74HCT138D-Q100,118](#) [SY89113UMY-TR](#) [74HCT139D-Q100J](#) [74LVC1G19GM,115](#)