QorIQ T1040 Reference Design Board User Guide

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Chapter 1
Overview

This manual describes the features and operation of a high performance reference platform that supports QorIQ Power Architecture® processors including:

- T1040
- T1020

The T1040RDB is optimized to support high-bandwidth DDR3L memory and a full complement of high-speed SerDes ports.

NOTE

The dual-core version of the T1040 SoC is known as T1020.

1.1 Related documentation

The documents below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Related documentation

Document name	Description
QorIQ T1040, T1020 Data Sheet (T1040, T1020)	Provides specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations
QorIQ T1040 Reference Manual (T1040RM)	This document provides a detailed description on the QorIQ T1040 multicore processor, and its features, such as memory map, serial interfaces, power supply, chip features, and clock information.

1.2 Acronyms and abbreviations

The following table contains acronyms and abbreviations used in this document.

Table 1-2. Acronyms and abbreviations

Term	Description
COP	Common On-chip Processor
CPC	CoreNet Platform Cache
CPLD	Complex Programmable Logic Device
DIMM	Dual in-line memory module
DIP	Dual in-line package
DMA	Direct Memory Access
DPAA	Data Path Acceleration Architecture
DRAM	Dynamic random-access memory
DUT	Device under test
ECC	Error detection and correction
EMI	Ethernet Management interface
eSDHC	Enhanced Secure Digital Host Controller
eSPI	Enhanced Serial Peripheral Interface
FXS	Foreign Exchange Station
FXO	Foreign Exchange Office
I^2C	Inter - Integrated Circuit
IFC	Integrated Flash Controller
JTAG	Joint Test Action Group
MDC	Management Data Clock
MDIO	Management Data Input/Output
PCIe	PCI Express
POR	Power-on reset
PSU	Power Supply Unit
QMan	Queue Manager
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
SYSCLK	System Clock
UART	Universal asynchronous receiver/transmitter
VCC	Voltage for circuit
VTT	Voltage for terminal

1.3 Silicon features

NOTE

For a description of the features of the T1040 SoC, see QorIQ T1040 Reference Manual (T1040RM).

1.4 Board features

The features of the T1040RDB-PA board are as follows:

- Eight lanes of SerDes connections with support for:
  - PCIe that supports Gen 1 and Gen 2
  - SGMII
  - QSGMII
  - SATA 2.0
- DDR controller
  - Supports data rates up to 1600 MHz
  - Supports one DDR3L DIMM of single-, dual-, or quad-rank type
  - DDR power supply (1.35 V) with automatic tracking of VTT
- IFC
  - NAND flash: 8-bit, async, 1 GB
  - NOR: 16-bit, non-multiplexed, 128 MB, support of eight virtual banks
- Ethernet
  - Two onboard RGMII 10/100/1G Ethernet ports, PHY #0 remains powered up during deep-sleep
  - One onboard SGMII 10/100/1G Ethernet Port
  - Two onboard QSGMII 10/100/1G PHYs connecting to 8 GE ports
- CPLD
  - Manages system power and reset sequencing
  - Manages DUT, board, clock configuration
  - Reset and interrupt monitor and control
  - General fault monitoring and logging
  - Sleep mode control
- Clocks
  - SYSCLK at 100 MHz
  - DDRCLK at 66.66 MHz
  - USBCLK at 24 MHz
  - Single Oscillator Source reference clocking at 100 MHz
- Power Supplies

- Dedicated PMBus regulator for core power adjustable from 0.7 V to 1.3 V at 35 A

- USB
  - Supports two USB 2.0 ports with integrated PHYs. Two type A ports with 5 V@1.5 A per port
- SDHC port that connects directly to card slot
- SPI
  - One onboard 64 MB SPI flash
  - Onboard support of SPI EEPROM, TDM SLAC control, and TDM riser card control
- TDM interface through optional riser card, also support FXS/FXO on board
- I2C bus
  - Devices connected: EEPROM, thermal monitor, VCore power controller
- Other IO
  - Two serial ports

1.5 Block diagram

This section provides a high-level overview of the T1040 SoC and the T1040RDB board.

The figures below show the major functional units within the T1040 device and the T1040RDB board.

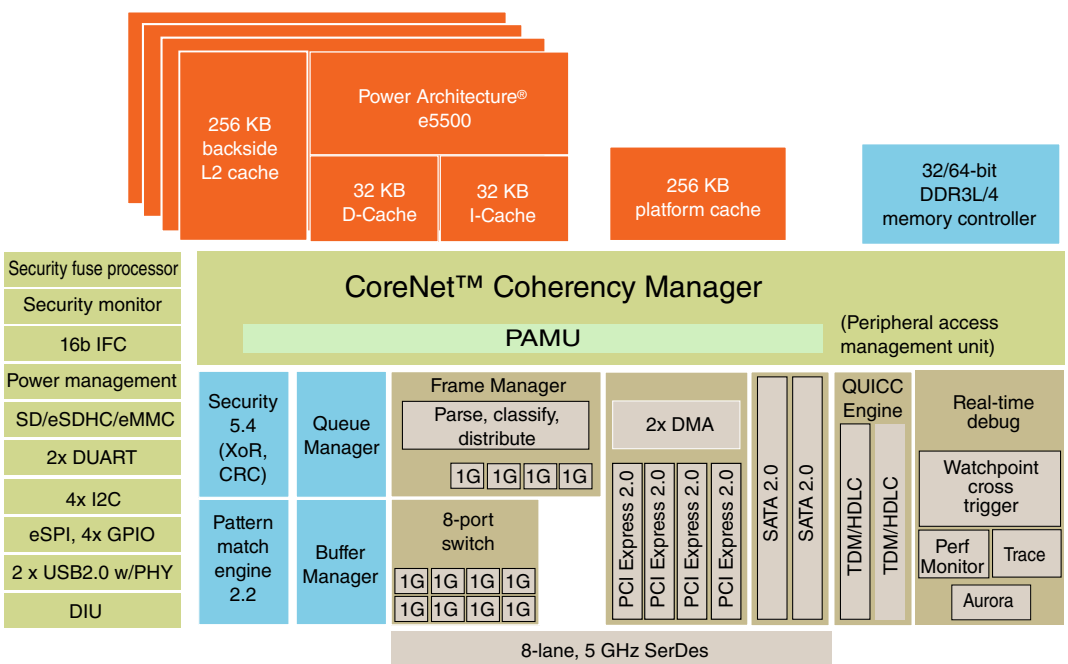


Figure 1-1. T1040 SoC block diagram

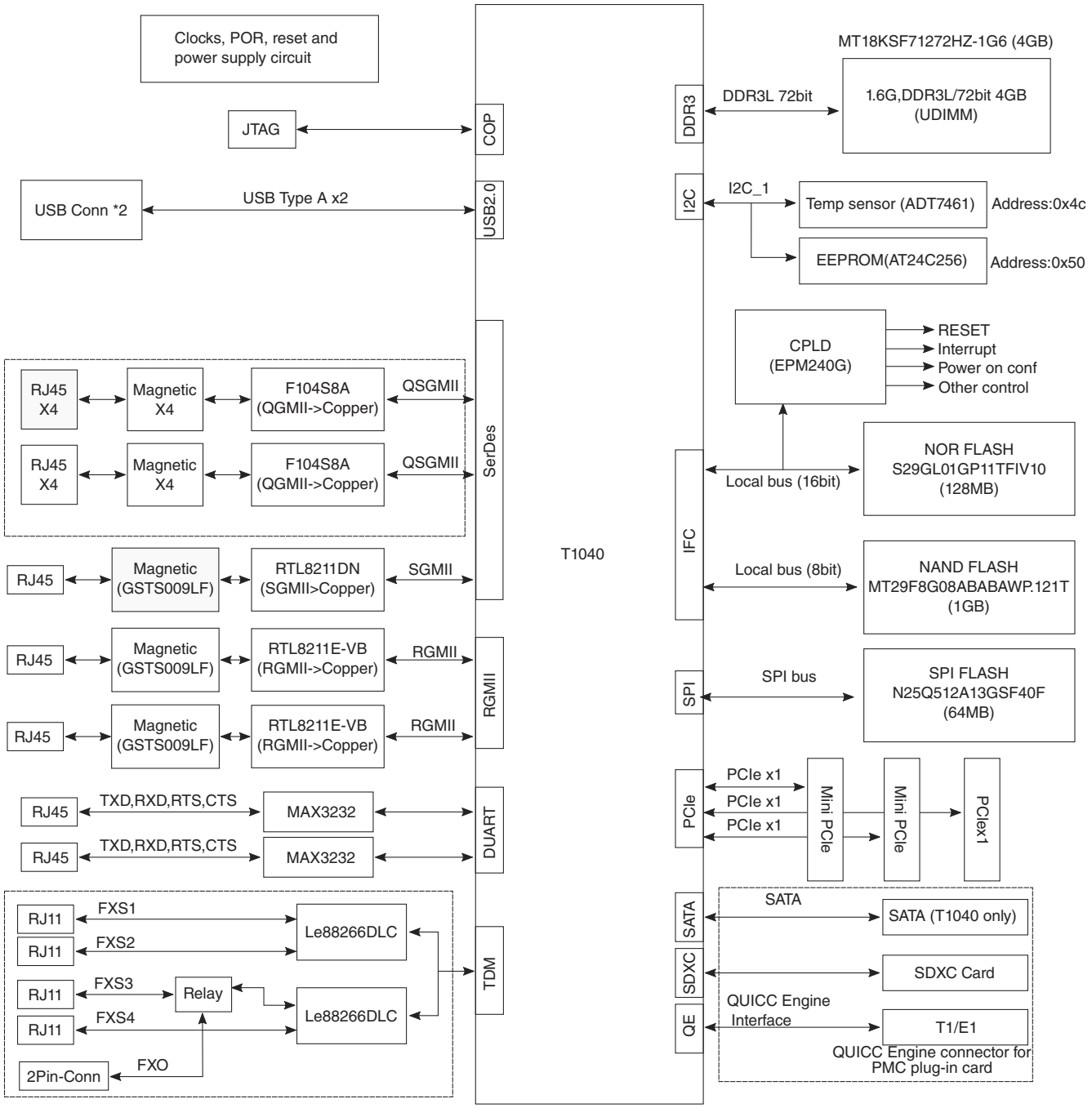


Figure 1-2. T1040RDB board block diagram

Chapter 2
Architecture

This section explains:

- Processor
- Power
- Clocks
- Reset
- DDR
- SerDes port
- Ethernet controllers
- Ethernet management interface
- I2C
- SPI interface
- Local bus
- SDHC interface
- USB interface
- Serial port
- SLIC/SLAC and TDM interface
- JTAG/COP port
- Connectors, headers, jumper, push buttons and LED
- Temperature
- DIP switch definition

2.1 Processor

The T1040RDB supports as many features of the T1040 as possible, as detailed in the following sections. The T1040RDB supports this by isolating OVDD-powered signals through external translation devices or the CPLD wherever required.

2.2 Power

The power supply system of the T1040RDB board uses power from a standard ATX power supply unit (PSU) to provide the required power supplies to the processor, CPLD, and peripheral devices. In addition to meeting required power specifications, the following goals guide the power supply architecture:

- Monolithic power supply for VCC that powers internal cores and platform logic
- T1040RDB can access IR36021 via software to check the current and voltage values or to program the voltage changes
- All power supplies are sequenced per hardware specifications

The figure below shows an overview of the power supply.

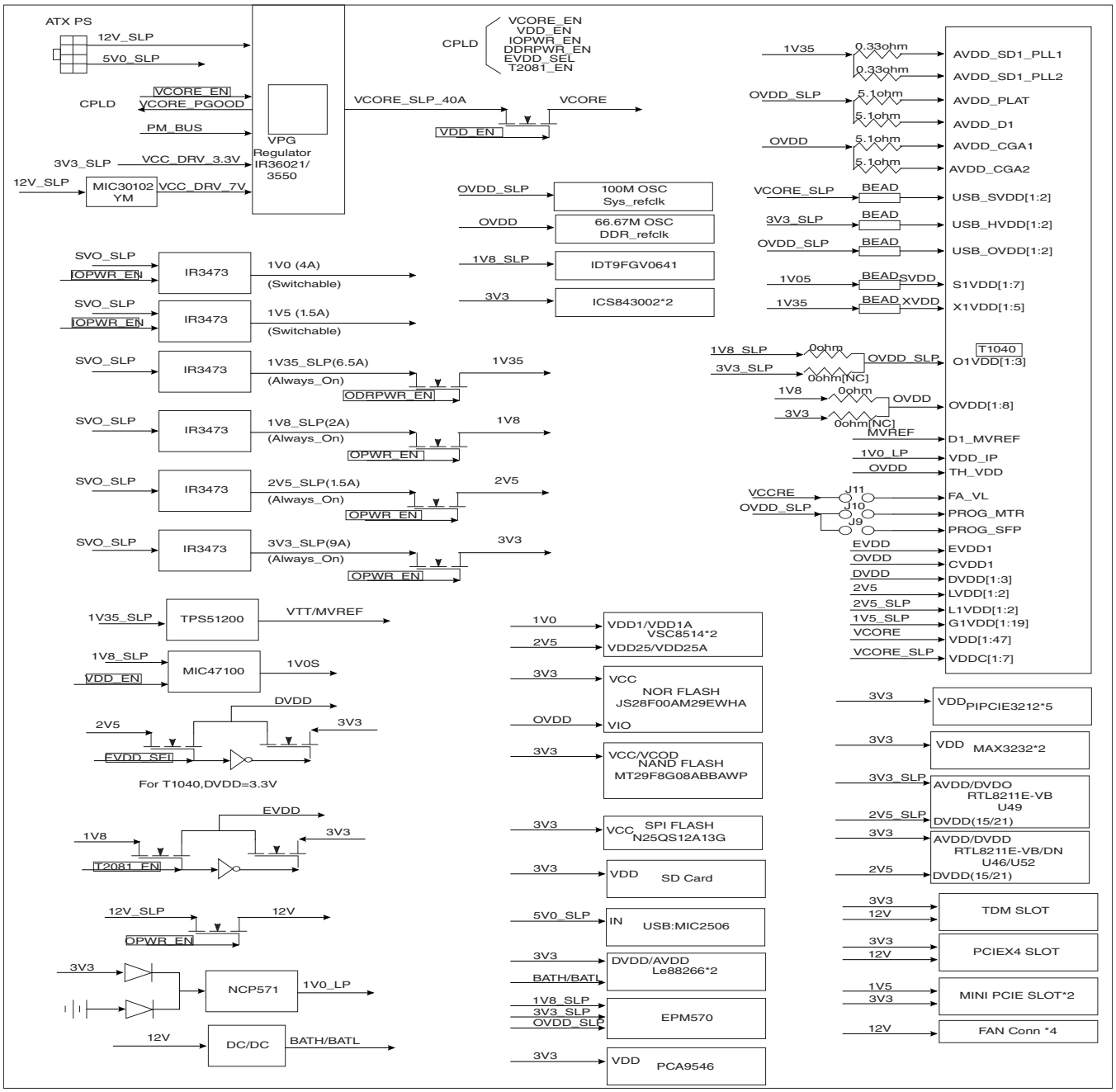


Figure 2-1. Power distribution

2.3 Clocks

The clock circuitry provides clocks for the processor for:

- SYSCLK (single-ended and differential)
- DDRCLK
- SerDes clocks (two independent options)

- Ethernet clocks
- USB clock

The architecture of the clock section is shown in the figure below.

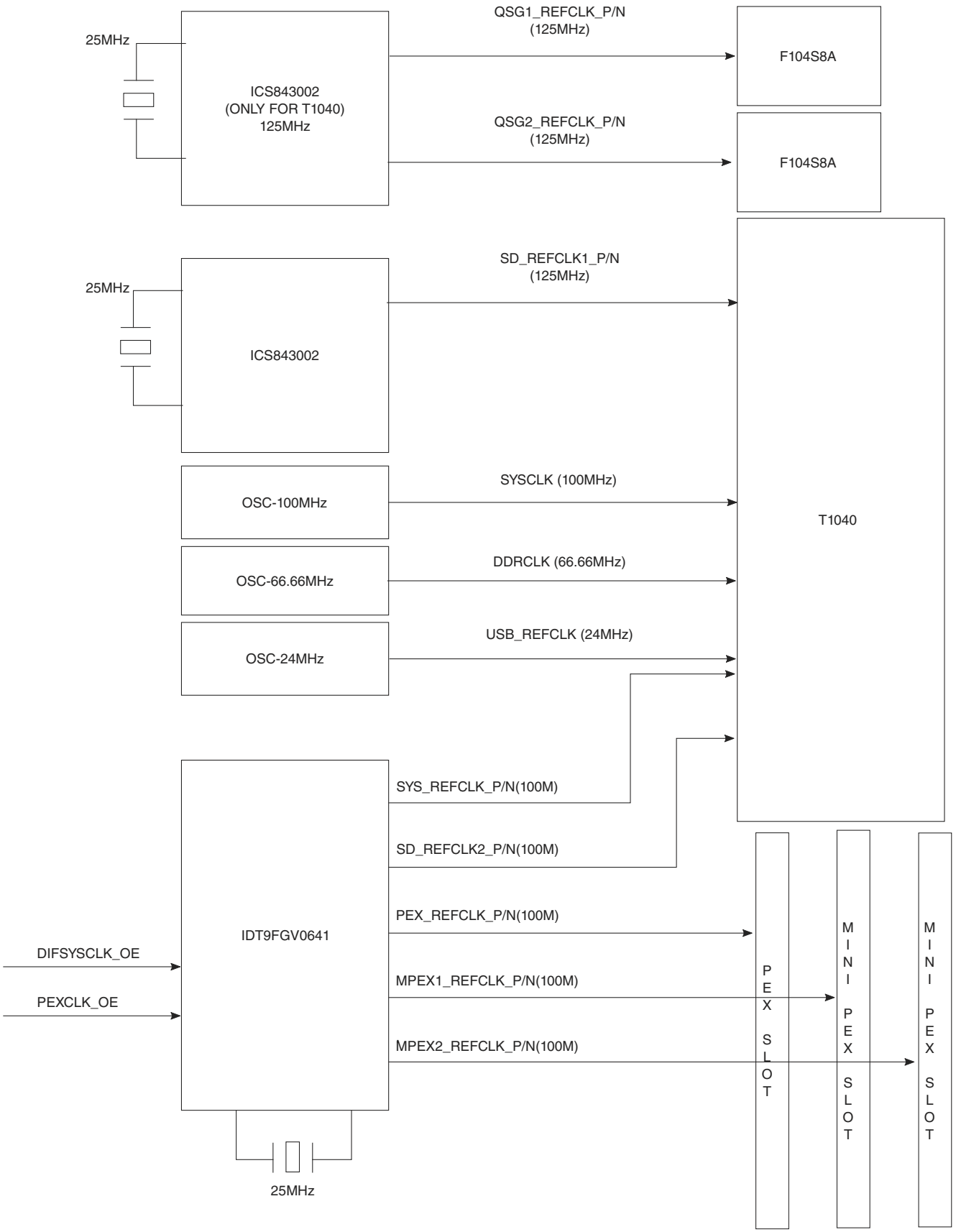


Figure 2-2. Clock distribution

2.4 Reset

The CPLD manages the reset signals to and from the T1040 processor and the other devices on the T1040RDB board. The figure below shows an overview of the reset architecture.

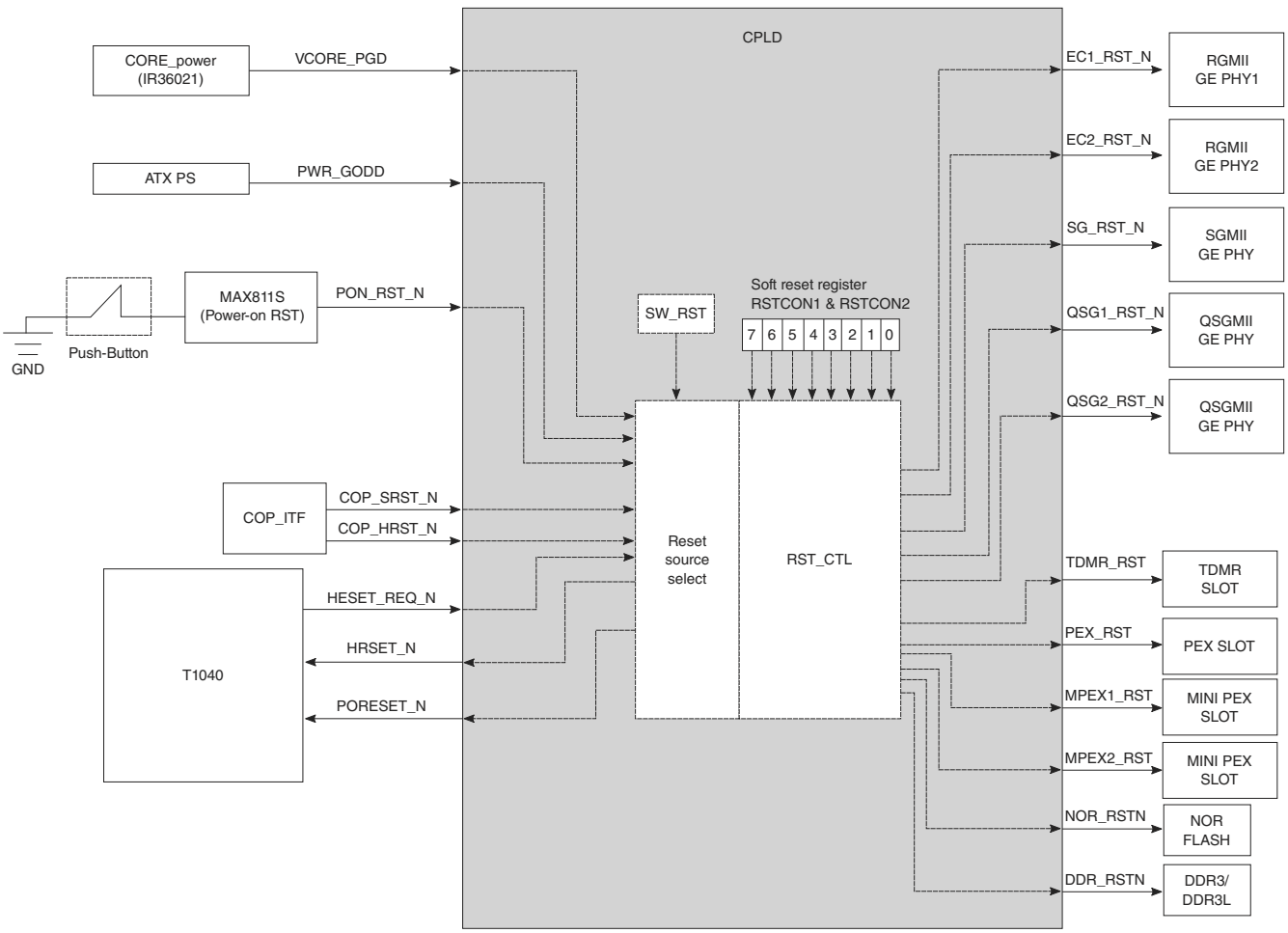


Figure 2-3. CPLD logical

2.5 DDR

The T1040RDB supports high-speed DRAM with an unbuffered DDR3L (240pin) socket (UDIMM), featuring single-, dual-, and quad-rank support. The memory interface includes all the necessary termination and I/O power, and is routed so as to achieve maximum performance of the memory bus, as shown in the below figure.

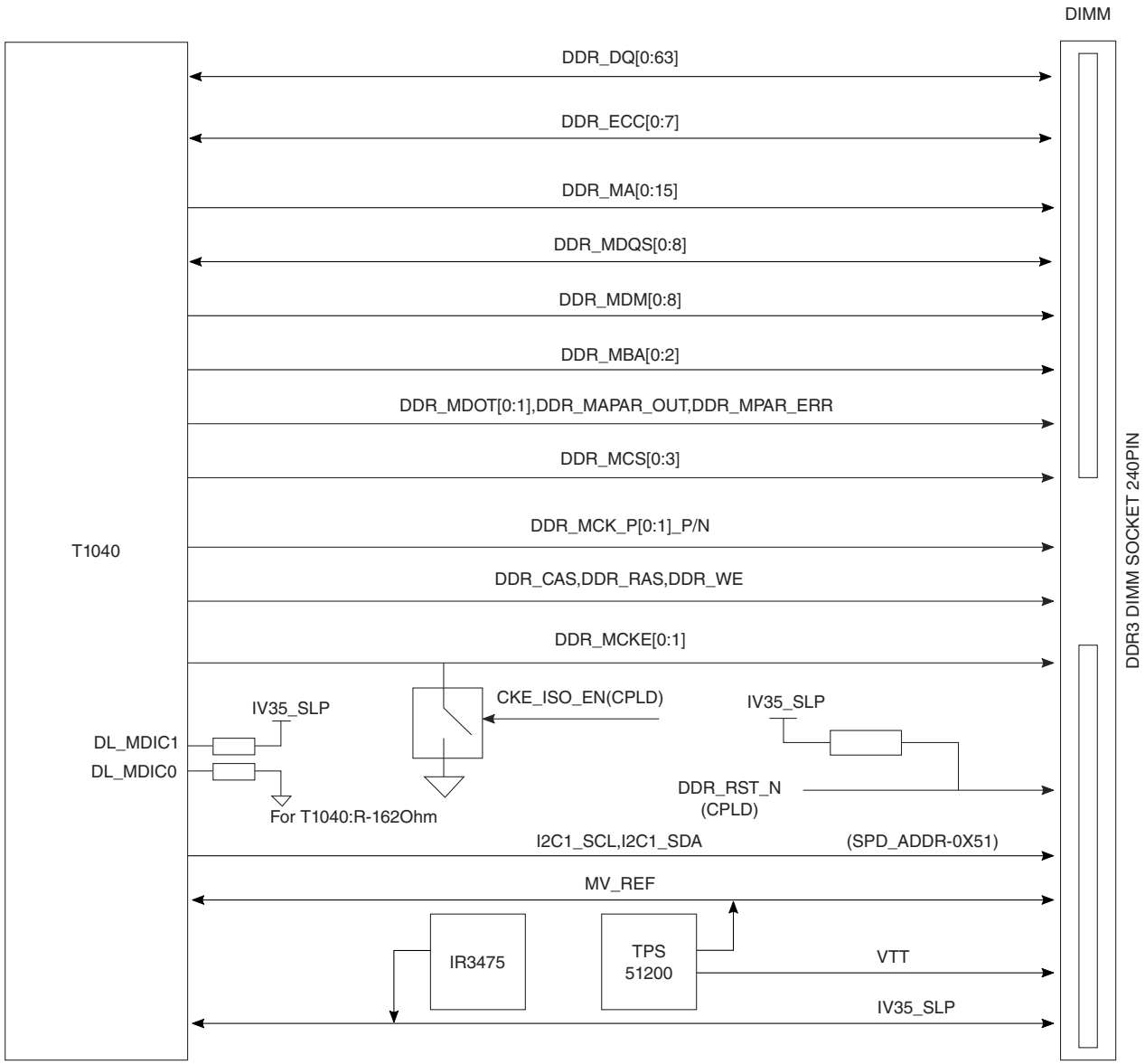


Figure 2-4. T1040 and DDR connection

Although the platforms support all types, ranks and speeds of DIMMs within the specification of the T1040, not all combinations of these three exist on the memory market. Thus, the system is shipped with a “representative” DIMM, as noted in the below table.

Other suitable memory DIMMs can be purchased and installed if needed; however, Freescale only supplies the device shown.

Table 2-1. DDR3L UDIMM support

Platform	Type	Speeds	Ranks	DIMM
T1040RDB	DDR3L	1600 MT/s	Single	Micron MT9KSF51272AZ-1G6

Table continues on the next page...

Table 2-1. DDR3L UDIMM support (continued)

			Dual	Micron MT18KSF51272AZ-1G6
			Quad	(TBD)

2.6 SerDes port

The T1040 SerDes block provides eight high-speed serial communication lanes supporting a variety of protocols, including:

- SGMII 1.25 Gbit/s
- QSGMII 5 Gbit/s
- PCIe Gen 1 x1 2.5 Gbit/s
- PCIe Gen 2 x1 5 Gbit/s
- SATA x1 1.5/3 Gbit/s

The following table explains the SerDes protocols supported on the T1040RDB board.

Table 2-2. SerDes protocol distribution

SerDes									
SRDS_PRTCL	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**Option**
T1040/T1020	PCIe	SGMII	QSGMII	QSGMII	PCIe	PCIe	PCIe	SATA	0x66

To comply with T1040 specifications, multiplexers are used to re-route and group the SerDes lanes as shown in the figure below.

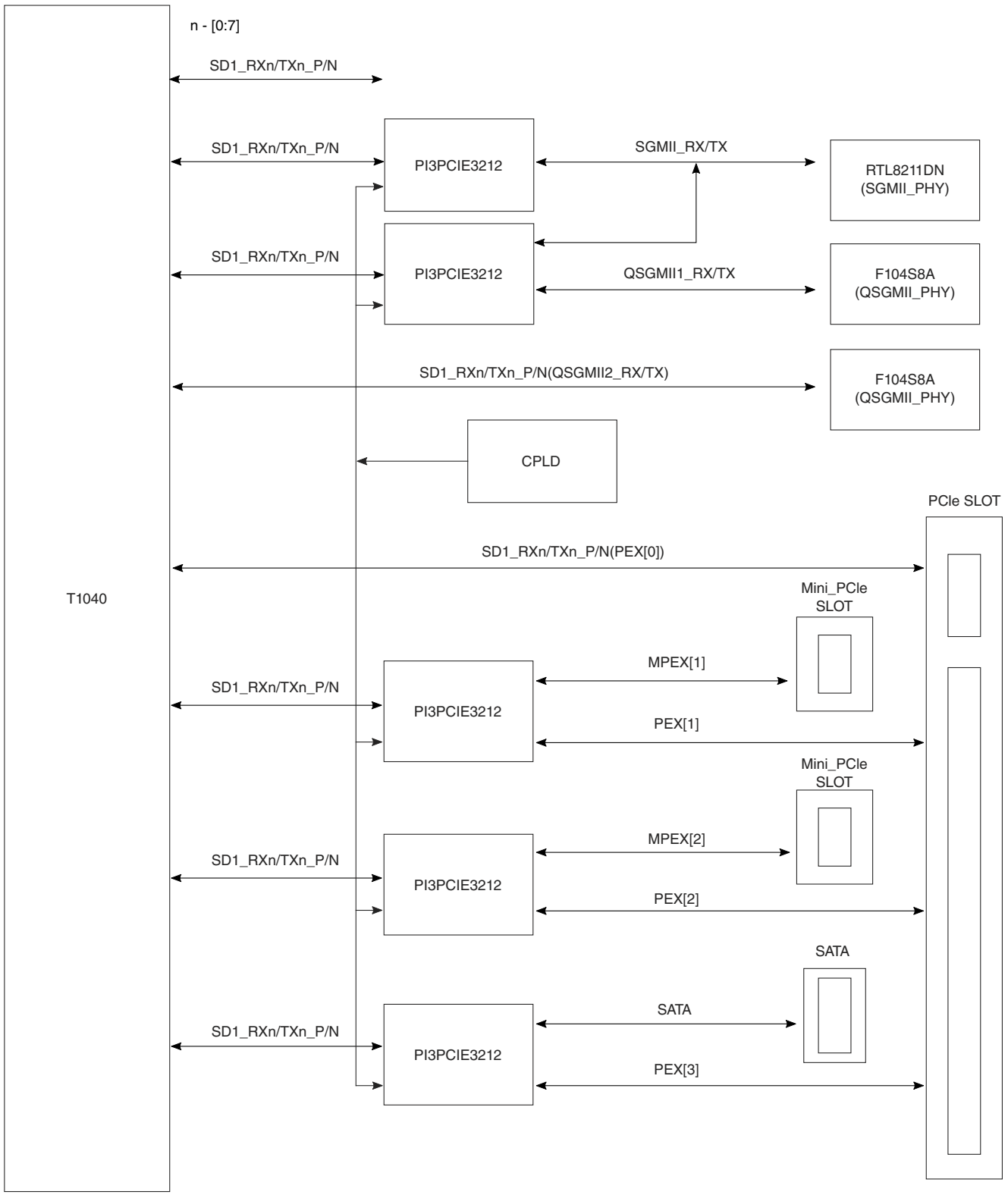


Figure 2-5. SerDes lane connections

2.6.1 PCIe support

The T1040RDB supports evaluation of PCIe using any standard PCIe Gen 1/Gen 2 card.

2.6.2 SGMII support

The T1040RDB board supports evaluation of the SGMII protocol using the RTL8211DN PHY.

The figure below shows the connectivity of the SGMII interface.

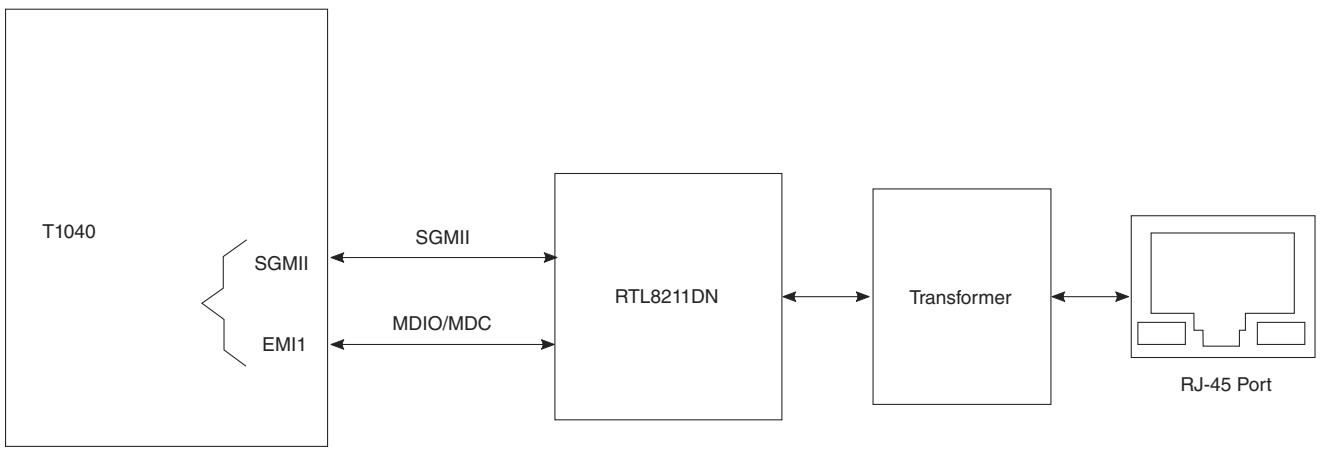


Figure 2-6. SGMII connection

2.6.3 QSGMII support

The T1040RDB board supports evaluation of the QSGMII protocol using an F104S8A four-port Ethernet PHY. The figure below shows the connectivity of the QSGMII interface.

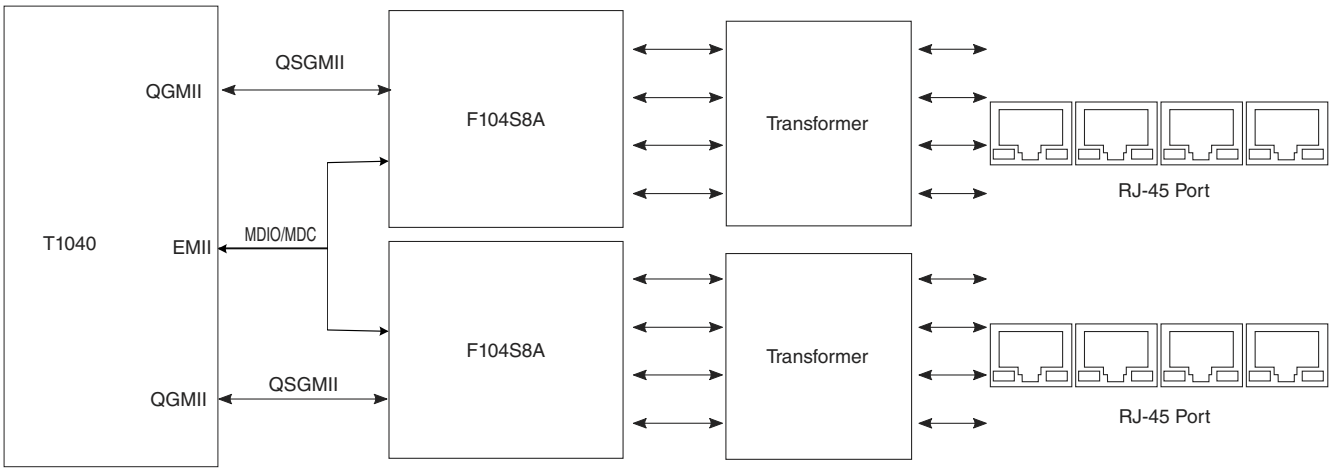


Figure 2-7. QSGMII connection

2.6.4 SATA support

SATA may be evaluated through an onboard SATA connector.

2.7 Ethernet controllers

The T1040 SoC supports two Ethernet controllers (EC), which can connect to the Ethernet PHYs using the MII or RGMII protocols. On the T1040RDB board, the EC1 and EC2 ports operate in the RGMII mode only. Both ports connect to the Realtek RTL8211 PHYs. The T1040RDB board supports energy efficient Ethernet on EC1 and sleep mode on EC2.

The figure below shows the connectivity of the EC1 and EC2 interfaces.

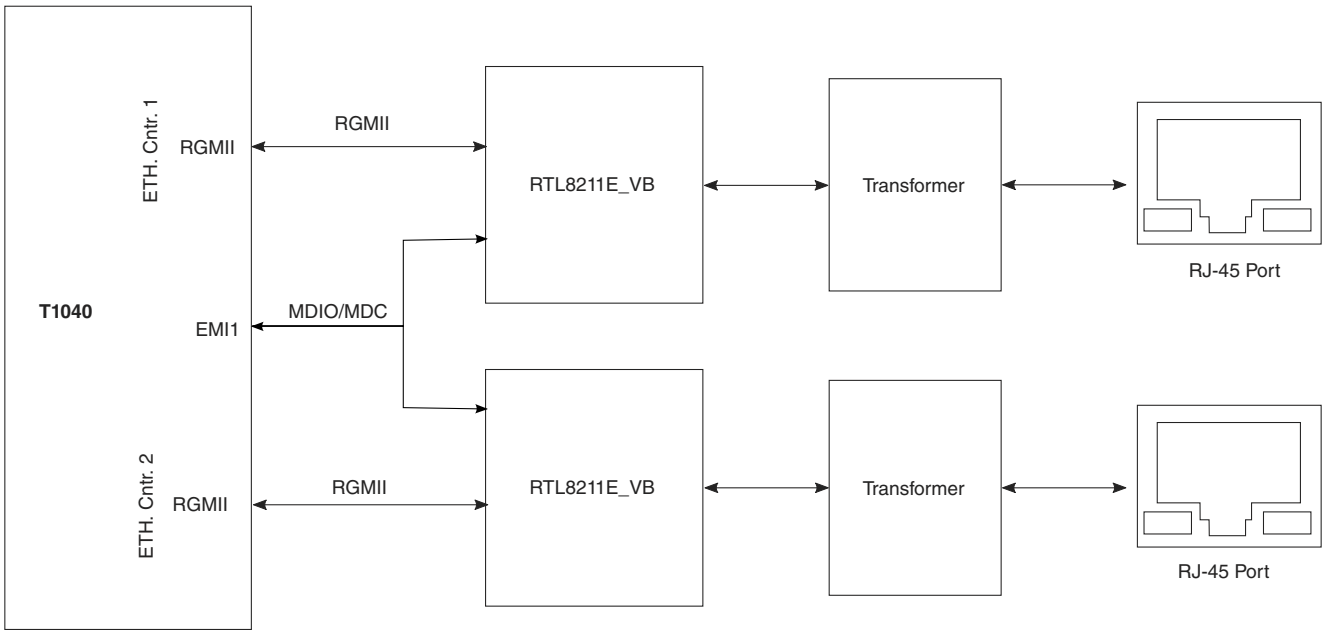


Figure 2-8. RGMII connection

2.8 Ethernet management interface

The T1040 Ethernet management interface (EMI1) is used with the onboard RGMII, SGMII, and QSGMII PHYs. The figure below shows the EMI block.

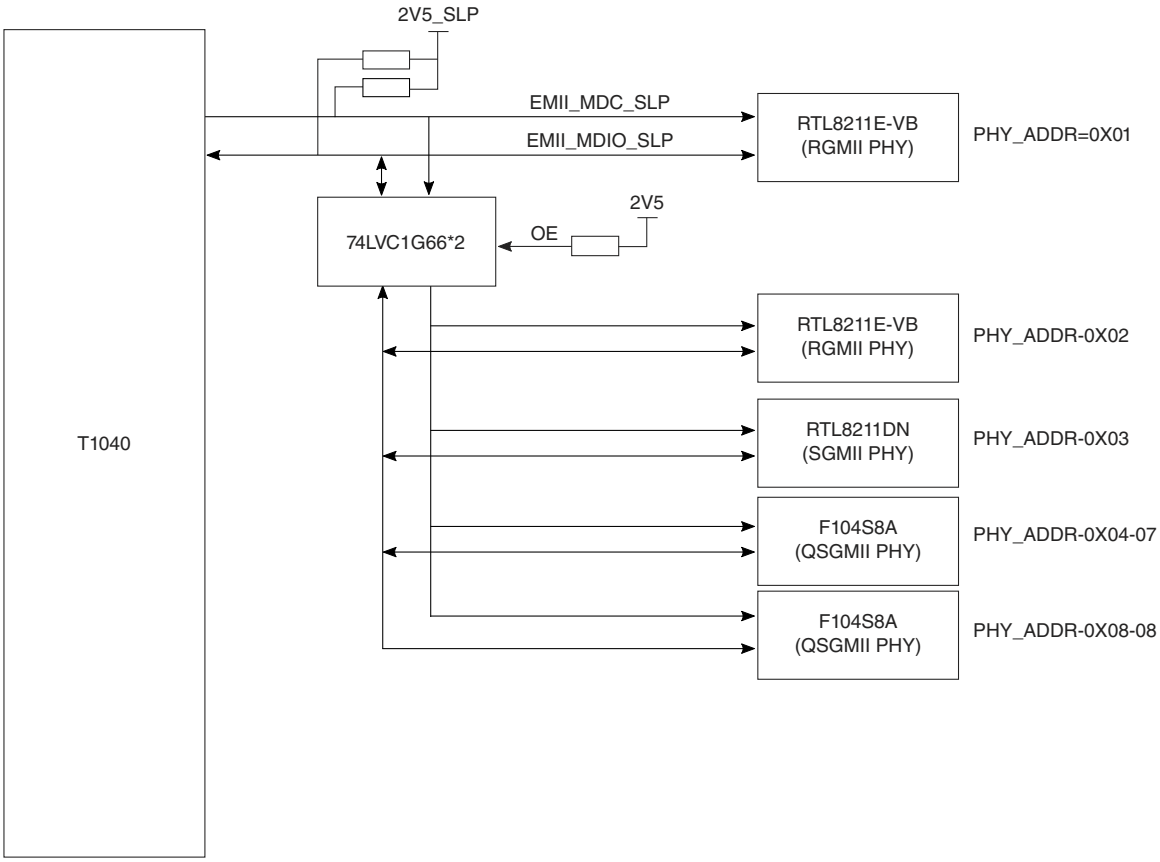


Figure 2-9. Management Data Input/Output (MDIO) connection

2.9 I2C

The T1040 devices support up to four I2C buses in order to make the I2C resources equally available to both local and remote systems. The T1040RDB board uses I2C1 port to access onboard devices, such as SPD on the DDR3L DIMM, thermal sensor (ADT7461), and core power regulator (IR36021) . The I2C2 bus uses multiplexers to partition the I2C bus into several sub-buses, called channels. The two mini-PCIe slots use channel 0-1, or I2C2_CH0-1, channel 2 is unused on the T1040RDB board. The PCIe slot uses channel 3.

The figure below shows the I2C subsystem.

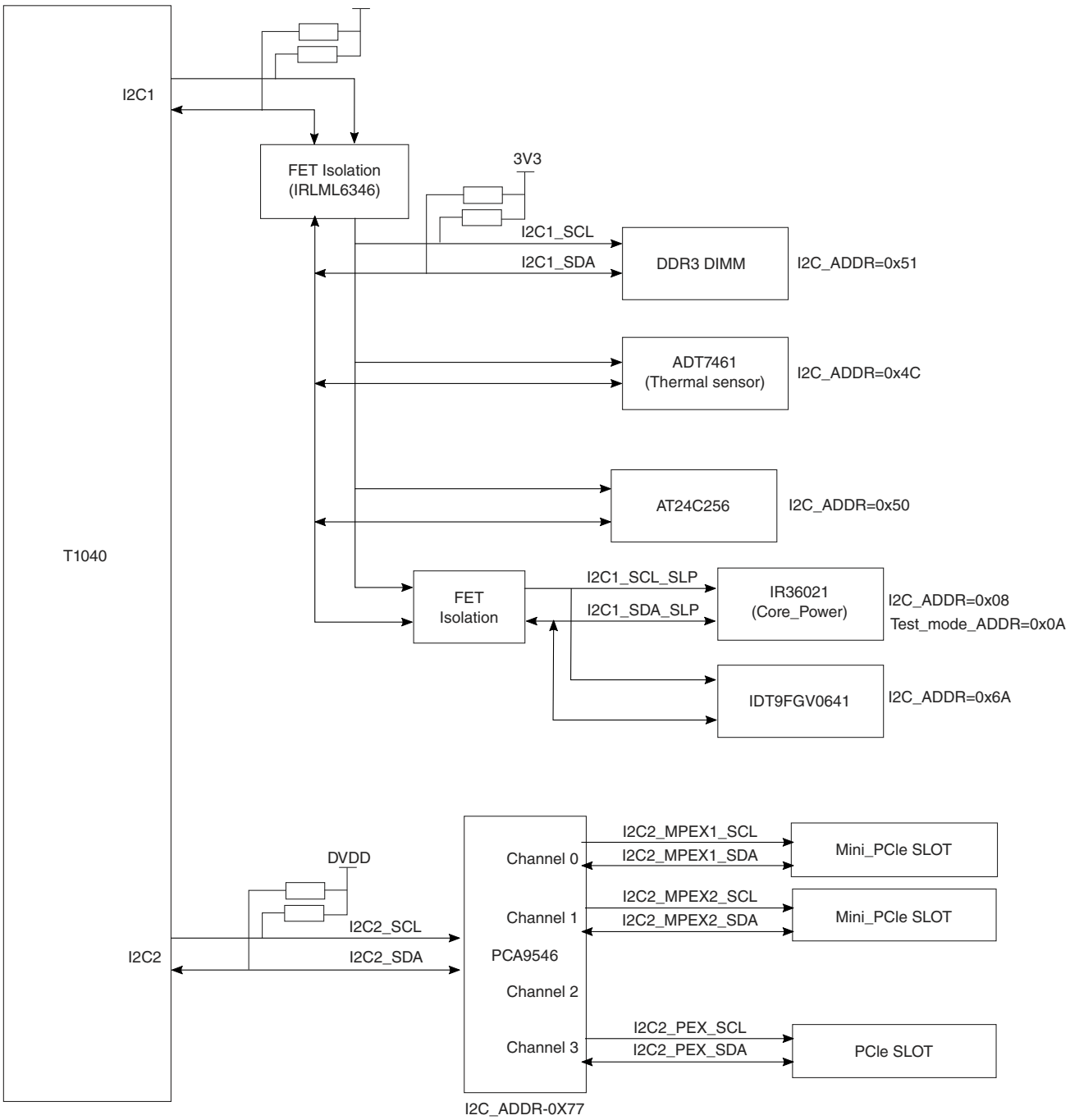


Figure 2-10. I2C bus connection

2.10 SPI interface

The T1040 serial peripheral interface (SPI) pins are used for the following purposes:

- Onboard SPI device access to various SPI memory devices

- Offboard (TDM riser) device
- Onboard SLAC device access

SPI 0 is connected to the SPI EEPROM. SPI 1 and 2 are connected to the SLAC chips for FXS voice support and SPI 3 is connected to the TDM riser card connector.

The figure below shows the overall connections of SPI.

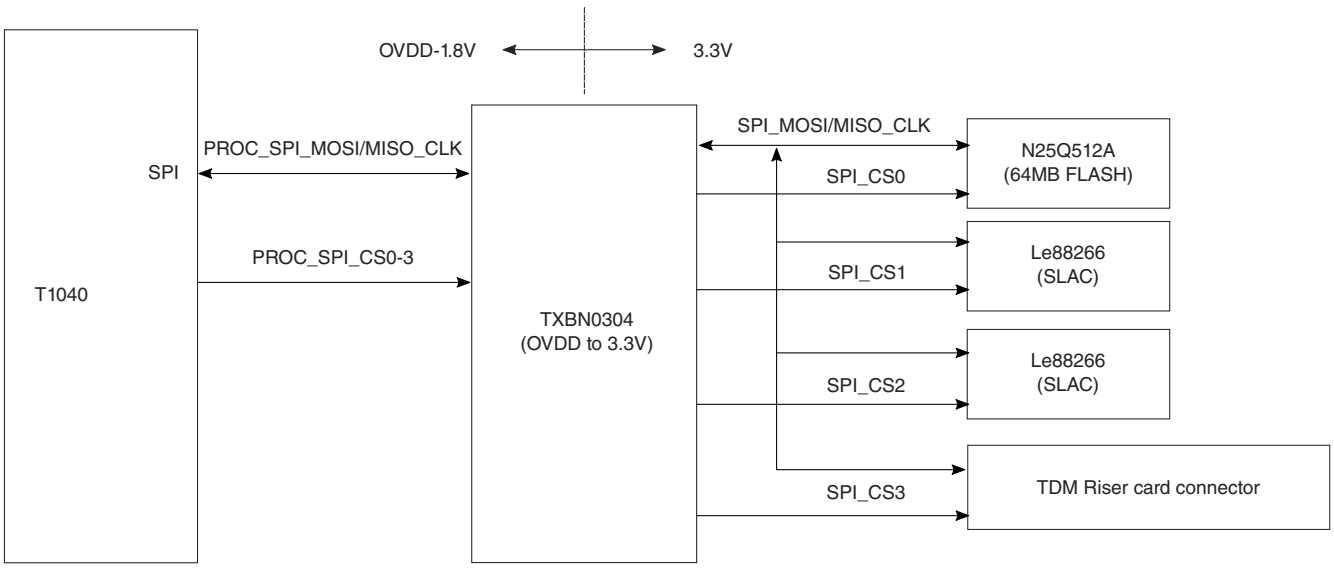


Figure 2-11. SPI bus connections

2.11 Local bus

The T1040 Integrated Flash Controller (IFC), also called the local bus, supports 32-bit addressing and 8- or 16-bit data widths, for a variety of devices. IFC lets to manage all these resources effectively with maximum performance and flexibility. The figure below shows an overview of the IFC bus.

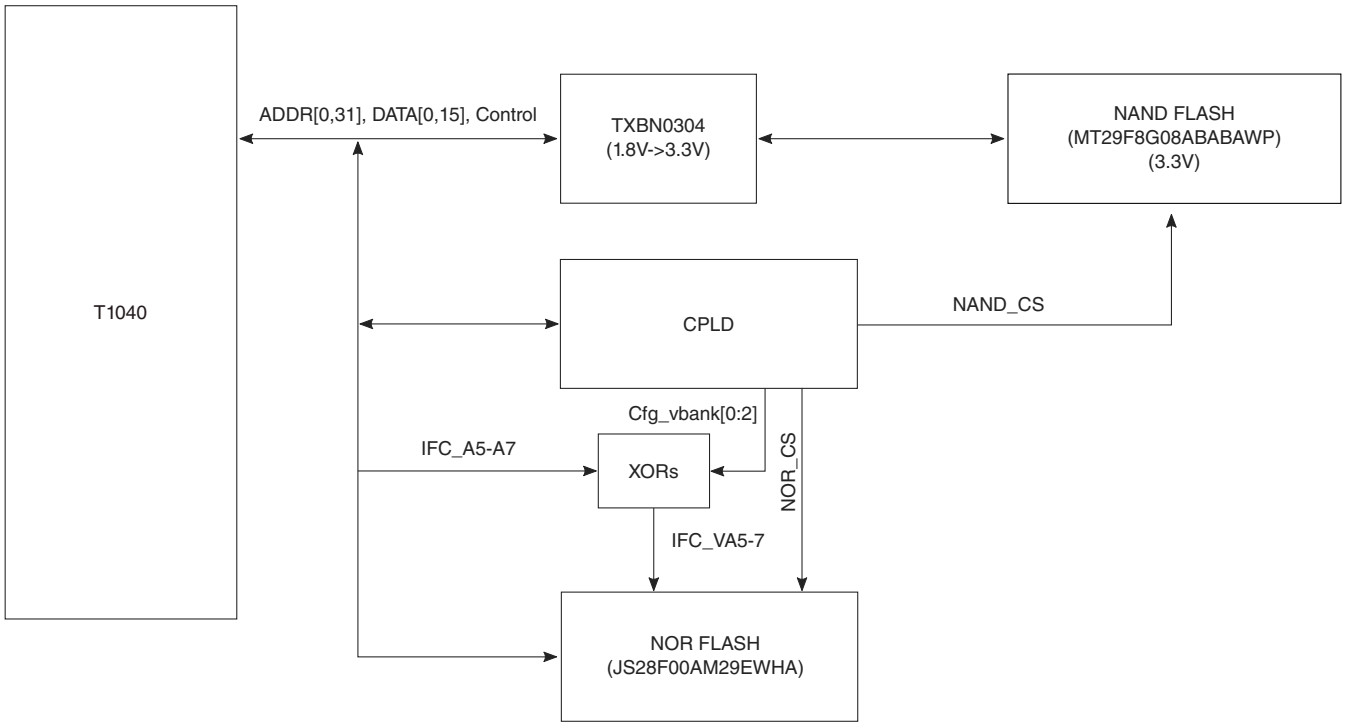


Figure 2-12. IFC bus connection

If SW3.4 is ON:

Table 2-3. IFC bus address

CS#	Memory	Address	Bus width
CS0	NOR flash	0xe8000000	16 bit
CS1	NAND flash	0xff800000	8 bit
CS2	CPLD	0xffdf0000	8 bit

If SW3.4 is OFF:

Table 2-4. IFC bus address

CS#	Memory	Address	Bus width
CS0	NAND flash	0xff800000	8 bit
CS1	NOR flash	0xe8000000	16 bit
CS2	CPLD	0xffdf0000	8 bit

2.12 SDHC interface

The enhanced SD host controller (eSDHC) provides an interface between the host system and SD/MMC cards. Booting from the eSDHC interface is supported via the processor's on-chip ROM.

On the RDB, a single connector is used for both SD and MMC memory cards as shown in the figure below.

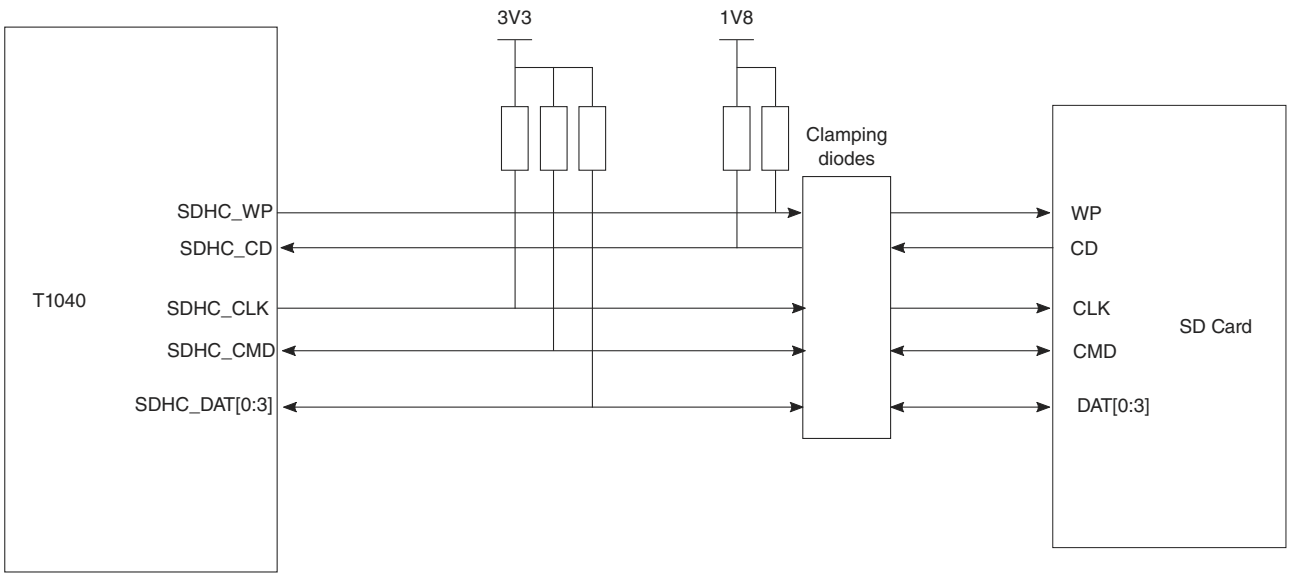


Figure 2-13. SDHC connection

2.13 USB interface

The T1040RDB board consists of two integrated USB 2.0 controllers that allow direct connection to the USB ports with appropriate protection circuitry and power supplies. The USB features are as follows:

- High-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operation
- Host mode
- Dual stacked Type A connection

The USB ports are connected to a standard Type A connector (USB1 and USB2) for compatibility with most USB peripherals.

Power for the ports is provided by a MIC2506YM switch, which supplies 5 V at up to 1 A per port. The power-enable and power-fault-detect pins are connected directly to the T1040 for individual port management.

The figure below shows the USB connectivity on the T1040RDB board.

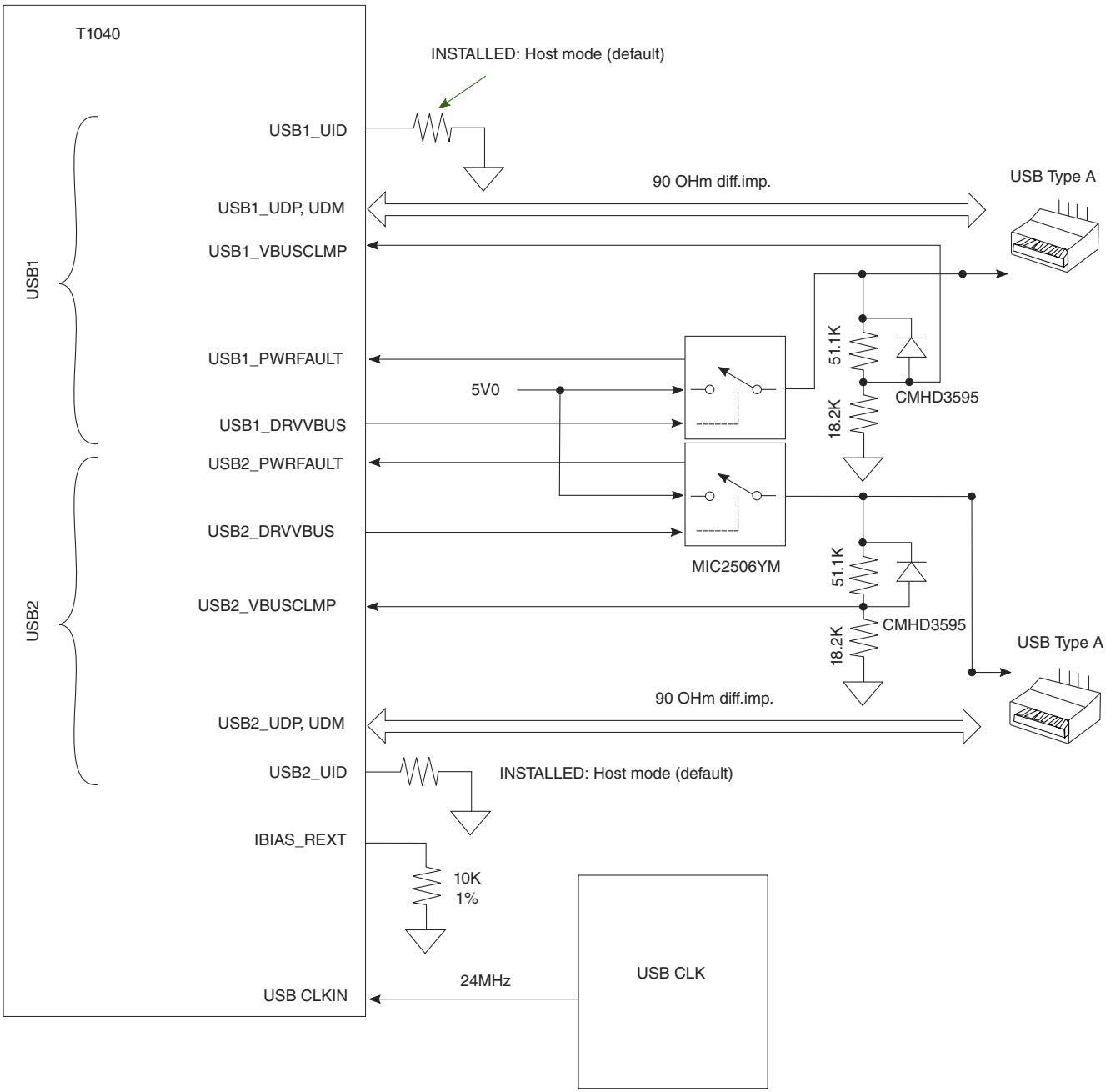


Figure 2-14. USB connection

2.14 Serial port

The T1040 processor has two UART controllers, which provide RS-232 standard interconnection between the board and an external host. The serial connection is configured to run at 115.2 kbit/s, with 8 bits, no parity, and one stop bit.

Each UART supports:

- Full-duplex operation
- Software-programmable baud generators
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions
- Software-selectable serial interface data format that includes:
  - Data length
  - Parity
  - 1/1.5/2 stop bit
  - Baud rate
  - Overrun, parity, and framing error detection

The UART ports are routed to the RJ45 connectors, as shown in the figure below.

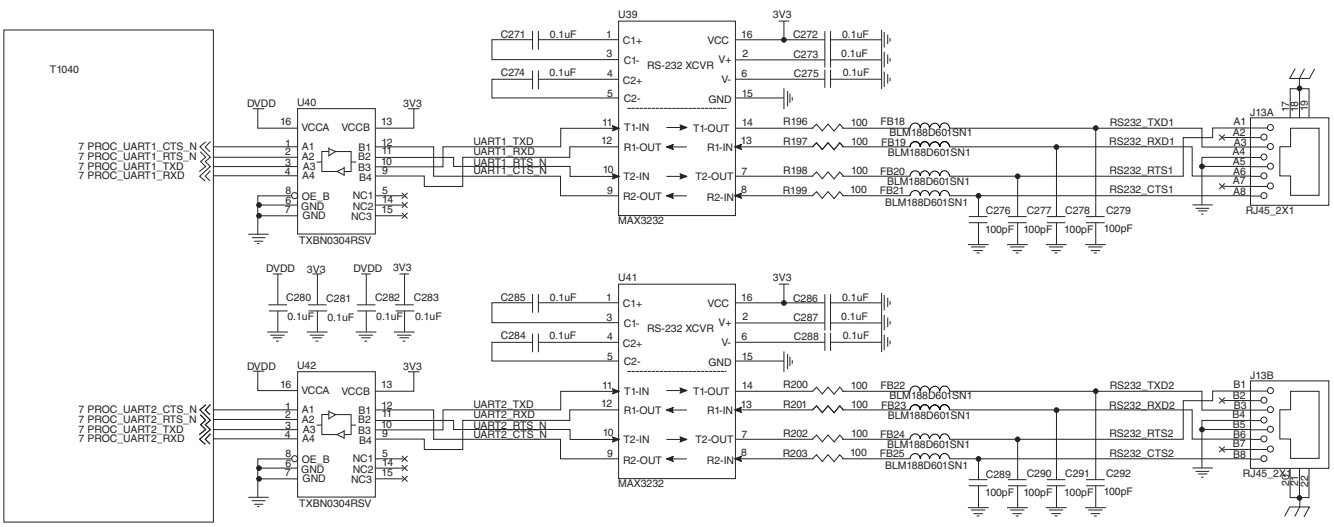


Figure 2-15. UART connection

The table below shows the connection setting for the UART RJ45 and the DB9 female cable (Part number: 600-76847-000).

Table 2-5. RJ45 and DB9 connection

RJ45 pin number	RS-232 signal	DB9 female pin number
1	RTS	8
2	N/C	
3	TXD	2
4	GND	
5	GND	5
6	RXD	3
7	N/C	
8	CTS	7

Before powering up the T1040RDB board, configure the serial port of the attached computer with the following values:

- Data rate: 115200 bit/s
- Number of data bits: 8
- Parity: None
- Number of stop bits: 1
- Flow control: Hardware/None

2.15 SLIC/SLAC and TDM interface

The T1040 TDM interface is connected to two dual SLIC/SLAC devices from Zarlink. The Zarlink Le88266 Automatic Battery Switching (ABS) VoicePort™ device implements a dual-channel telephone line interface by providing all the necessary voice interface functions from the high voltage subscriber line to the T1040 digital TDM interface.

The Zarlink device provides a line interface which meets the requirements of short and medium loop (up to 1500 Ohms total at 1 REN) applications. Features include: high voltage switching regulator, line test capabilities, integrated ringing (up to 92-Vpk), worldwide software programmability with wideband capability, flexible signal generator with tone cadencing and caller ID generation. These device features allow for Voice over Broadband solutions to be enabled on the T1040RDB. The below Figure shows how the SLIC is connected to the TDM interface of T1040 device

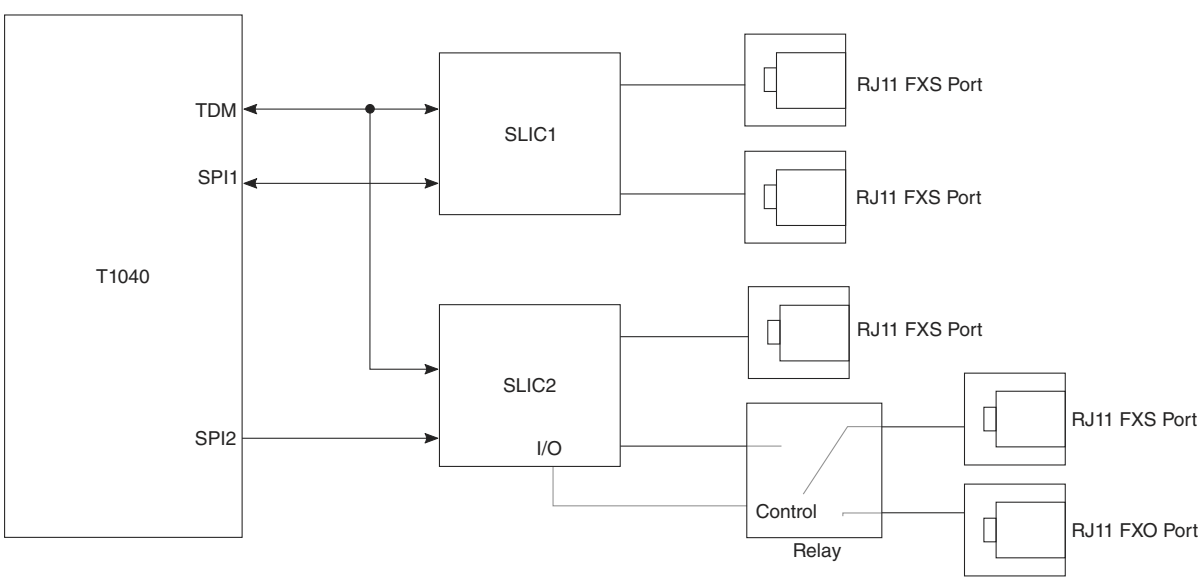


Figure 2-16. TDM connection

2.16 JTAG/COP port

The common on-chip processor (COP) is part of the T1040 JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated probe and debugger for extensive system debugging. Freescale offers CodeWarrior as debugger and CodeWarrior TAP as probe. Several third-party probes in the market can also connect to the host computer through the Ethernet port or USB port. A setup using a USB based probe is shown in the figure below.

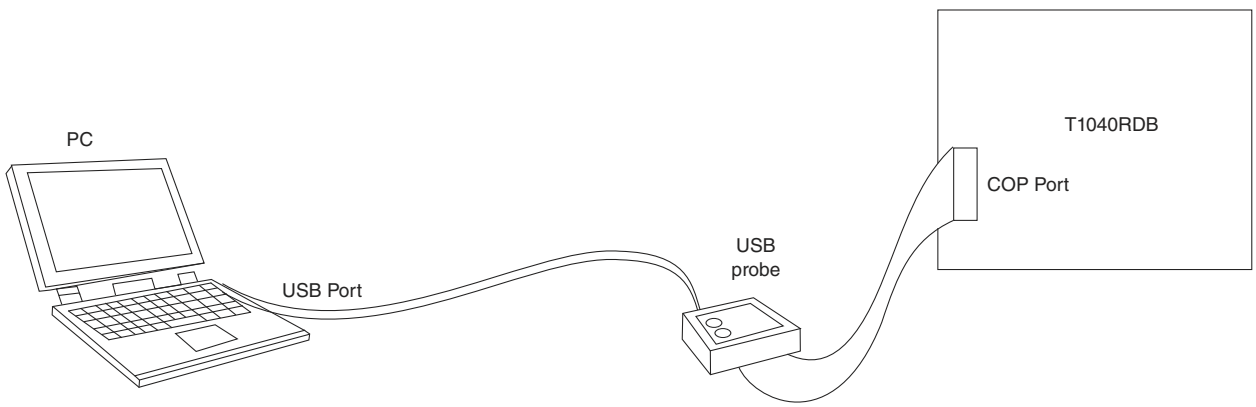


Figure 2-17. Debugger connection

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pin-out of this connector is shown in the figure below.

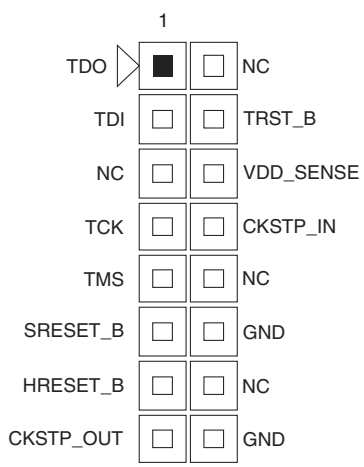


Figure 2-18. JTAG header

The table below displays the connections made from the T1040RDB COP Connector.

Table 2-6. JTAG header definition

Pin#	Signal name	Connection
1	TDO	Connected directly between the processor and JTAG/COP connector.
2	NC	Not connected
3	TDI	Connected directly between the processor and JTAG/COP connector
4	TSRT	Routed to the RESET PLD. TRST to the processor is generated from the PLD.
5	NC	Not connected
6	VDD_SENSE	Pulled to 3.3V via a 10 Ohm resistor
7	TCK	Connected directly between the processor and JTAG/COP connector.
8	CKSTP_IN	Connected directly between the processor and JTAG/COP connector.
9	TMS	Connected directly between the processor and JTAG/COP connector.
10	NC	Not connected
11	SRESET	Routed to the RESET PLD. SRESET to the processor is generated from the PLD.
12	GND	Connected to ground
13	HRESET	Routed to the RESET PLD. SRESET to the processor is generated from the PLD.
14	KEY	Not connected
15	CSKTP_OUT	Connected directly between the processor and JTAG/COP connector
16	GND	Connected to ground

2.17 Connectors, headers, jumper, push buttons and LED

This section explains:

- Connectors
- Headers
- Jumper
- Push buttons
- LEDs

The figure below shows the diagram of T1040RDB platform.

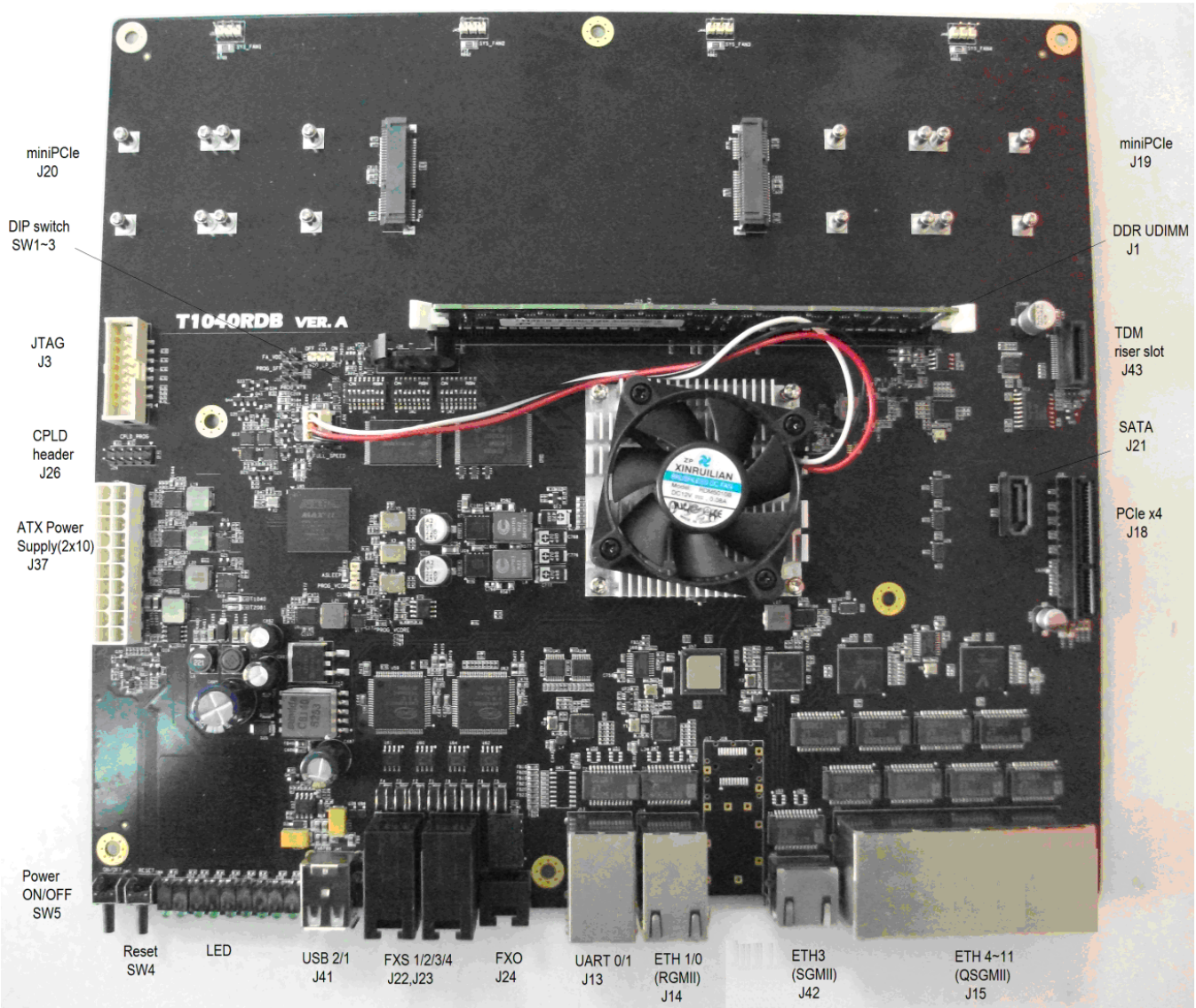


Figure 2-19. T1040RDB

2.17.1 Connectors

The table below lists the various connectors on the T1040RDB platform.

Table 2-7. Connector on board

Reference Designators	Used For	Notes
J1	UDIMM	
J3	COP/JTAG	Used for debugging T1040
J5	SD card	
J13(2 ports)	UART	

Table continues on the next page...

Table 2-7. Connector on board (continued)

J14(2 ports)	Ethernet ports	RGMII -> Copper
J15 (4 ports)	Ethernet ports	QSGMII -> Copper
J18	PCIe x4 Card	Intended use is for PCIe cards that are 25 W or less
J19,J20	Mini-PCIe cards	
J21	SATA	
J22,J23	FXS ports	
J24	FXO port	
J30	Battery Holder	
J34	CPU fan	
J37	ATX power	
J41	Dual Type A USB	
J42	Ethernet port	SGMII -> Copper
J43	TDM Riser card	
J33,J44-J46	Case fan	

2.17.2 Headers

The below table lists the various headers on the T1040RDB platform.

Table 2-8. Header on Board

Reference Designators	Used For	Notes
J26	Altera CPLD Header	Used for programming the Altera CPLD device
J28	IR36021 Header	Used for programming IR36021

2.17.3 Jumper

The below table describes how jumpers are used on the T1040RDB platform:

Table 2-9. Jumper on board

Reference designator	Description	Status 1	Status 2
J9	PROG_SFP selection	Mounted : Fuse Programming	Un-mounted : normally operate (default setting)
J10	PROG_MTR selection	Mounted : Fuse Programming	Un-mounted : normally operate (default setting)

Table continues on the next page...

Table 2-9. Jumper on board (continued)

J11	FA_VAL selection	-	Un-mounted : normally operate (default setting)
J27	NOT Used	-	-

2.17.4 Push buttons

The table below describes how the push button is used on the T1040RDB platform.

Table 2-10. Button on board

Reference Designators	Used for	Notes
SW4	Reset	Used to reset the whole board
SW5	Power on/off	Used to power on or off the board

2.17.5 LEDs

The table below lists all the LEDs on the T1040RDB board.

Table 2-11. LEDs on board

LED	**Part identifier**	Color	**Used for**	**Controlled by**
3.3 V power supply LED	D44	Green	Power on	+3.3 V power rail
Status LED	D43	Green	Status	CPLD
FXS1 LED	D38	Green	FXS1	CPLD
FXS2 LED	D39	Green	FXS2	CPLD
FXS3 LED	D41	Green	FXS3	CPLD
FXS4 LED	D42	Green	FXS4	CPLD
FXO LED	D40	Green	FXO	CPLD
T1040/T1020 LED	D5	Green	Detects onboard device	CPLD
T2081 LED	D6	Green	Detects onboard device	CPLD

2.18 Temperature

The T1040 has a thermal diode attached to the die, allowing direct temperature measurement. These pins are connected to an ADT7461 2-channel thermal monitor, which allows direct reading of the temperature of the die and is accurate to ±1° C. The second channel of the ADT7461 measures the ambient (board) temperature. The ADT7461 temperature warning and alarm signals are connected to the CPLD for monitoring. The CPLD or user software may use these signals to adjust CPU FAN speed to protect the CPU from over-temperature failure.

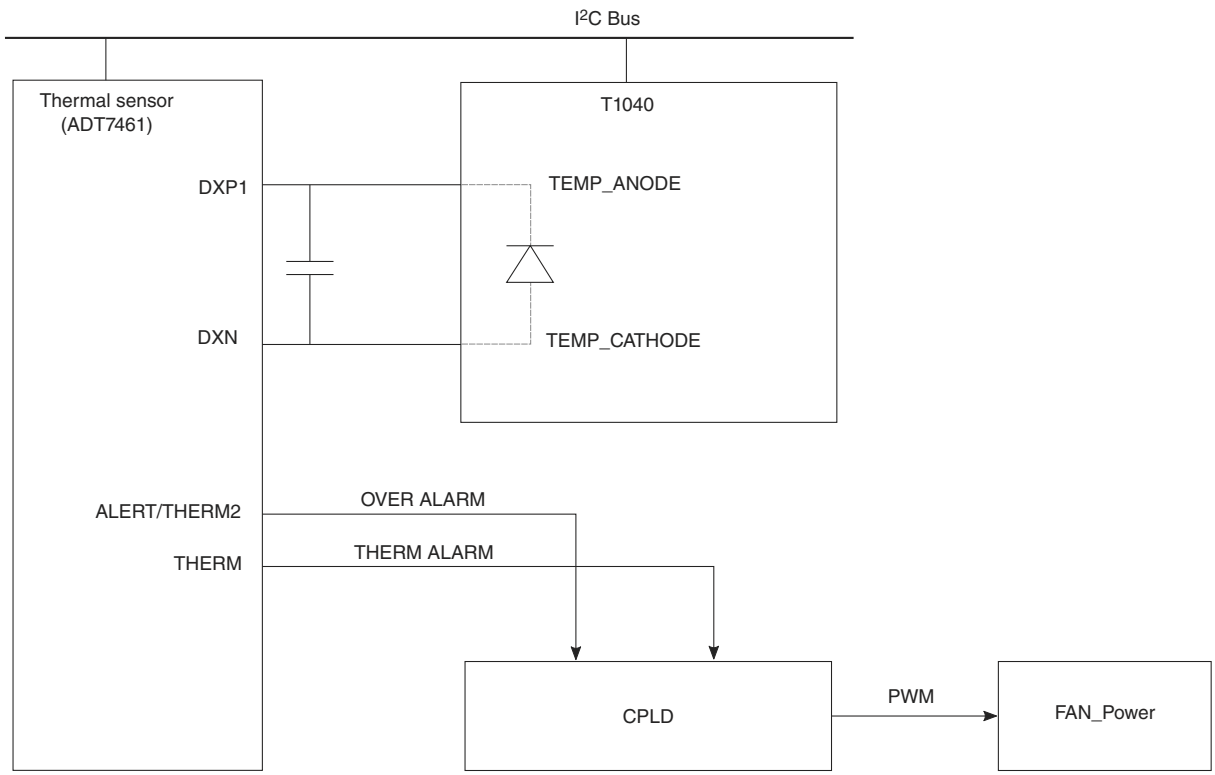


Figure 2-20. Thermal Sensor connection

2.19 DIP switch definition

The T1040RDB card has user selectable switches, for evaluating different boot configurations and other special configurations for this device. The CPLD allows software to override the configuration pins; for example, when the board is in a board farm. In order to use the CPLD override option, software sets an override bit that allows the CPLD to override the switch setting during reset.

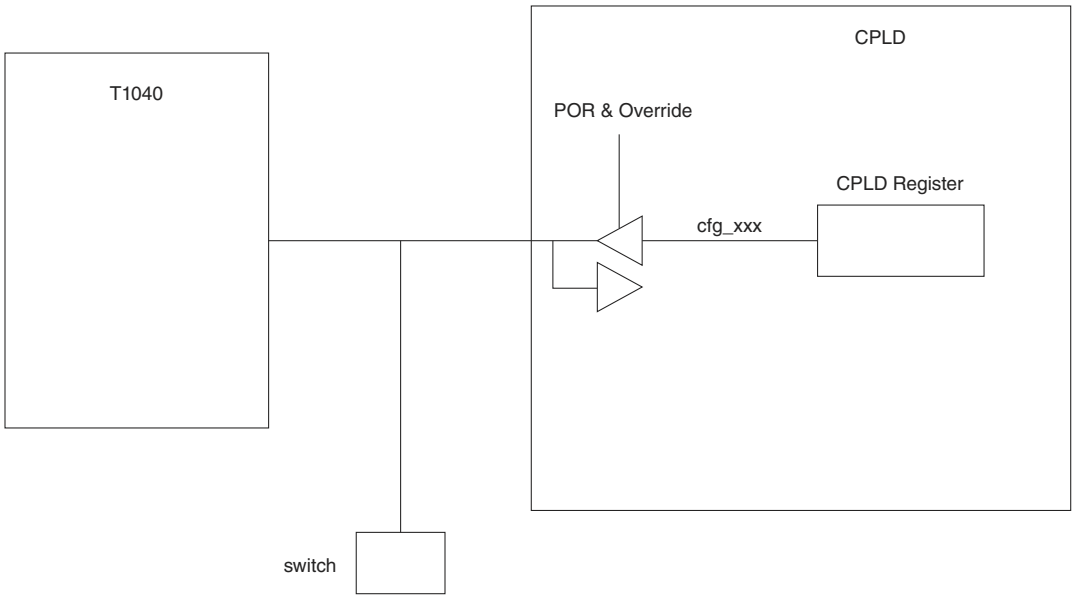


Figure 2-21. CPLD and DIP switch connection

The table below shows how POR configuration is done through switches.

NOTE

0 and 1 are represented by ON and OFF respectively on the board.

NOTE

The recommended value for the switch settings for NOR flash is below. Refer this for value of reserved switches:

SW1: 0001 0011

SW2: 1011 1011

SW3: 1110 0001

Table 2-12. POR configuration through switches

Switch	Signal name	Pin Name	Signal meaning	Setting
SW1[1:8]	cfg_rcw_src[0:7]	IFC_AD[8:15]	Reset Configuration word source	Detail description see T1040 RM
SW2[1]	cfg_rcw_src[8]	IFC_CLE	Reset Configuration word source	Detail description see T1040 RM
SW2[2]	cfg_ifc_te	IFC_TE	IFC external transceiver enable polarity select	0: IFC drives logic 1 for TE assertion 1: IFC drives logic 0 for TE assertion
SW2[3]	cfg_pll_config_sel_b	IFC_A18	Reserved	Reserved
SW2[4]	cfg_por_ainit	IFC_A19	Reserved	Reserved

Table continues on the next page...

Table 2-12. POR configuration through switches (continued)

SW2[5:6]	cfg_svr[0:1]	IFC_A[16:17]	Reserved	Reserved
SW2[7]	cfg_dram_type	IFC_A21	DRAM type selection	0: DDR4(1.2V) 1: DDR3L(1.35V)
SW2[8]	cfg_rsp_dis	IFC_AVD	Reserved	Reserved
SW3[1]	cfg_eng_use0	IFC_WE0	Sys_clock selection	0: differential sys_clk is selected 1:single sys_clk is selected
SW3[2:3]	cfg_eng_use[1:2]	Reserved	Reserved	Reserved
SW3[4]	BOOT_FLASH_SEL	-	Boot flash selection	0: NOR Flash 1: NAND Flash[1]
SW3[5:7]	CFG_VBANK[0:2]	-	Flash bank select	0: Default[2]
SW3[8]	TEST_SEL_N	TEST_SEL_B	-	0: T1020 1: T1040

1. For SW3[4] : BOOT_FLASH_SEL, it can act as boot flash selection. When BOOT_FLASH_SEL=0, NOR Flash is boot flash, when BOOT_FLASH_SEL=1, NAND Flash is boot flash.
2. SW3[5:7] can be used to change the staring address for the memory banks. For example, the NOR FLASH memory is divided into eight memory banks with 16MB size each. Eight different U-Boot image can be programmed into each memory bank, though normally only settings for bank 0 and bank 4 are used. When NOR FLASH is selected as boot flash (CS0 is connected to NOR FLASH by setting SW3[4] to ON, RCW[0:8] is set to 0_0111_xxxx using SW1[1:8] and SW2[1]), a different U-Boot image can be selected to boot up the board, by setting SW3[5:7].

   For other boot sources configured by the DIP switch, see the QorIQ T1040 Reference Manual (T1040RM).

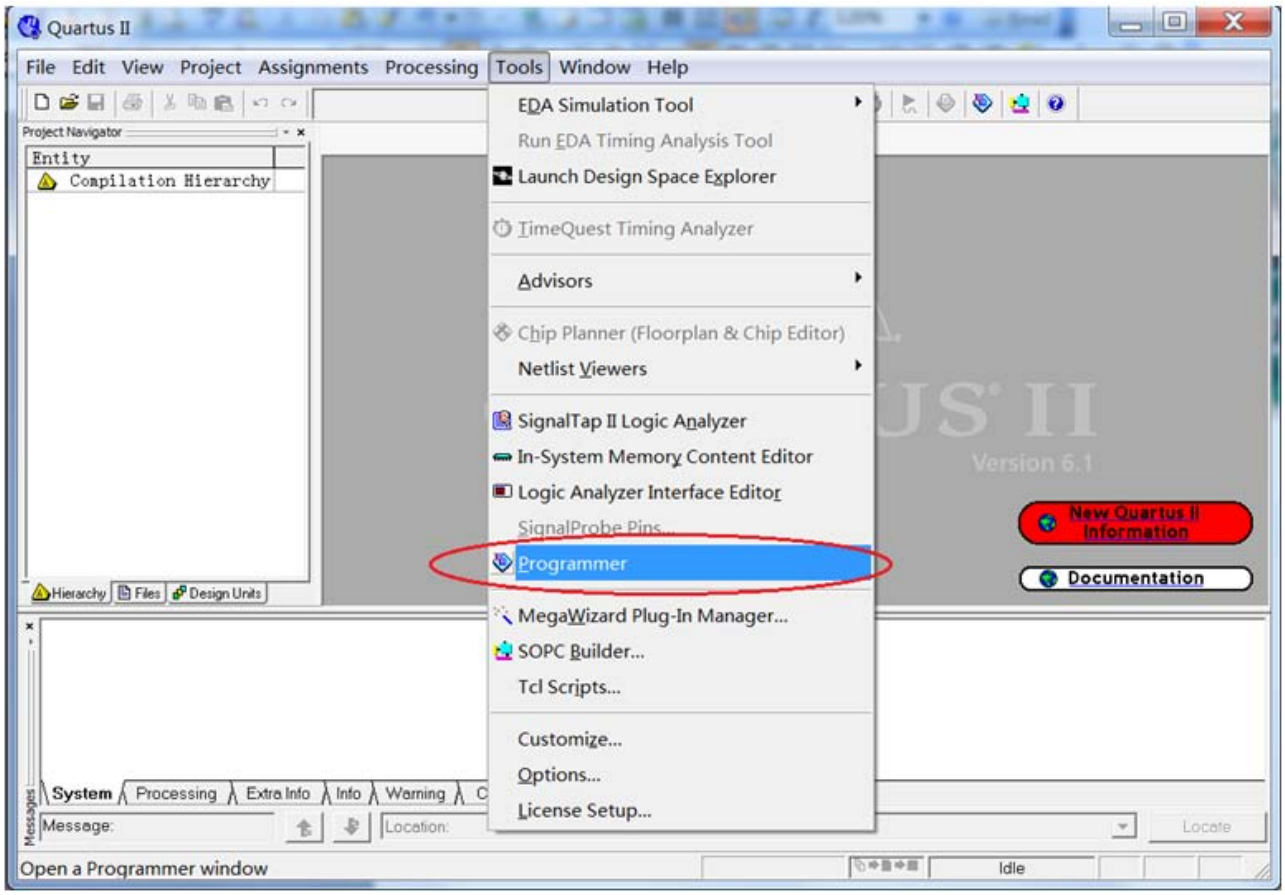
Chapter 3
CPLD specification

This section explains how to program CPLD and provide details about the CPLD memory map.

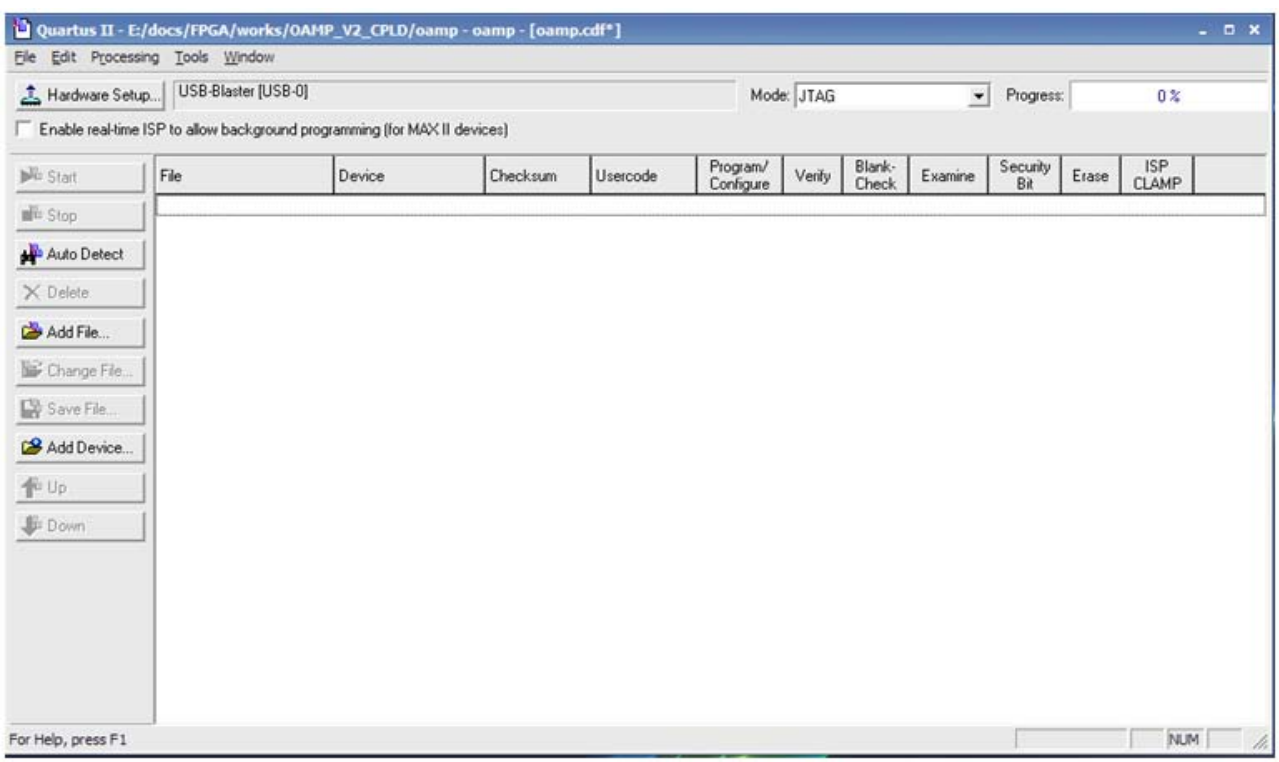
3.1 CPLD programming

To program CPLD:

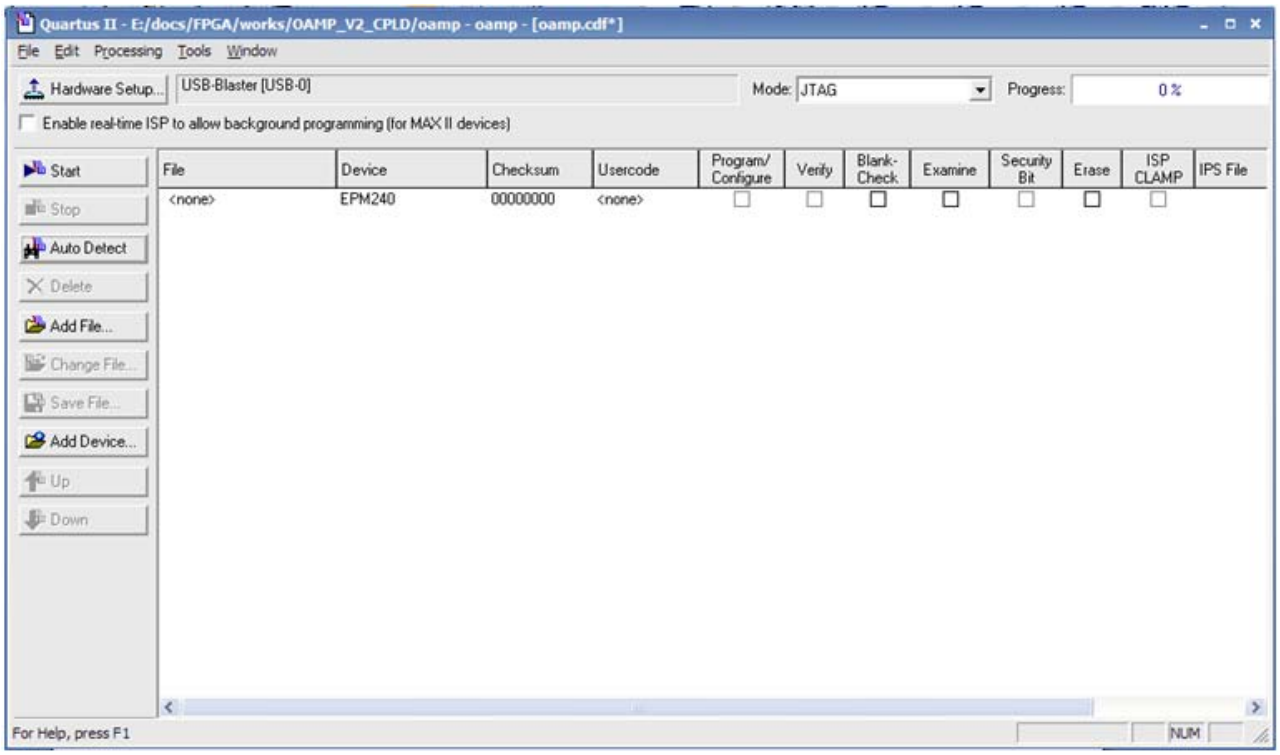
1. Connect Altera USB-blaster to the CPLD header.
2. Run `altera\61\quartus\bin\quartus.exe` to open Quartus II.
3. Select **Tools->Programmer** from the menu bar.



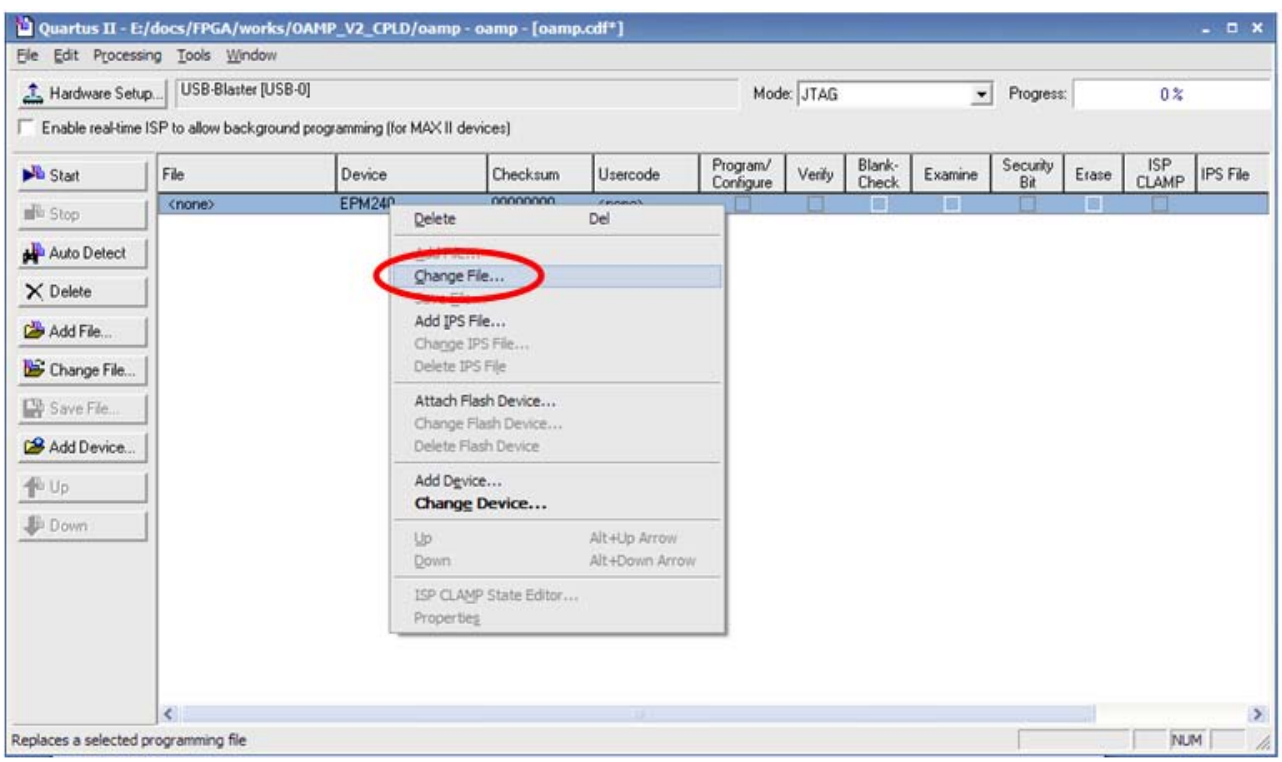
4. Click the **Hardware Setup** button to find the USB-blaster connected to the PC.



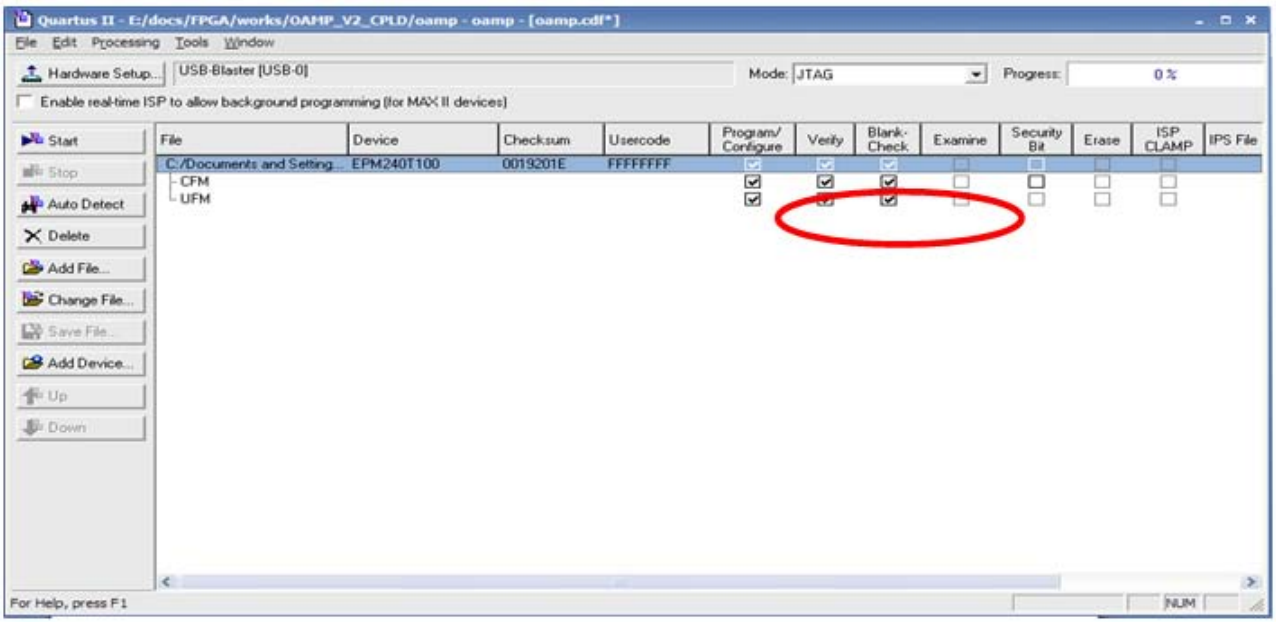
5. Switch on the board, click **Auto Detect** to detect **EPM240**.



6. Right-click **EPM240**, select **Change File** from the context menu and find the `*.pof` file.



7. Select **Program/Configure**, **Verify**, **Blank-Check** checkboxes.



8. Click **Start**. The 100% status on the progress bar indicates that the CPLD is programmed successfully.

3.2 CPLD memory map

memory map

Offset address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Chip ID1 register (CHIPID1)	8	R	55h	3.2.1/44
1	Chip ID2 register (CHIPID2)	8	R	AAh	3.2.2/45
2	Hardware version register (HWVER)	8	R	See section	3.2.3/45
3	Software version register (SWVER)	8	R	See section	3.2.4/46
10	Reset control register (RSTCON1)	8	w1c	See section	3.2.5/46
11	Reset control register (RSTCON2)	8	w1c	See section	3.2.6/47
12	INTSR	8	R	See section	3.2.7/48
13	Flash control and status register (FLHCSR)	8	R/W	See section	3.2.8/49
14	Fan control and status register (FANCSR)	8	R/W		3.2.9/49
15	Panel LED control and status register (LEDCSR)	8	R/W	See section	3.2.10/50
16	SFP+ control and status register (SFPCSR)	8	R/W	00h	3.2.11/51
17	Miscellaneous control and status register (MISCCSR)	8	R/W	See section	3.2.12/51
18	Boot configuration override register (BOOTOR)	8	R/W	See section	3.2.13/52
19	Boot configuration register 1 (BOOTCFG1)	8	R/W	See section	3.2.14/52
1A	Boot configuration register 2 (BOOTCFG2)	8	R/W	See section	3.2.15/52

3.2.1 Chip ID1 register (CHIPID1)

Address: 0h base + 0h offset = 0h

Bit	0	1	2	3	4	5	6	7
Read	CHIPID1							
Write								
Reset	0	1	0	1	0	1	0	1

CHIPID1 field descriptions

Field	Description
0–7 CHIPID1	0x55, Identification of the CPLD image.

3.2.2 Chip ID2 register (CHIPID2)

Address: 0h base + 1h offset = 1h

Bit	0	1	2	3	4	5	6	7
Read	CHIPID2							
Write								
Reset	1	0	1	0	1	0	1	0

CHIPID2 field descriptions

Field	Description
0–7 CHIPID2	0xaa, Identification of the CPLD image.

3.2.3 Hardware version register (HWVER)

Address: 0h base + 2h offset = 2h

Bit	0	1	2	3	4	5	6	7
Read	HW_VER							
Write								
Reset	n*	n*	n*	n*	n*	n*	n*	n*

* Notes:
- HW_VER field: n=Depends on PLD image revision

HWVER field descriptions

Field	Description
0–7 HW_VER	The version field of the hardware board.

3.2.4 Software version register (SWVER)

Address: 0h base + 3h offset = 3h

Bit	0	1	2	3	4	5	6	7
Read	SW_VER							
Write								
Reset	n*	n*	n*	n*	n*	n*	n*	n*

* Notes:
- SW_VER field: n=Depends on PLD image version

SWVER field descriptions

Field	Description
0–7 SW_VER	The version field of the CPLD software.

3.2.5 Reset control register (RSTCON1)

Address: 0h base + 10h offset = 10h

Bit	0	1	2	3	4	5	6	7
Read	SW_RST	Reserved	EC1_RST	EC2_RST	SG_RST	QSG1_RST	QSG2_RST	XG_RST
Write	w1c		w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

RSTCON1 field descriptions

Field	Description
0 SW_RST	0: No reset occurs. 1: Writing logic 1 will produce whole board reset# signal, this bit can auto clear.
1 -	This field is reserved.
2 EC1_RST	0: No reset occurs. 1: Write a logic 1 produces RGMII PHY1(RTL82111E-VB) reset# signal, this bit can auto clear.
3 EC2_RST	0: No reset occurs. 1: Writing logic 1 produces RGMII PHY2(RTL82111E-VB) reset# signal, this bit can auto clear.

Table continues on the next page...

RSTCON1 field descriptions (continued)

Field	Description
4 SG_RST	0: No reset occurs. 1: Writing logic 1 produces SGMII PHY(RTL82111DN) reset# signal, this bit can auto clear.
5 QSG1_RST	0: No reset occurs. 1: Writing logic 1 produces QSGMII PHY(VSC8514) reset# signal, this bit can auto clear.
6 QSG2_RST	0: No reset occurs. 1: Writing logic 1 produces 10G PHY(CS4315) reset# signal, this bit can auto clear.
7 XG_RST	0: No reset occurs 1: Writing logic 1 produces 10G PHY (CS4315)reset# signal, this bit can auto clear.(Bit 7 needs to go)

3.2.6 Reset control register (RSTCON2)

Address: 0h base + 11h offset = 11h

Bit	0	1	2	3	4	5	6	7
Read	Reserved				TDMR_RST	PEX_RST	MPEX1_RST	MPEX2_RST
Write					w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

RSTCON2 field descriptions

Field	Description
0–3 -	This field is reserved.
4 TDMR_RST	0: No reset occurs. 1: Writing logic 1 produces TDM riser card reset# signal, this bit can auto clear.
5 PEX_RST	0: No reset occurs. 1: Writing logic 1 produces PCIe x4 slot reset# signal, this bit can auto clear.
6 MPEX1_RST	0: No reset occurs. 1: Writing logic 1 produces miniPCIe card1 reset# signal, this bit can auto clear.
7 MPEX2_RST	0: No reset occurs 1: Writing logic 1 produces miniPCIe card2 reset# signal, this bit can auto clear.

3.2.7 INTSR

Address: 0h base + 12h offset = 12h

Bit	0	1	2	3	4	5	6	7
Read	THERM_INT	SG_INT	QSG1_INT	QSG2_INT	POTSA_INT	POTSB_INT	TDMR1_INT	TDMR2_INT
Write								
Reset	n*	n*	n*	n*	n*	n*	n*	n*

* Notes:
- TDMR2_INT field: Depends on PLD image revision.
- TDMR1_INT field: Depends on PLD image revision.
- POTSB_INT field: Depends on PLD image revision.
- POTSA_INT field: Depends on PLD image revision.
- QSG2_INT field: Depends on PLD image revision.
- QSG1_INT field: Depends on PLD image revision.
- SG_INT field: Depends on PLD image revision.
- THERM_INT field: Depends on PLD image revision.

INTSR field descriptions

Field	Description
0 THERM_INT	0: No interrupt occurs. 1: Board over temperature interrupt occurs.
1 SG_INT	0: No interrupt occurs. 1: SGMII PHY(RTL8211DN) interrupt occurs
2 QSG1_INT	0: No interrupt pending 1: QSGMII PHY1(VSC8514) interrupt occurs.
3 QSG2_INT	0: No interrupt pending 1: QSGMII PHY2(VSC8514) interrupt occurs
4 POTSA_INT	0: No interrupt pending 1: POTS A interrupt occurs
5 POTSB_INT	0: No interrupt pending 1: POTS B interrupt occurs.
6 TDMR1_INT	0: No interrupt pending 1: TDM riser card interrupt 1 occurs.
7 TDMR2_INT	0: No interrupt pending 1: TDM riser card interrupt 2 occurs.

3.2.8 Flash control and status register (FLHCSR)

Address: 0h base + 13h offset = 13h

Bit	0	1	2	3	4	5	6	7
Read	BOOT_SEL	BANK_OR	SW_BANK_SEL0	SW_BANK_SEL1	SW_BANK_SEL2	BANK_SEL0	BANK_SEL1	BANK_SEL2
Write								
Reset	n	0	n	n	n	0	0	0

FLHCSR field descriptions

Field	Description
0 BOOT_SEL	0: Boot from 16-bit NOR flash. 1: Boot from 8-bit NAND flash.
1 BANK_OR	0: NOR flash bank select from CPLD override disable. 1: NOR flash bank select from CPLD override enable.
2 SW_BANK_SEL0	NOR flash bank select bit0 of switch status is 0. 1: NOR flash bank select bit0 of switch status is 1.
3 SW_BANK_SEL1	0: NOR flash bank select bit1 of switch status is 0. 1: NOR flash bank select bit1 of switch status is 1.
4 SW_BANK_SEL2	0: NOR flash bank select bit2 of switch status is 0. 1: NOR flash bank select bit2 of switch status is 1.
5 BANK_SEL0	0: NOR flash bank select bit0 set 0. 1: NOR flash bank select bit0 set 1.
6 BANK_SEL1	0: NOR flash bank select bit1 set 0. 1: NOR flash bank select bit1 set 1
7 BANK_SEL2	0: NOR flash bank select bit2 set 0. 1: NOR flash bank select bit2 set 1.

3.2.9 Fan control and status register (FANCSR)

Address: 0h base + 14h offset = 14h

Bit	0	1	2	3	4	5	6	7
Read Write	Reserved				FAN_PWM			
Reset								

FANCSR field descriptions

Field	Description
0–3 -	This field is reserved.
4–7 FAN_PWM	0000: PWM duty cycle is 0%, fan stop running. 0001~1110: PWM duty cycle is 6.7%~93.3%, fan speed control. 1111: PWM duty cycle is 100%, fan full speed.

3.2.10 Panel LED control and status register (LEDCSR)

Address: 0h base + 15h offset = 15h

Bit	0	1	2	3	4	5	6	7
Read	STS_LED	FXS1_LED	FXS2_LED	FXS3_LED	FXS4_LED	FXO_LED	XG_LED1	XG_LED2
Write								
Reset	0	0	0	0	0	0	n	n

LEDCSR field descriptions

Field	Description
0 STS_LED	0: Panel STATUS LED off. 1: Panel STATUS LED on.
1 FXS1_LED	0: Panel FXS1 LED off 1: Panel FXS1 LED on
2 FXS2_LED	0: Panel FXS2 LED off 1: Panel FXS2 LED on
3 FXS3_LED	0: Panel FXS3 LED off 10: Panel FXS3 LED on
4 FXS4_LED	0: Panel FXS4 LED off 1: Panel FXS4 LED on
5 FXO_LED	0: Panel FXO LED off 1: Panel FXO LED on
6 XG_LED1	0: Panel XG TX LED off when SFP+ not present or TX disabled 1: Panel XG TX LED on when SFP+ present and TX enabled
7 XG_LED2	0: Panel XG RX LED off when SFP+ not present or RX los. 1: Panel XG RX LED on when SFP+ present and RX optical received

3.2.11 SFP+ control and status register (SFPCSR)

Address: 0h base + 16h offset = 16h

Bit	0	1	2	3	4	5	6	7
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

SFPCSR field descriptions

Field	Description
0–7 -	This field is reserved.

3.2.12 Miscellaneous control and status register (MISCCSR)

Address: 0h base + 17h offset = 17h

Bit	0	1	2	3	4	5	6	7
Read	SPI_CS3_SEL	SLEEP_EN	REQ_MD		TDMR_PRS	PEX_PRS	T2081_DET	TEST_SEL_N
Write								
Reset	0	0	1	1	0	n	n	n

MISCCSR field descriptions

Field	Description
0 SPI_CS3_SEL	0: SPI_CS3 select TDMR SPI CS0 1: SPI_CS3 select TDMR SPI CS1
1 SLEEP_EN	Before entering deep sleep mode, set ‘1’ to this bit, after exiting deep sleep mode, set ‘0’ to this bit 0 Normal operation 1 Deep sleep enable bit
2–3 REQ_MD	00 No reset occurs when HRESET_REQ triggered. 01 HRESET occurs when HRESET_REQ triggered. 10 Reserved 11 PORESET occurs when HRESET_REQ triggered.
4 TDMR_PRS	0: TDM riser card not present 1: TDM riser card present
5 PEX_PRS	0 PCIe card not present in x4 slot. 1 PCIe card present in x4 slot.
6 T2081_DET	0: T1040 on board 1: T2081 on board
7 TEST_SEL_N	0: TEST_SEL_N pin status is 0 1: TEST_SEL_N pin status is 1

3.2.13 Boot configuration override register (BOOTOR)

Address: 0h base + 18h offset = 18h

Bit	0	1	2	3	4	5	6	7
Read Write	Reserved							BOOT_OR
Reset								

BOOTOR field descriptions

Field	Description
0–6 -	This field is reserved.
7 BOOT_OR	0: Boot configuration from CPLD override disable 1: Boot configuration from CPLD override enable

3.2.14 Boot configuration register 1 (BOOTCFG1)

Address: 0h base + 19h offset = 19h

Bit	0	1	2	3	4	5	6	7
Read Write	cfg_rcw_src[0:7]							
Reset								

BOOTCFG1 field descriptions

Field	Description
0–7 cfg_rcw_src[0:7]	**NOTE:** For more information, see QorIQ T1040, T1020 Data Sheet.

3.2.15 Boot configuration register 2 (BOOTCFG2)

NOTE

For more information, refer T1040 datasheet.

Address: 0h base + 1Ah offset = 1Ah

Bit	0	1	2	3	4	5	6	7
Read Write	cfg_rcw_ src8	Reserved	cfg_svr[0:1]		Reserved	cfg_eng_use[0:2]		
Reset								

BOOTCFG2 field descriptions

Field	Description
0 cfg_rcw_src8	RCW source bit 8.
1 -	This field is reserved.
2–3 cfg_svr[0:1]	cfg_svr bit for T1040 Power-on-reset use
4 -	This field is reserved.
5–7 cfg_eng_use[0:2]	cfg_eng_use bit for T1040 Power-on-reset use.

Chapter 4
Software configuration

This section explains:

- Preparing board
- Ethernet port map
- NOR flash image layout
- **Switch settings**
- SDK Build details
- Flashing and updating images

4.1 Preparing board

The figure below shows the front panel of the T1040 RDB.

Figure 4-1. T1040RDB front panel

To prepare the T1040RDB for use, default configuration should be: CPU: 1.4 GHz, DDR: 1600 MT/s. The steps are:

1. Attach an RS-232 cable between the T1040RDB UART0 port and host computer
2. Open a serial console tool on the host computer to communicate with the T1040RDB
3. Configure the host computer's serial port with the following settings:
    - Data rate: 115200 bps
    - Number of data bits: 8
    - Parity: None
    - Number of stop bits: 1
    - Flow control: Hardware/None

Push the power button on the front side of the chassis. The board will boot and show the U-Boot console messages, similar to the following.

```
U-Boot 2014.01QorIQ-SDK-T1040-BSP0.2 (Mar 07 2014 - 01:04:58)

CPU0:  T1040E, Version: 1.0, (0x85280010)
Core:  e5500, Version: 2.0, (0x80241020)
Clock Configuration:
       CPU0:1400 MHz, CPU1:1400 MHz, CPU2:1400 MHz, CPU3:1400 MHz,
       CCB:600  MHz,
       DDR:800  MHz (1600 MT/s data rate) (Asynchronous), IFC:150  MHz
       FMAN1: 600 MHz
       QMAN:  300 MHz
       PME:   300 MHz
L1:    D-cache 32 KiB enabled
       I-cache 32 KiB enabled
Reset Configuration Word (RCW):
       00000000: 0c18000e 0e000000 00000000 00000000
       00000010: 66000002 80000002 ec027000 01000000
       00000020: 00000000 00000000 00000000 00032810
       00000030: 00000000 0342500f 00000000 00000000
Board: T1040RDB
Board rev: 0x01 CPLD ver: 0x06, vBank: 0
I2C:   ready
SPI:   ready
DRAM:  Initializing....using SPD
Detected UDIMM 18KSF51272AZ-1G6K1
2 GiB left unmapped
    DDR: 4 GiB (DDR3, 64-bit, CL=11, ECC on)
       DDR Chip-Select Interleaving Mode: CS0+CS1
Flash: 256 MiB
L2:    256 KiB enabled
Corenet Platform Cache: 256 KiB enabled
Using SERDES1 Protocol: 102 (0x66)
NAND:  1024 MiB
MMC:  FSL_SDHC: 0
PCIe1: Root Complex, no link, regs @ 0xfe240000
PCIe1: Bus 00 - 00
PCIe2: Root Complex, x1 gen1, regs @ 0xfe250000
  02:00.0     - 8086:10d3 - Network controller
PCIe2: Bus 01 - 02
PCIe3: Root Complex, no link, regs @ 0xfe260000
PCIe3: Bus 03 - 03
PCIe4: Root Complex, no link, regs @ 0xfe270000
PCIe4: Bus 04 - 04
In:    serial
Out:   serial
Err:   serial
Net:   Initializing Fman
Fman1: Uploading microcode version 106.4.14
FSL_MDIO0:0 is connected to FM1@DTSEC1.  Reconnecting to FM1@DTSEC2
FSL_MDIO0:0 is connected to FM1@DTSEC2.  Reconnecting to FM1@DTSEC3
e1000: 68:05:ca:04:d5:6a
       FM1@DTSEC1, FM1@DTSEC2, FM1@DTSEC3, FM1@DTSEC4 [PRIME], FM1@DTSEC5, e1000#0
Warning: e1000#0 MAC addresses don't match:
Address in SROM is         68:05:ca:04:d5:6a
Address in environment is  00:04:9f:ef:00:00

Hit any key to stop autoboot:  0
```

The system auto boots and shows the following Linux login screen.

```
t1040rdb
login: root
root@t1040rdb:~#
```

4.2 Ethernet port map

The table below shows how Ethernet ports match to Linux, U-Boot, and the front-panel label on the 1U box.

Table 4-1. Ethernet mapping table

Label on 1U box	Port in U-Boot	Port in Linux	FMan address	Type
Internal port	FM1@DTSEC1 [1]	fm1-gb0		
Internal port	FM1@DTSEC2 [1]	fm1-gb1		
ETH0	FM1@DTSEC4	fm1-gb3	0xfe4e6000	RGMII
ETH1	FM1@DTSEC5	fm1-gb4	0xfe4e8000	RGMII
ETH2	FM1@DTSEC3	fm1-gb2	0xfe4e4000	SGMII
ETH3	Not supported in U-Boot		0xfe4e0000	L2 switch
ETH4	Not supported in U-Boot			L2 switch
ETH5	Not supported in U-Boot			L2 switch
ETH6	Not supported in U-Boot			L2 switch
ETH7	Not supported in U-Boot		0xfe4e2000	L2 switch
ETH8	Not supported in U-Boot			L2 switch
ETH9	Not supported in U-Boot			L2 switch
ETH10	Not supported in U-Boot			L2 switch

1. Connected to L2 switch port at 2.5 Gbit/s. This port cannot be connected to external PHYs, as T1040RDB supports only SerDes protocol, 0x66

NOTE

ETH3-ETH10 belong to the switch. They are not visible as interfaces in Linux. Switch control software is required to control them.

4.3 NOR flash image layout

NOR flash can be divided into two flash banks (0 and 4) to store a main image and an alternative backup image. This is shown in the below table.

Table 4-2. Image layout in NOR flash

Start address	End address	Image	Max size
0xEFF40000	0xEFFFFFFF	U-Boot (current bank)	768KB
0xEFF20000	0xEFF3FFFF	U-Boot env (current bank)	128KB
0xEFF10000	0XEFF1FFFF	QUICC Engine microcode (current bank)	64KB
0xEFF00000	0xEFF0FFFF	FMan microcode (current bank)	64KB
0xED300000	0xEFEFFFFF	rootfs (alternative bank)	43MB
0xEC800000	0xEC8FFFFF	Hardware device tree (alternative bank)	1MB
0xEC020000	0XEC7FFFFF	Linux.uImage (alternative bank)	7MB+875KB
0xEC000000	0XEC01FFFF	RCW (alternative bank)	7MB+875KB
0xEBF40000	0XEBFFFFFF	U-Boot (alternative bank)	768KB
0xEBF20000	0XEBF3FFFF	U-Boot env (alternative bank)	128KB
0xEBF10000	0XEBF1FFFF	QUICC Engine microcode (alt bank)	64KB
0XEBF00000	0XEBF0FFFF	FMan microcode (alternative bank)	64KB
0xE9300000	0XEBEFFFFF	rootfs (current bank)	43MB
0XE8800000	0XE88FFFFF	Hardware device tree (current bank)	1MB
0xE8020000	0xE86FFFFF	Linux.uImage (current bank)	7MB+875KB
0xE8000000	0xE801FFFF	RCW (current bank)	128KB

4.4 Switch settings

This chapter defines the default switch settings and other boot source settings.

NOTE

You may find slightly different default switch settings, depending on the SDK being used; check the relevant information.

4.4.1 Switch default settings (NOR flash boot)

This section defines the default switch settings for NOR flash boot.

NOTE

ON and OFF are being represented as 0 and 1 respectively, on the board.

DIP	Switch binary value	1	2	3	4	5	6	7	8
SW1	0001 0011	ON	ON	ON	OFF	ON	ON	OFF	OFF
SW2	1011 1011	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

4.4.2 Other boot source settings

This section defines the settings for NAND boot, SPI boot SW, and SD boot.

NAND boot settings:

DIP	Switch binary value	1	2	3	4	5	6	7	8
SW1	1000 1000	OFF	ON	ON	ON	OFF	ON	ON	ON
SW2	0011 1011	ON	ON	OFF	OFF	OFF	ON	OFF	OFF
SW3	1111 0001	OFF	OFF	OFF	OFF	ON	ON	ON	OFF

SPI boot SW settings:

DIP	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0010	ON	ON	OFF	ON	ON	ON	OFF	ON
SW2	1011 1011	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

SD boot settings:

DIP	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0000	ON	ON	OFF	ON	ON	ON	ON	ON
SW2	0011 1011	ON	ON	OFF	OFF	OFF	ON	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

4.4.3 Switch detailed description

For a detailed switch default description, see Table 2-12

4.5 SDK Build details

For information on build details, see the SDK documentation.

4.6 Flashing and updating images

This section explains:

- Flashing images on NOR flash and booting from NOR Flash
- Flashing eSPI boot images
- Booting Linux

4.6.1 Flashing images on and booting from NOR flash

Onboard Images can be updated as mentioned below. On board re-start, the board should boot with new images. For information about switch settings, see **Switch settings**

- RCW programming on current bank (from U-Boot prompt)

  For T1040RDB, use rcw/t1040rdb/RR_P_66/ rcw_1400MHz.bin

NOTE

This RCW can change depending upon the requirements

```
=>    tftp 1000000 <rcw>.bin
=>    protect off all
=>    erase 0xe8000000 0xe801ffff
=>    cp.b 0x1000000 0xe8000000 $filesize
```

- FMan microcode programming on current bank (from U-Boot prompt)

```
=> tftp 0x3000000 <fsl_fman_ucode>.bin
=> protect off all
Un-Protect Flash Bank # 1
=> erase 0xEFF00000 eff1ffff

. done
Erased 1 sectors
=> cp.b 3000000 0xEFF00000 10000
Copy to Flash...
9....8....7....6....5....4....3....2....1....done
```

- U-Boot binary programming on current bank (from U-Boot prompt)

```
=> tftp 0x1000000 u-boot.bin
```

```
=> protect off all
Un-Protect Flash Bank # 1
=> erase 0xeff40000 0xeffffff

.... done
Erased 4 sectors
=> cp.b 0x1000000 0xeff40000 0xc0000
Copy to Flash...
9....8....7....6....5....4....3....2....1....done
```

- RCW programming on alternate bank (from U-Boot prompt)

  For T1040RDB, use rcw/t1040rdb/RR_P_66/ rcw_1400MHz.bin

NOTE

This RCW can change depending upon the requirements.

```
=>    tftp 1000000 <rcw>.bin
=>    protect off all
=>    erase 0xec000000 0xec01ffff
=>    cp.b 0x1000000 0xec000000 $filesize
```

- FMan microcode programming on alternate bank (from U-Boot prompt)

```
=> tftp 0x3000000 <fsl_fman_ucode>.bin
=> protect off all
Un-Protect Flash Bank # 1
=> erase 0xebf00000 ebf1ffff

. done
Erased 1 sectors
=> cp.b 3000000 0xebf00000 10000
Copy to Flash...
9....8....7....6....5....4....3....2....1....done
```

- U-Boot binary programming on alternate bank (from U-Boot prompt)

```
=> tftp 0x1000000 u-boot.bin
=> protect off all
Un-Protect Flash Bank # 1
=> erase 0xebf40000 0xebffffff

.... done
Erased 4 sectors
=> cp.b 0x1000000 0xebf40000 0xc0000
Copy to Flash...
9....8....7....6....5....4....3....2....1....done
```

4.6.2 Flashing eSPI boot images

The steps for flashing and updating images for eSPI are as follows:

1. Write `PBL1.bin` (created using QCS tool) at offset 0:

```
=>tftp 100000 PBL1.bin
=>sf probe 0
=>sf erase 0 100000
=>sf write 100000 0 $filesize
```

2. Write u-boot.bin at offset 0x40000 (256 KB):

```
=>tftp 100000 u-boot.bin
=>sf write 100000 40000 $filesize
```

3. Write FMan microcode to eSPI from offset 0x110000:

```
=>tftp 100000 fsl_fman_ucode_xx.bin
=>sf erase 110000 10000
=>sf write 100000 110000 $filesize
```

4. Shut down the board.
5. Change board switch configuration for eSPI boot.
6. Switch on the board.

NOTE

For more information about building U-Boot images, generating PBL images, see eSPI/SD/NAND boot in SDK documentation.

4.6.3 Flashing NAND boot images

The steps for flashing and updating images for NAND are as follows:

All operations are done on the target in the U-Boot console.

1. Write PBL1.bin to NAND from offset 0x0:

```
=>tftp 100000 PBL1.bin
=>nand info
=>nand erase 0 100000
=>nand write 100000 0 $filesize
```

2. Write u-boot.bin to NAND from offset 0x40000 (256 KB):

```
=>tftp 100000 u-boot.bin
=>nand write 100000 40000 $filesize
```

3. Write FMan microcode to NAND from offset 0x180000:

```
=>nand info
=>tftp 100000 fsl_fman_ucode_xx.bin
=>nand erase 180000 80000
=>nand write 100000 180000 $filesize
```

4. Shut down the board.
5. Change board switch configuration for NAND boot.
6. Switch on the board.

NOTE

For more information about building U-Boot images, generating PBL images, see eSPI/SD/NAND boot in SDK documentation.

4.6.4 Flashing SD card boot images

The steps for flashing and updating images for SD card are as follows:

You need to write two images, the first is the `PBL1.bin` produced by QCS tool, the second is the `u-boot.bin`.

1. Write `PBL1.bin` at offset block 8:

```
=>tftp 100000 PBL1.bin
=>mmcinfo
=>mmc write 100000 8 block_number
```

2. Write u-boot.bin at offset 0x41000 (260KB), for example, 520(0x208) blockes.

```
=>tftp 100000 u-boot.bin
=>mmc write 100000 208 block_number
```

3. Write FMan microcode to SD card from block 0x820:

```
=>tftp 100000 fsl_fman_ucode_xx.bin
=>mmc write 100000 820 block_number
```

4. Shut down the board.
5. Change board switch configuration for SD boot.
6. Switch on the board.

NOTE

For more information about building U-Boot images, generating PBL images, see eSPI/SD/NAND boot in SDK documentation.

4.6.5 Booting Linux

- Setting bootargs and serverip at U-Boot prompt:

```
                =>    setenv bootargs "root=/dev/ram rw console=ttyS0,115200
ramdisk_size=700000”
                =>    setenv ethact  FM1@DTSEC4
                =>    setenv ipaddr  <ipaddr>
                =>    setenv serverip <serverip>
```

- From U-Boot prompt, for booting Linux with 32-bit configuration on T1040RDB:

```
                =>    setenv my_kern 'tftp 0x1000000  <uImage>’
                =>    setenv my_fs 'tftp 0x2000000  <rfs_e5500.bin>'
```

```
=>    setenv my_dtb 'tftp 0x00c00000 <t1040rdb.dtb>'
=>    setenv my_boot bootm 0x1000000 0x2000000 0x0c00000
=>    setenv boot run my_dtb my_fs my_kern my_boot
=>    save
=>    run boot
```

- From U-Boot prompt, for booting Linux with 64-bit configuration on T1040RDB:

```
=>    setenv my_kern 'tftp 0x1000000  <uImage_64bit>’
=>    setenv my_fs 'tftp 0x2000000  <rfs_e5500.bin>'
=>    setenv my_dtb 'tftp 0x00c00000 <t1040rdb.dtb>'
=>    setenv my_boot bootm 0x1000000 0x2000000 0x0c00000
=>    setenv boot run my_dtb my_fs my_kern my_boot
=>    save
=>    run boot
```

Appendix A
Revision History

Table A-1 summarizes revisions to this document.

Table A-1. Revision history

Revision	Date	Description
0	06/2015	Initial release.

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