UM12404

KITPF8150FRDMEVM/KITPF8250FRDMEVM evaluation board

Rev. 1.0 — 19 November 2025 User manual

Document information

Information	Content
Keywords	UM12404, KITPF8150FRDMEVM, KITPF8250FRDMEVM, PF8150, PF8250, buck, regulator, FlexGUI, FRDM-KL25Z, freedom, board, PMIC, EVB
Abstract	The KITPF8150FRDMEVM/KITPF8250FRDMEVM evaluation board features the PF8150/PF8250 power management IC.

1 Introduction

This document is the user guide for the PF8150/PF8250 evaluation boards. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of multi-channel power management integrated circuit PF8150/PF8250.

The scope of this document is to provide the user with information to evaluate the multi-channel power management integrated circuit PF8150/PF8250. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

These customer evaluation boards provide full access to all the features in the PF8150 or PF8250 device.

Table 1. Device support

Evaluation board	PMIC device	Link
KITPF8150FRDMEVM	PF8150	https://www.nxp.com/products/PF81-PF82
KITPF8250FRDMEVM	PF8250	https://www.nxp.com/products/PF81-PF82

1.1 KITPF8150FRDMEVM/KITPF8250FRDMEVM evaluation board

The following figure depicts the KITPF8150FRDMEVM/KITPF8250FRDMEVM evaluation board.

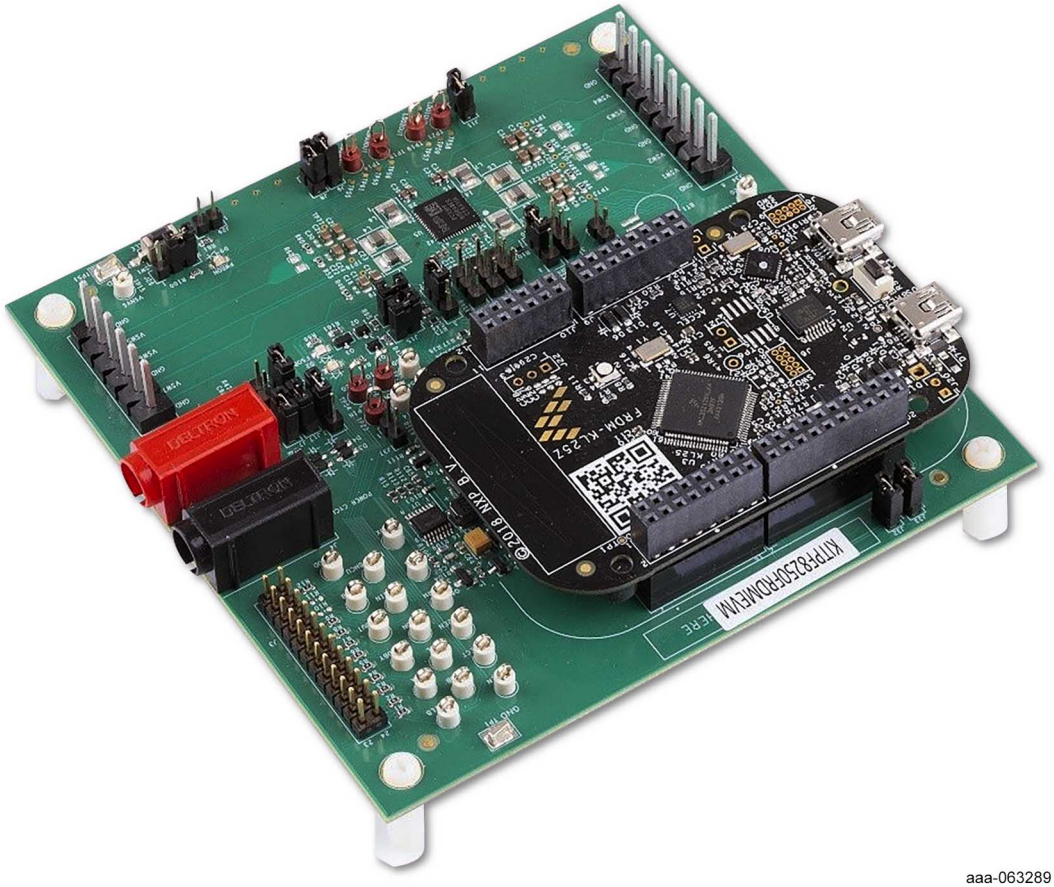


Figure 1. KITPF8150FRDMEVM/KITPF8250FRDMEVM evaluation board

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides this evaluation product under the following conditions:

Evaluation kits or reference designs are intended solely for technically qualified professionals, specifically for use in research and development environments to facilitate evaluation purposes. This evaluation kit or reference design is not a finished product, nor is it intended to be a part of a finished product. Any software or software tools provided with an evaluation product are subject to the applicable terms that accompany such software or software tool.

The evaluation kit or reference design is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit or reference design may be used with any development system or other source of I/O signals by connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality. This evaluation kit or reference design provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the evaluation product. Due to the open construction of the evaluation product, it is the responsibility of the user to take all appropriate precautions for electric discharge. To minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 Finding kit resources and information on the NXP web site

NXP provides online resources for evaluation boards and its supported device(s) on https://www.nxp.com/.

The information page for evaluation boards are at https://www.nxp.com/KITPF8X50FRDMEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to these evaluation boards, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP Power Management community is at https://community.nxp.com/t5/Power-Management/bd-p/Power-Management.

3 Getting ready

Working with these evaluation boards requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0ft. USB-STD A to USB-B-mini cable or USB-Type C cable, this depends on the FRDM-KL25Z board version
- Quick Start Guide

Note: *This document describes the steps to follow for the old version of the FRDM-KL25Z USB-B mini connector. However, if you get the board with the new version of FRDM-KL25Z, the picture may be different, but you have to follow the same steps.*

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 3.0 V to 5.0 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 7.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 to 11

3.4 Software

Installing software is necessary to work with this evaluation board. There is one universal GUI for NXP's Automotive PMIC products, which can be found in the link: NXP GUI for Automotive PMIC Families

Download and install the latest version GUI in PC. The evaluation board (EVB) can be operated easily using the GUI. In this document, we made an example by using Rev 10.0.0.

One version of the PF8x firmware can be found in the GUI folder. This version may need to be updated to use the FRDM-KL25Z auxiliary board. More information will be introduced in Section 5.

4 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

4.1 Kit overview

These customer evaluation boards feature the PF8150/PF8250 power management IC. The kit integrates all hardware needed to fully evaluate the PMIC.

It integrates a communication bridge based on the FRDM-KL25Z freedom board to interface with the PMIC GUI software interface to fully configure and control the PF8150/PF8250 PMIC.

4.1.1 Evaluation board features

Buck regulators

- SW1, SW2, SW3, SW4, SW5, SW6: 0.4 V to 1.8 V; 2500 mA; 1.5 % accuracy and dynamic voltage scaling and single, dual, triple, or quad-phase configuration
- SW7; 1.0 V to 4.1 V; 2500 mA; 2 % accuracy
- Configurable VTT termination mode on SW6
- Programmable current limit
- Spread-spectrum and manual tuning of switching frequency

LDO regulators

- 4x LDO regulator 1.5 V to 5.0 V, 400 mA: 3 % accuracy with optional load switch mode
- Selectable hardware/software control on LDO2

RTC supply

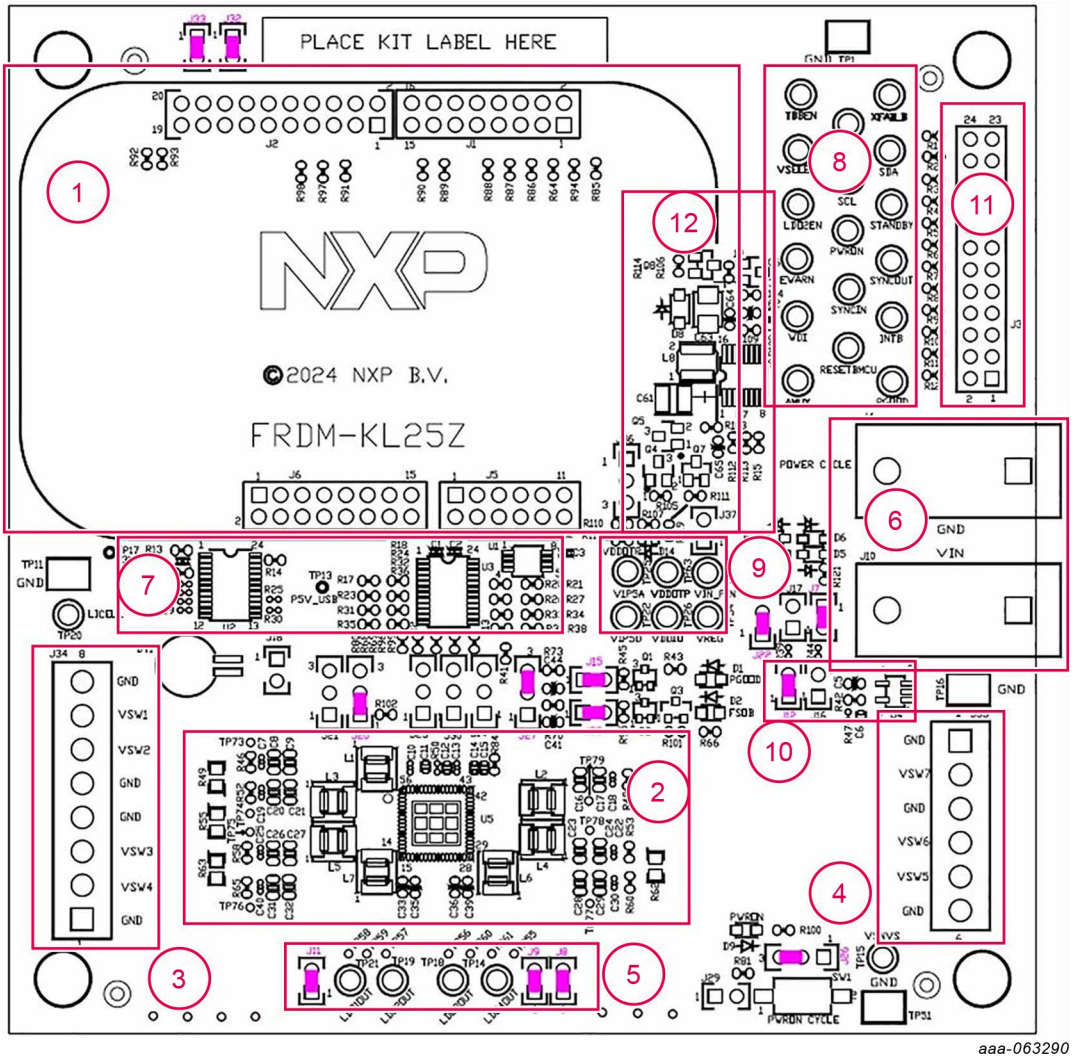
- VSNVS 1.8 V/3.0 V/3.3 V, 10 mA
- Battery backed memory including coin cell charger with programmable charge current and voltage

System features

- 2.7 V to 5.5 V operating input voltage range
- USB to I^2C communication via the FRDM-KL25Z interface
- Selectable hardwire default PMIC configuration or OTP/TBB operation
- Fast mode I^2C communication at 400 kHz (high speed operation supported by PMIC)
- Advance system monitoring/diagnostic via PMIC and/or system analog multiplexer (AMUX)
- Primary/secondary interface connector
- Onboard I/O regulator with 1.8 V/3.3 V selectable output voltage

4.2 Kit featured components

Figure 2 identifies important components on the board.



1. FRDM-KL25Z Freedom board connector
2. PF8150/PF8250 PMIC
3. SW1 to SW4 power connector
4. SW5 to SW7 power connector
5. LDO output test points
6. Input power banana jack
7. External analog multiplexer
8. PMIC I/O test points
9. Analog supplies test points
10. 1.8 V/3.3 V external LDO regulator
11. Primary/secondary interface connector
12. Boost circuit to generate 8V for VDDOTP

Figure 2. Evaluation board featured component locations

4.2.1 PF8150/PF8250: 12-channel power management integrated circuit for high performance applications

4.2.1.1 General description

The PF8150 and PF8250 are compatible with PF8100 and PF8200. The PF81-PF82 family of devices feature a power management integrated circuit (PMIC) designed for high performance applications based on NXP's i.MX 8 and S32x processors, and on other non-NXP processors. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory, and miscellaneous peripherals.

Built-in one time programmable memory stores key startup configurations, drastically reducing the number of external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C after start up offering flexibility for different system states.

The PF8150/PF8250 family comprises two versions of this PMIC, to address different market needs:

- PF8250 is the flagship version of this family providing a full feature PMIC with integrated functional safety mechanism to comply with the ISO 26262 standard and providing a powerful and flexible solution for automotive safety integrity level (ASIL) B automotive modules.
- PF8150 is the non-safety version of this product. It provides all the power management and digital control included in PF8250 without the functional safety overhead, for a more economic platform for non-safety systems. The industrial and consumer grade PF8150 is also available for non-automotive uses.

4.2.1.2 Features

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Monitoring circuit developed in compliance with ASIL B process (PF8250 only)
- One time programmable device configuration
- 3.4 MHz I^2C communication interface
- 56-pin 8 mm x 8 mm QFN package

4.3 Schematic, board layout and bill of materials

The board layout and bill of materials for these evaluation boards are available at https://www.nxp.com/KITPF8X50FRDMEVM.

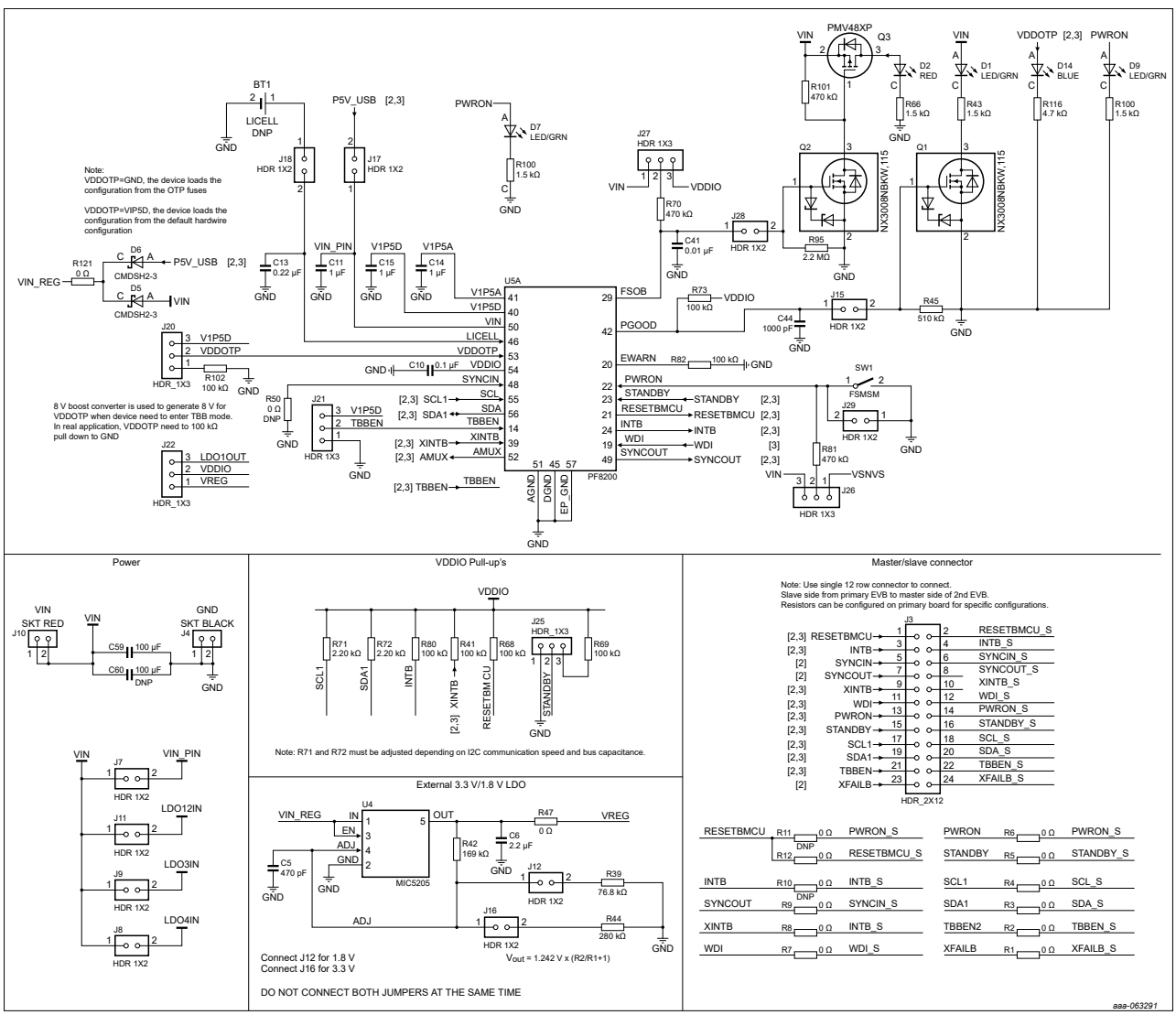


Figure 3. PF8150/PF8250 system I/O

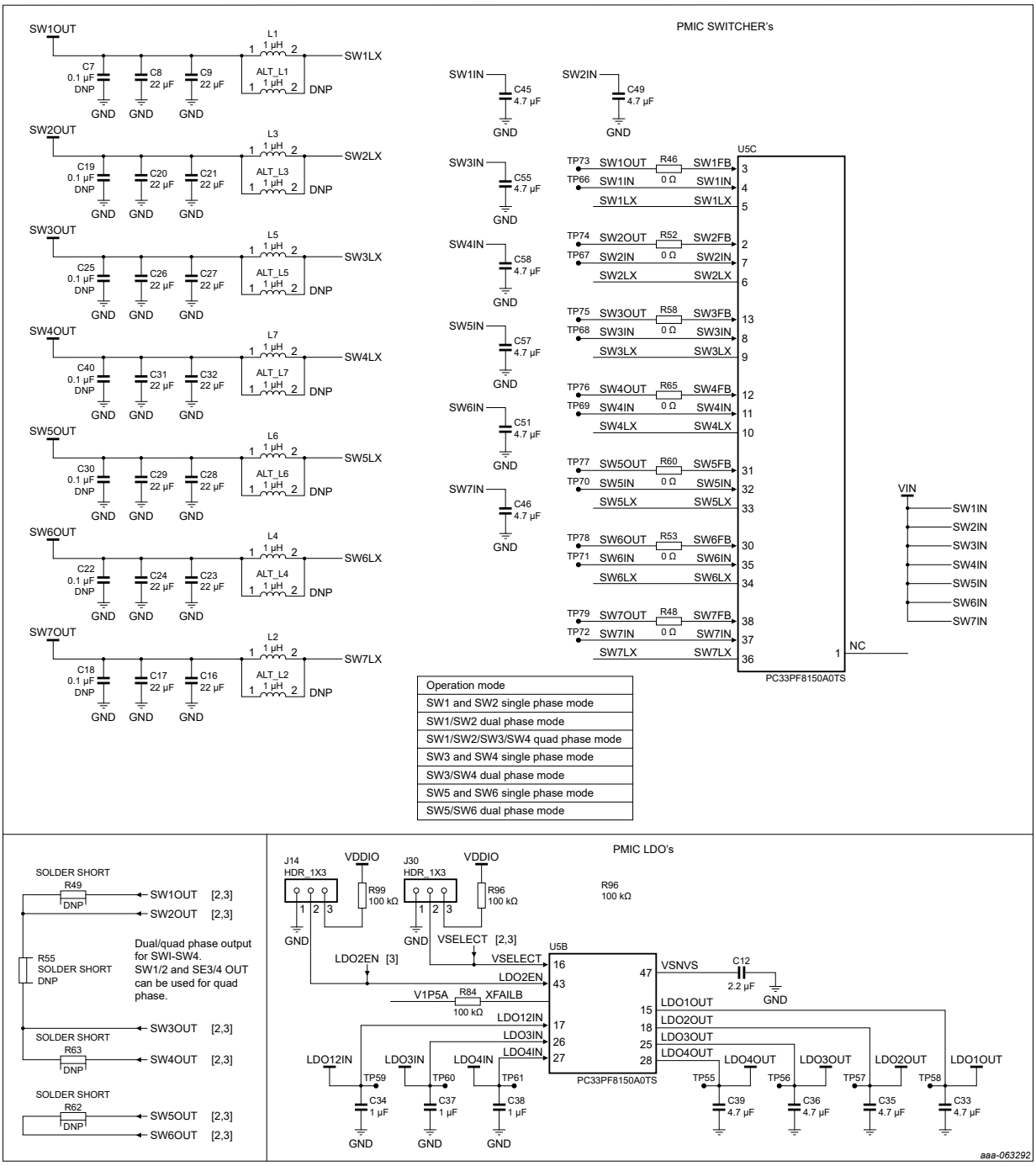


Figure 4. Voltage regulators

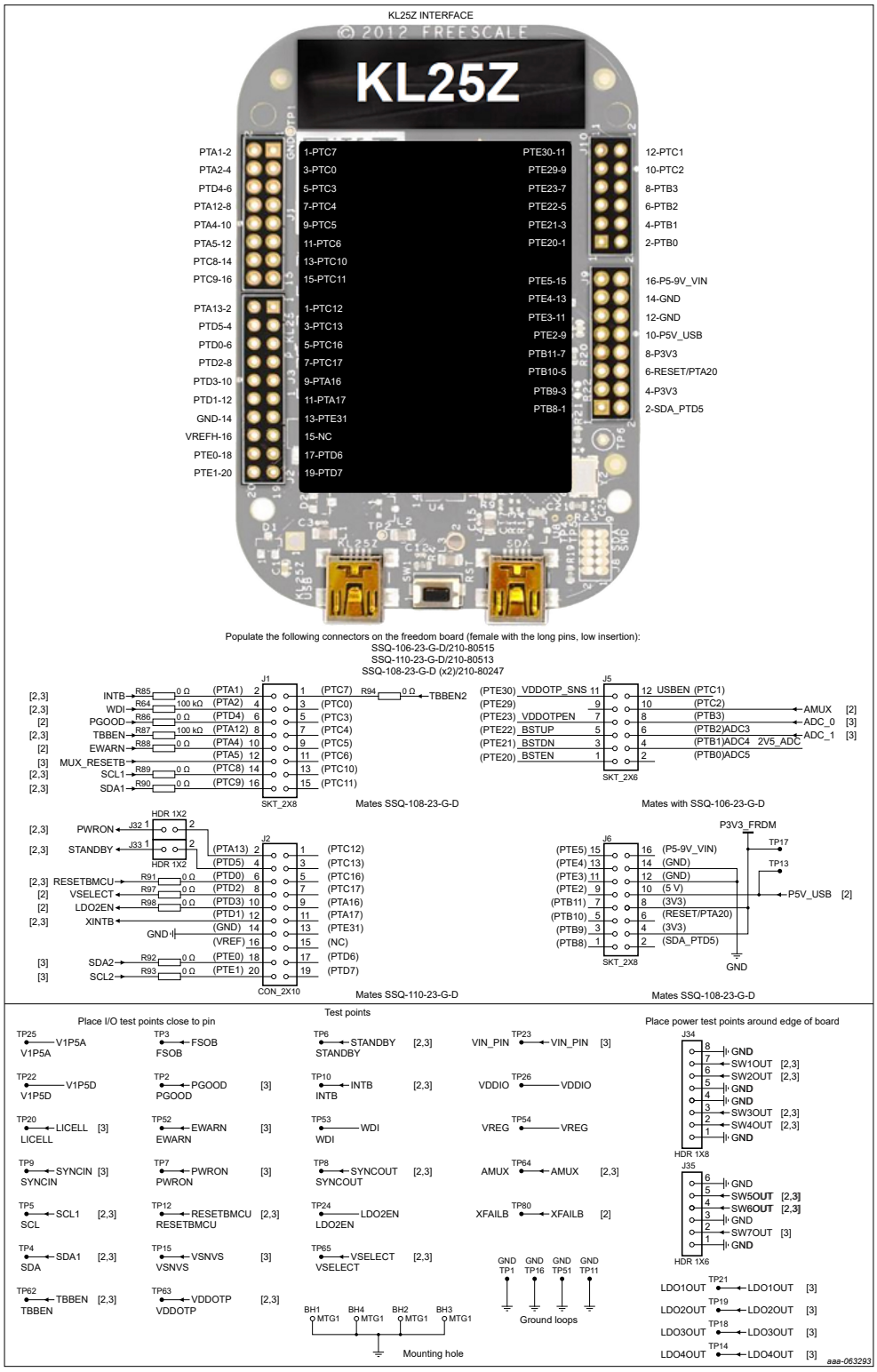


Figure 5. Connectors and test points

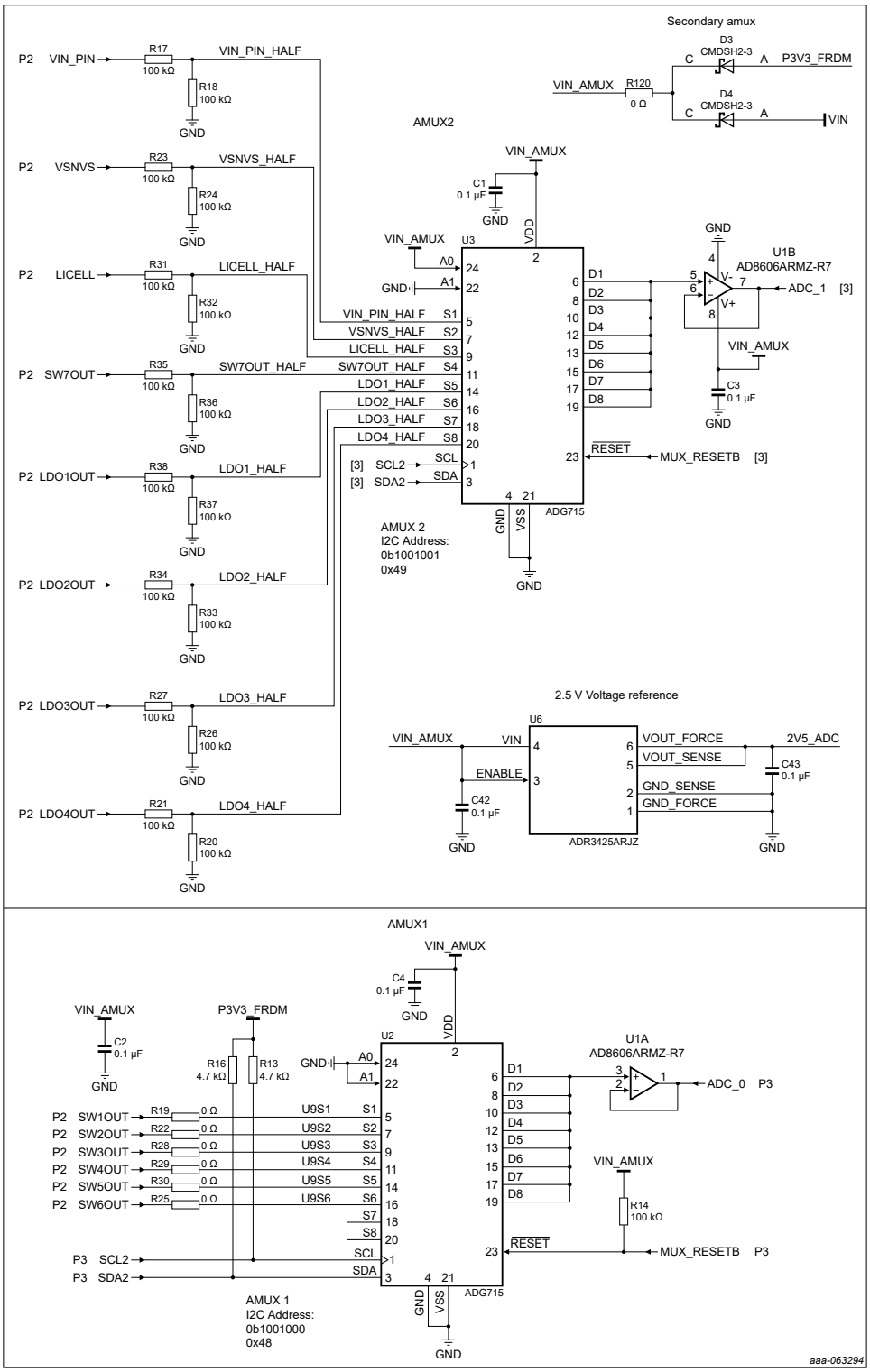


Figure 6. Onboard analog multiplexing blocks

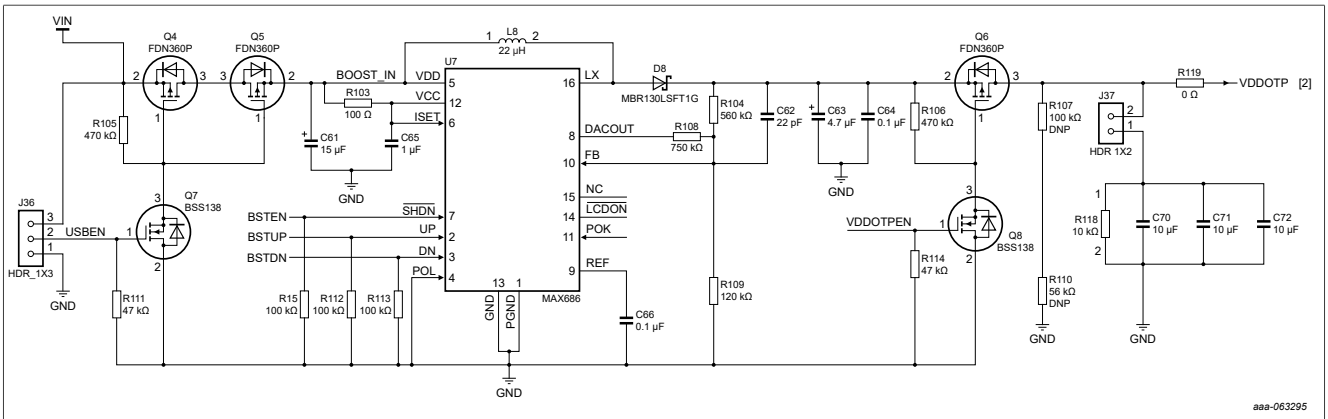


Figure 7. 8V – Boost converter

4.4 Default jumper configurations

Table 2. Evaluation board jumper descriptions

Name	Default	Description
J1, J2, J5, J6	—	Freedom board interface
J3	—	Primary/secondary connector • Odd row is connected directly to pins in the primary board • Even row is used to connect a secondary board signals • Interface connection is made via shunt resistors R1 to R11
J7	Shorted	Connects PMIC VIN to main board VIN node
J8	Shorted	Connects LDO4IN to main board VIN node
J9	Shorted	Connects LDO3IN to main board VIN node
J11	Shorted	Connects LDO12IN to main board VIN node
J12	Shorted	Selects the external LDO voltage • J12 → 1.8 V • J16 → 3.3 V
J16	Open	
J14	Open	LDO2EN pin control • 1-2 → LDO2EN pin pulled low • 2-3 → LDO2EN pin pulled high • Open → full MCU control with no pull up
J15	Shorted	Enables the PGOOD green LED
J17	Open	Supplies PMIC VIN from 5.0 V supply on Freedom Board (used only for demo functional operation, no loading capability in this operation mode)
J18	Open	Connects coin cell to the LICELL node
J20	1-2 shorted	Selects PF8150/PF8250 default register configuration • 1-2 → OTP mode • 2-3 → Hardwire mode
J21	Open	Enables TBB mode on PF8x00 device • 1-2 → TBB mode disabled • 2-3 → TBB mode enabled • Open → MCU has control of this pin
J22	1-2 shorted	Selects VDDIO supply • 1-2 → VDDIO is supplied by external LDO regulator • 2-3 → VDDIO is supplied by LDO1
J25	Open	Selects STANDBY pin voltage level

Table 2. Evaluation board jumper descriptions...*continued*

Name	Default	Description
		• 1-2 → STANDBY pin low • 2-3 → STANDBY pin high • Open → STANDBY pin controlled by MCU
J26	2-3 shorted	Controls PWRON pull up source • 1-2 → PWRON pulled up to VSNVS • 2-3 → PWRON pulled up to VIN • Open → full MCU control with no pull up
J27	2-3 shorted	Selects pull up for FSOB pin • 1-2 → FSOB pulled up to VIN • 2-3 → FSOB pulled up to VDDIO
J28	Shorted	Enables the FSOB red LED
J29	Open	Pulls down PWRON pin to ground
J30	Open	VSELECT pin control • 1-2 → VSELECT pin pulled low • 2-3 → VSELECT pin pulled low • Open → full MCU control with no pull up
J32	Shorted	PWRON connection from PMIC to MCU
J33	Shorted	STANDBY connection from PMIC to MCU
J36	Open	Boost circuit control by MCU
J37	Open	8 V output cap disable

4.5 Test points

Table 3. Evaluation board test point descriptions

Name (label)	Signal name	Description
Ground test points		
TP1, TP11, TP16, TP51 (GND)	GND	Ground plane test points
Digital I/O signal		
TP2 (PGOOD)	PGOOD	Connected to pin 42 (PGOOD) on PMIC
TP3 (FSOB)	FSOB	Connected to pin 29 (FSOB) on PMIC
TP4 (SDA)	SDA1	Connected to pin 56 (SDA) on PMIC. Main system I^2C bus.
TP5 (SCL)	SCL1	Connected to pin 55 (SCL) on PMIC. Main system I^2C bus.
TP6 (STANDBY)	STANDBY	Connected to pin 23 (STANDBY) on PMIC
TP7 (PWRON)	PWRON	Connected to pin 22 (PWRON) on PMIC
TP8 (SYNCOUT)	SYNCOUT	Connected to pin 49 (SYNCOUT) on PMIC
TP9 (SYNCIN)	SYNCIN	Connected to pin 48 (SYNCIN) on PMIC
TP10 (INTB)	INTB	Connected to pin 24 (INTB) on PMIC
TP12 (RESETBMCU)	RESETBMCU	Connected to pin 21 (RESETBMCU) on PMIC
TP24 (LDO2EN)	LDO2EN	Connected to pin 43 (LDO2EN) on PMIC
TP52 (EWARN)	EWARN	Connected to pin 20 (EWATN) on PMIC
TP53 (WDI)	WDI	Connected to pin 19 (WDI) on PMIC
TP62 (TBBEN)	TBBEN	Connected to pin 14 (TBBEN) on PMIC
TP65 (VSELECT)	VSELECT	Connected to pin 16 (VSELECT) on PMIC

Table 3. Evaluation board test point descriptions*...continued*

Name (label)	Signal name	Description
TP80 (XFAILB)	XFAILB	Connected to pin 44 (XFAILB) on PMIC
Analog signals		
TP15 (VSNVS)	VSNVS	Connected to pin 47 (VSNVS) on PMIC
TP20 (LICELL)	LICELL	Connected to pin 46 (LICELL) on PMIC
TP22 (V1P5D)	V1P5D	Connected to pin 40 (V1P5D) on PMIC
TP23 (VIN_PIN)	VIN_PIN	Connected to pin 50 (VIN) on PMIC
TP25 (V1P5A)	V1P5A	Connected to pin 41 (V1P5A) on PMIC
TP26 (VDDIO)	VDDIO	Connected to pin 54 (VDDIO) on PMIC
TP54 (VREG)	VREG	1.8 V or 3.3 V external regulator output
TP63 (VDDOTP)	VDDOTP	Connected to pin 53 (VDDOTP) on PMIC
TP64 (AMUX)	AMUX	Connected to pin 52 (AMUX) on PMIC
LDO test points		
TP14 (LDO4OUT)	LDO4OUT	Power path for the LDO4 output
TP18 (LDO3OUT)	LDO3OUT	Power path for the LDO3 output
TP19 (LDO2OUT)	LDO2OUT	Power path for the LDO2 output
TP21 (LDO1OUT)	LDO1OUT	Power path for the LDO1 output
TP55	LDO4OUT sense	LDO4 output sense path. Connected directly to pin 28 (LDO4OUT) on PMIC.
TP56	LDO3OUT sense	LDO3 output sense path. Connected directly to pin 25 (LDO3OUT) on PMIC.
TP57	LDO2OUT sense	LDO2 output sense path. Connected directly to pin 18 (LDO2OUT) on PMIC.
TP58	LDO1OUT sense	LDO1 output sense path. Connected directly to pin 15 (LDO1OUT) on PMIC.
TP59	LDO12IN sense	LDO1 and LDO2 input sense path. Connected directly to pin 17 (LDO12IN) on PMIC.
TP60	LDO3IN sense	LDO3 input sense path. Connected directly to pin 26 (LDO3IN) on PMIC.
TP61	LDO4IN sense	LDO4 input sense path. Connected directly to pin 27 (LDO4IN) on PMIC.
Switching regulator test points		
TP66	SW1IN sense	SW1 input sense path. Connected directly to pin 4 (SW1IN) on PMIC.
TP67	SW2IN sense	SW2 input sense path. Connected directly to pin 7 (SW2IN) on PMIC.
TP68	SW3IN sense	SW3 input sense path. Connected directly to pin 8 (SW3IN) on PMIC.
TP69	SW4IN sense	SW4 input sense path. Connected directly to pin 11 (SW4IN) on PMIC.
TP70	SW5IN sense	SW5 input sense path. Connected directly to pin 32 (SW5IN) on PMIC.
TP71	SW6IN sense	SW6 input sense path. Connected directly to pin 35 (SW6IN) on PMIC.
TP72	SW7IN sense	SW7 input sense path. Connected directly to pin 37 (SW7IN) on PMIC.
TP73	SW1OUT sense	SW1 output sense path. Connected directly to pin 3 (SW1FB) on PMIC through R46.
TP74	SW2OUT sense	SW2 output sense path. Connected directly to pin 2 (SW2FB) on PMIC through R52.
TP75	SW3OUT sense	SW3 output sense path. Connected directly to pin 13 (SW3FB) on PMIC through R58.

Table 3. Evaluation board test point descriptions*...continued*

Name (label)	Signal name	Description
TP76	SW4OUT sense	SW4 output sense path. Connected directly to pin 12 (SW4FB) on PMIC through R65.
TP77	SW5OUT sense	SW5 output sense path. Connected directly to pin 31 (SW5FB) on PMIC through R60.
TP78	SW6OUT sense	SW6 output sense path. Connected directly to pin 30 (SW6FB) on PMIC through R53.
TP79	SW7OUT sense	SW7 output sense path. Connected directly to pin 38 (SW7FB) on PMIC through R48.

4.6 Connectors

4.6.1 V_{IN} input power connector

V_{IN} is supplied to the board through standard banana jacks.

Table 4. V_{IN} Banana connectors

Schematic label	Signal name	Description
J4	GND	Main system ground
J10	V_{IN}	Main system input power supply System operating range from 2.7 V to 5.5 V

4.6.2 Switching regulators output power connectors

Table 5. SW1 through SW4 output power connector (J34)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW4OUT	SW4 regulator output
J34-3	SW3OUT	SW3 regulator output
J34-4	GND	System ground
J34-5	GND	System ground
J34-6	SW2OUT	SW2 regulator output
J34-7	SW1OUT	SW1 regulator output
J34-8	GND	System ground

Table 6. SW5 through SW7 output power connector (J35)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW7OUT	SW7 regulator output
J34-3	GND	System ground
J34-4	SW6OUT	SW6 regulator output
J34-5	SW5OUT	SW5 regulator output
J34-6	GND	System ground

4.6.3 Interface connector

Table 7. Primary/secondary interface connector (J3)

Schematic label	Signal name	Description
J3-1	RESETBMCU	Direct connection to RESETBMCU pin on board
J3-2	RESETBMCU_S	Connection to external RESETBMU signal from secondary PMIC • RESETBMCU_S may be connected to local RESETBMCU pin through R12 (default)
J3-3	INTB	Direct connection to INTB pin on board
J3-4	INTB_S	Connection to external INTB signal from secondary PMIC • INTB_S may be connected to local INTB pin through R10 (optional) • INTB_S may be connected to local XINTB pin through R8 (default)
J3-5	SYNCIN	Direct connection to SYNCIN pin on board.
J3-6	SYNCIN_S	Connection to external SYNCIN signal from secondary PMIC • SYNCIN_S may be connected to local SYNCOUT pin through R9 (default)
J3-7	SYNCOUT	Direct connection to SYNCOUT pin on board
J3-8	n.c.	Not connected
J3-9	XINTB	Direct connection to XINTB pin on board
J3-10	n.c.	Not connected
J3-11	WDI	Direct connection to WDI pin on board
J3-12	WDI_S	Connection to external WDI signal from secondary PMIC • WDI_S may be connected to local WDI pin through R7 (default)
J3-13	PWRON	Direct connection to PWRON pin on board
J3-14	PWRON_S	Connection to external PWRON signal from secondary PMIC. • PWRON_S may be connected to RESETBMCU pin through R11 (optional) • PWRON_S may be connected to PWRON pin through R6 (default)
J3-15	STANDBY	Direct connection to STANDBY pin on board
J3-16	STANDBY_S	Connection to external STANDBY signal from secondary PMIC • STANDBY_S may be connected to STANDBY pin through R5 (default)
J3-17	SCL1	Direct connection to SCL1 signal on board
J3-18	SCL_S	Connection to external SCL signal from secondary PMIC • SCL_S may be connected to SCL1 pin through R4 (default)
J3-19	SDA1	Direct connection to SDA1 signal on board
J3-20	SDA_S	Connection to external SDA signal from secondary PMIC • SDA_S may be connected to SDA1 pin through R3 (default)
J3-21	TBBEN	Direct connection to TBBEN pin on board
J3-22	TBBEN_S	Connection to external TBB signal from secondary PMIC • TBBEN_S may be connected to TBBEN2 signal controlled by MCU through R2 (default)
J3-23	XFAIL	Direct connection to XFAILB pin on board
J3-24	XFAIL_S	Connection to external XFAILB signal from secondary PMIC • XFAILB_S may be connected to XFAILB signal on PMIC through R1 (default)

5 Installing and configuring software and tools

These evaluation boards use PMIC-GUI for PF8150/PF8250 device. The latest version GUI should be downloaded and used to do the operation of PMIC. In this document, the GUI version is Rev10.0.

5.1 Downloading the GUI

1. Sign into the NXP website and open the link to NXP GUI for Automotive PMIC Families, and then download the zip files. Read the agreement for the GUI and if everything is okay, accept that. The download will start to the location you select.

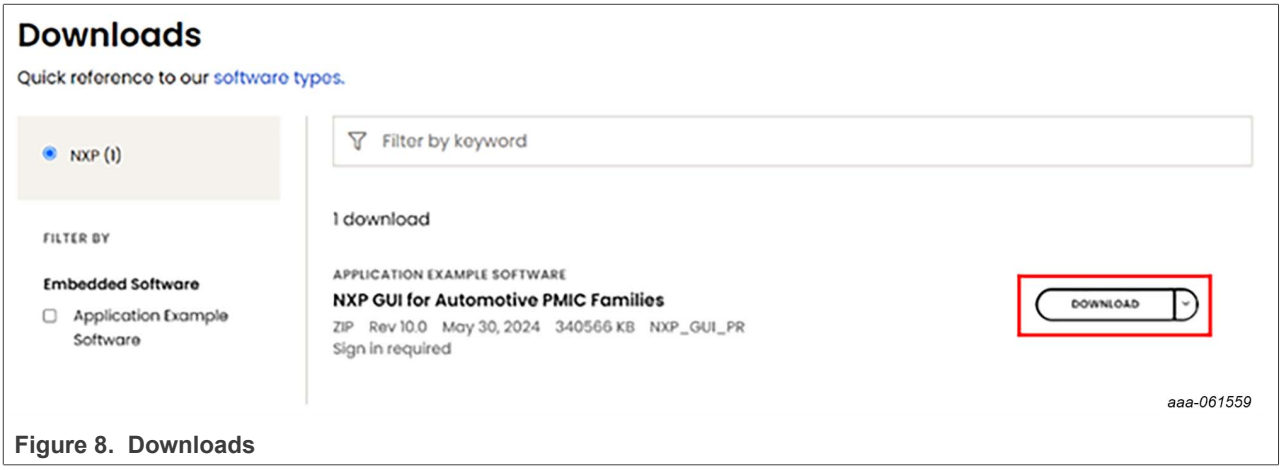


Figure 8. Downloads

2. Go to the folder location in which the GUI package is saved, unzip the files and open them. The files in the folder should be as below:

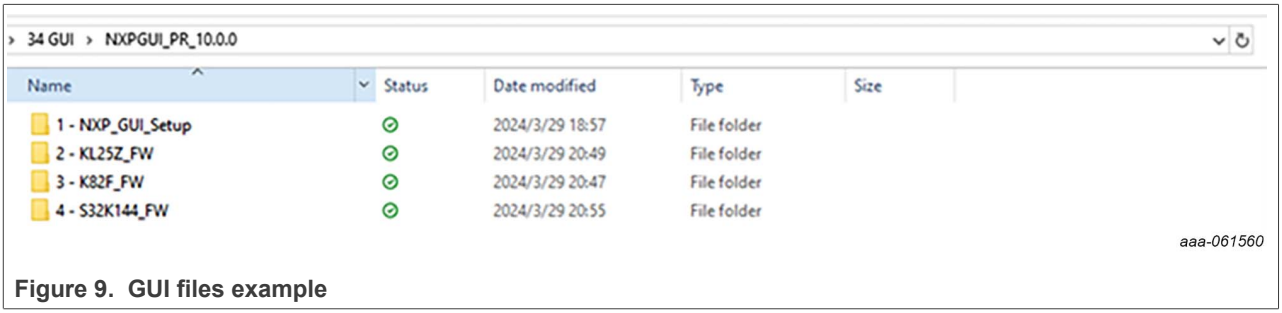


Figure 9. GUI files example

5.2 Installing and Opening GUI

1. Open the “1-NXP_GUI_Setup” folder and click the file named "NXP_GUI-10.0.0-Setup.exe”, then the GUI will be installed in the PC.

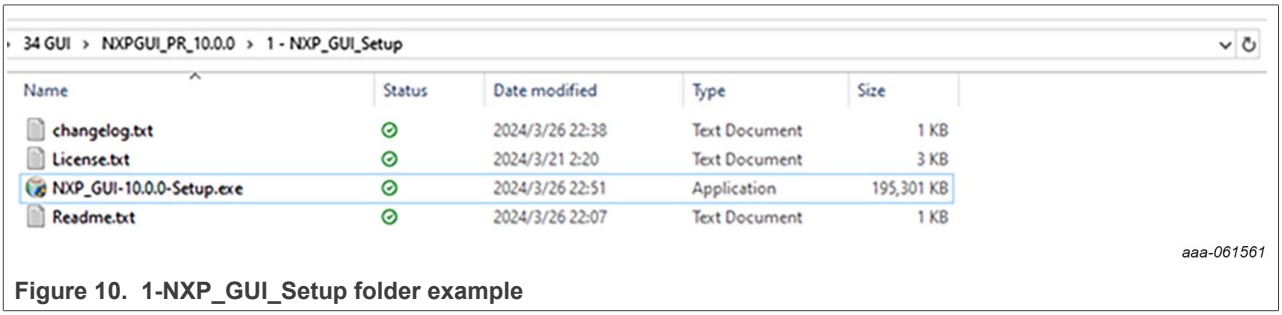


Figure 10. 1-NXP_GUI_Setup folder example

2. After the installation, open the GUI. One GUI interface, which integrates multiple products of the NXP Auto PMICs, can be found as below. Select the PMIC product on the evaluation board and open that. For example, if the evaluation board is KITPF8150FRDMEVM, select PF8150 and click **OK**.

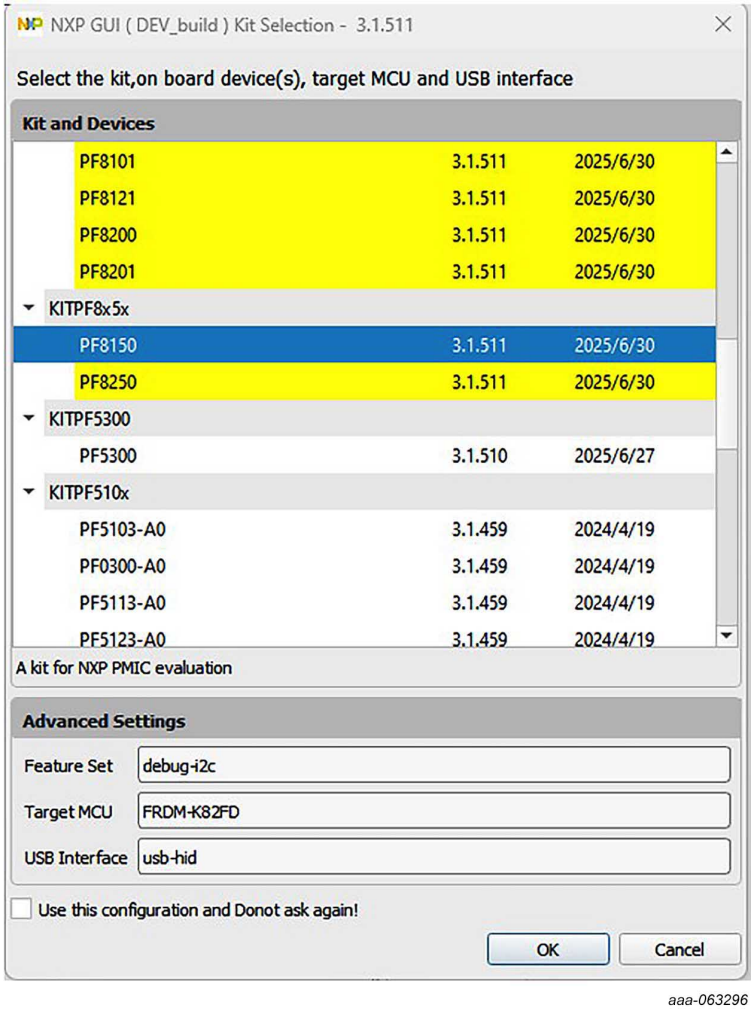


Figure 11. PF8150 kit selection example

5.3 Updating the PF8150/PF8250 firmware

The FRDM-KL25Z freedom board is used as a communication bridge to interface the GUI with the PMIC and other I^2C devices. The firmware is organized in three levels:

1. At the first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed to avoid permanent damage to the Freedom board.
2. At the second level, the SDA provides a *firmware loader* for a drag and drop update of the KL25Z MCU firmware.
3. At the third level, the KL25Z MCU provides the GUI firmware in charge of converting the USB communication into MCU instructions to control digital I/Os as well as I^2C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

Note: *The following firmware updates are optional and can be skipped if the firmware is up-to-date. First, try to connect the FRDM-KL25Z USB connector with PC, and open the GUI, if the board connects successfully after clicking* ***Start****, it means that the firmware does not need to be updated.*

5.3.1 Flashing the FRDM-KL25Z firmware loader

1. Press the **Push** button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer.

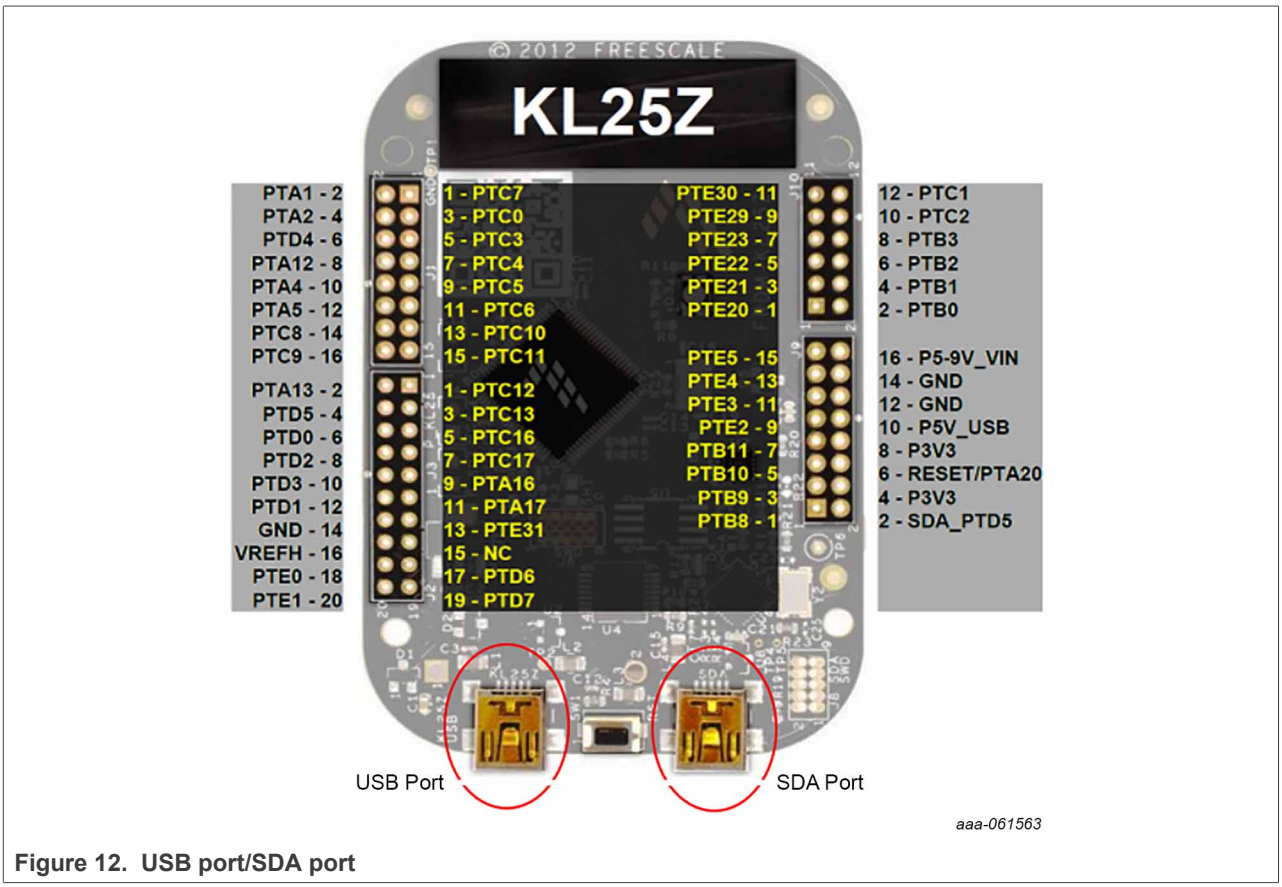


Figure 12. USB port/SDA port

2. Drag the file *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA* into the BOOTLOADER drive. The file should be located in the *KL25Z_FW* folder.

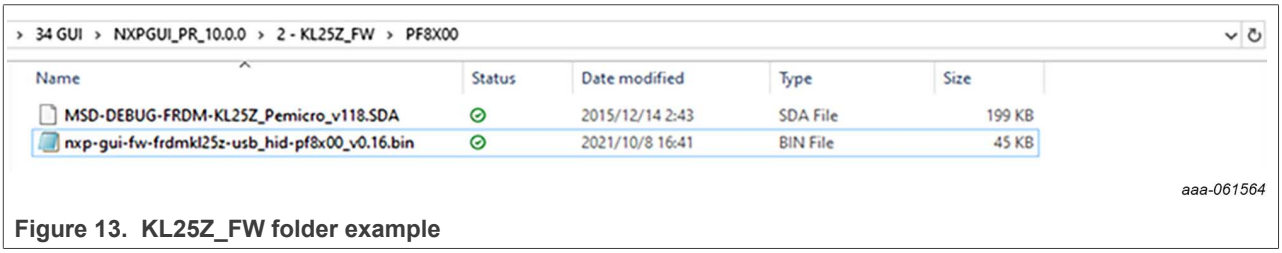


Figure 13. KL25Z_FW folder example

3. Disconnect and reconnect the USB cable into the SDA port (this time without pressing the **Push** button). A new device called *FRDM_KL25Z* is installed on the PC.

5.3.2 Flashing the GUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following procedure to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

1. Connect the USB cable in the SDA port (without holding the **Push** button).
2. Locate the ".bin" GUI driver to be installed, for example *nxp-gui-fw-frdmkl25z-usb_hid-pf8x00_v0.16.bin*, drag the file into the FRDM_KL25Z driver.

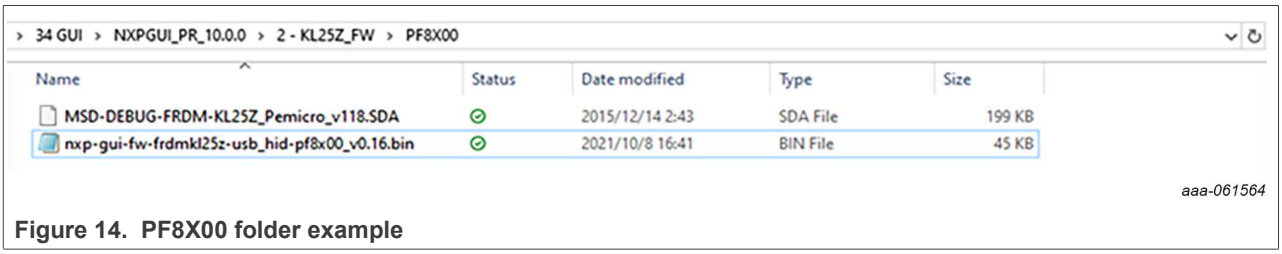


Figure 14. PF8X00 folder example

3. Freedom board firmware is successfully loaded.

6 Configuring the hardware for startup

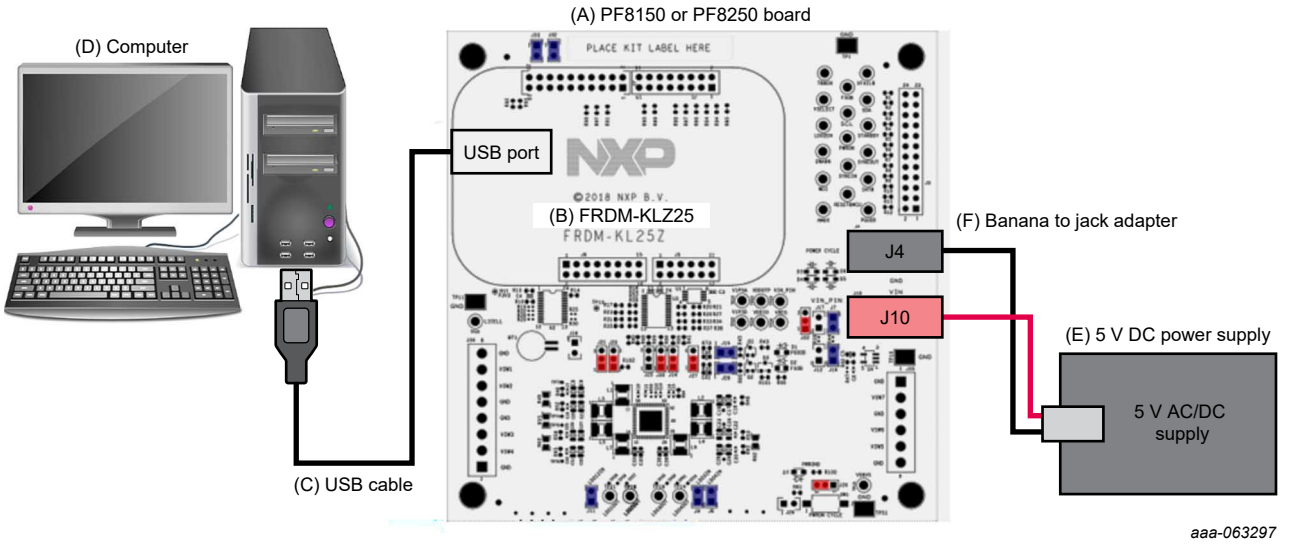


Figure 15. Typical initial configuration

1. Apply VIN to the evaluation board with the USB cable connected to the PC and the USB port in the freedom board to perform any of the following.
   - Provide external VIN between 2.5 V to 5.5 V on J10 (VIN) and J4 (GND)
   - Short jumper J17 to provide 3V3 VIN from Freedom board (use this mode of operation for functional demonstration only, no regulation loading allowed in this mode)
     Note: *Do not apply power to J10 while J17 is shorted. This could damage the onboard regulator on the FRDM-KL25Z Freedom board.*
2. Press **Reset** on the Freedom board to ensure board is properly recognized.
3. Go to Windows Start Menu and find the NXP GUI folder. Open the GUI. Once the GUI interface is launched, go trough the Kit and Devices to find the KITPF8x family. Select the part name on the evaluation board. If the board is KITPF8150FRDMEVM, select PF8150; otherwise select PF8250 if the board is KITPF8250FRDMEVM.

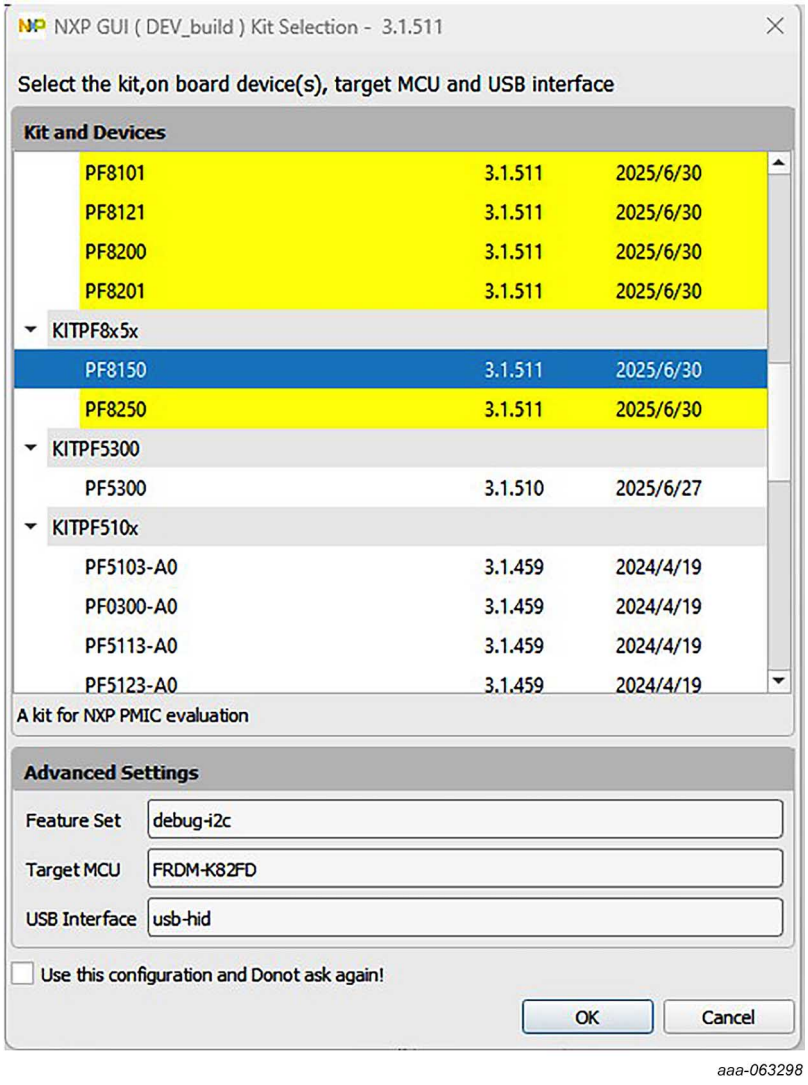


Figure 16. GUI interface kit selection

4. Open the GUI. If the firmware is matched, one blue light appears on the FRDM-KL25Z and the GUI **Start** button is operational. Click **Start**, then the FRDM-KL25Z should be connected successfully with the device in **user-mode**. If the **Start** button is gray, try to flash the firmware as Section 5.3.

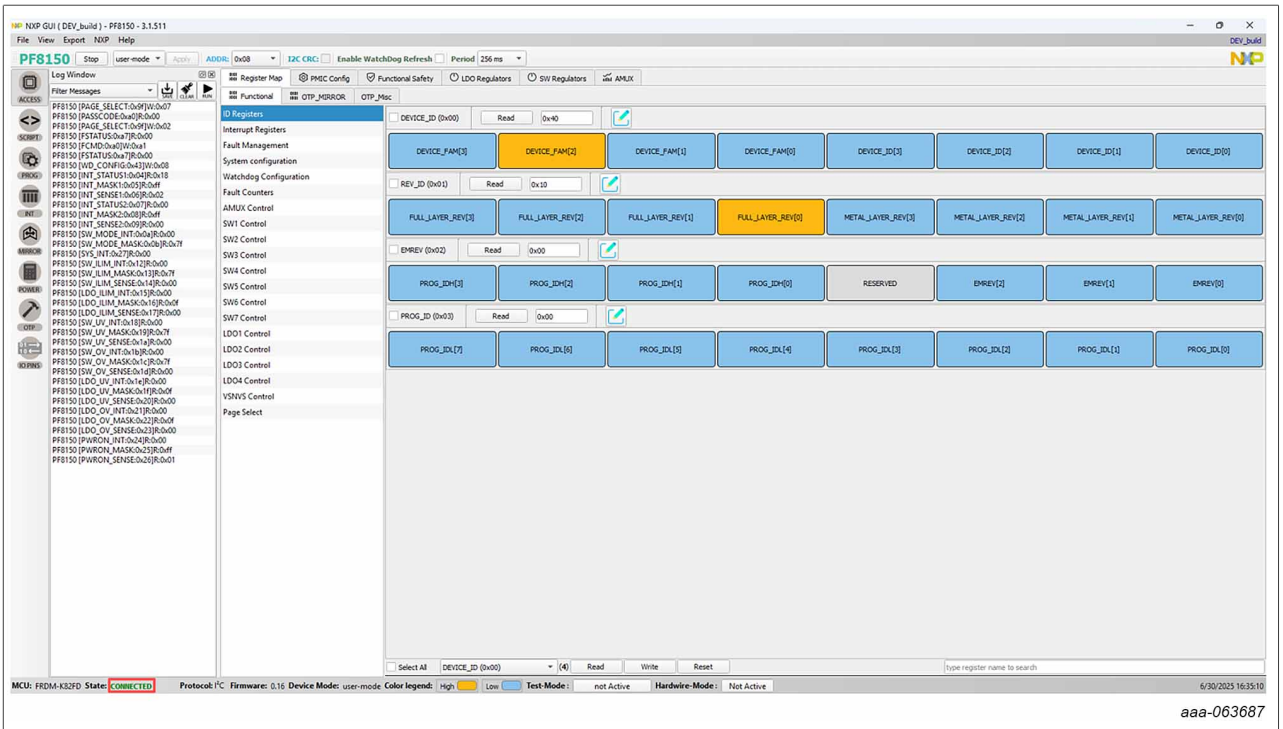


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Figure 17. FRDM_KL25Z successfully connected example

In the **user-mode**, PWRON is high and TBBEN is low, and the Functional register map can be accessed directly. The PMIC should work in Hardwire Mode or OTP Mode according to the configuration of Jumper 20.

6.1 Operating in OTP mode

By default, while the device is connected successfully, the PMIC should operate in OTP mode after a power on event using this sequence: select **user-mode** and click **Apply**. In OTP mode, the default configuration should be:

- PWORN is high by the “User mode control”, J26 is open or short 2-3 by default
- Short J20 in position 1-2 (VDDOTP=0)
- TBBEN is low by the “User mode control”, J21 is open by default.

This kind of configuration is the normal use case for most applications. In this mode, because the PMIC is not programmed and with blank OTP, there should be no output voltage. In the **ACCESS** page, functional registers can be written and read to do some PMIC operations.

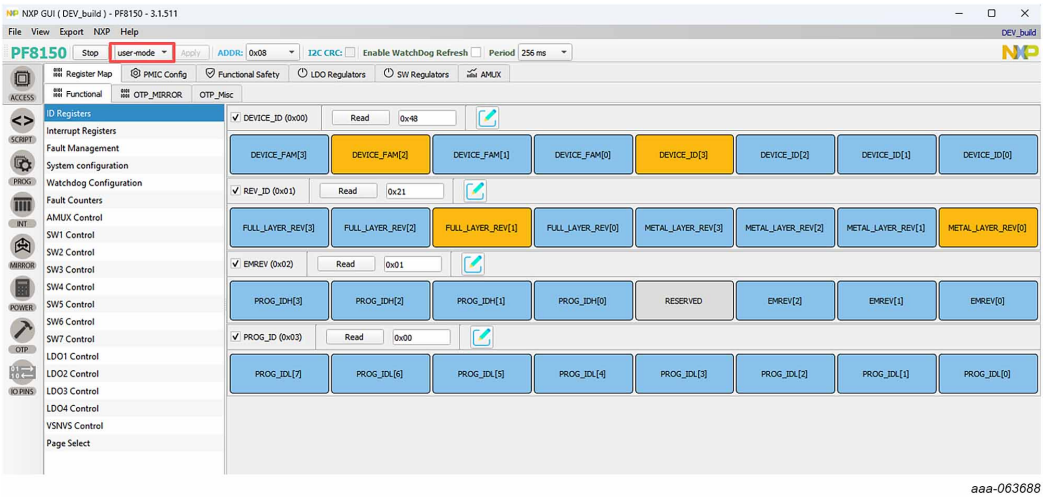

Figure 18. user-mode control

If the PMIC is programmed, there should be output voltage and sequence according to OTP configuration when PWRON is controlled from Low to high. In the real use case, as most projects use OTP part PMIC, the schematic design should follow this hardware configuration.

6.2 Operating in Hardwire mode

To operate the board with the default hardwire configuration:

- Open J29 and J26 to allow the MCU to control the PWRON pin
- Short J20 in position 2-3 (VDDOTP = V1P5D)
- Open J21 to allow the MCU to control the TBBEN pin

To generate the Power on event, select the **User mode** and **Apply**.

In Hardwire mode, the device is working with the predefined configuration and supplies turn on when the PWRON pin is set to high. The default hardwire configuration can be found in Table 78 of the PF8150_PF8250 Rev 12.0 datasheet.

To do more evaluation, the GUI can be used to operate the PMIC in Hardwire mode. See Section 7 for detailed instructiosn for how to control the PMIC with the GUI.

Hardwire mode is only for evaluation, and it is not suitable for real use cases. Make sure VDDOTP = 0 is in the real schematic design.

6.3 Operating in TBB mode

To operate the board in TBB mode:

- Open J29
- Short J20 in position 1-2 (OTP/TBB operation)
- Open J21 to allow the MCU to control the TBBEN pin

There are two ways to operate the device in TBB mode:

1. Manual configuration of the OTP mirror registers using the TBB mode control
2. Load the OTP mirror registers with a custom TBB script

6.3.1 Manual TBB configuration

During manual TBB configuration, select **tbb-mode** and click **Apply**, the device will enter TBB mode and OTP mirror registers in the PF8150/PF8250 device can be accessed from the GUI.

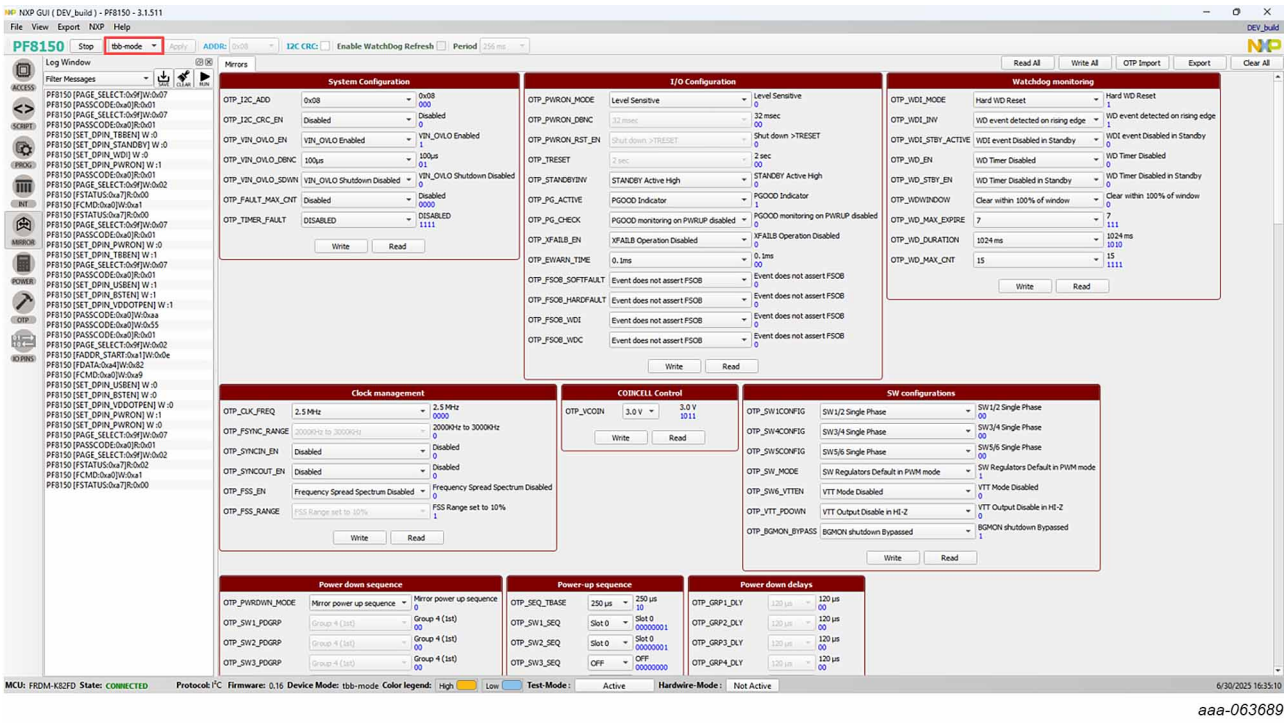

Figure 19. TBB user mode

When the GUI is operating in TBB mode, the **MIRROR** interface uses command controls to communicate with the OTP mirror registers directly, enabling the user to manually set the default configuration one feature at a time.

After configuring the features to be used during the device evaluation, change the operating mode to user mode to generate a power on event and allow command controls to modify the functional I^2C registers again.

See Section 7 for detailed instructions for controlling the PMIC using the GUI.

6.3.2 Running TBB script

To operate the TBB mode by running TBB script, one TBB script file is needed.

If a standard part that appears in the comparison table needs to be evaluated, the TBB script and configuration files can be downloaded from the comparison table.

Part Number	Description	OTP ID*	Safety Grade	Package
MC33PF8150CFTS	i.MX8QXP	CFTS Report, Programming and Configuration Files	QM	HVQFN56
MC33PF8150EATS	LS1046A	EATS Report, Programming and Configuration Files	QM	HVQFN56
MC33PF8150EPTS	i.MX8QM	EPTS Report, Programming and Configuration Files	QM	HVQFN56
MC33PF8150EQTS	i.MX8QM	EQTS Report, Programming and Configuration Files	QM	HVQFN56
MC33PF8150FJTS	i.MX8QXP	FJTS Report, Programming and Configuration Files	QM	HVQFN56
MC33PF8250CXTS	LS1043A	CXTS Report, Programming and Configuration Files	ASIL-B	HVQFN56
MC33PF8250D2TS	S32V	D2TS Report, Programming and Configuration Files	ASIL-B	HVQFN56
MC33PF8250DBTS	i.MX8QM	DBTS Report, Programming and Configuration Files	ASIL-B	HVQFN56
MC33PF8250DETS	i.MX8QXP	DETS Report, Programming and Configuration Files	ASIL-B	HVQFN56

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Figure 20. Comparison table

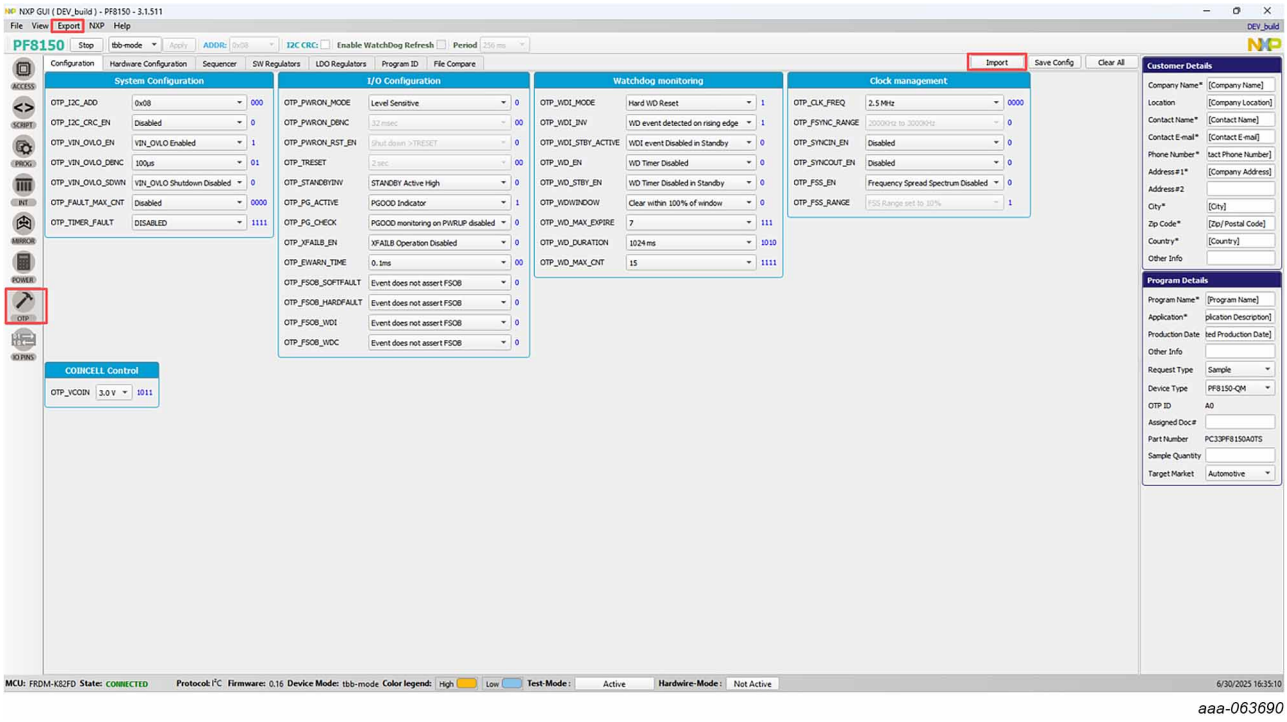
For example, when MC33PF8150FJTS is needed, and the customer needs to verify the functionality using the EVB, the downloaded files as below, each of which has a TBB script, can run directly in the **SCRIPT** page.

PF8150_FJ_CONFIG_Rev_A.txt	Text Document	2 KB	No	6 KB	66%	2025/6/12 17:07
PF8150_FJ_IHEX_Rev_A.txt	Text Document	1 KB	No	1 KB	37%	2025/6/12 17:07
PF8150_FJ_OTP_Rev_A.txt	Text Document	1 KB	No	7 KB	85%	2025/6/12 17:07
PF8150_FJ_PRF_Rev_A.txt	Text Document	1 KB	No	1 KB	48%	2025/6/12 17:07
PF8150_FJ_SHEX_Rev_A.txt	Text Document	1 KB	No	1 KB	43%	2025/6/12 17:07
PF8150_FJ_TBB_Rev_A.txt	Text Document	1 KB	No	4 KB	83%	2025/6/12 17:07
R_MC33PF8150FJ_Rev_A.pdf	Kofax Power PDF Docum...	423 KB	No	762 KB	45%	2025/6/12 17:07

aaa-063300

Figure 21. Example of downloaded files

If the customer needs to adjust the configuration depending on the standard part, go to the **OTP** GUI page and import the downloaded CONFIG file, then do the modifications on the page. Export the TBB files and save them in one location.

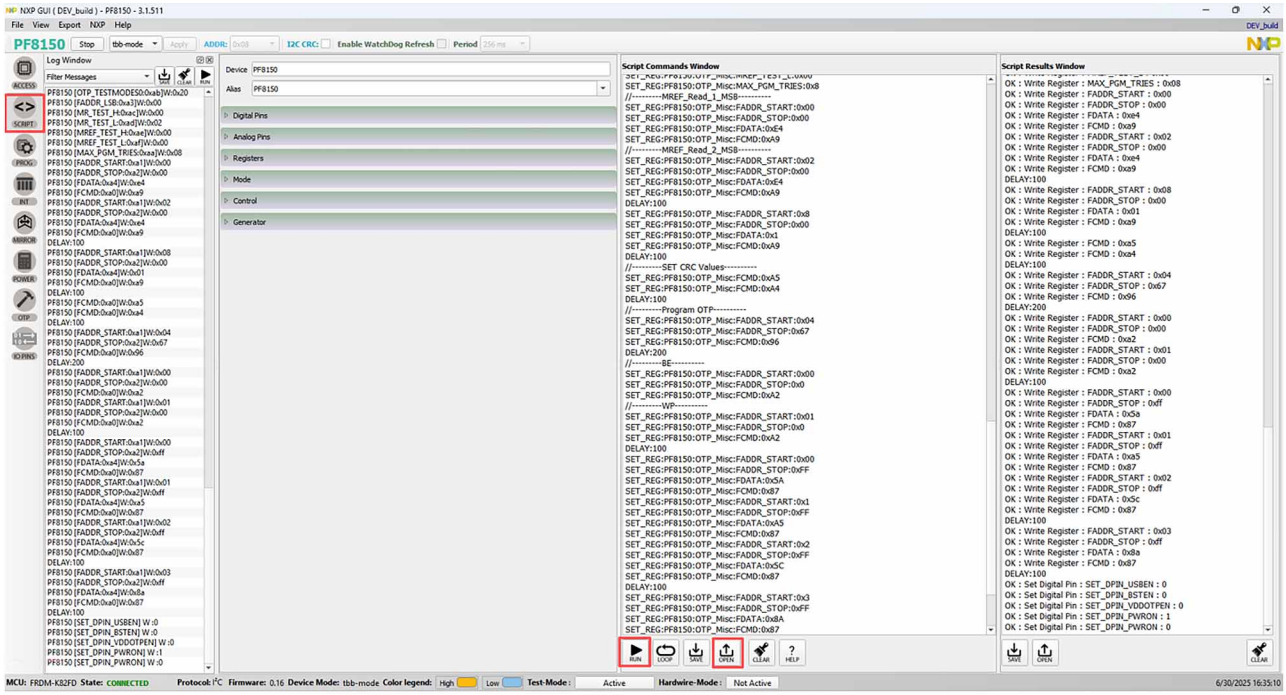


aaa-063690

Figure 22. OTP controls

Customers can configure the mirror register in the OTP page by themselves, and then export the TBB files, saving them in one location in PC.

After the TBB file is ready and saved, open the GUI **SCRIPT** page and click **OPEN** button in **Script Commands** Window to load the TBB files, then click **RUN** to write the mirror register in the PMIC by TBB mode.



aaa-063691

Figure 23. OTP SCRIPT view

The device is automatically enabled with the selected TBB configuration after the programming is done. D7 is lighted to show PWRON is high. If PGOOD is used to indicate the status of each of the power rails, D1 is lighted to show there is no OV and UV of each power rails as well. The device works as the OTP mirror register setting.

Note: *If there are multiphase power rails setting in the OTP mirror register map, R49, R55, R63, and R62 can be used to mount 0 ohm register(s) to short the multiphase power rails.*

7 Evaluating the PF8150/PF8250 using GUI

7.1 PMIC GUI introduction

NXP GUI for Automotive PMIC Families is developed by a third party, which supports nearly all NXP Auto PMIC products. The GUI is professional and easily to be used to evaluate the complicated product. Customers should download the newest version from the website and install that.

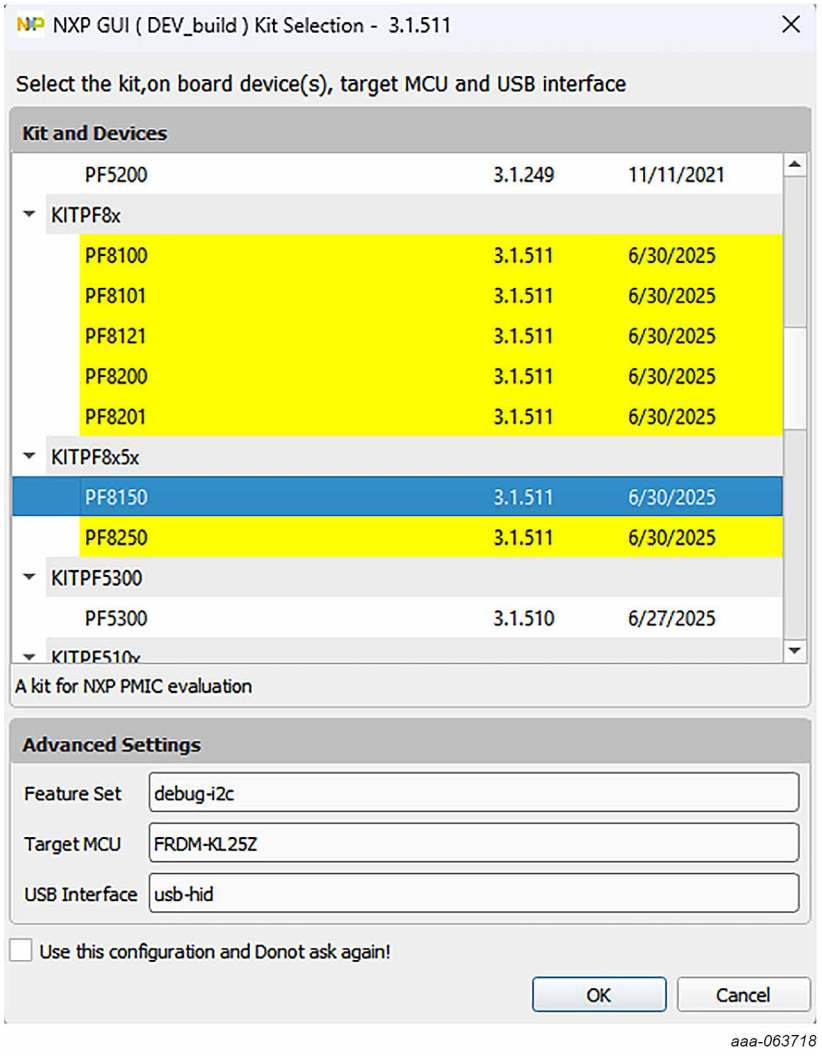


Figure 24. PMIC GUI

When starting the GUI, select the dedicated product you are working on, for example, if KITPF8150FRDMEVM is used, select PF8150 in the GUI, and if KITPF8250FRDMEVM is used, select PF8250 KIT in the GUI.

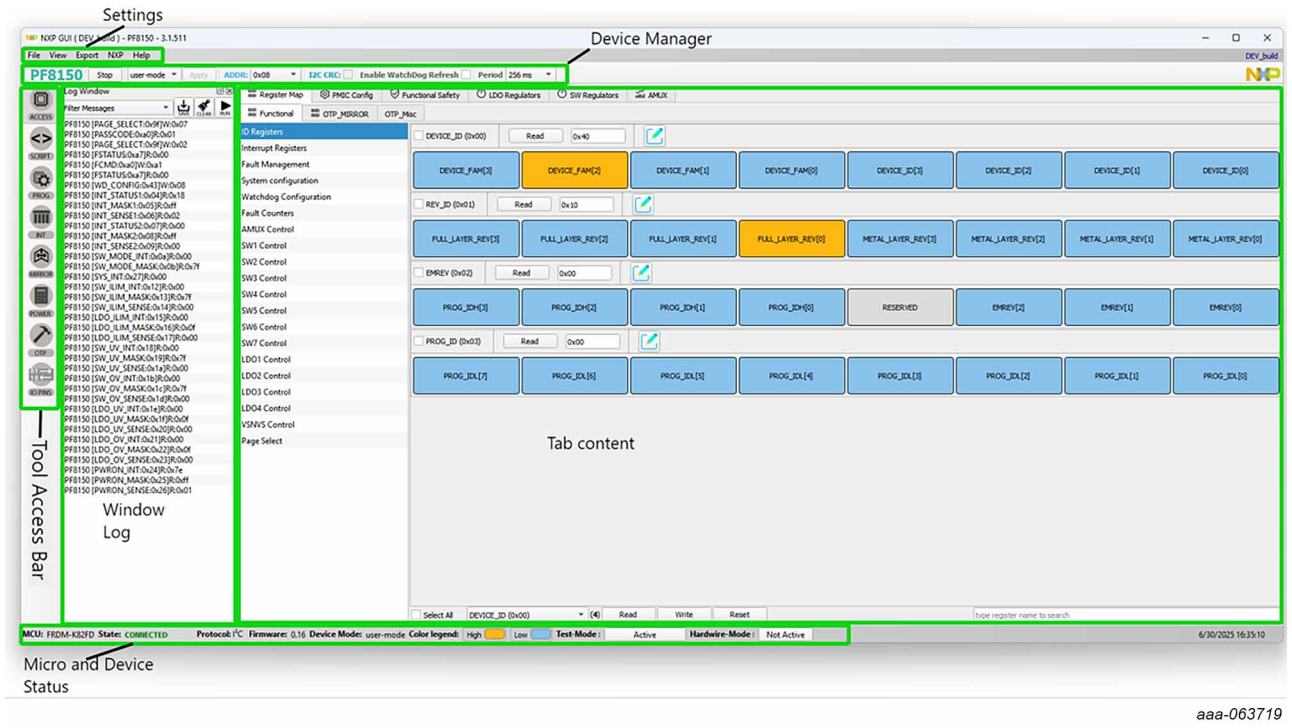


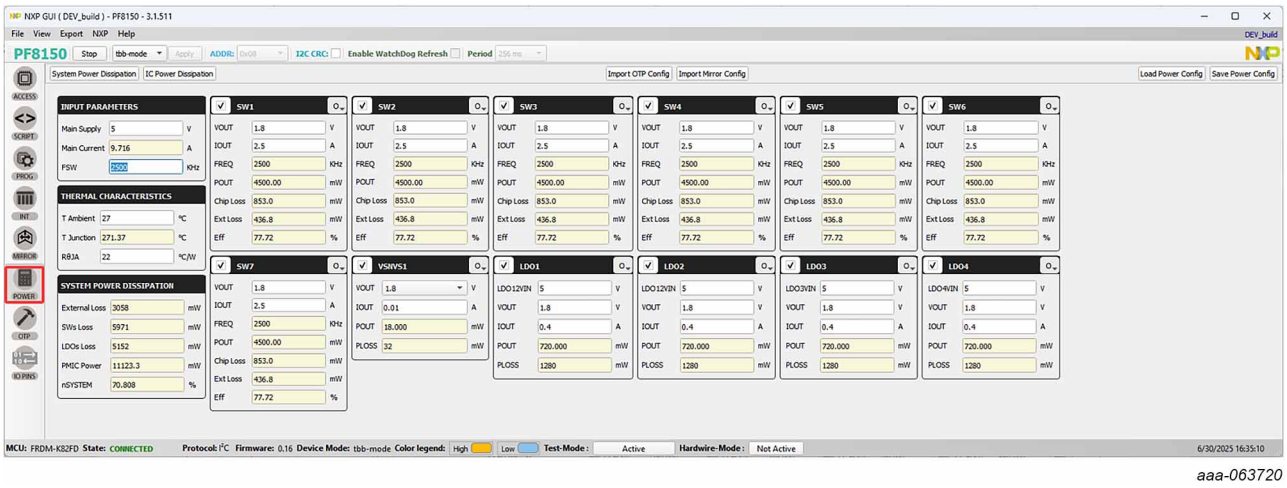
Figure 25. PMIC GUI user view

After starting the GUI, the Interface of PF8x00 is shown as above. It is divided in several parts:

- **Settings:** Import or export files, configure framework
- **Device Manager:** Start and stop communication, user mode and tbb mode switch, I^2C communication settings
- **Tool Access Bar:** Quick access to the PF8x00 evaluation tools and features
- **Window Log:** Microcontroller and device communication events
- **Tab Content:** Content of each tool or tab. There can be more tabs, boxes, or windows
- **Micro and Device Status:** Displays if USB or device is connected or disconnected, firmware and GUI version, and the device mode

7.2 Power tab

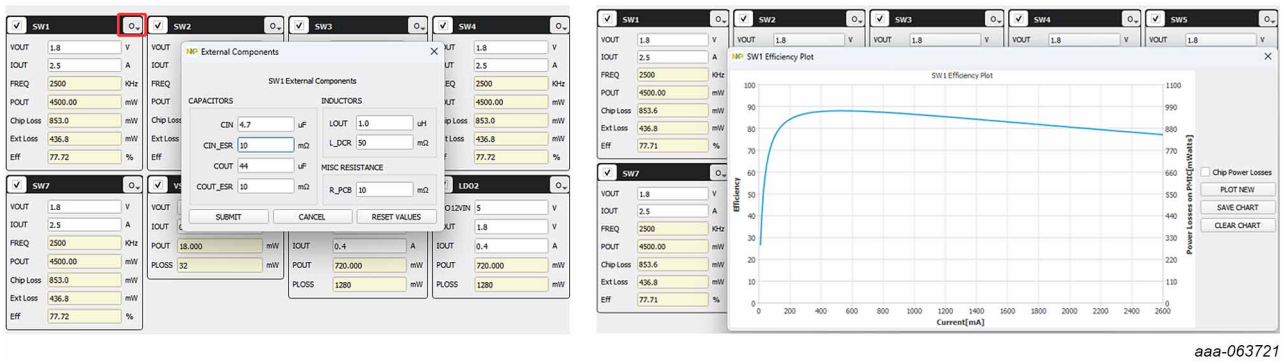
The POWER tool allows the calculation of PF8x00 power dissipation.



aaa-063720

Figure 26. Power tab

Customer can use Power tool to calculate the temperature raise and evaluate the power dissipations of device, to make sure the junction temperature can remain below TSD threshold. If the OTP config is ready, the tool can import the config first and adjust the work environment the customer uses. Include the input voltage, output current, and ambient temperature. For each channel, multiphase can be set in the operation button, and external components settings can be changed as well. For each channel BUCK, the PWM mode efficiency chart can be shown basing on the settings.

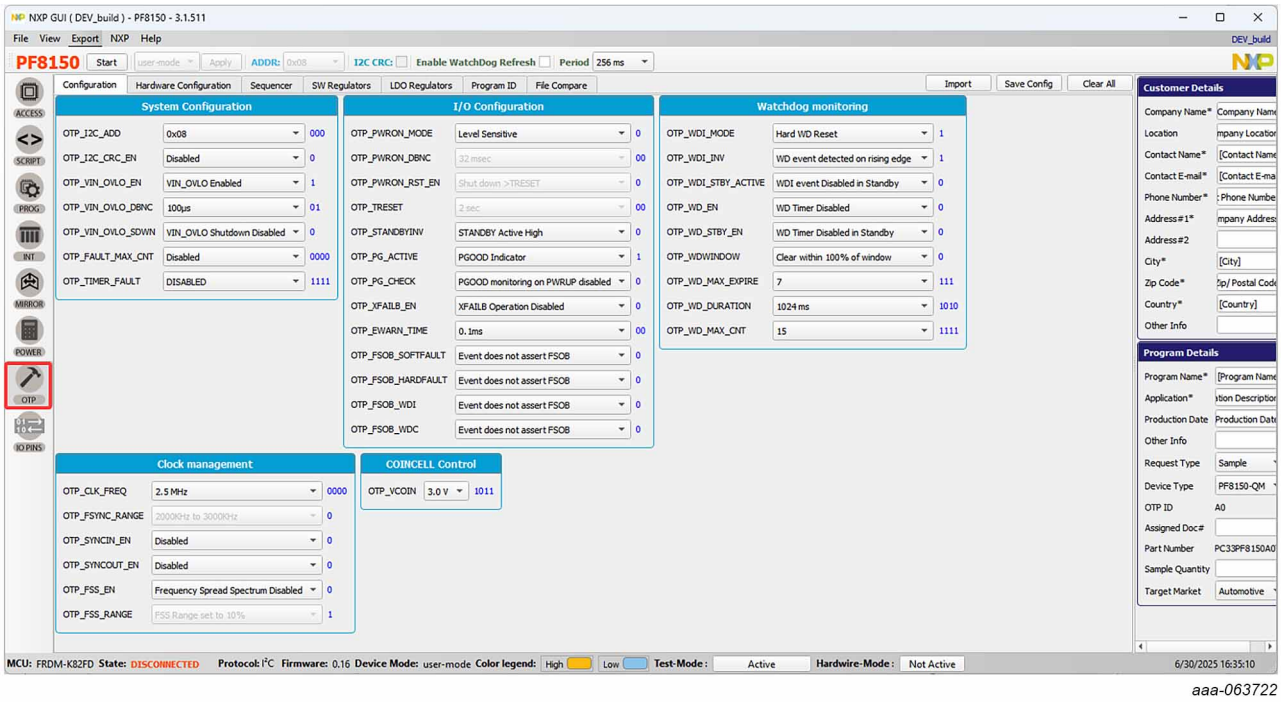


aaa-063721

Figure 27. Example of temperature raise and power dissipations evaluation

7.3 OTP tab

PMIC GUI provides one OTP tab which can be used to do the OTP configuration of device. The configuration files for PF8x00 and PF8x50 are compilable, it means that the OTP files of two family devices can be imported to each other OTP tabs. For example, if customer has configuration files of PF8100, and they want to create the same OTP configuration for PF8150, user can import the configuration files directly through the OTP tab In the GUI. The opposite is also true.



aaa-063722

Figure 28. OTP tab

If the user has no configuration file, the OTP tab is easily used to do the configuration, it has different blocks including: *Configuration, Hardware configuration, Sequencer, SW regulators and LDO regulators.* The configuration files can be saved in local when finished, and depending on the configuration. The user can export the TBB, OTP, and HEX files as needed.

7.4 Controlling the PF8150/PF8250 using GUI

The **Access Tab** and **INT Tab** are used to control the PMIC when device works in different modes.

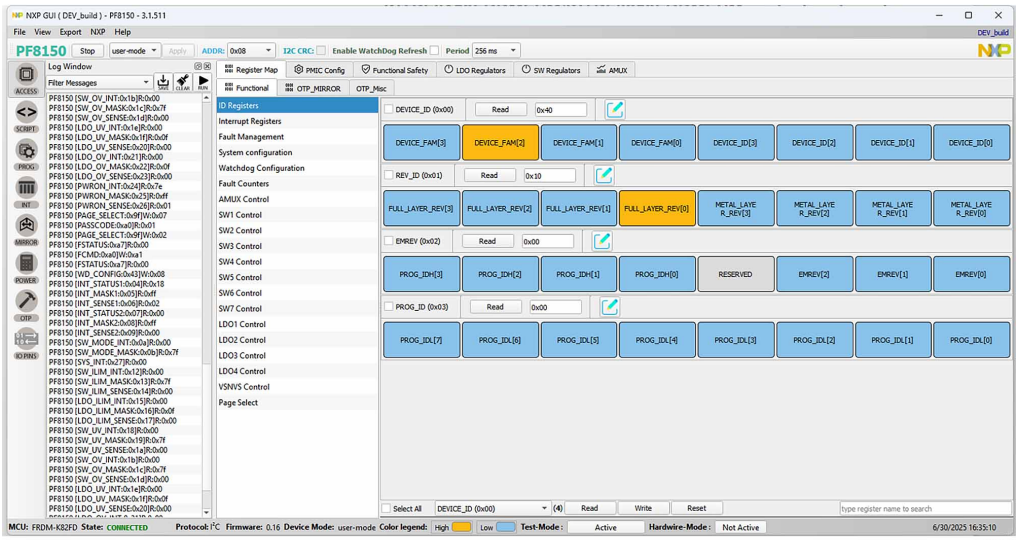


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Figure 29. Access tab and INT tab

In Access tab, there are 6 sections, which are used to do the controlling of the device, they include:

- Register map
- PMIC configuration
- Functional safety
- LDO regulators
- Switching regulators
- AMUX control

In addition, there is INT Tab, which can be used to read the status of the device.

7.4.1 Register map

The PF8150/PF8250 registers are organized in register pages or sectors. The GUI organizes the registers in various types and multiple register groups. See the *PF8150_PF8250 data sheet* for a more detailed view.

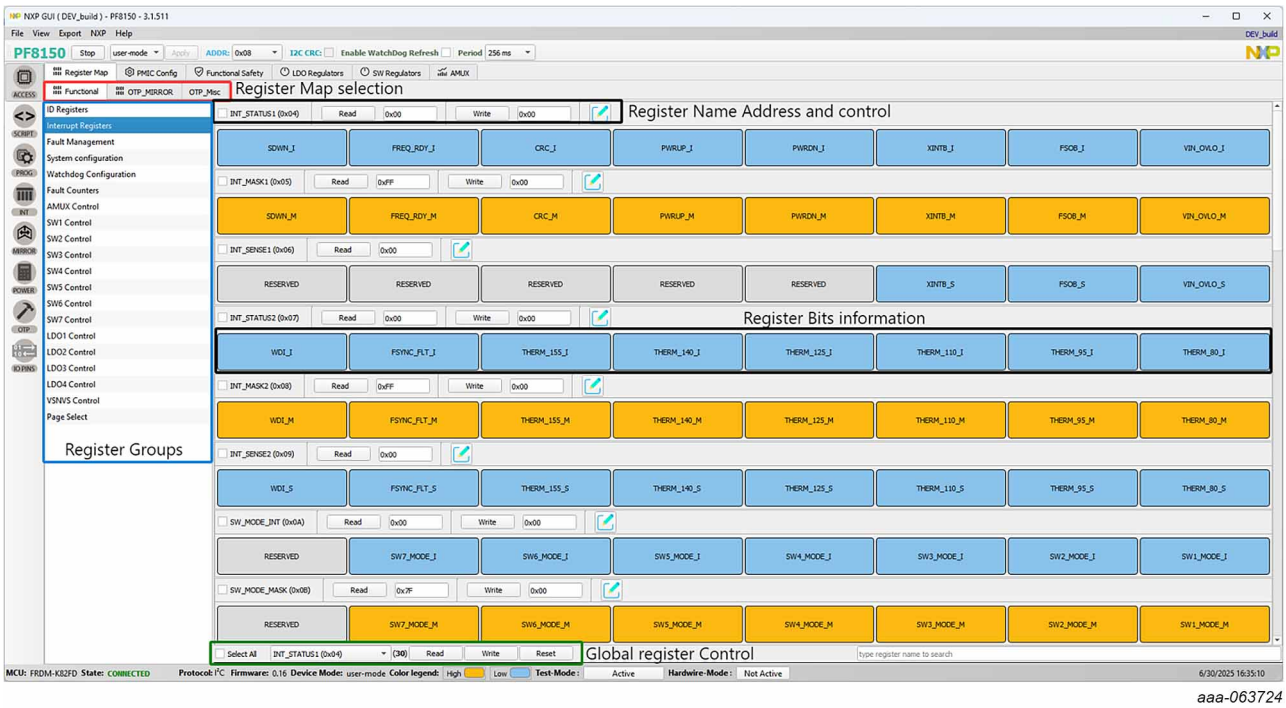


Figure 30. Register map

There are 3 register maps in this section.

- **Functional register map**: Functional register is used to do the PMIC operation in user mode.
- **OTP_Mirror register map**: OTP_Mirror register map is used to do the controlling in TBB mode.
- **OTP control register map**: OTP Control register map, the user will not use that.

Note: *Click the register map name to select the register map needed.*

Each register group contains all registers related to a specific channel or feature. Read/write registers provide independent lines to read and write the values on the selected registers.

Click **Read** to read Individual registers and click **Write** to write on the corresponding register. For each register bit, the yellow color means the value is 1 and the blue color means value is 0.

Use the global register controls to read, write, or reset multiple registers.

Click **Reset** to undo the changes on the write line and reset to the previous value. When using the global register controls, the selected command is performed on all registers with the checkbox selected. Only functional and OTP mirror registers are intended for user evaluation.

- **Functional registers**: provide access to the current configuration of the PMIC. Configuration can be changed and changes are applied once the command is sent.
- **OTP mirror registers**: provide access to the default configuration to be used at PWRON event. Access to these registers is only meant for debug or development purposes, therefore, these registers can only be read or modified when TBBEN is high. The TBBEN can be set as high externally via the J21 header or by the MCU via the script edit.

Click **R** to read Individual registers and click **W** to write on the corresponding register.

Use the global register controls to read, write, copy, or reset multiple registers.

Click **Copy** to copy the latest read value onto the write line.

7.4.2 PMIC configuration

The PMIC configuration tab provides access to the global configuration of the PMIC.

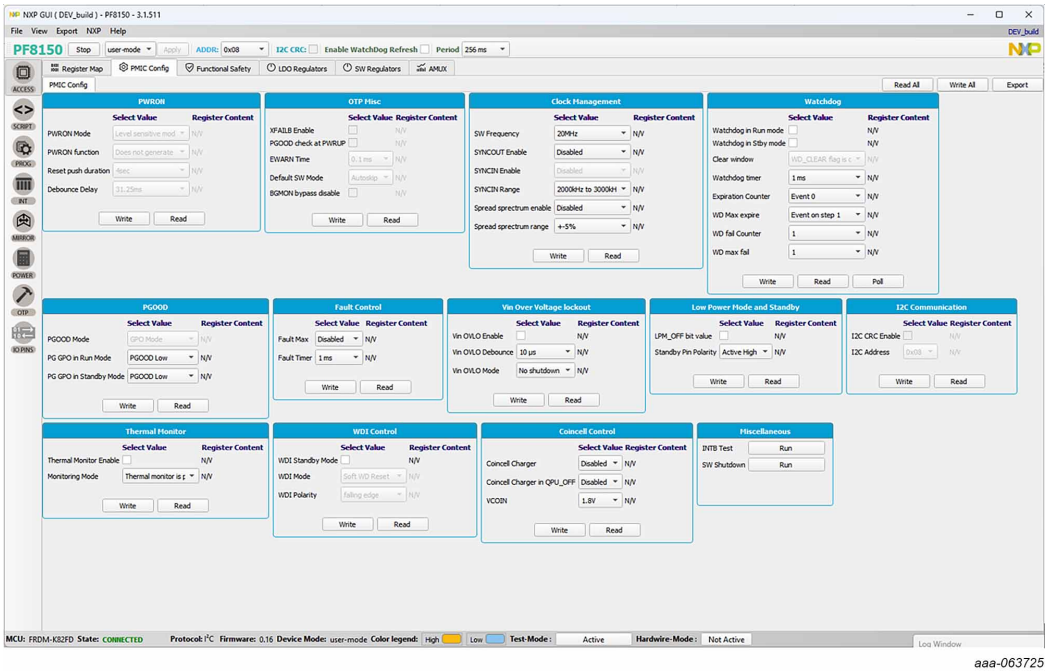


Figure 31. PMIC configuration

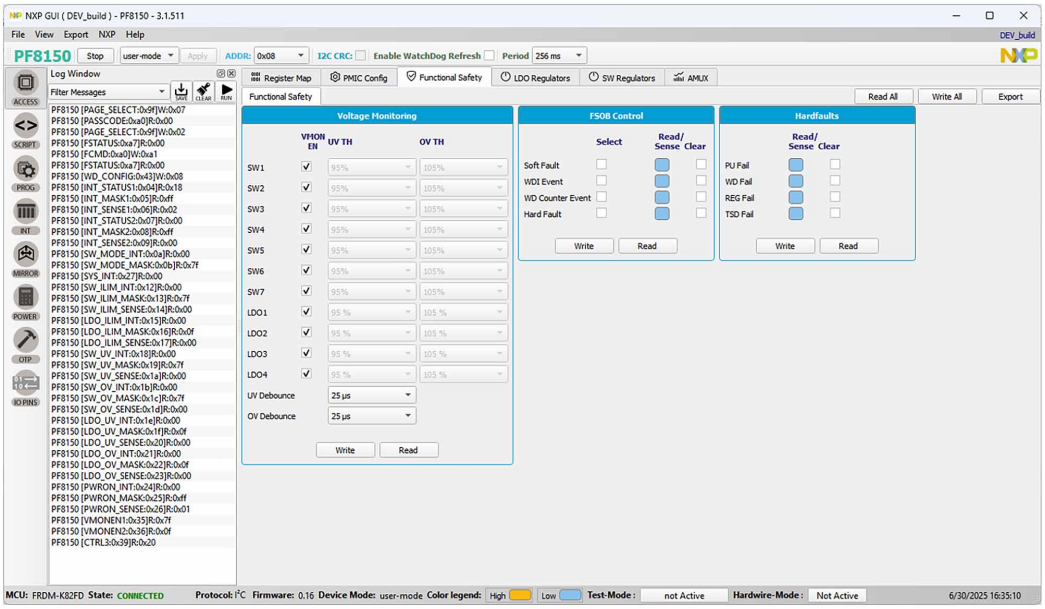
The functions that can be programmed in the PMIC configuration are listed below:

- PWRON: configuration and mode of operation of the PWRON pin
- PGOOD: configuration and control of the PGOOD pin
- STANDBY: configuration of the STANDBY pin
- WDI control: configuration of WDI pin and PMIC reaction when WDI pin toggles
- Coin cell control: configuration of coin cell voltage level and the coin cell charger
- Low power mode: configures the selection of the LP_OFF or QPU_OFF state when device is off
- Clock management: configuration of the clock frequency, spread spectrum, and frequency synchronization pins
- Fault control: configuration of the fault protection mechanisms
- VIN overvoltage lockout: configuration of the OVLO protection circuit
- Thermal monitor: configuration of the thermal monitor
- Watchdog: configuration and control of the internal Watchdog counter
- MCU watchdog management: provides parameters to allow the MCU to clear the internal PMIC watchdog
- I^2C communication: sets the I^2C address and enables the CRC check during I^2C communication (available in OTP only)
- OTP miscellaneous: sets default OTP configuration for various PMIC features

See the PF8150_PF8250 data sheet for a detailed description on the PMIC configuration.

7.4.3 Functional safety

The functional safety tab provides access to the fault monitoring circuits available on PF8150 and PF8250 as well as the functional safety features specific to the PF8250 device.



aaa-063726

Figure 32. Functional safety

Voltage monitoring: the user can perform the following actions using this control.

- Enable or disable the voltage monitor
- Select the OV and UV threshold (in OTP only)
- Select the OV and UV detection debounce
- Monitor/clear the ABIST flags in case of failure

FSOB control: use this control to select the FSOB mode and select/monitor the FSOB reaction on any of the following faults.

- Soft fault
- WDI event
- WD counter event
- Hard fault

Hard faults: use this control to monitor the source for the hard fault causing a power down event.

- Power up fail
- Watchdog fail
- Regulator fail
- Thermal shutdown

Fail-safe controls: use this control to perform the following actions (available only in PF8250 device).

- Disable the fail-safe state
- Set the maximum number of failures before entering the fail-safe state
- Read the real time fail-safe counter
- Set the fail-safe clear timer

7.4.4 LDO regulators

The LDO tab is used to configure and control the LDO regulators.

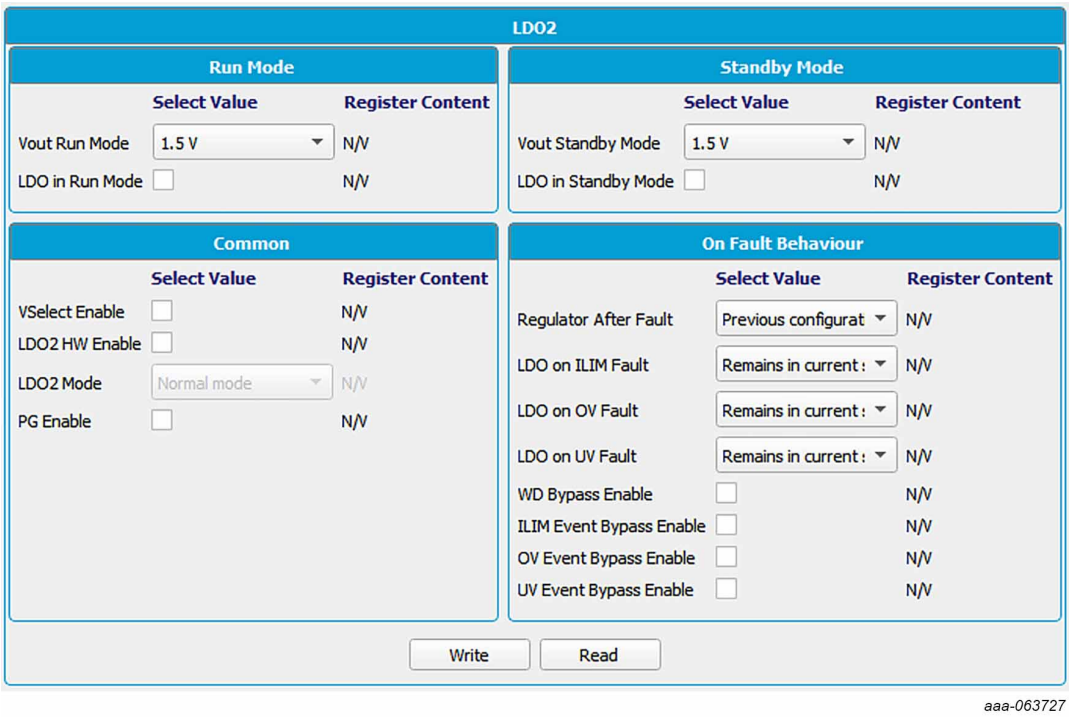


Figure 33. LDO control

Each LDO can change the following features:

- The output voltage in Run and Standby state
- LDO status in Run and Standby state
- LDO operating mode (OTP only)
- Set the reaction of the LDO output on an OV, UV, or ILIM event
- Bypass OV, UV, or ILIM events
- Bypass reaction during a soft watchdog event
- Enable the LDO to assert he PGOOD pin on an OV or UV fault
- Enable or disable the voltage monitor

In addition, the LDO2 can set the output to be enabled and modified via the LDO2EN and the VSELECT pin.

VSNVS can be disabled or changed to a different voltage during the system-on states.

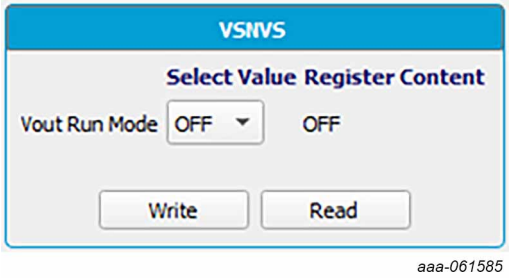


Figure 34. VSNVS control

7.4.5 Switching regulators

The SW regulator tab provides access to all features for each of the switching regulators.

SW1 to SW6 are valley current mode controlled buck regulators configurable as single, dual, triple, and quad phase regulators as described in the PF8150_PF8250 data sheet.

All regulators capable of multiphase operation share the same feature set as shown in Figure 35.

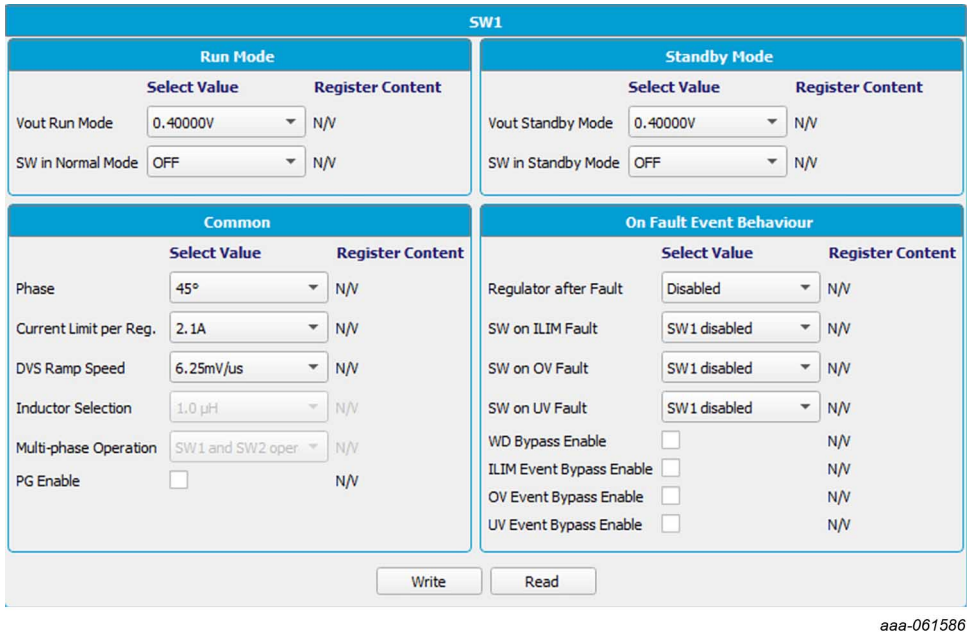


Figure 35. Type 1 buck regulators

SW7 is a peak current mode controlled buck regulator operating in single phase only, which provides higher output voltage settings typically used for 3.3 V I/O supply.

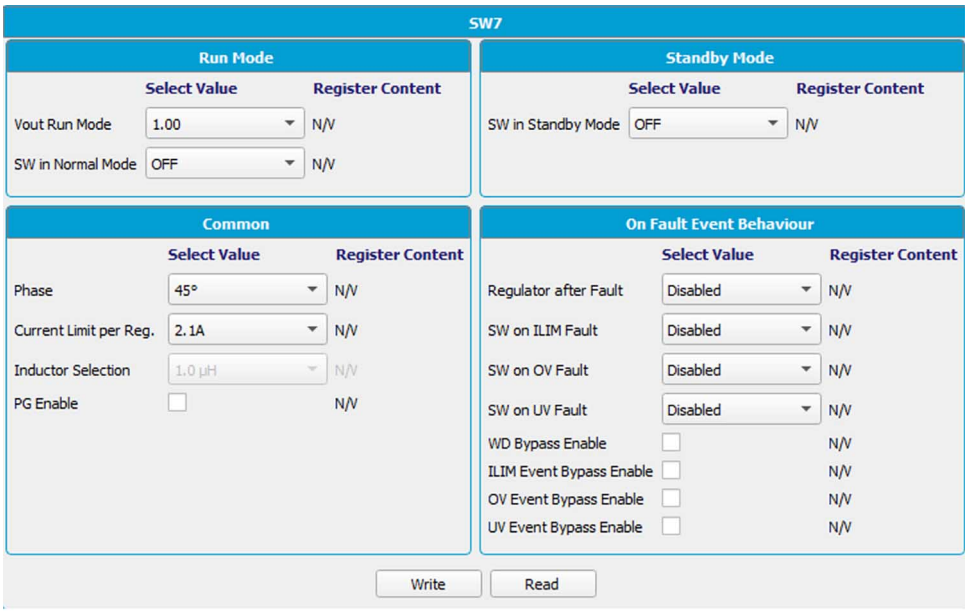


Figure 36. Type 2 buck regulator

SW regulators can modify the following properties:

- Mode of operation in Run state
- Mode of operation in Standby state
- Output voltage in Run state
- Output voltage in Standby state
- The phase of its switching frequency
- Current limit
- DVS ramp rate
- SW6 can additionally be set in VTT mode to follow the voltage on SW5

7.4.6 AMUX control

The AMUX control tab provides the ability to automate the AMUX channel selection to display the reading of the selected channels through a polling cycle.

Click read to show the information of the device, which can be monitored by AMUX, in the summary section.

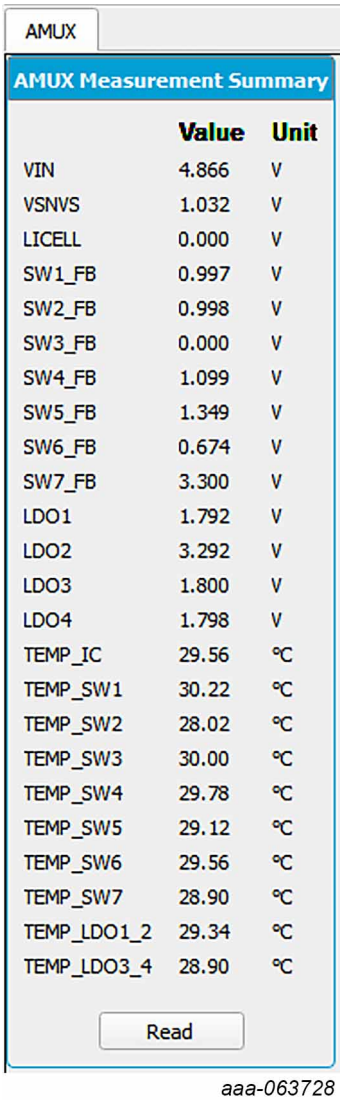


Figure 37. Example of AMUX summary section

There are two measurement areas for polling cycle, one for voltage measurement and another for temperature measurement. The GUI automatically displays the calculated value to show the real value after applying conversion and scaling factors to eliminate the need for manual calculation using the raw voltage at the AMUX pin.

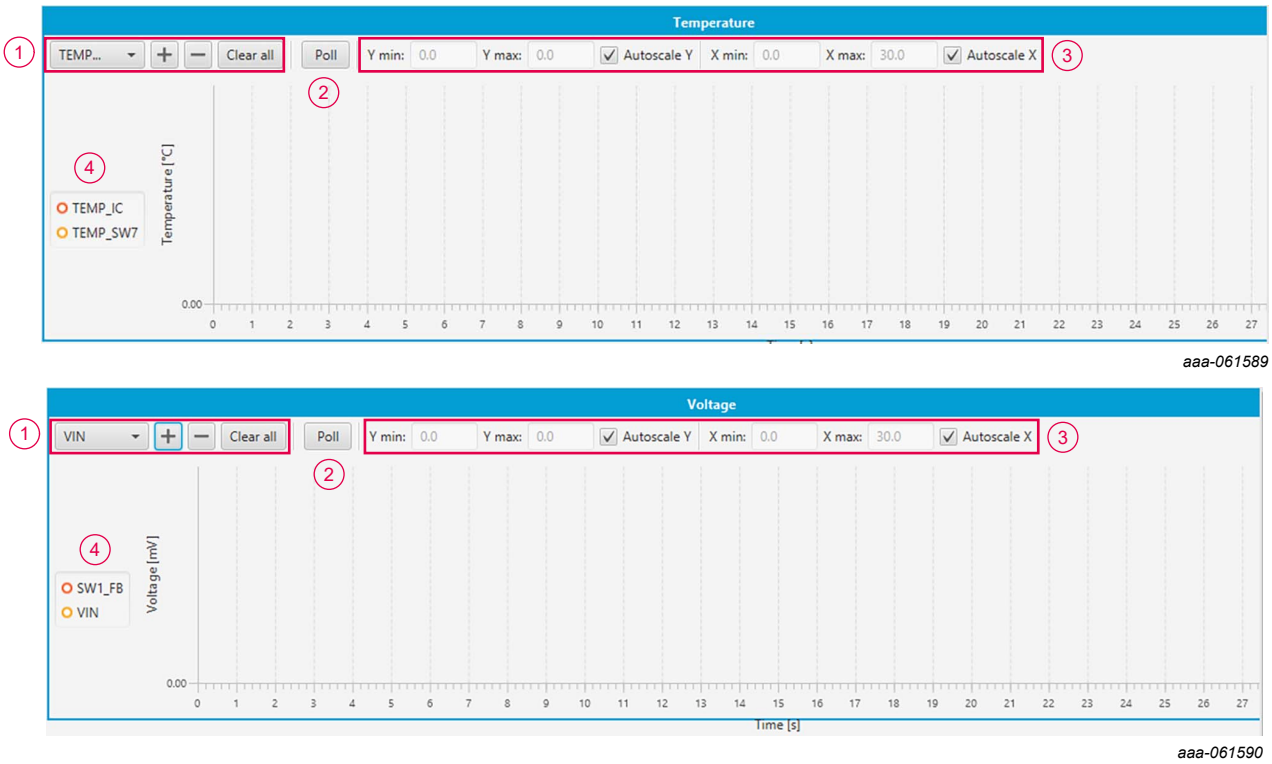


Figure 38. AMUX control

1. **AMUX channel selection:**
   - Use the drop-down list to select the channel to be added to the AMUX polling cycle.
   - Use **+** and **-** to add or remove signal from the polling list.
   - Use **Clear All** to remove all signals from the polling list.
2. **Start polling:**
   - Use **Poll** to start the polling cycle to read the AMUX channels selected in the polling list.
3. **Display scaling:**
   - Use the scaling controls to change the display scale for the AMUX measurements.
4. **Polling list:**
   - The selected channels added to this list will be added to the polling cycle in order to provide real time data for all the channels in the list.

7.4.7 Interrupt tab

The interrupt tab provides access to all the interrupts, mask, and status registers in the PF8150/PF8250.

One system interrupt register is provided to work as first level detection of a physical interrupt. The system interrupt flags are asserted only when one or more unmasked interrupts are detected in any of the second level interrupts registers and driving the INTB pin low. Interrupt events that are masked are not notified in the system interrupt register.

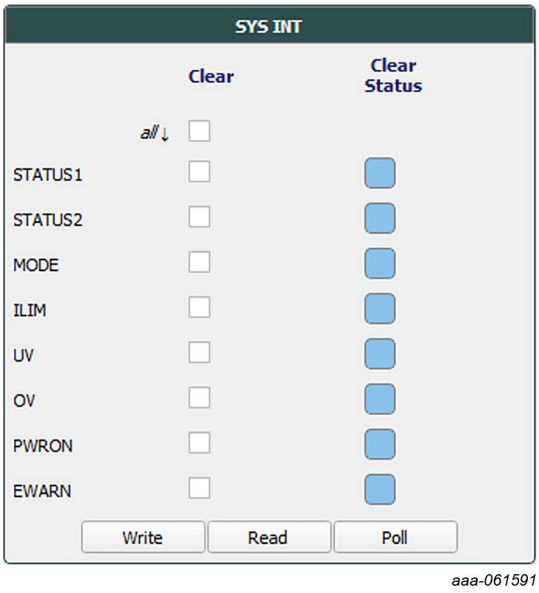


Figure 39. System interrupts

At a second level, the specific interrupt flags are organized in ten registers; allowing the system to identify the source of an interrupt in a maximum of three I^2C transactions.

Each interrupt event provides 3 bits to allow a flexible interrupt management scheme:

- Status bits: a red box indicates that an event on the corresponding function has occurred. Setting the clear box and writing to the registers will write a 1 to the corresponding latch, causing the interrupt latch to be cleared.
- Mask bits: checking the mask bit prevents the INTB pin to be asserted when the respective event is present.
- Sense bits: when the sense bit is green, the corresponding sense signal is low. When it is red, the corresponding sense signal is high.

Four global interrupt registers are provided to notify global system events such as thermal interrupts, I/O events, global fault events, switching regulator mode transitions, etc.

Figure 40. Global interrupts

Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the switching regulators.

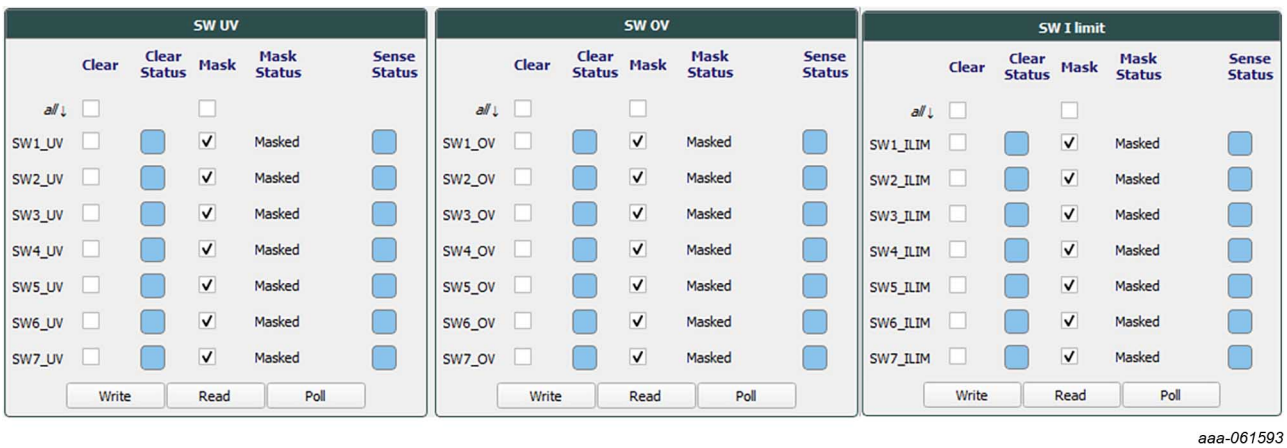


Figure 41. Switching regulator interrupts

Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the LDO regulators.

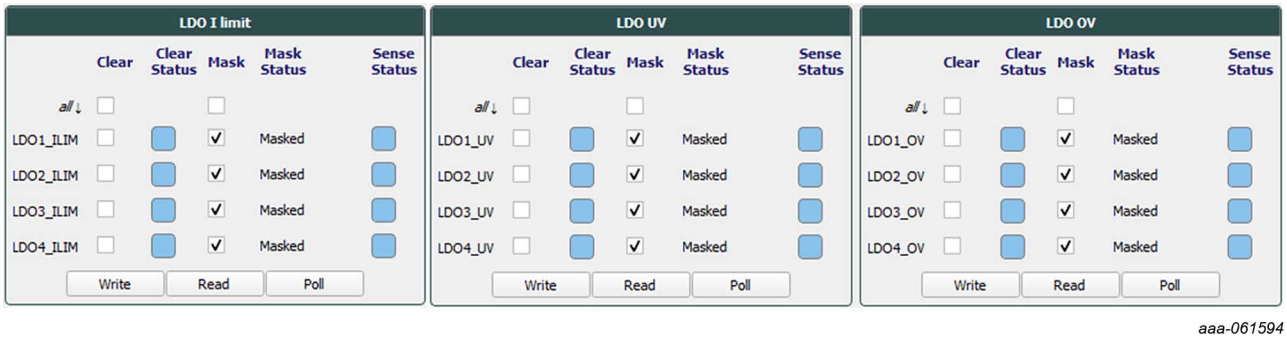


Figure 42. LDO regulator interrupts

See the PF8150_PF8250 data sheet for more details on the specific conditions that may cause any of the interrupt events.

7.5 Working with the Script tab

The script editor is a tool that enables sequential execution of commands, which can access registers, digital and analog pins of a device. The graphical interface facilitates creation and working with commands.

7.5.1 Script editor environment

The graphical interface resides in the Script editor tab, see Figure 43. It consists of three main parts: command generation, script area, and script log.

The command generation pane assists the user in the creation of script commands. The script area contains a list of commands to be executed, one command per line. The user can write commands manually or use the command generation pane. Format of commands is described in Section 7.5.2. Lastly, the script log shows the results of the script processing. A line in this pane corresponds to the same line in the script control panel.

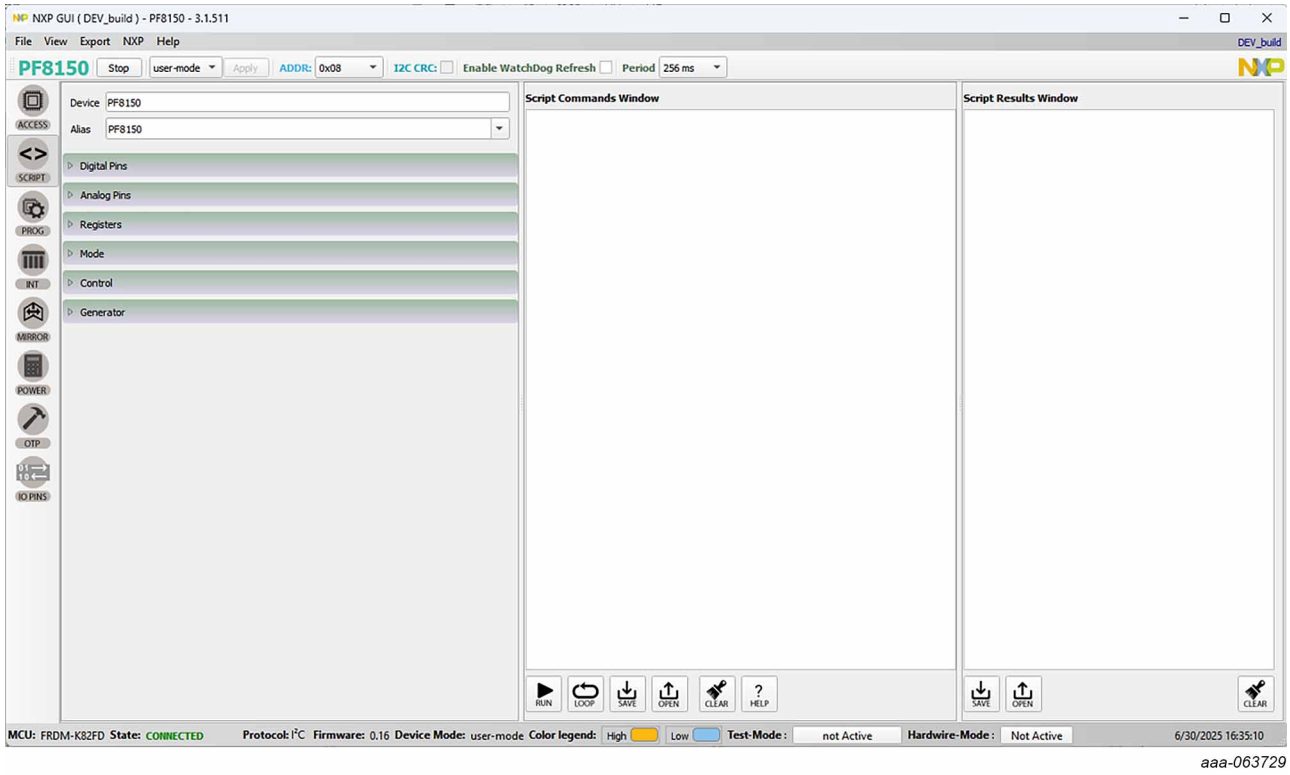


Figure 43. Script editor environment

The following steps describe how to create and execute a simple script:

1. The GUI must be connected to the device.
2. The GUI loads the appropriate values to generate the script commands (that is, register names, pin names).
3. Create commands to be executed. The user can write the command manually or utilize the command generation pane which offers valid options.
   - To automatically generate a command, select the command attributes and the tool inserts a new line into the script control pane. The write register command requires the register value in hexadecimal value (0x prefix, for example, 0x12).
   - I/O control commands can be used to set pin high or low to generate specific events.
4. Click **Run** to execute commands. To process the script in a loop, set *Run in loop option* in the script control pane and then run the script. In this case, the script is processed until the user clicks Stop.
5. The script log provides a summary of all the command executed in the script. Note that results are cleared when another processing begins.

The user can save or load scripts in .txt format. The execution result can also be saved or loaded from a file.

The Export button can be used to export all the SET commands in a simple hex format:

```
<register address>, <register value to be written>,
```

Use the script generation option to create the following commands:

- Read the status of a digital pin
- Set a digital pin high or low
- Select the analog channel to read at the AMUX
- Write a register
- Read a register
- Change the operating mode
- Generate a TBB or OTP script with the data configured in the device control tabs

7.5.2 Definition of commands

This section describes commands supported by the script editor and their format. All commands are listed in Table 8.

Table 8. Script editor commands

Command name	Description
SET_REG	Sets value of a selected register
READ_REG	Reads value of a selected register
SET_DPIN	Sets value of a selected digital pin
GET_DPIN	Gets value of a selected digital pin
GET_APIN	Gets value of a selected analog pin. Returned value is in mV.
PAUSE	Shows a dialog with a user defined message. The script execution is paused until the user confirms the dialog.
SET_MODE	Sets the mode of operation

7.5.3 Format of commands

General format of script editor command is as follows:

```
<command name>:<list of parameters separated by a colon>
```

Table 9 shows parameters of script editor commands. All parameters are mandatory.

Table 9. Parameters of script editor commands

Command name	1. item	2. item	3. item	4. item
SET_REG	Device	Reg. set	Reg. name	Reg. value
GET_REG	Device	Reg. set	Reg. name	–
SET_DPIN	Device	Pin name	Pin value	–
GET_DPIN	Device	Pin name	–	–
GET_APIN	Device	Pin name	–	–
SET_MODE	Device	Mode of operation	–	–
PAUSE	Message	–	–	–

Table 10. Items definitions

Device	Device name/command ID
Reg. set	Register set name. Register set enables association of registers having similar function.
Reg. name	Register name as defined in a data sheet
Reg. address	Register address in the decimal or hexadecimal (with 0x prefix) format
Reg. value	Register value in the decimal or hexadecimal (with 0x prefix) format
Pin name	Name of a digital or analog pin as defined in a device data sheet
Pin value	Value of digital pin. Allowed strings are low and high.
Mode of operation	TBB mode, Normal mode, User mode
Message	A message to be displayed in a dialog. It cannot contain the colon character, which is used as a delimiter of parameters.

8 References

[1] **KITPF8150FRDMEVM/KITPF8250FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools https://www.nxp.com/KITPF8X50FRDMEVM

[2] **PF8150/PF8250** — product information on multi-channel power management integrated circuit https://www.nxp.com/products/PF81-PF82

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10 Revision history

Revision history

Document ID	Release date	Description
UM12404 v.1.0	19 November 2025	Initial public version

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