UM11887

FRDMGD3162RPEVM half-bridge evaluation board

Rev. 2 — 8 May 2024 User manual

Document information

Information	Content
Keywords	gate driver, half-bridge, RoadPak, GD3162
Abstract	This document describes key features and usage requirements for performing evaluation of GD3162 gate driver with FRDMGD3162RPEVM.

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit or reference design is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY.

It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit or reference design may be used with any development system or other source of I/O signals by connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. To minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 FRDMGD3162RPEVM

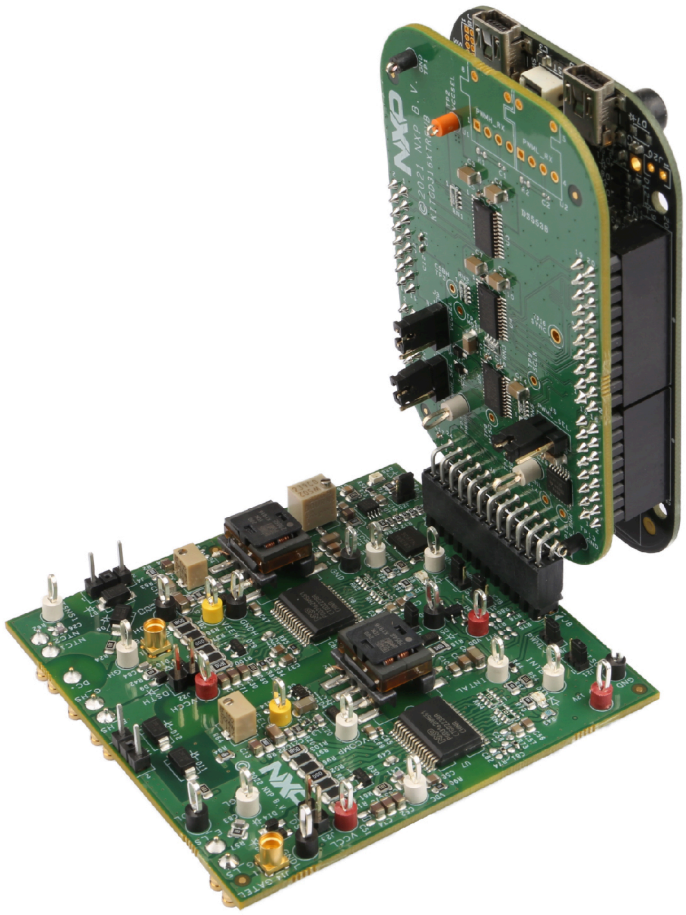

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Figure 1. FRDMGD3162RPEVM

3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDMGD3162RPEVM is at http://www.nxp.com/FRDMGD3162RPEVM. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDMGD3162RPEVM.

1. Go to http://www.nxp.com/FRDMGD3162RPEVM.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link, review each entry, and download an entry by clicking the title.
4. After reviewing the **Overview** tab, visit the other product-related tabs for additional information:
   - **Documentation**: download current documentation
   - **Software & Tools**: download current hardware and software tools
   - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The FRDMGD3162RPEVM kit contents include:

- Assembled and tested FRDMGD3162RPEVM board in an antistatic bag
- 3.3 V to 5.0 V translator board (KITGD316xTREVB) connected to FRDM-KL25Z MCU board
- USB cable, type A male/type mini B male, 3 ft
- Quick start guide

3.2 Required equipment

To use this kit, you need:

- Compatible SiC RoadPak module
- DC link capacitor compatible with the SiC RoadPak module
- 1.27 mm jumpers for configuration (included with kit)
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 20 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, AC current probe (smaller diameter)
- Isolated high-voltage probes
- Digital voltmeter

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 10 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD3162RPEVM is a half-bridge evaluation kit populated with two GD3162 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with FlexGUI 2 for GD3162 software for communication to the serial peripheral interface (SPI) registers on the GD3162 gate drive devices in either daisy chain or standalone configuration.

The KITGD316xTREVB translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and GD3162 gate drivers. The evaluation kit can be connected to a compatible insulated gate bipolar transistor (IGBT) or SiC metal-oxide-semiconductor field-effect transistor (MOSFET) module for half-bridge evaluations and applications development.

4.2 Board features

- Capability to connect to Hitachi RoadPak module for half-bridge evaluations
- Adjustable negative VEE gate low drive level (–1.5 V to –7.5 V DC)
- Adjustable VCC gate high drive level (10 V to 25 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access to power, ground, and signal test points
- Easy to install and use FlexGUI 2 for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Negative temperature coefficient (NTC) connection and configurable for monitoring module temperature

4.3 Device features

Table 1. Device features

Device	Description	Features
GD3162	The GD3162 is an advanced single channel gate driver for IGBT and SiC power devices.	• Compatible with current sense and temp sense IGBT and SiC MOSFET modules • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBT and SiC MOSFET with current sense feedback • Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation up to 8 kV • Integrated boost capability for increased drive strength • Interrupt pins for fast response to faults and real-time reporting capability • Compatible with negative gate supply • Active bus discharge functionality

4.4 Board description

The FRDMGD3162RPEVM is a half-bridge evaluation board populated with two GD3162 single channel IGBT or SiC MOSFET gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3162 shutdown protection capabilities.

The evaluation board is designed to connect to a RoadPak SiC MOSFET for evaluation of the GD3162 performance and capabilities.

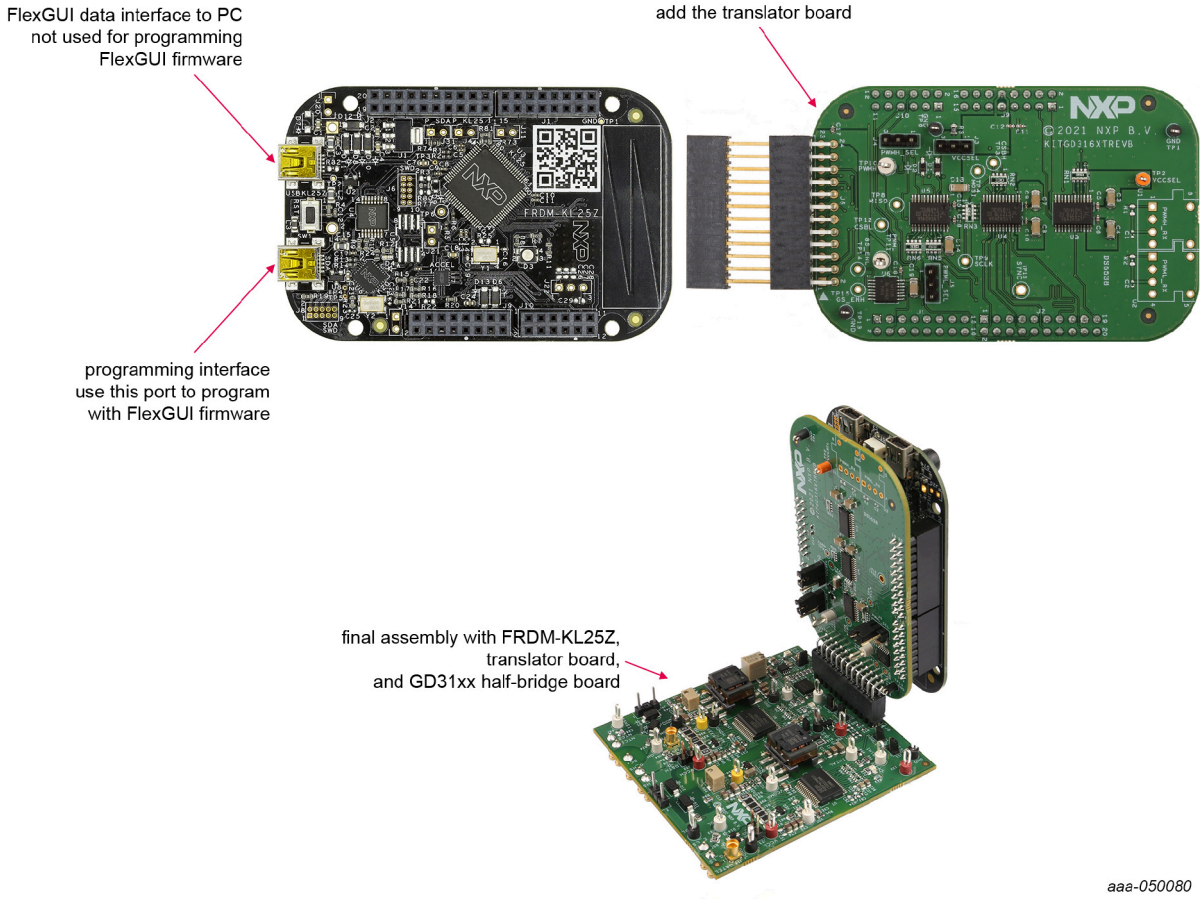


Figure 2. Connecting FRDM-KL25Z, GD31xx half-bridge EVB and translator board

4.4.1 Low-voltage logic and control connector

Low-voltage domain requires an externally supplied 12 V VSUP, which supplies an onboard flyback supply for high-side driver and low-side driver domain VCC/VEE and an onboard regulator for low-voltage domain 5 V VDD. The low-voltage domain interfaces with the MCU and GD3162 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to RoadPak module single phase connections and test points.

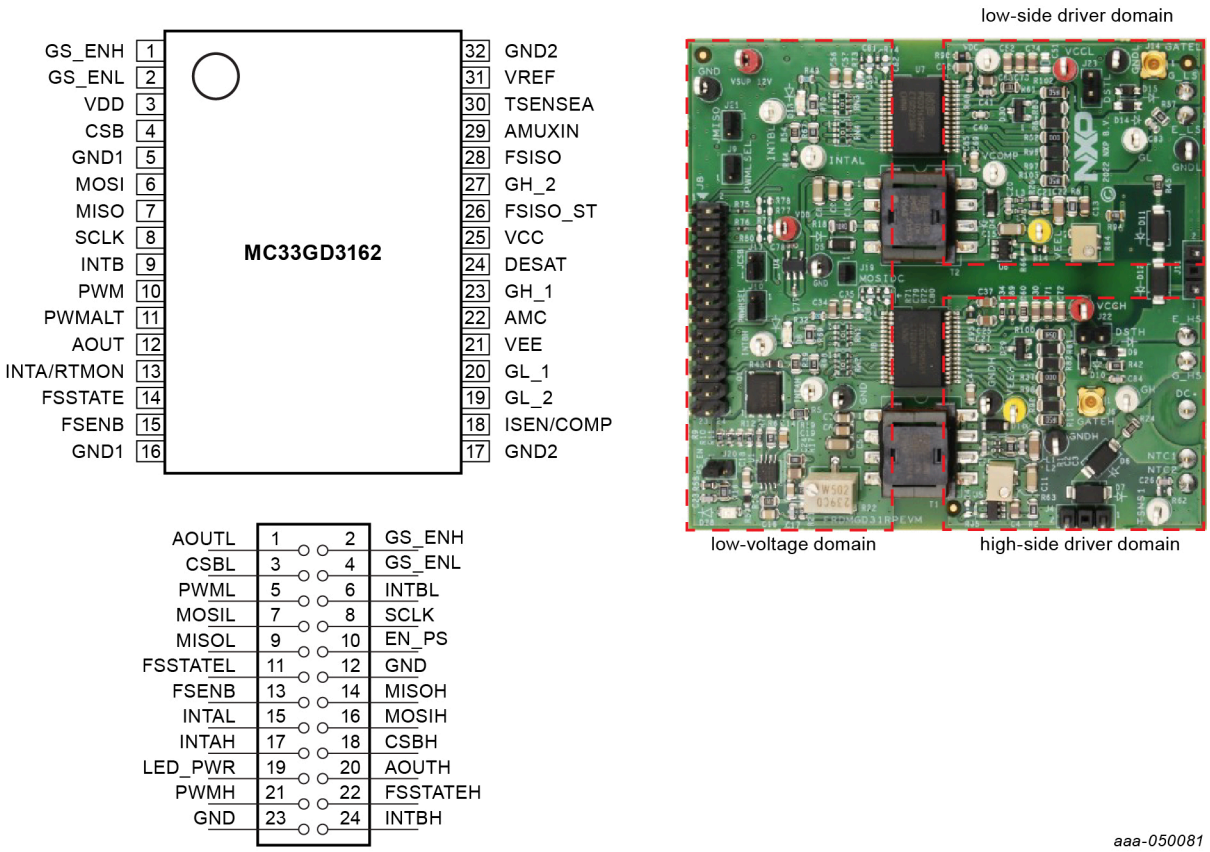


Figure 3. Evaluation board voltage and interface domains

Table 2. Low-voltage domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or voltage via AMUXIN
2	GS_ENH	gate strength enable HIGH; gate drive pull-up strength control logic
3	CSBL	chip select bar (low side)
4	GS_ENL	gate strength enable LOW; gate drive pull-down strength control logic
5	PWML	pulse width modulation (PWM) input (low side)
6	INTBL	interrupt bar (low side)
7	MOSIL	master out slave in (low side)
8	SCLK	serial clock input
9	MISOL	master in slave out (low side)
10	EN_PS	MCU control of flyback power supply
11	FSSTATEL	fail-safe state (low side)
12	GND	ground
13	FSENB	fail-safe enable (high side and low side)

Table 2. Low-voltage domain 24-pin connector definitions...*continued*

Pin	Name	Function
14	MISOH	master in slave out (high side)
15	INTAL	fault reporting and real time V_{CE} and VGE monitoring (low side)
16	MOSIH	master out slave in (high side)
17	INTAH	fault reporting and real time V_{CE} and VGE monitoring (high side)
18	CSBH	chip select bar (high side)
19	LED_PWR	USB 3.3 V power for INTB LEDs (high side and low side)
20	AOUTH	duty cycle encoded signal (high side)
21	PWMH	PWM input (high side)
22	FSSTATEH	fail-safe state (high side)
23	GND	ground
24	INTBH	interrupt bar (high side)

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

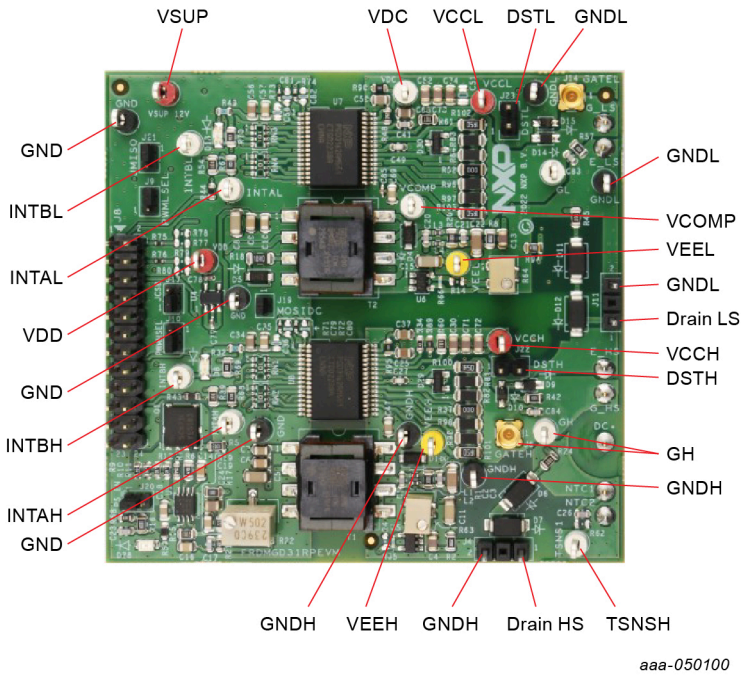


Figure 4. Key test point locations

Table 3. Test point definitions

Test point	Definition
Low-voltage domain	
VSUP	DC Voltage source connection point for low-voltage domain to 5 V low dropout (LDO) regulator. Externally supplied 12 V DC supply voltage.
VDD	Test point for 5 V LDO regulator output. Supply voltage for VDD inputs and LED indicator pull-up.
GND	grounding points for low-voltage domain
INTAH	fault monitor and VCE/VGE real-time report monitor high-side test point
INTBL	interrupt bar low-side test point
INTAL	fault monitor and VCE/VGE real-time report monitor low-side test point
INTBH	interrupt bar high-side test point
Low-side driver domain	
GNDL	low-side domain ground point
VCCL	positive voltage supply flyback output test point for isolated circuitry and low-side driver domain
Drain LS	low-side SiC MOSFET drain connection
VCOMP	Test point for analog comparator input ISEN/COMP pin. Refer to the data sheet for details on this pin.
GL	module gate test point on low-side driver domain, which is the charging pin of the gate; including MMCX probe connection
DSTL	V_{CE} desaturation test point connected to low-side driver DESAT pin and circuitry
VEEL	negative voltage supply flyback output test point for low-side driver gate of IGBT or SiC module
VDC	DC link voltage test point at voltage divider and input to AMUXIN pin on low side
High-side driver domain	
VCCH	positive voltage supply flyback output test point for isolated circuitry and high-side driver domain
GNDH	high-side domain ground point
Drain HS	high-side SiC MOSFET drain connection
TSNSH	temperature sense connection high-side test point
GH	module gate test point on high-side driver domain, which is the charging pin of the gate; including MMCX probe connection
DSTH	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
VEEH	negative voltage supply flyback output test point for high-side driver gate of IGBT or SiC module

4.4.3 Power supply and jumper configuration

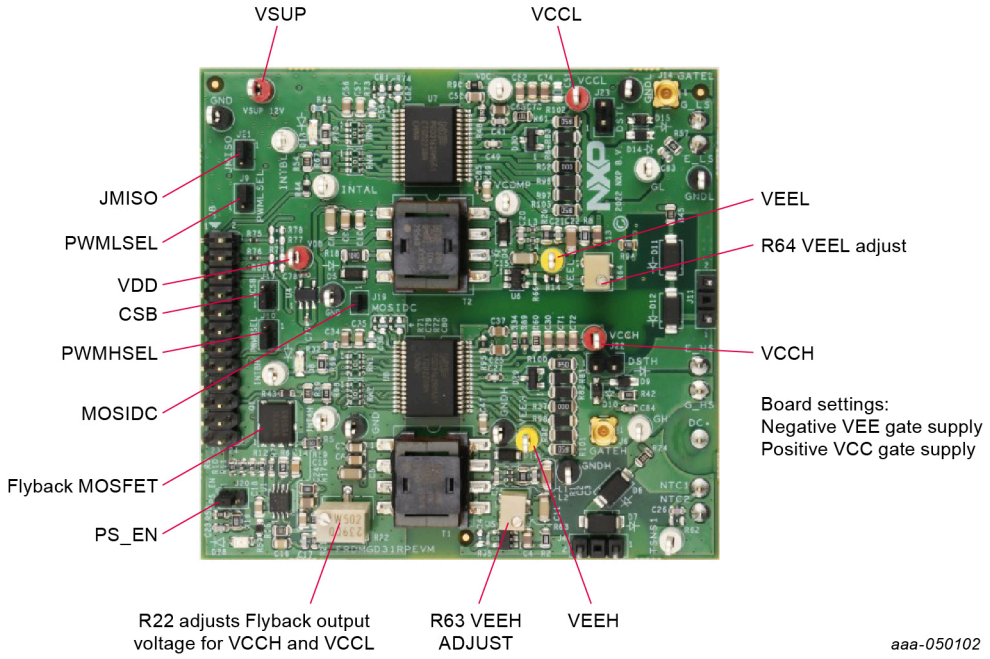


Figure 5. Power supply and jumper configuration

Table 4. Jumper definitions

Jumper	Position	Function
PWMHSEL (J10)	1-2	dead time fault protection enabled (high side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
PWMLSEL (J9)	1-2	dead time fault protection enabled (low side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
CSB (J17)	1-2	chip select for normal operation
	2-3	chip select for daisy chain operation
MOSIDC (J19)	closed	normal operation
	open	daisy chain operation
MISO (J21)	1-2	normal operation
	2-3	daisy chain operation
PS_EN (J6)	1-2	MCU control of flyback supply enable
	2-3	flyback supply enable tied to VSUP
R63	adjust resistor	VEEH negative supply voltage for high side VEE
R64	adjust resistor	VEEL negative supply voltage for low side VEE
R22	adjust resistor	VCCH (high side) and VCCL (low side) positive supply voltage

4.4.4 Bottom view

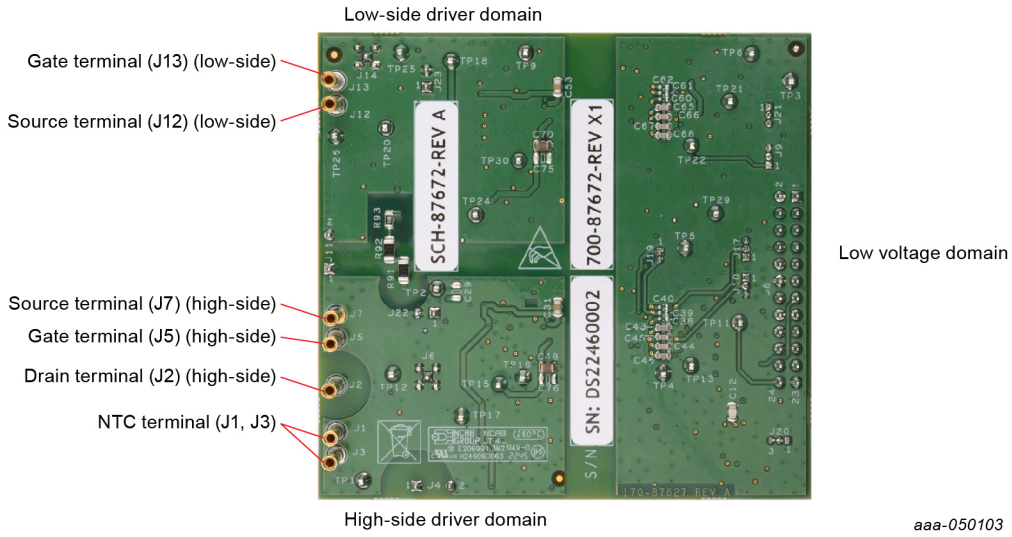


Figure 6. Evaluation board bottom view

4.4.5 Gate drive resistors

- RGH_1 – gate high resistor in series with the GH_1 pin at the output of the GD3162 gate high driver and RoadPak module gate that controls the strong turn-on current for SiC MOSFET gate.
- RGH_2 – gate high resistor in series with the GH_2 pin at the output of the GD3162 gate high driver and RoadPak module gate that controls the weak turn-on current for SiC MOSFET gate.
- RGL_1 – gate low resistor in series with the GL_1 pin at the output of the GD3162 gate low driver and RoadPak module gate that controls the strong turn-off current for SiC MOSFET gate.
- RGL_2 – gate low resistor in series with the GL_2 pin at the output of the GD3162 gate low driver and RoadPak module gate that controls the weak turn-off current for SiC MOSFET gate.
- RAMC – series resistor between RoadPak module gate and active Miller clamp (AMC) input pin of the GD3162 driver for gate sensing and active Miller clamping.

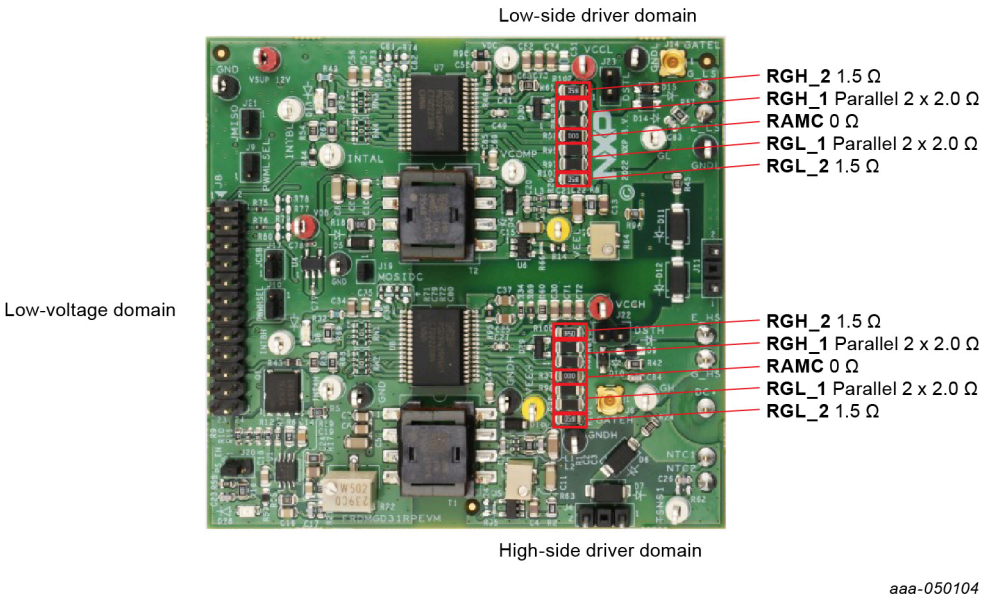


Figure 7. Gate drive resistors

4.4.6 LED interrupt indicators

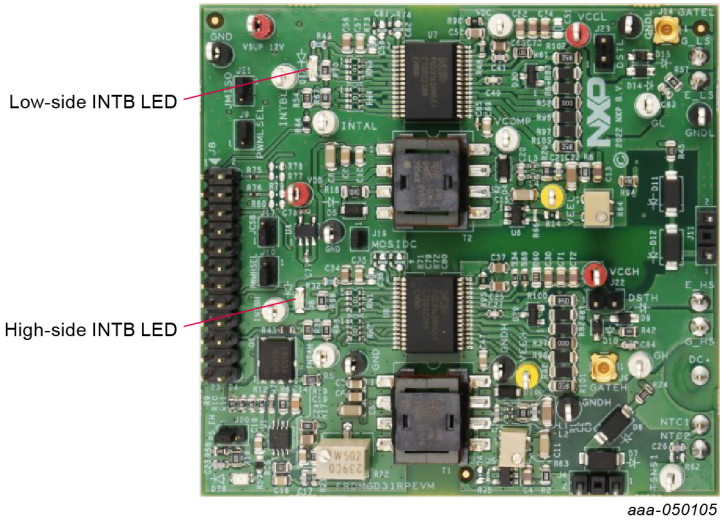


Figure 8. LED interrupt indicators

Table 5. LED interrupt indicators

LED	Description
Low-side INTB	connected to the INTB output pin of low-side driver indicating reported fault status when on (active LOW)
High-side INTB	connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active LOW)

4.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

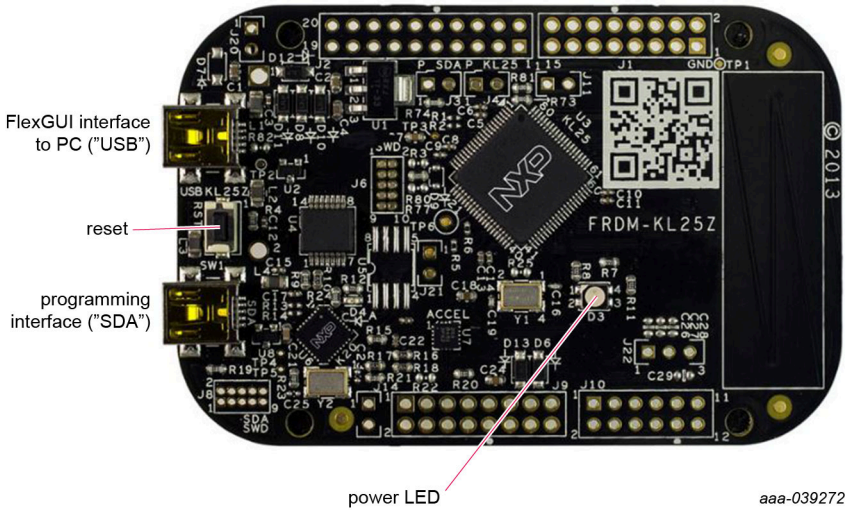


Figure 9. Freedom development platform

4.6 3.3 V to 5.0 V translator board

KITGD316xTREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

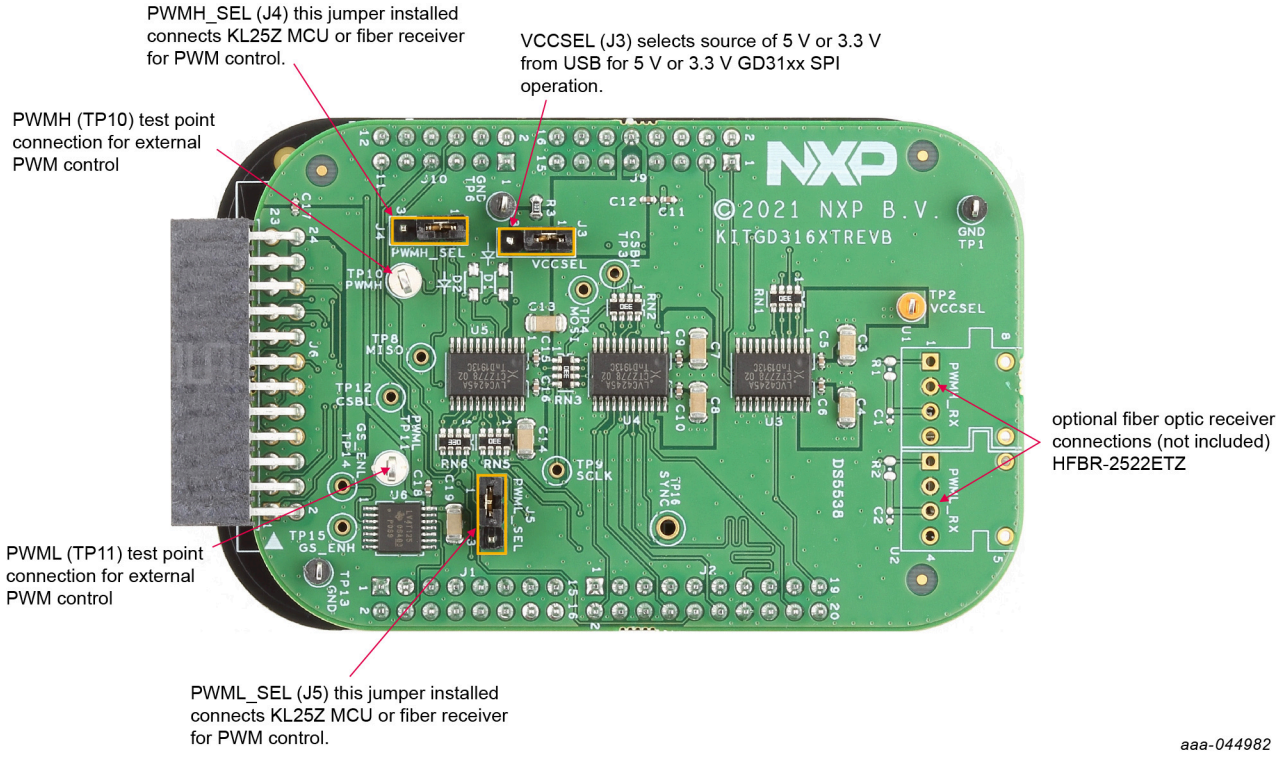


Figure 10. Translator board

Table 6. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

5 Configuring the hardware

FRDMGD3162RPEVM is connected to compatible SiC MOSFET RoadPak module with a DC link capacitor as shown in Figure 11. Double pulse and short-circuit testing can be conducted utilizing a Windows based PC with FlexGUI 2 software.

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor compatible with RoadPak module
- SiC MOSFET RoadPak module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse and short-circuit testing

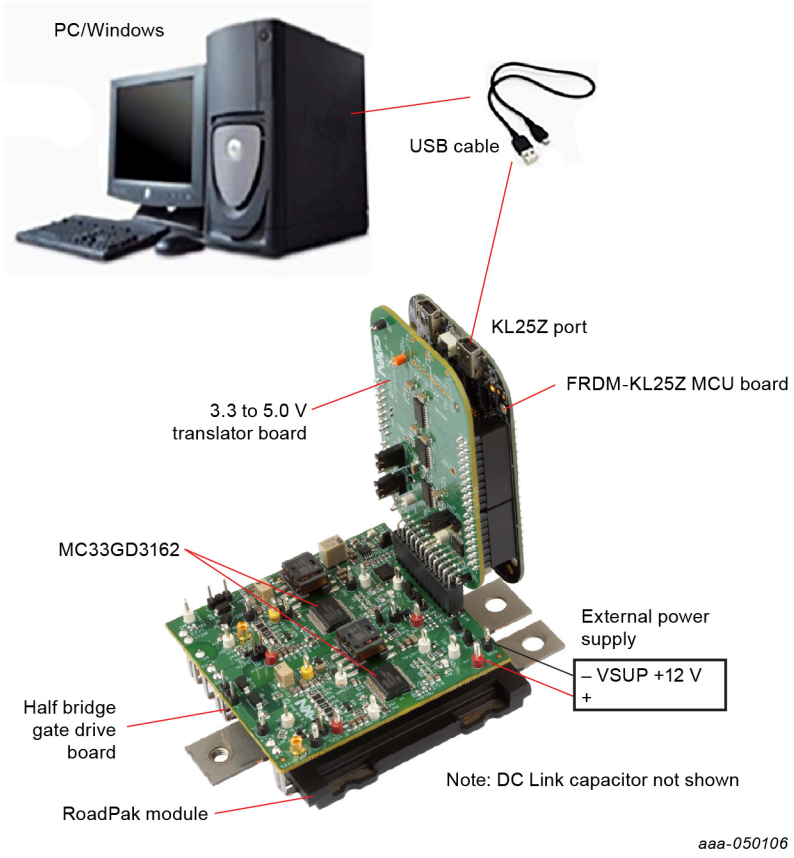


Figure 11. Evaluation board and system setup

6 Installation and use of software tools

Software for the FRDMGD3162RPEVM is distributed with the FlexGUI 2 for GD3162 tool (available on NXP.com). Necessary firmware comes preinstalled on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install the software for the FRDMGD3162RPEVM as a backup or to help debugging.

6.1 Installing FlexGUI 2 for GD3162 on your computer

The latest version of FlexGUI 2 supports GD3162. It is designed to run on any Windows 10 or higher based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI 2 software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI 2 wizard creates a shortcut, an NXP FlexGUI 2 icon appears on the desktop. By default, the FlexGUI 2 executable file is installed at **C:\NXP_GD3162_GUI-x.x.x.msi**.
   Installing the device drivers overwrites any previous FlexGUI 2 installation and replaces it with a current version containing the GD3162 drivers. However, configuration files from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

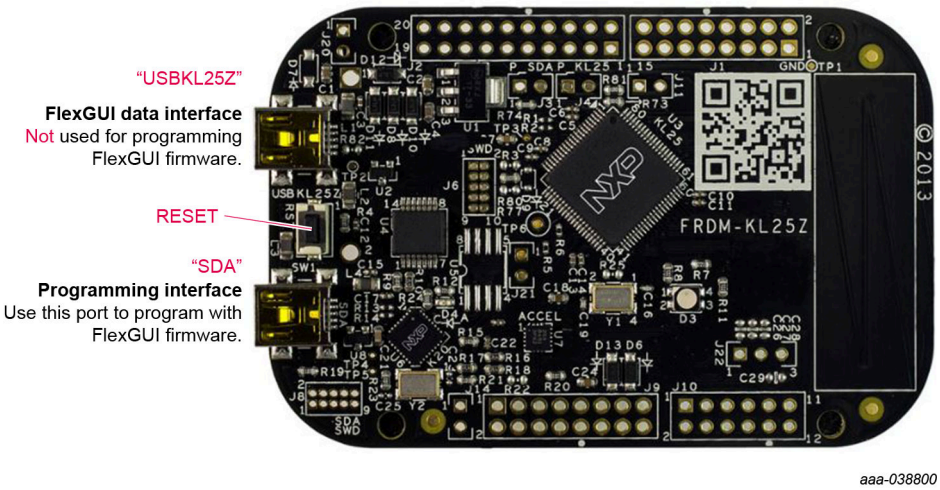


Figure 12. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI 2 for GD3162, and verify that the software version at the bottom is 6.4 or later (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as FRDM-KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI 2 for GD3162 package.
   a. From the FlexGUI 2 install directory or zip file, downloaded, find the firmware bin file "flexgui2_fw_kl25z_gd3162_vx.x.x.bin".
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD3162RPEVM.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory at PC drive FRDM-KL25Z (D:). Once done, disconnect the USB for OpenSDA port and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.

8. The FRDM-KL25Z board is now fully set up to work with FRDMGD3162RPEVM and the FlexGUI 2.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in nonvolatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.3 Using the FlexGUI 2

FlexGUI 2 for GD3162 is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD3162-specific functionality, configuration, and fault reporting. FlexGUI 2 also includes basic capacity for the FRDMGD3162RPEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD3162 on the board via daisy chain. See Figure 13 to Figure 28 for FlexGUI 2 for GD3162 internal register read and write access.

Starting FlexGUI 2 for GD3162

- FlexGUI 2 for GD3162 install program (C:\NXP_GD3162_GUI-x.x.x.msi)
- Download FlexGUI 2 and run the install program on your PC
- When you start the application, Figure 13 allows you to select the target application board, half-bridge EVB or three-phase inverter (x3 - 2 channel) or (x6 - 1 channel), kit preset (standard or daisy chain), target MCU

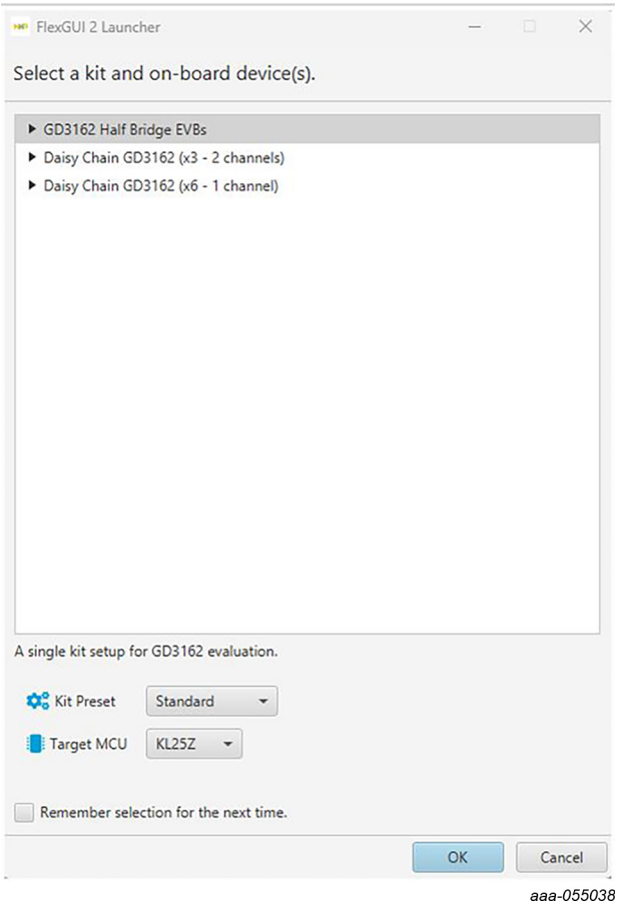


Figure 13. Kit selection

FlexGUI 2 connection

- Select FRDM-KL25Z COM port from the drop-down menu and select Connect to establish USB connection
  - If connection is not established, check USB cable connection between PC and KL25Z port and or scan again and select an alternate COM port for FRDM-KL25Z
  - If connection is not established, ensure that proper firmware is installed on FRDM-KL25Z MCU for FlexGUI 2 (refer to step 6 in Section 6.2)

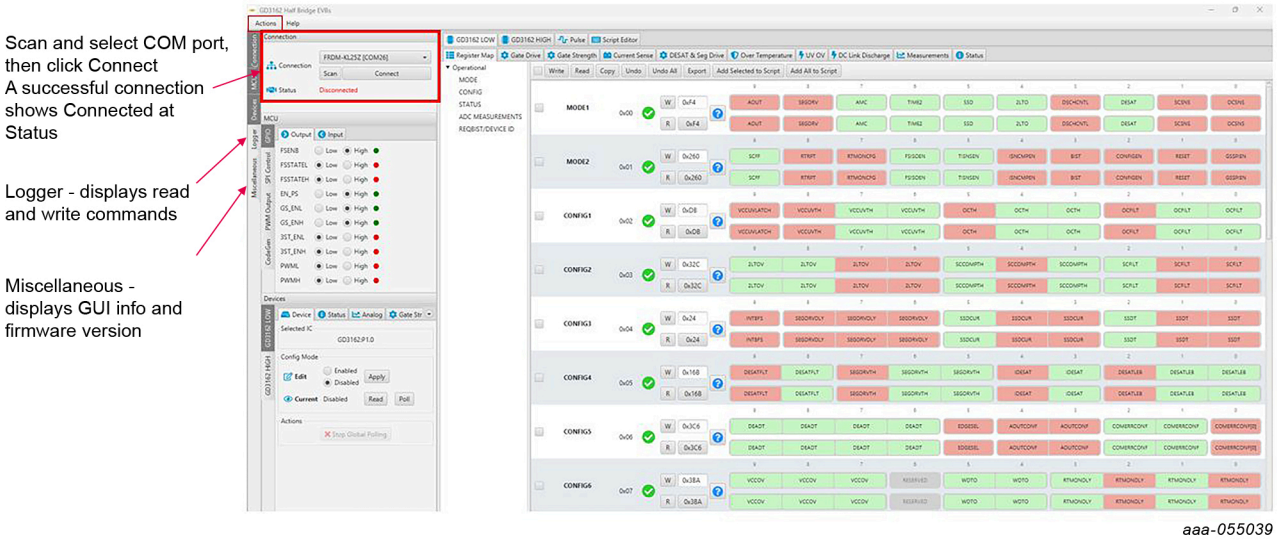
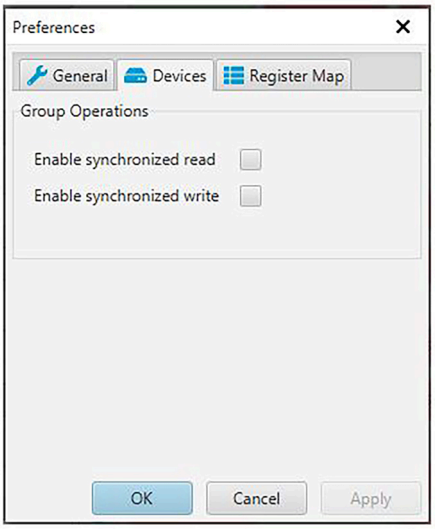


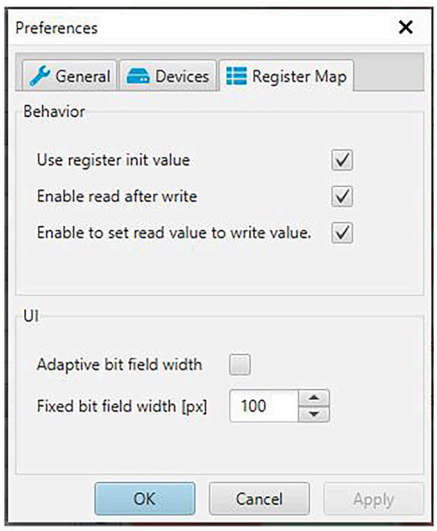
Figure 14. FlexGUI 2 connection

Set GUI actions and preferences

Access preferences from Actions menu at top left of GUI



Enable synchronized read and write to set both HS and LS devices simultaneously with same settings if desired



Enable Use register init value and Enable read after write and Enable to set read value to write value if desired (recommended)

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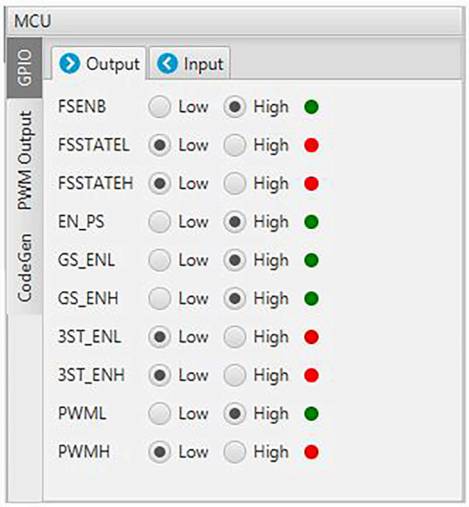
Figure 15. Actions and preferences settings



Fail-safe mode enable (active LOW) (high side and low side)

Fail-safe state (low side)

Fail-safe state (high side)

Enable power supply (flyback) VCC on board (17 V high side and low side)

Gate strength enable LOW (high side and low side)

Gate strength enable HIGH (high side and low side)

Gate strength enable LOW 3-state (high side and low side)

Gate strength enable HIGH 3-state (high side and low side)

Pulse width modulation (low side)

Pulse width modulation (high side)

Set logic level on gate drive and hardware inputs as desired.

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Figure 16. MCU GPIO output control

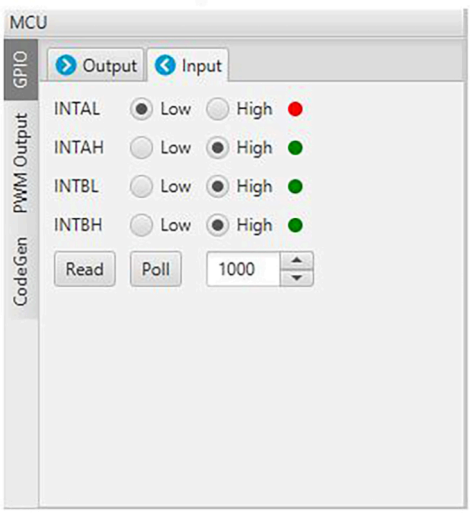


Figure 17. MCU GPIO input

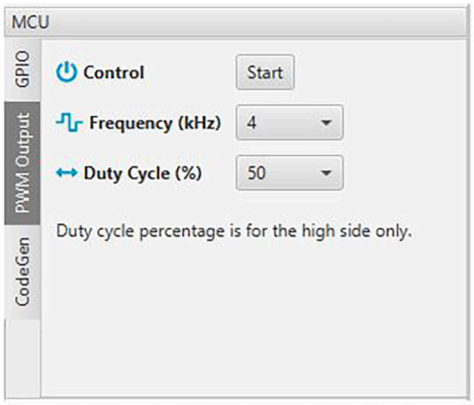


Figure 18. MCU PWM output

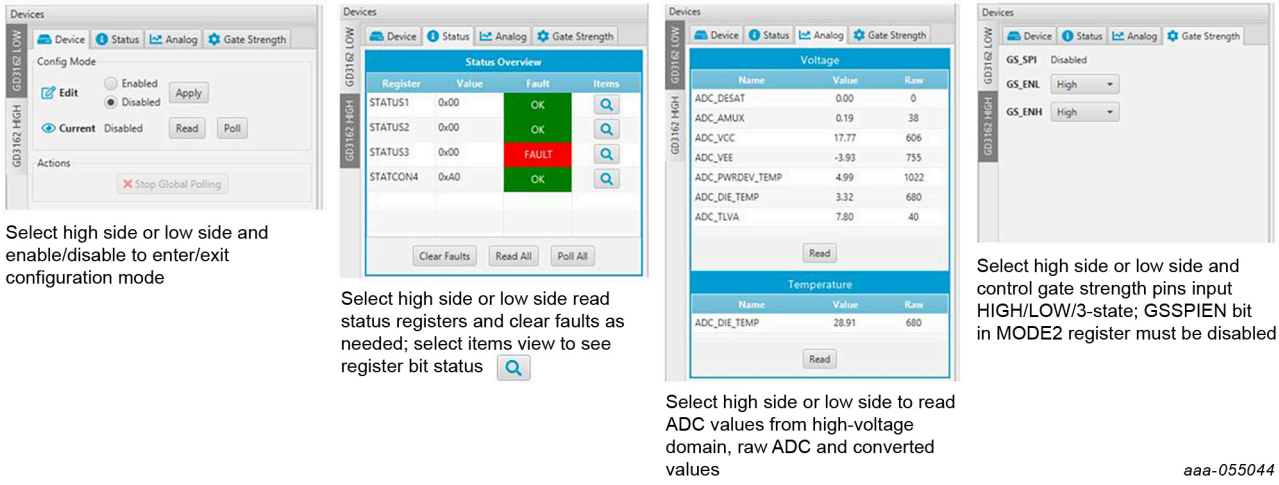


Figure 19. Devices

Figure 20. GUI tabs

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking the R button and can be written by using the W button
- Copy button to copy the read values to the write line; can be set to copy automatically
- Global register controls perform the selected command on all registers with the checkbox selected
- Add to Script adds current and selected register values to a script in the script editor window

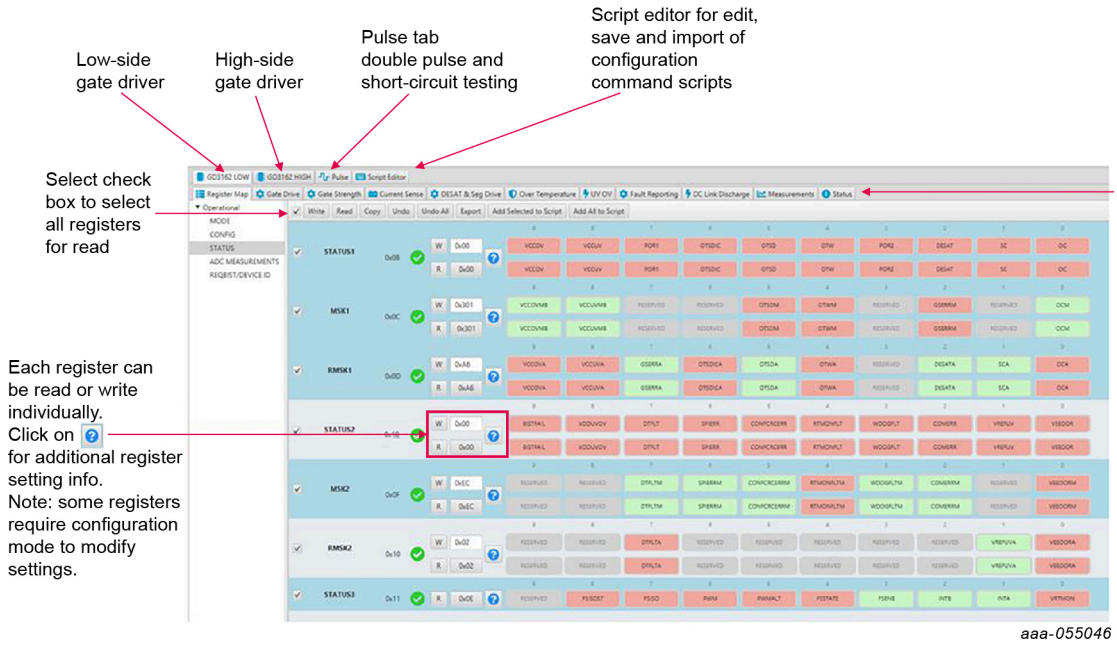
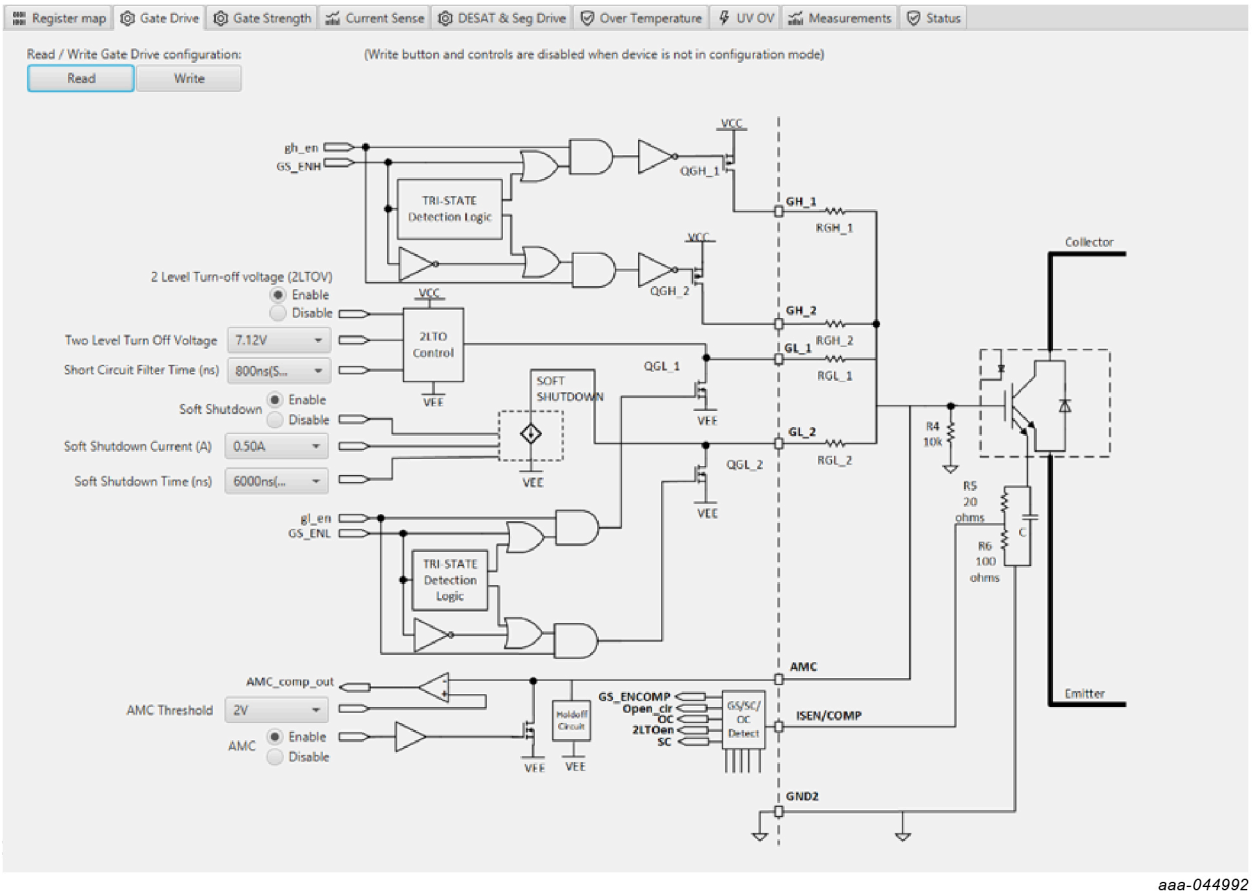


Figure 21. GUI tabs continued

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.



aaa-044992

Figure 22. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

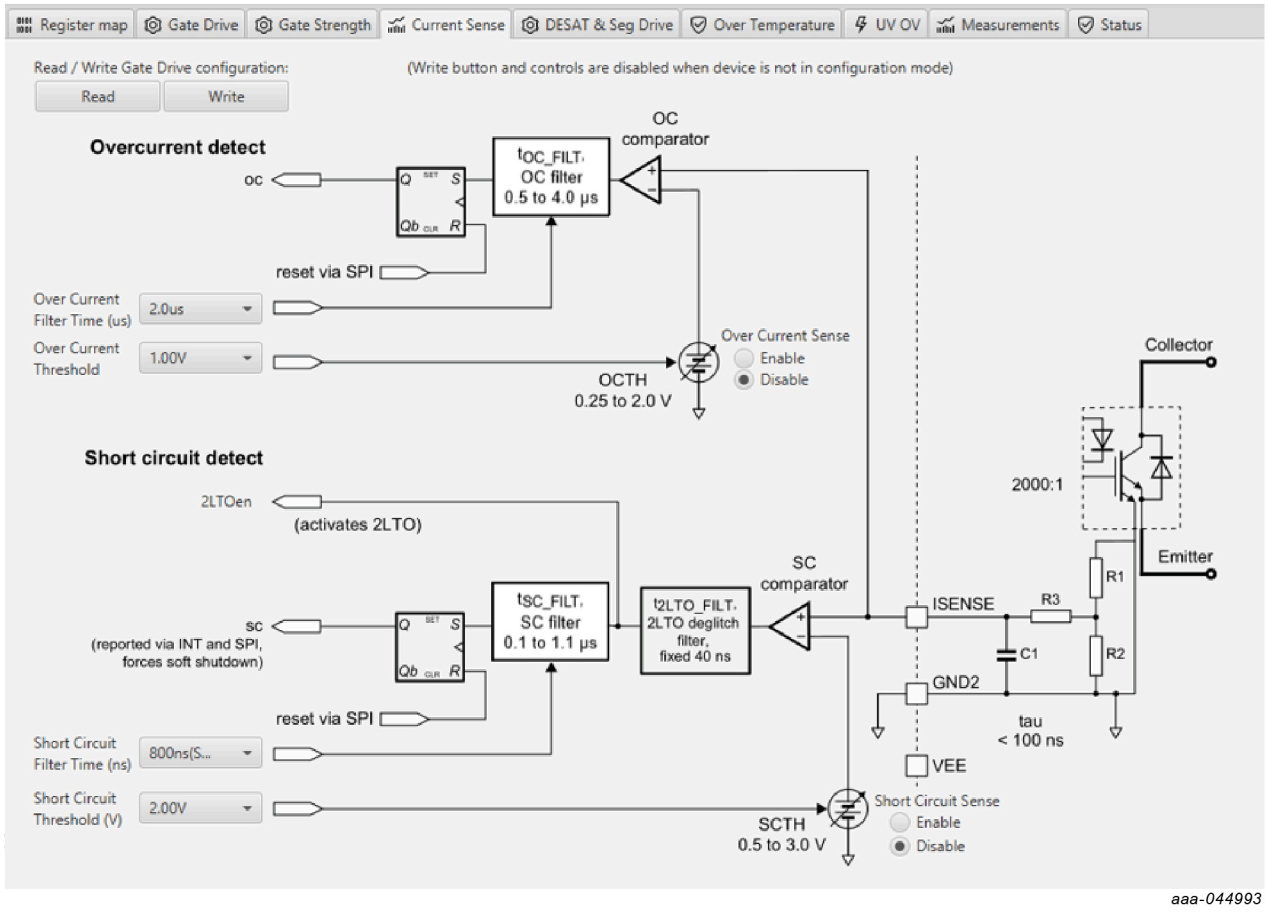


Figure 23. Current sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

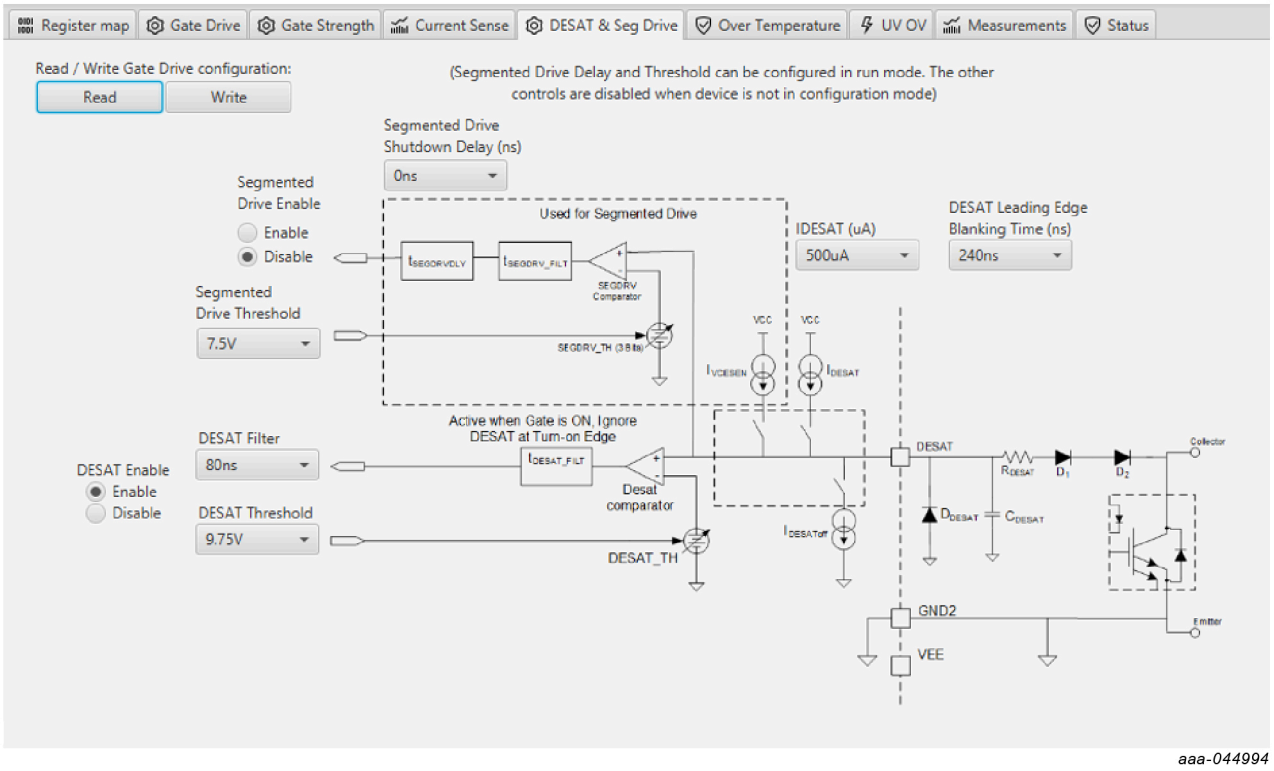


Figure 24. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

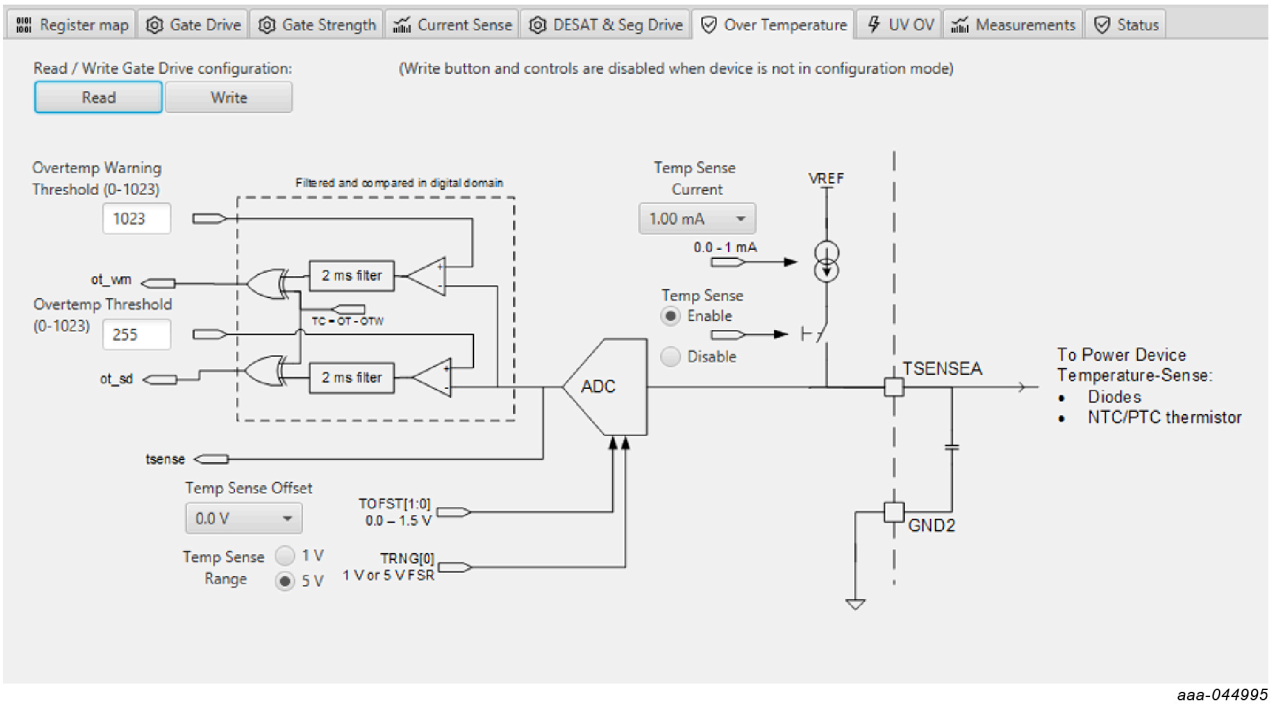


Figure 25. Overtemperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

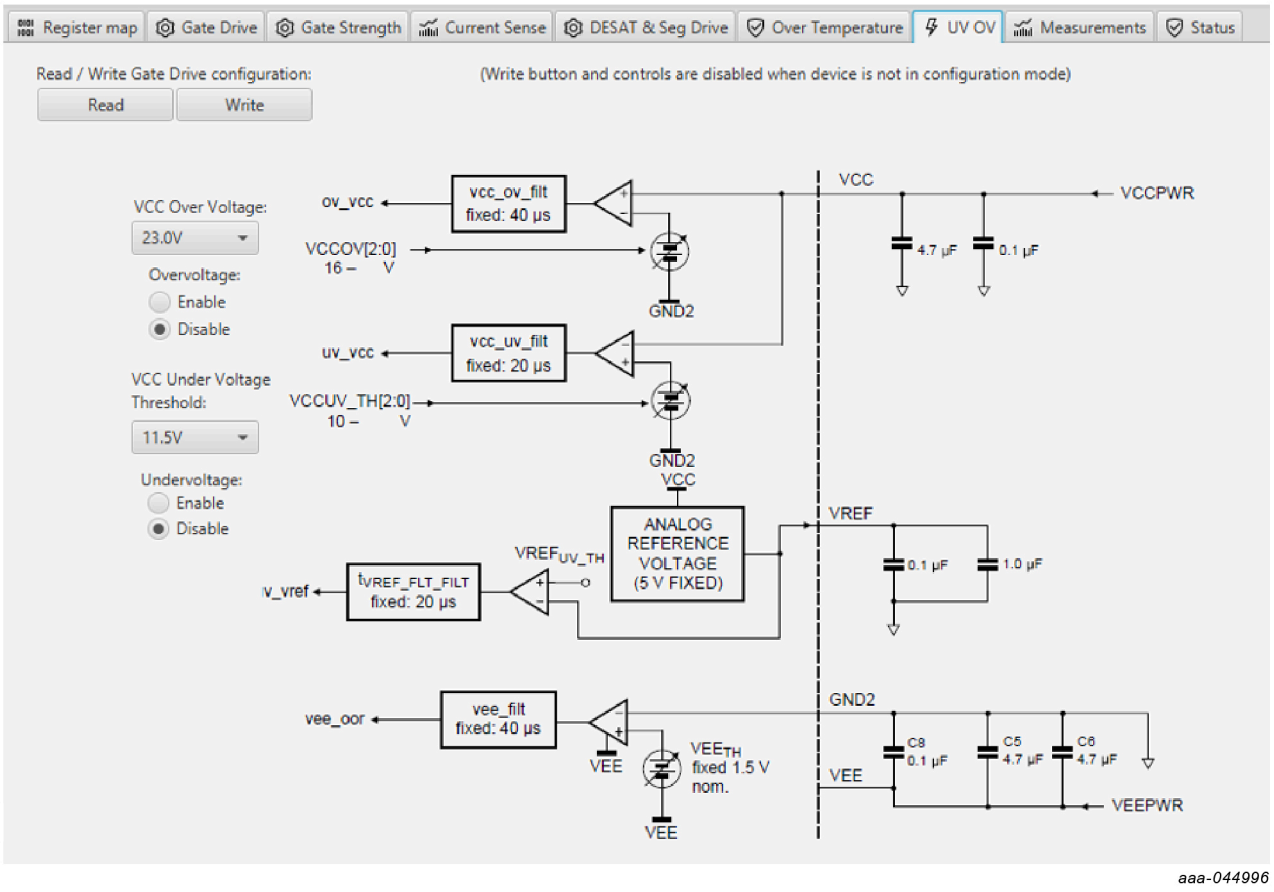


Figure 26. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

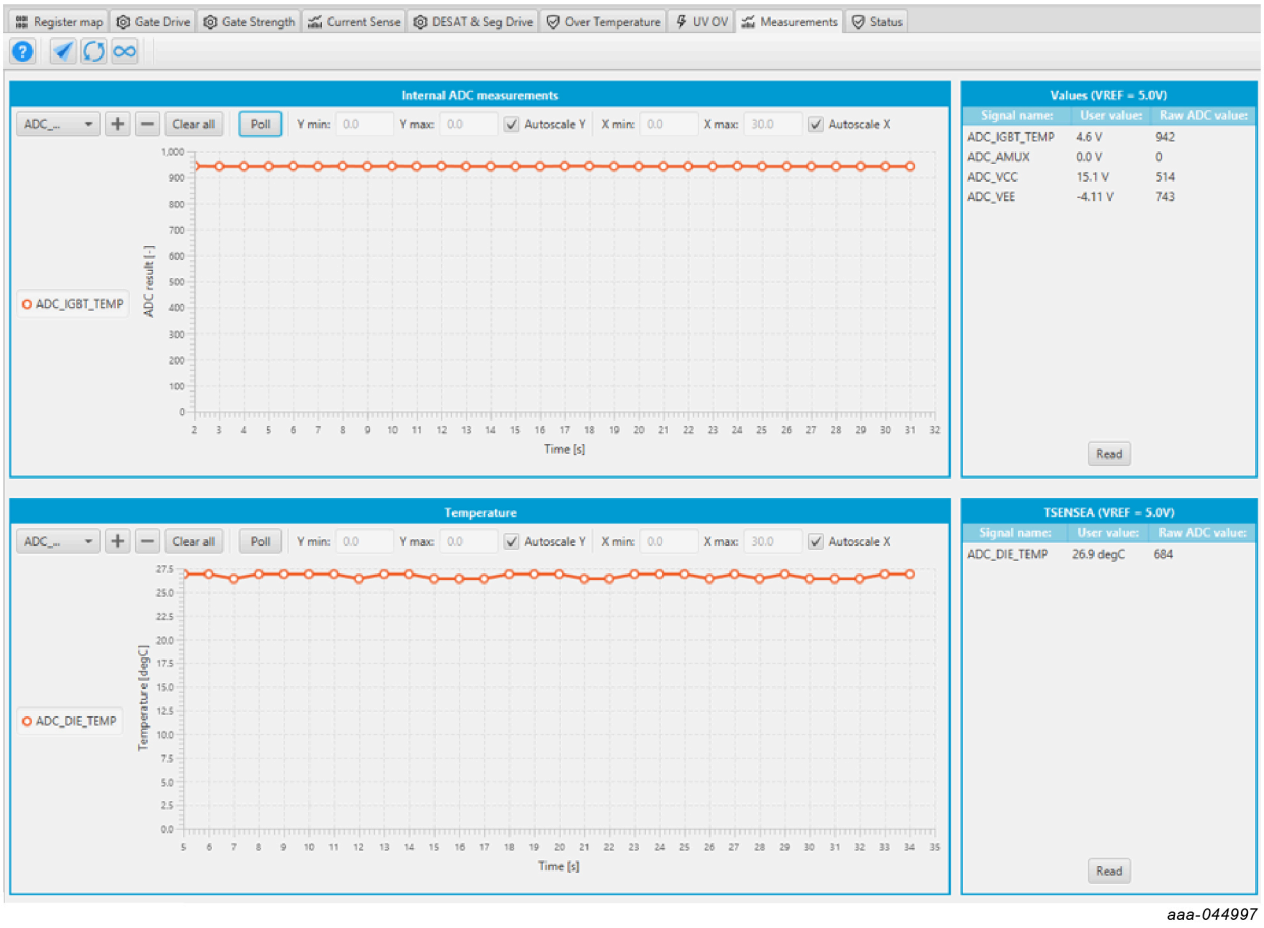


Figure 27. Measurements tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired t1, t2, and t3 timings for each test type; select enable then generate pulses

KL25Z MCU generates the desired pulses from selectable timings (t1, t2, t3)

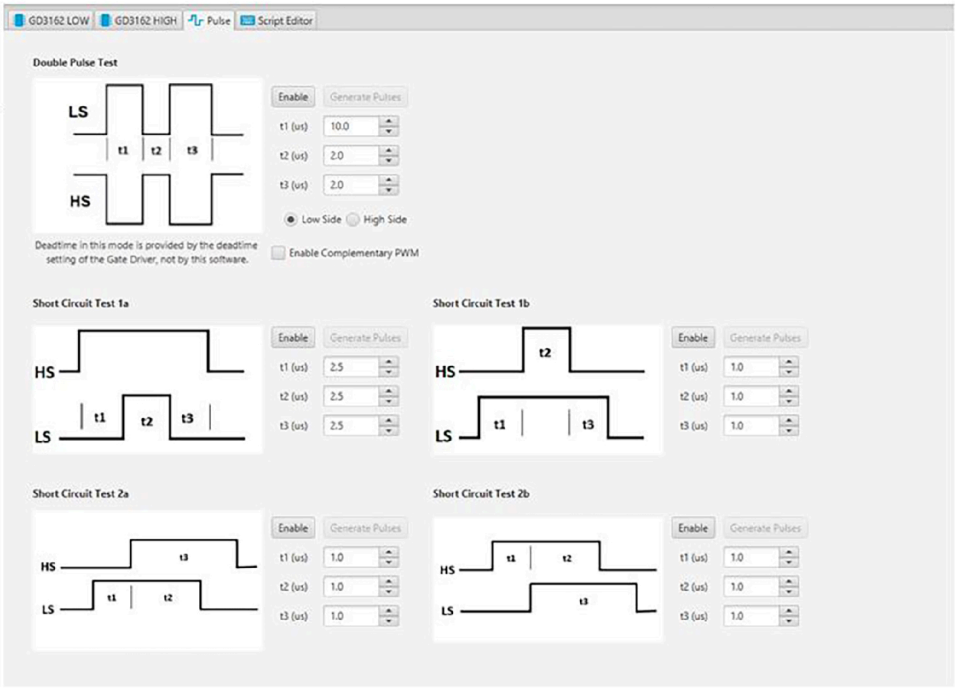


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Figure 28. Pulse tab

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
Unable to establish COM port connection	Check USB cable is connected to KL25Z port on FRDM-KL25Z MCU	If the USB cable is not connected to PC USB and KL25Z port GUI will not be able to establish USB connection	Plug in USB cable to PC USB port and FRDM-KL25Z KL25Z port
	Incorrect firmware installed on FRDM-KL25Z MCU	If the incorrect firmware is installed on the FRDM-KL25Z MCU board GUI will not be able to establish USB connection	Go to step 5 in this user guide for installing FlexGUI 2 on your computer to locate firmware file in GUI download package and copy to FRDM-KL25Z through openSDA port on MCU board.
	Check the COM port setting on FlexGUI 2. The drop-down menu will show the various COM ports available.	Selecting the incorrect COM port in the COM port drop-down menu will not be able to establish USB connection.	Select an alternative COM in the COM port drop-down menu on FlexGUI 2.

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.6
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3162	Monitor PWML (TP11) and PWMH (TP10) on translator board for commanded PWM state. Check position of jumpers J4 and J5 on translator board.
	Check FSENB status (see GD3162 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3162: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J14) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3162: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3162: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3162 VDD voltage	Low translator output voltage (compared with correct VDD at GD3162) causes the high threshold at the GD3162 pin to be crossed later than commanded	Check translator output voltage selection (J3) is configured to the same level as the GD3162 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3162 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3162 after translator is powered (over USB).

Problem	Evaluation	Explanation	Corrective action(s)
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R37).
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R37 feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R37). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J14) and PWMHSEL (J10) to bypass dead time. See Section 4.4.3 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check PS_EN is set to HIGH in FlexGUI 2; see Figure 16	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from FlexGUI 2. See Section 4.4.3 for details.
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R37 feedback

7 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at http://www.nxp.com/FRDMGD3162RPEVM on the Overview tab under Get Started.

8 References

[1] Tool summary page for FRDMGD3162RPEVM http://www.nxp.com/FRDMGD3162RPEVM

[2] Product summary page for GD3162 device http://www.nxp.com/GD3162

9 Revision history

Table 7. Revision history

Document ID	Release date	Description
UM11887 v.2	8 May 2024	• Update for FlexGUI 2
UM11887 v.1	13 February 2023	• Initial version

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