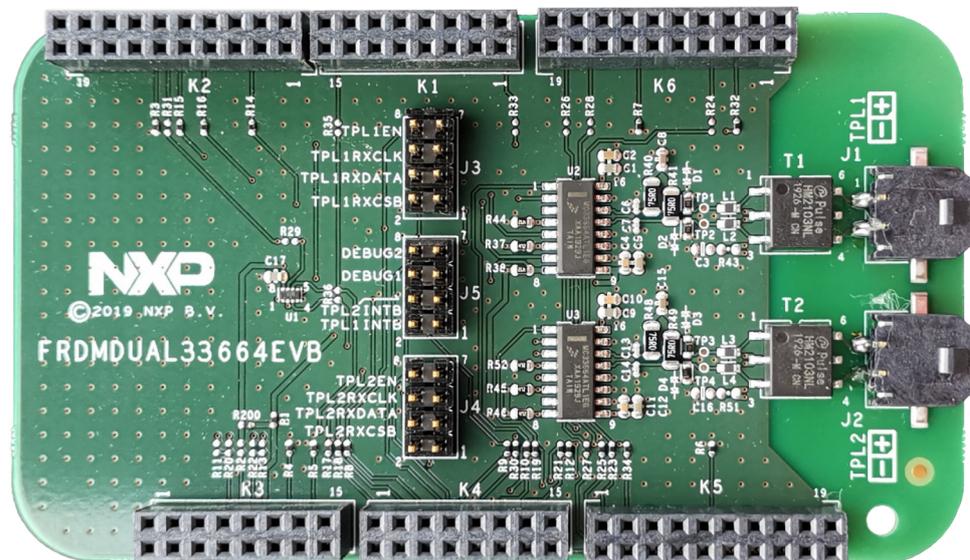


UM11334

FRDMDUAL33664EVB evaluation board

Rev. 1 — 15 January 2020

User guide



aaa-036222

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1 Introduction

This document is the user guide for the FRDMDUAL33664EVB evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of MC33664, Isolated network high-speed transceiver.

The scope of this document is to provide the user with information to evaluate the MC33664, Isolated network high-speed transceiver. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for FRDMDUAL33664EVB evaluation board is at <http://www.nxp.com/FRDMDUAL33664EVB>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the FRDMDUAL33664EVB evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

3 Getting ready

Working with the FRDMDUAL33664EVB requires the kit contents, additional hardware, and software, depending on the use case.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 20 cm TPL bus cable
- Quick start guide

3.2 Additional hardware

- Use with the S32K144 EVB (recommended)
- Use with other microcontroller platform (requires breadboard design)
- Use as standalone EVB, requires 5.0 V, 200 mA power supply (optional 3.3 V power supply 200 mA) and signal stimulation with signal generator

4 Getting to know the hardware

4.1 Kit overview

The FRDM DUAL33664EVB is a hardware tool for evaluation and development and is ideal for rapid prototyping of an isolated network high-speed transceiver. It can be used to evaluate the features of the MC33664A device.

The evaluation board allows the user to connect SPI signals from the MCU to the device SPI_TX and be able to create bit pulses transmission to the bus through the transformer. The messages received by the device can be converted bit by bit and transferred to the MCU by SPI.

4.1.1 FRDM DUAL33664EVB features

- Two MC33664ATL1EG isolated communication transceiver in a 16-pin SOICN package
- Isolated communication by transformers with connector
- Single TPL chain interface (requires two SPIs)
- Dual TPL chain interface (requires three SPIs)
- Compatible to S32K144EVB-Q100

Note: The FRDM DUAL33664EVB does not support the Fault line feature.

4.2 Kit featured components

Figure 1 identifies important components on the board and Table 1 provides additional details on these components.

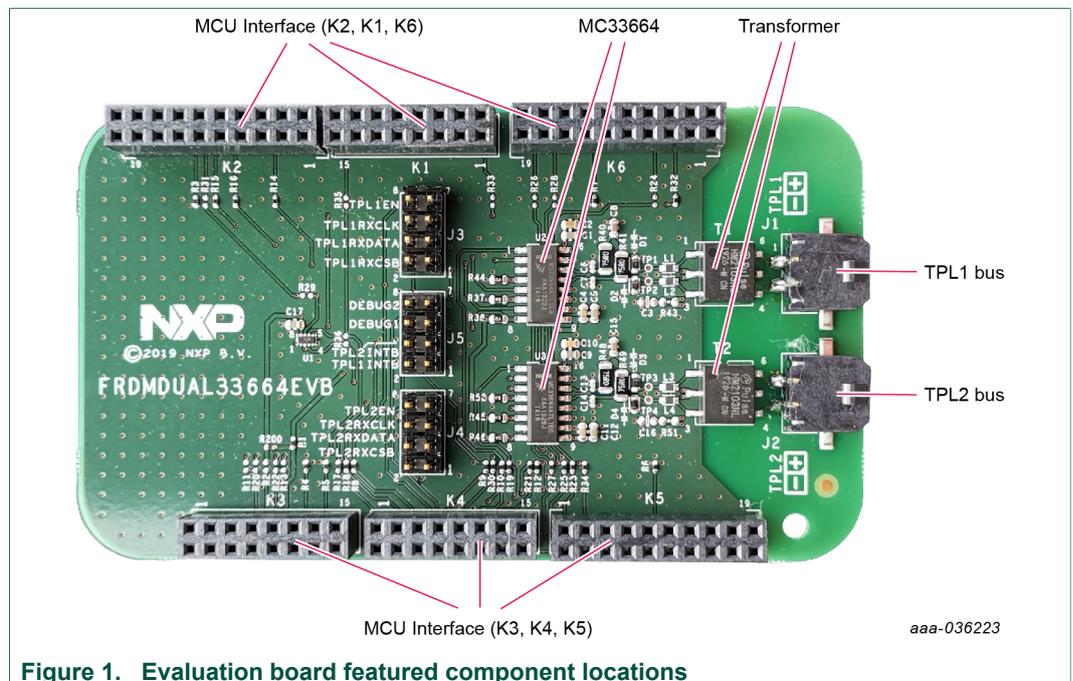


Figure 1. Evaluation board featured component locations

Table 1. Evaluation board component descriptions

Name	Description
MCU interface (K2, K1, K6)	Interface pin for microcontroller development platform (recommended S32K144-EVB)
MC33664	Isolated network high-speed transceiver
Transformer	Bus isolator transformer (T1, T2)
TPL1 bus	TPL1 bus interface
TPL2 bus	TPL2 bus interface
MCU interface (K3, K4, K5)	Interface pin for microcontroller development platform (recommended S32K144-EVB)

4.2.1 MC33664: Isolated network high-speed transceiver

4.2.1.1 General description

The MC33664 is a SMARTMOS transceiver physical layer transformer driver designed to interface a microcontroller conveniently to a high speed isolated communication network. MCU serial peripheral interface (SPI) data bits are directly converted to pulse bit information and transferred to the bus network.

Slave response messages use the same structure to send pulse bit information to the MC33664, which is converted and sent back to the MCU as a SPI bit stream.

4.2.1.2 Block diagram

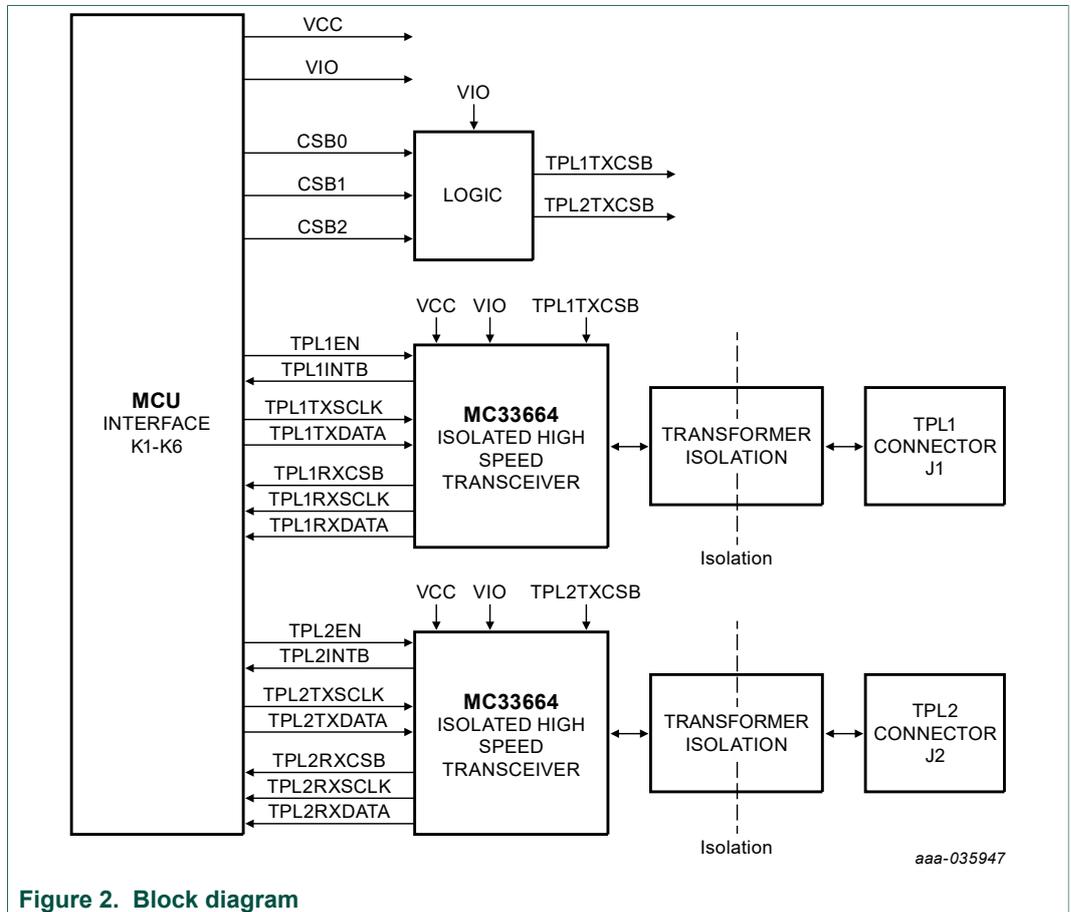


Figure 2. Block diagram

4.2.1.3 Features

- 2.0 Mbit/s isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions

4.2.1.4 Modes of operation

The modes of operation followed by MC33664 for the VIO and EN pins are shown in [Table 2](#).

Table 2. Modes of operation

Device mode	EN pin	VIO pin	LED pin	Comment
Normal	1	1	On	The MC33664 operates as a full transceiver. MCU messages transmitted on the SPI_TX emerge on the SPI_RX for the MCU to read.
Sleep	0	1	Off	In Sleep mode, the transceiver activates the INTB pin when a valid wake-up sequence is detected. The INTB pin remains low until the rising edge of the EN pin places the device in Normal mode.

4.2.2 Connectors

Figure 3 shows the location of connectors on the board.

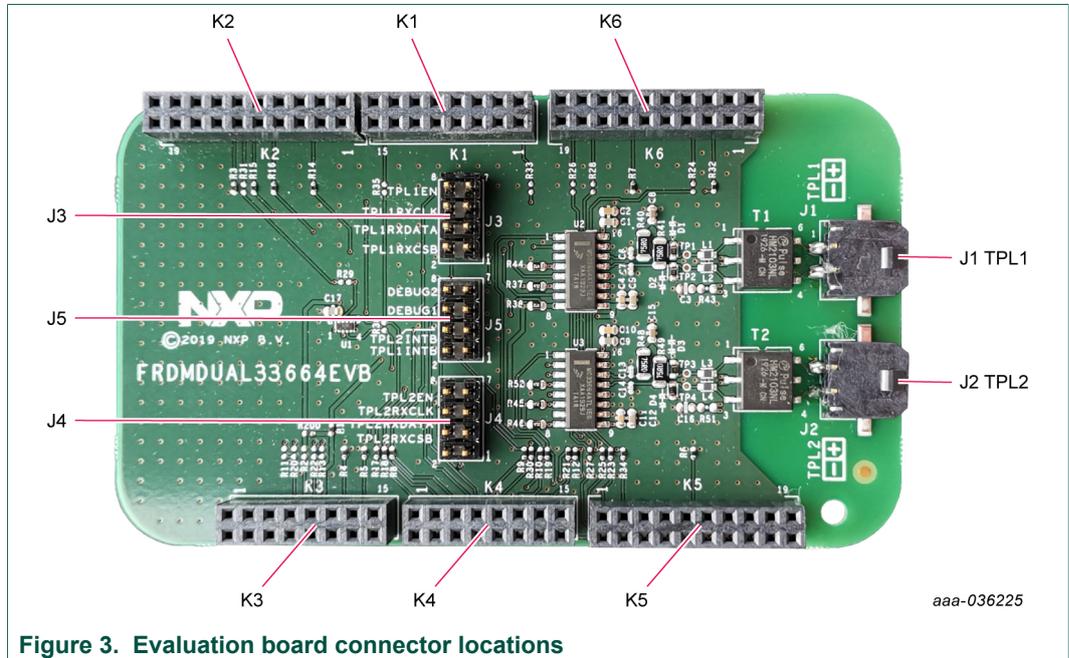


Figure 3. Evaluation board connector locations

4.2.2.1 TPL bus connectors

The connectors J1 and J2 provide access to TPL1 and TPL2 bus.

Table 3. TPL bus 1 connector J1

Schematic label	Signal name	Description
J1-1	TPL1RDTXP	TPL bus 1 – Receive/transmit input positive
J1-2	TPL1RD TXN	TPL bus 1 – Receive/transmit input negative

Table 4. TPL bus 2 connector J2

Schematic label	Signal name	Description
J2_1	TPL2RDTXP	TPL bus 2 – Receive/transmit input positive
J2_2	TPL2RD TXP	TPL bus 2 – Receive/transmit input negative

4.2.2.1.1 TPL bus selection

The FRDMDUAL33664EVB provides an option to dynamically select which TPL bus is used. Using three signals is possible to individually transmit on the TPL1 or TPL2 bus, or to transmit simultaneously on both TPL1 and TPL2 bus.

Note: For proper operation, the logic circuitry expects the unused PCS signals to be high.

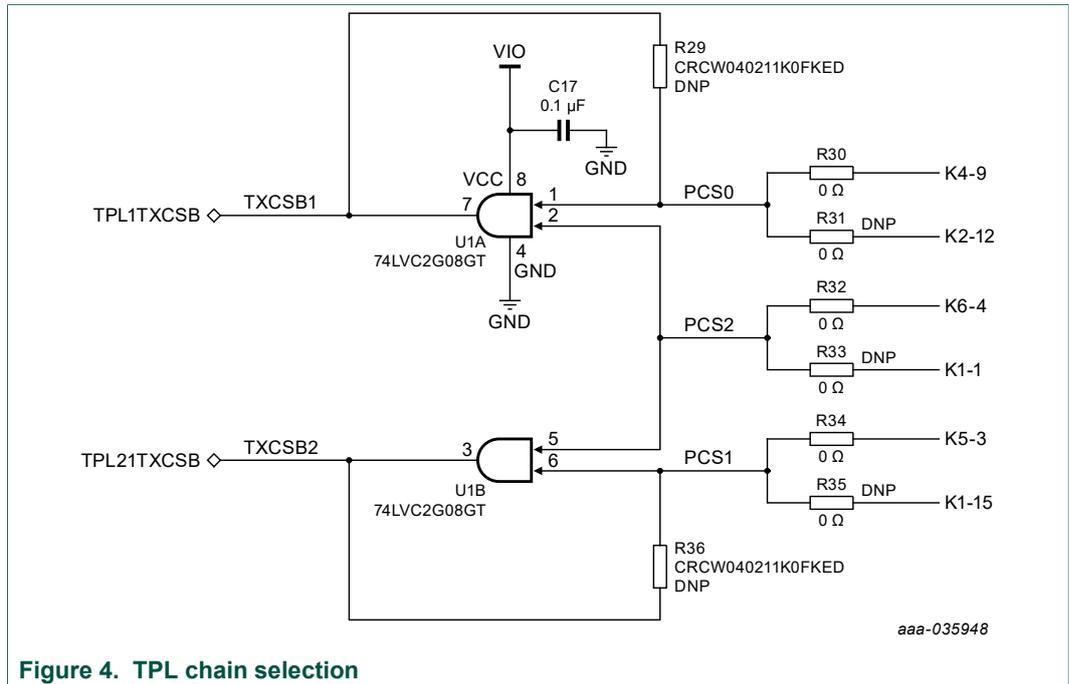


Figure 4. TPL chain selection

Table 5. TPL bus selection

Selected PCS line (low active)	Selected TPL line (low active)
PCS0	TPL1TXCSB
PCS1	TPL2TXCSB
PCS2	TPL1TXCSB and TPL2TXCSB

4.2.2.1.2 VIO selection

The FRDMDUAL33664EVB provides to option to select the IO voltage.

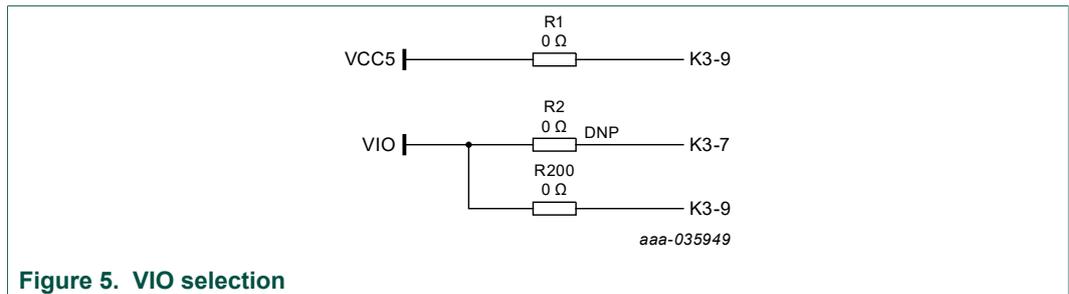


Figure 5. VIO selection

4.2.2.2 MCU interface connectors

The connectors K1 to K6 enable interface to an NXP microcontroller development platform. The mechanical dimensions and pinout is selected to fit the S32K144EVB-Q100 (recommended hardware platform). The evaluation board has a number of configuration options (0 Ohm resistors), which provides routing options.

The following table details the default configuration (S32K144EVB-Q100) signal mapping.

Table 6. Jumper (0 Ohm resistors) setting for S32K144-EVB (default)

Jumper	Setting	Signal	MCU interface
R1	populated	VCC5	K3-9
R2	—	VIO	K3-7
R200	populated	VIO	K3-9
R3	populated	GND	K2-13
R4	populated	GND	K3-11
R5	populated	GND	K3-13
R6	populated	GND	K5-12
R7	populated	GND	K6-12
R8	populated	TPL1EN	K4-5
R9	populated	TPL1INTB	K4-7
R10	populated	TPL1TXSCLK	K4-8
R11	—	TPL1TXSCLK	K3-6
R12	populated	TPL1TXDATA	K4-12
R13	—	TPL1TXDATA	K3-10
R14	populated	TPL1RXCSB	K2-5
R15	populated	TPL1RXSCLK	K2-11
R16	populated	TPL1RXDATA	K2-9
R17	populated	TPL2EN	K4-1
R18	populated	TPL2INTB	K4-3
R19	populated	TPL2TXSCLK	K4-8
R20	—	TPL2TXSCLK	K3-6
R21	populated	TPL2TXDATA	K4-12
R22	—	TPL2TXDATA	K3-10
R23	populated	TPL2RXCSB	K5-1
R24	—	TPL2RXCSB	K6-6
R25	populated	TPL2RXSCLK	K5-4
R26	—	TPL2RXSCLK	K6-18
R27	populated	TPL2RXDATA	K5-2
R28	—	TPL2RXDATA	K6-16
R29	—	TPL2RXDATA	bypass
R30	populated	TPL2RXDATA	K4-9
R31	—	TPL2RXDATA	K2-12
R32	populated	TPL2RXDATA	K6-4
R33	—	TPL2RXDATA	K1-1
R34	populated	TPL2TXCSB	K5-3
R35	—	TPL2TXCSB	K1-15
R36	—	TPL2TXCSB	bypass

The following table details the signals used for the S32K144EVB-Q100 evaluation boards.

Table 7. Signal routing for S32K144EVB-Q100

MCU Interface	Signal	MCU Signal	Description
K3-9	VCC5	5V	5.0 V supply
K3-9	VIO	5V	5.0 V IO supply
K2-13	GND	GND	Ground
K3-11	GND	GND	Ground
K3-13	GND	GND	Ground
K5-12	GND	GND	Ground
K6-12	GND	GND	Ground
K6-4	TPL12TXCSB	LPSP11_PCS0	TPL1 and TPL2 TX chip select
K4-5	TPL1EN	PTB0	TPL1 enable
K4-9	TPL1TXCSB	PTA6/LPSP11_PCS1	TPL1 TX chip select
K4-7	TPL1INTB	PTB1	TPL1 interrupt
K4-8	TPL12TXCLK	PTB14/LPSP11_SCK	TPL1 and TPL2 TX clock
K4-12	TPL12TXDATA	PTB16/LPSP11_SOUT	TPL1 and TPL2 TX data
K2-5	TPL1RXCSB	PTB5/LPSP10_PCS1	TPL1 RX chip select
K2-11	TPL1RXCLK	PTB2/LPSP10_SCK	TPL1 RX clock
K2-9	TPL1RXDATA	PTB3/LPSP10_SIN	TPL1 RX data
K5-3	TPL2TXCSB	PTA16/LPSP11_PCS2	TPL2 TX chip select
K4-1	TPL2EN	PTD4	TPL2 enable
K4-3	TPL2INTB	PTB12	TPL2 interrupt
K5-1	TPL2RXCSB	PTA15/LPSP12_PCS3	TPL2 RX chip select
K5-4	TPL2RXCLK	PTE15/LPSP12_SCK	TPL2 RX clock
K5-2	TPL2RXDATA	PTE16/LPSP12_SIN	TPL2 RX data
K5-13	Debug1	PTC1	GPIO for debugging purposes
K5-15	Debug2	PTC2	GPIO for debugging purposes

4.2.2.3 Logic analyzer interface connectors J3, J4, J5

These connectors are intended for software development and debugging purposes. They allow easy access to used signals and to monitor them for instance with a logic analyzer or an oscilloscope.

Table 8. Connector J3

Pin	Name	Description
1	J3_1	Ground
2	J3_2	TPL1RXCSB
3	J3_3	Ground
4	J3_4	TPL1RXDATA
5	J3_5	Ground
6	J3_6	TPL1RXCLK
7	J3_7	Ground
8	J3_8	TPL1EN

Table 9. Connector J4

Pin	Name	Description
1	J4_1	Ground
2	J4_2	TPL2RXCSB
3	J4_3	Ground
4	J4_4	TPL2RXDATA
5	J4_5	Ground
6	J4_6	TPL2RXCLK
7	J4_7	Ground
8	J4_8	TPL2EN

Table 10. Connector J5

Pin	Name	Description
1	J5_1	Ground
2	J5_2	TPL1INTB
3	J5_3	Ground
4	J5_4	TPL2INTB
5	J5_5	Ground
6	J5_6	Debug1
7	J5_7	Ground
8	J5_8	Debug2

4.2.3 Compatible NXP MCU development platforms

FRDMDUAL33664EVB is compatible with the S32K144EVB-Q100 MCU development platform.

The information related to MCU development platform ordering and instruction is available at nxp.com.

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the FRDMDUAL33664EVB evaluation board are available at <http://www.nxp.com/FRDMDUAL33664EVB>.

5 Configuring the hardware

The FRDMDUAL33664EVB is configured as a shield board for the S32K144EVB-Q100 board. It can also be used in a standalone configuration. For other configurations, check mechanical/electrical fit or use, for example, a breadboard design.

5.1 S32K144EVB-Q100 board configuration

The FRDMDUAL33664EVB is configured for the S32K144EVB-Q100 board by default. Ensure that the S32K144EVB is configured correctly before connecting both boards together.

Table 11. S32K144EVB-Q100 jumper settings

Jumper	Configuration	Description
J104	1-2	Reset signal to OpenSDA, use to enter into OpenSDA Bootloader mode
	2-3 (Default)	Reset signal direct to the MCU, use to reset S32K144
J106	1-2	S32K144 powered by 12 V power source
	2-3 (Default)	S32K144 powered by USB micro connector (Open SDA)
J109/108	1-2 (Default)	Removes CAN termination resistor

The S32K144EVB uses 5.0 V for the GPIOs (see [Figure 6](#)). The FRDMMDUAL33664EVB has the configuration resistor R200 installed to use 5.0 V for the VIO.

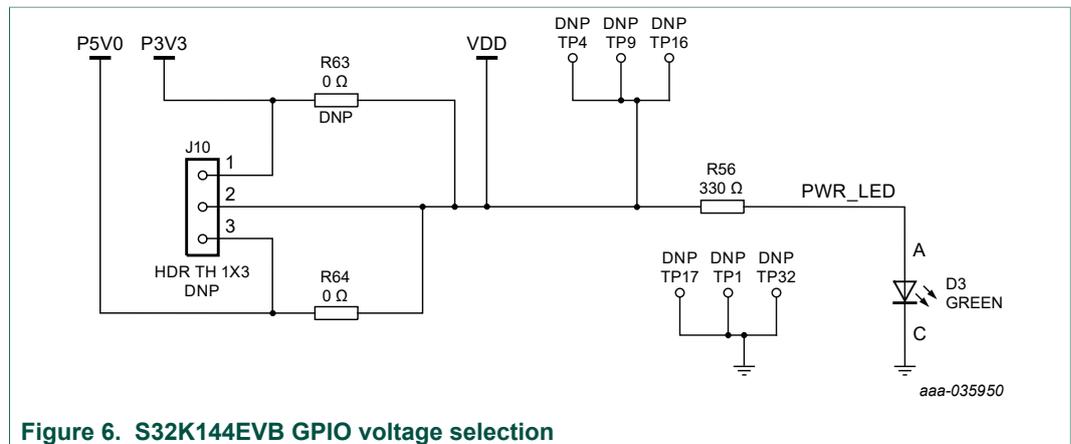


Figure 6. S32K144EVB GPIO voltage selection

When both boards are connected, the SPI and other signals are directly connected with suitable MCU pins. Power is supplied to the FRDMMDUAL33664EVB through the 5.0 V from the S32K144EVB. No external power supply is required.

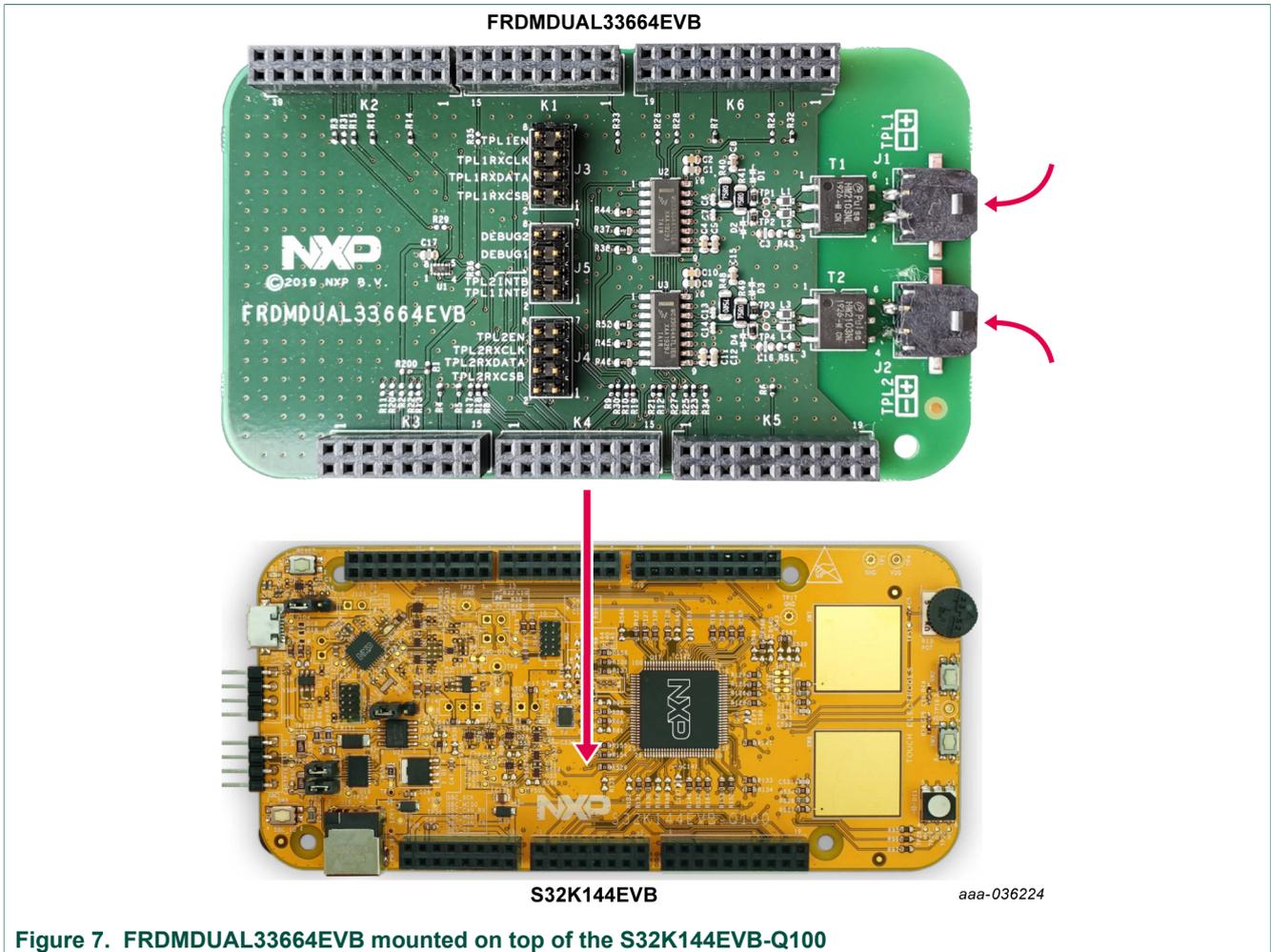


Figure 7. FRDMDUAL33664EVB mounted on top of the S32K144EVB-Q100

5.2 Standalone or other microcontroller platforms

When the board is used in standalone or with other microcontroller platforms, the SPI signals must be manually connected to the MCU interface connectors K1 to K6.

Table 12. Standalone configuration

MCU Interface	Signal	Description
K3-9	VCC5	5.0 V supply
K3-7	VIO	3.3 V supply
K2-13	GND	Ground
K3-11	GND	Ground
K3-13	GND	Ground
K5-12	GND	Ground
K6-12	GND	Ground
K6-4	TPL12TXCSB	TPL1 and TPL2 TX chip select
K4-5	TPL1EN	TPL1 enable
K4-9	TPL1TXCSB	TPL1 TX chip select
K4-7	TPL1INTB	TPL1 interrupt

MCU Interface	Signal	Description
K4-8	TPL12TXCLK	TPL1 and TPL2 TX clock
K4-12	TPL12TXDATA	TPL1 and TPL2 TX data
K2-5	TPL1RXCSB	TPL1 RX chip select
K2-11	TPL1RXCLK	TPL1 RX clock
K2-9	TPL1RXDATA	TPL1 RX data
K5-3	TPL2XCSB	TPL2 TX chip select
K4-1	TPL2EN	TPL2 enable
K4-3	TPL2INTB	TPL2 interrupt
K5-1	TPL2RXCSB	TPL2 RX chip select
K5-4	TPL2RXCLK	TPL2 RX clock
K5-2	TPL2RXDATA	TPL2 RX data
K5-13	Debug1	GPIO for debugging purposes
K5-15	Debug2	GPIO for debugging purposes

Required power supply connections are:

- VCC5 must be provided with 5.0 V
- VIO must be provided with 3.3 V or 5.0 V depending on the required communication signal levels

6 References

- [1] **FRDMDUAL33664EVB** — detailed information on this board, including documentation, downloads, and software and tools
<http://www.nxp.com/FRDMDUAL33664EVB>
- [2] **MC33664** — product information on MC33664, Isolated network high-speed transceiver
<http://www.nxp.com/MC33664>
- [3] **S32K144EVB-Q100** — detailed information on this board, including documentation, downloads, and software and tools
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7 Revision history

Revision history

Rev	Date	Description
v.1	20200115	Initial version

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Date of release: 15 January 2020
Document identifier: UM11334

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