Automotive NP8700
Quad Channel Combination Regulator

FEATURES

- AEC-Q100 grade1
- Operating temperature range -40 to 125°C
- Including four regulators
  Ch.1: High voltage 1.2A synchronous buck converter.
  Ch.2: Low voltage 1.0A synchronous buck converter.
  Ch.3: Selectable regulator.
  Low voltage 1.0A synchronous buck converter
  or Low voltage 0.2A LDO
  Ch.4: Low voltage 0.2A LDO
  or Low voltage Load switch (0.2A)
  e.g.) Ta=85°C
  DCDC Ch.1: 12V →3.3V/1.2A
  (Included supply for Ch.2, 3, 4)
  Ch.2: 3.3V→1.8V/0.5A (maximum 1.0A)
  Ch.3: 3.3V→1.2V/1.0A (maximum 1.0A)
  LDO Ch.4: 3.3V→2.8V/0.2A (maximum 0.2A)
- Wide operating input voltage range
  3.9V to 20V (Ch.1)
  2.4V to 5.5V (Ch.2, Ch.3, Ch.4)
- Output voltage range
  2.5V to 5.5V (Ch1.)
  0.8V to 3.6V (Ch.2, Ch.3, Ch.4)
- Free power-on sequence and power-good function
  - Select power-on sequence at R_{SEQ}
  - Power-good function reduces RESET IC
  - (NP8700 can be adding delay time by C_{DELAY})
- Protection function
  - UVLO (Under Voltage Lockout) can be selectable
  - Over current protection function for more safety operation (Hiccup/Foldback or Latch)
  - Thermal shutdown
- Oscillating frequency Fixed 2.0MHz
- External clock synchronization
- Spread Spectrum Frequency Modulation (SSFM function selectable)
- Anti-phase operation between Ch.1 and Ch.2 / 3
- Built-in compensation circuit
- Soft start function

APPLICATIONS

- Camera modules
- Photoelectric sensors
- Small Application and other.

GENERAL DESCRIPTION

The NP8700 is quad channel combination regulator including one wide input range buck converter, two secondary synchronous buck converters and one LDO, using a BCD process.

Ch.3 can be selectable to the synchronous buck converter mode or LDO mode. Ch4. can be selectable to LDO mode or load switch mode. Therefore, the NP8700 expands the choices when building power supply block suitable for various applications.

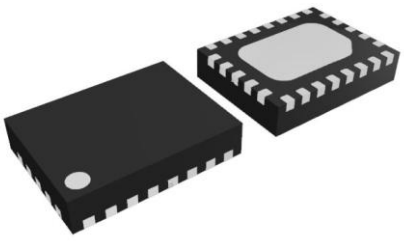
The NP8700 is operated anti-phase operation between Ch.1 and Ch.2 / 3 in order to reduce EMI noise.

Also, NP8700 included SSFM operation.

The power on sequence can be set with just one external resistor. Therefore, flexible power on sequence configuration is available, and the power-good function's delay time can be set using an external C_{DELAY}, eliminating the need for an additional reset IC. NP8700 has two types of over-current protection: hiccup/foldback and latch, which can be switched depending on the application requirements. The over-current protection uses a detection method that is safer and contributes to the miniaturization of inductors.

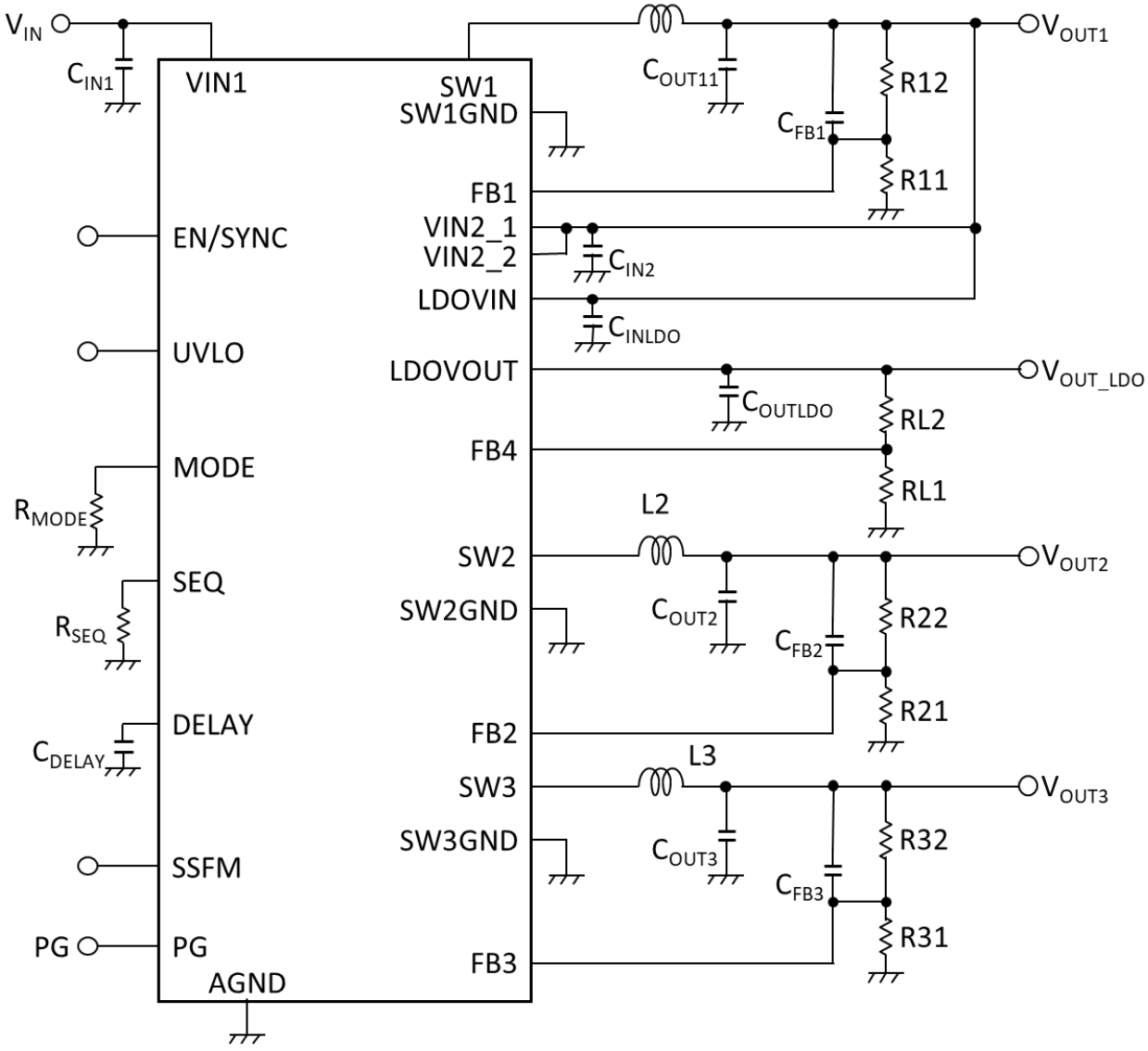
Small package: 3.4mm × 2.6mm QFN is adopted suitable for small application such as camera module.

PACKAGE

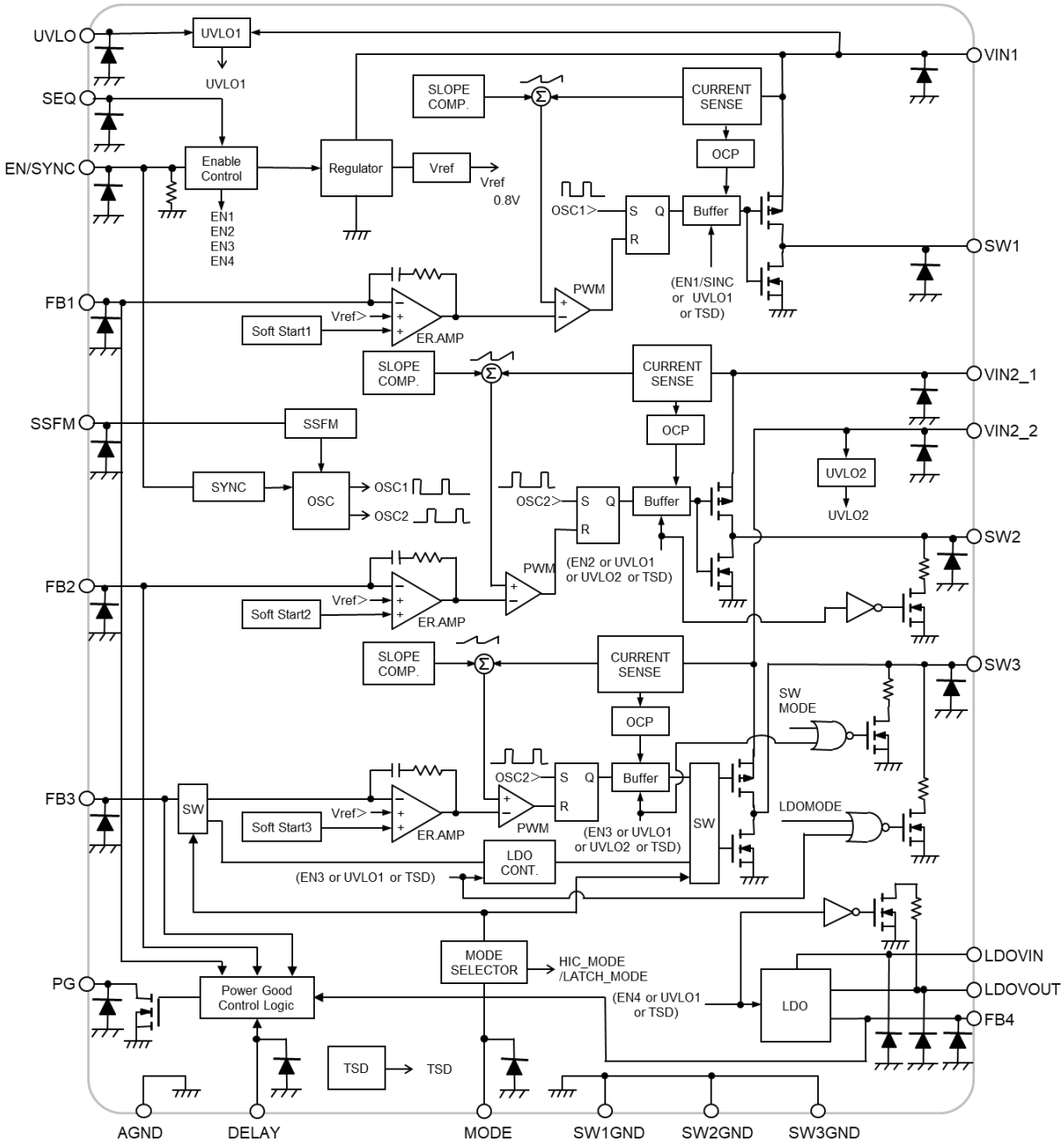


QFN2634-26-NC
3.4 mm x 2.6 mm x 0.75 mm

▪ TYPICAL APPLICATION



■ BLOCK DIAGRAM



■ PRODUCT NAME INFORMATION

NP8700 aa b cc d

NP8700NCAE2P

Description of configuration

Composition	Item	Description
aa	Package code	Indicates the package. Refer to the order information NC: QFN2634-26-NC
b	Version	Indicates IC version: Version A.
cc	Packing	E2: Refer to the packing specifications.
d	Grade	Indicates the quality grade. P: Automotive

Grade

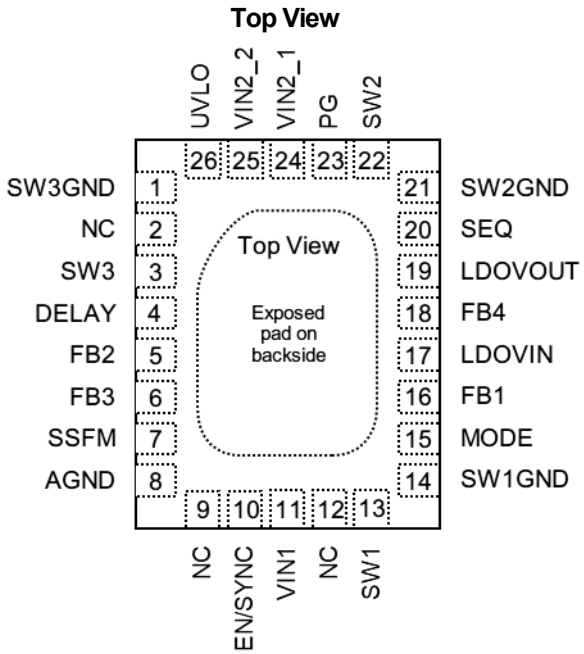
d	Applications	Operating Temperature Range	Test Temperature
P	Chassis, Body control and In-vehicle	−40 °C to 125 °C	25°C, 125 °C

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
NP8700NCAE2P	QFN2634-26-NC	✓	✓	✓	18	1500

Note: Contact our sales representatives for other voltages.

■ PIN DESCRIPTIONS



QFN2634-26-NC Pin Configuration

Pin No.	Pin Name	I/O	Description
1	SW3GND	GND	SW3 Ground
2	NC	-	NC
3	SW3	O	Ch.3 Output
4	DELAY	I	Delay setting for PG
5	FB2	I	Ch.2 Voltage feedback input
6	FB3	I	Ch.3 Voltage feedback input
7	SSFM	I	SSFM ON/OFF control
8	AGND	GND	Analog Ground
9	NC	-	NC
10	EN/SYNC	I	Enable input/External CLK input
11	VIN1	Power	Ch.1 Power supply input
12	NC	-	NC
13	SW1	O	Ch.1 Output
14	SW1GND	GND	SW1 Ground
15	MODE	I	Ch3. Mode select/ OCP Setting
16	FB1	I	Ch.1 Voltage feedback input
17	LDOVIN	I	Ch.4 Power supply input
18	FB4	I	Ch.4 Voltage feedback input
19	LDOVOUT	O	Ch.4 Output
20	SEQ	I	Power on sequence select
21	SW2GND	GND	SW2 Ground
22	SW2	O	Ch.2 Output
23	PG	O	Power-good output
24	VIN2_1	Power	Ch.2, Ch.3 Power supply input (When using, short it to VIN2_2.)
25	VIN2_2	Power	Ch.2, Ch.3 Power supply input (When using, short it to VIN2_1.)
26	UVLO	I	UVLO Select

■ ABSOLUTE MAXIMUM RATINGS

	SYMBOL	RATING	UNIT
Supply Voltage	V_{VIN1}	−0.3 to 22	V
	V_{VIN2_1}, V_{VIN2_2}, V_{VINLDO}	−0.3 to 7	V
Voltage between pins VIN1 - SW1	$V_{VIN1-SW1}$	22	V
SW2/SW3 pin Voltage	V_{SW2} V_{SW3}	−0.3 to 7	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	−0.3 to 22	V
UVLO pin Voltage	V_{UVLO}	−0.3 to 7	V
MODE pin Voltage	V_{MODE}	−0.3 to 7	V
SEQ pin Voltage	V_{SEQ}	−0.3 to 7	V
DELAY pin Voltage	V_{DELAY}	−0.3 to 7	V
SSFM pin Voltage	V_{SSFM}	−0.3 to 7	V
FB pin Voltage	V_{FB1}, V_{FB2} V_{FB3}, V_{FB4}	−0.3 to 7	V
PG pin Voltage	V_{PG}	−0.3 to 7	V
Junction Temperature ※1	T_j	−40 to 150	°C
Storage Temperature	T_{stg}	−40 to 150	°C

*1 Calculate the power consumption of the IC from the operating conditions, and calculate the junction temperature with the thermal resistance.

Please refer to "*THERMAL CHARACTERISTICS*" for the thermal resistance under our measurement board conditions

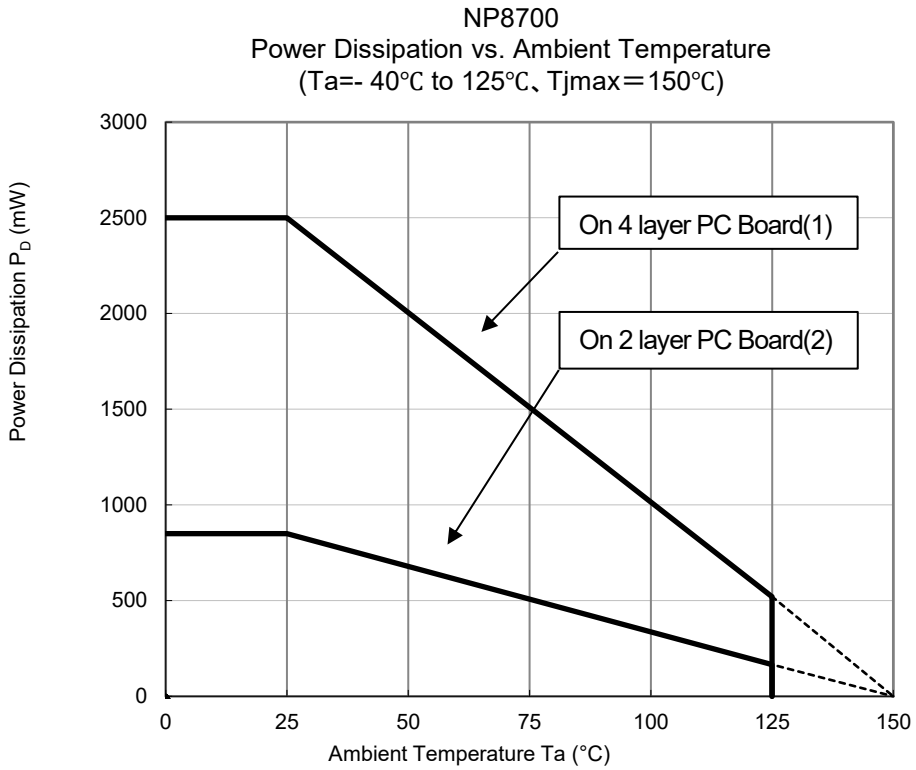
ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ THERMAL CHARACTERISTICS

Package	Parameter	Measurement Result	unit
QFN2634-26-NC	Thermal Resistance (θja)	146.3(1) 50.5(2)	°C/W
	Thermal Characterization Parameter (ψjt)	6.1(1) 0.8(2)	

θja：Junction-to-Ambient Thermal Resistance
ψjt：Junction-to-Top Thermal Characterization Parameter
(1) 2-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4) with exposed pad.
(2) 4-Layer: Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.
(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)



■ ELECTROSTATIC DISCHARGE RATINGS

	Condition	Protection Voltage
HBM	C = 100pF, R = 1.5kΩ	±2000V
CDM		±1000V

ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge test is done based on JESD47. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

	SYMBOL	VALUE	UNIT
Operating Voltage	V_{VIN1}	3.9 to 20	V
	V_{VIN2_1}, V_{VIN2_2}, V_{VINLDO}	2.4 to 5.5	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	0 to 20	V
PG pin Voltage	V_{PG}	0 to 5.5	V
External Clock Input	f_{SYNC}	1.9 to 2.5	MHz
Operating Temperature	T_a	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

Ch.1(Primary synchronous buck converter) (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VIN2_1}=V_{VIN2_2} = 3.3V, Ta = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCK OUT						
ON Threshold Voltage	V_{T_ON1L}	V_{UVLO} = L, V_{VIN1} = L →H	3.50	3.75	3.90	V
		V_{UVLO} = L, V_{VIN1} = L →H Ta = −40 to 125°C	3.50	–	3.90	
OFF Threshold Voltage	V_{T_OFF1L}	V_{UVLO} = L, V_{VIN1} = H →L	3.00	3.20	3.45	V
		V_{UVLO} = L, V_{VIN1} = H →L Ta = −40 to 125°C	3.00	–	3.45	
ON Threshold Voltage	V_{T_ON1H}	V_{UVLO} = H, V_{VIN1} = L →H	5.45	5.80	6.20	V
		V_{UVLO} = H, V_{VIN1} = L →H Ta = −40 to 125°C	5.45	–	6.20	
OFF Threshold Voltage	V_{T_OFF1H}	V_{UVLO} = H, V_{VIN1} = H →L	4.90	5.25	5.60	V
		V_{UVLO} = H, V_{VIN1} = H →L Ta = −40 to 125°C	4.90	–	5.60	
Hysteresis Voltage	V_{HYS1}		500	550	–	mV
SOFT START						
Soft Start Time	t_{SS1}	V_{FB1} = 0.55V	1.0	2.5	4.0	ms
		V_{FB1} = 0.55V Ta = −40 to 125°C	0.5	–	4.5	
OSCILLATOR						
Oscillating Frequency	f_{OSC1}		1.86	2.0	2.20	MHz
		Ta = −40 to 125°C	1.76	–	2.20	
Modulation Frequency Range	f_{FS1}	V_{SSFM} = H	–	±5	–	%
ERROR AMPLIFIER						
Reference Voltage	V_{B1}		-1.0%	0.6	+1.0%	V
		Ta = −40 to 125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B1}		-0.1	–	0.1	µA
		Ta = −40 to 125°C	-0.1	–	0.1	
PWM COMPARATOR						
Maximum Duty Cycle	$MAXDUTY1$	V_{FB1} = 0.5V	100	-	-	%
		V_{FB1} = 0.5V、Ta = −40 to 125°C	100	-	-	
Minimum OFF Time	$t_{OFF1\text{-}min}$		-	50	110	ns
		Ta = −40 to 125°C	-	-	110	
Minimum ON Time	$t_{ON1\text{-}min}$		-	55	110	ns
		Ta = −40 to 125°C	-	-	110	
Over Current Protection Circuit						
Cool Down Time	t_{COOL1}	R_{MODE} = 33kΩ or 10kΩ	-	115	-	ms
Output Block						
Pch. Output ON Resistance	R_{ONP1}	$I_{SW1SOURCE}$ = 0.8A	-	0.55	0.85	Ω
Nch. Output ON Resistance	R_{ONN1}	$I_{SW1SINK}$ = 0.8A	-	0.25	0.5	Ω
Switching Current Limit	I_{LIM1}		1.8	2.2	2.6	A
Switch Leak Current (High-Side)	I_{LEAKH1}	$V_{EN/SYNC}$ = 0V, V_{VIN1} = 20V, V_{SW1} = 0V, T_a = -40°C to +125°C	-	-	4	µA
Switch Leak Current (Low-Side)	I_{LEAKL1}	V_{SW1} = 20V, T_a = -40°C to +125°C	-	-	4	µA

Ch.2(Secondary synchronous buck converter) (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VIN2_1}=V_{VIN2_2} = 3.3V, Ta = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCK OUT						
ON Threshold Voltage	V_{T_ON2}	V_{VIN2_1}=V_{VIN2_2}= L →H	2.05	2.25	2.40	V
		V_{VIN2_1}=V_{VIN2_2}= L →H Ta = −40 to 125°C	2.05	–	2.40	
OFF Threshold Voltage	V_{T_OFF2}	V_{VIN2_1}=V_{VIN2_2}= H →L	2.00	2.15	2.35	V
		V_{VIN2_1}=V_{VIN2_2}= H →L Ta = −40 to 125°C	2.00	–	2.35	
Hysteresis Voltage	V_{HYS2}		50	100	–	mV
SOFT START						
Soft Start Time	t_{SS2}	V_{FB2} = 0.55V	1.0	2.5	4.0	ms
		V_{FB2} = 0.55V Ta = −40 to 125°C	0.5	–	4.5	
OSCILLATOR						
Oscillating Frequency	f_{OSC2}		1.86	2.0	2.20	MHz
		Ta = −40 to 125°C	1.76	–	2.20	
Modulation Frequency Range	f_{FS2}	V_{SSFM} = H	–	±5	–	%
ERROR AMPLIFIER						
Reference Voltage	V_{B2}		-1.0%	0.6	+1.0%	V
		Ta = −40 to 125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B2}		-0.1	–	0.1	µA
		Ta = −40 to 125°C	-0.1	–	0.1	
PWM COMPARATOR						
Maximum Duty Cycle	$MAXDUTY2$	V_{FB2} = 0.5V	100	–	–	%
		V_{FB2} = 0.5V Ta = −40 to 125°C	100	–	–	
Minimum OFF Time	$t_{OFF2\text{-}min}$		–	55	120	ns
		Ta = −40 to 125°C	—	—	120	
Minimum ON Time	$t_{ON2\text{-}min}$		–	60	110	ns
		Ta = −40 to 125°C	—	—	110	
OVER CURRENT PROTECTION						
Cool Down Time	t_{COOL2}	R_{MODE} = 33kΩ or 10kΩ	–	115	–	ms
Output block						
Pch Output ON Resistance	R_{ONP2}	$I_{SW2SOURCE}$ = 0.5A	–	0.5	0.7	Ω
Nch Output ON Resistance	R_{ONN2}	$I_{SW2SINK}$ = 0.5A	–	0.25	0.4	Ω
Switching Current Limit	I_{LIM2}		1.2	1.5	1.8	A
Switch Leak Current (High-Side)	I_{LEAKH2}	$V_{EN1/SYNC}$ = 0V, V_{VIN2_1}=V_{VIN2_2}= 5.5V, V_{SW2} = 0V Ta = −40 to 125°C	–	–	5	µA
Switch Leak Current (Low-Side)	I_{LEAKL2}	V_{SW2} = 5.5V Ta = −40 to 125°C	–	–	5	µA

Ch.3 (SW REG MODE) (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VIN2_1}=V_{VIN2_2} = 3.3V, R_{MODE} = 33kΩ or 91 kΩ, Ta = 25°C unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCK OUT (Common with Ch.3 LDO mode)						
ON Threshold Voltage	V_{T_ON3}	V_{VIN2_1} = V_{VIN2_2}= L →H	2.05	2.25	2.40	V
		V_{VIN2_1} = V_{VIN2_2}= L →H Ta = −40 to 125°C	2.05	–	2.40	
OFF Threshold Voltage	V_{T_OFF3}	V_{VIN2_1} = V_{VIN2_2}= H →L	2.00	2.15	2.35	V
		V_{VIN2_1} = V_{VIN2_2} = H →L Ta = −40 to 125°C	2.00	–	2.35	
Hysteresis Voltage	V_{HYS3}		50	100	–	mV
SOFT START						
Soft Start Time	t_{SS3}	V_{FB3} = 0.55V	1.0	2.5	4.0	ms
		V_{FB3} = 0.55V Ta = −40 to 125°C	0.5	–	4.5	
OSCILLATOR						
Oscillating Frequency	f_{OSC3}		1.86	2.0	2.20	MHz
		Ta = −40 to 125°C	1.76	–	2.20	
Modulation Frequency Range	f_{FS3}	V_{SSFM} = H	–	±5	–	%
ERROR AMPLIFIER						
Reference Voltage	V_{B3}		-1.0%	0.6	+1.0%	V
		Ta = −40 to 125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B3}		-0.1	–	0.1	µA
		Ta = −40 to 125°C	-0.1	–	0.1	
PWM COMPARATOR						
Maximum Duty Cycle	$MAXDUTY3$	V_{FB3} = 0.5V	100	–	–	%
		V_{FB3} = 0.5V Ta = −40 to 125°C	100	–	–	
Minimum OFF Time	$t_{OFF3\text{-}min}$		–	55	120	ns
		Ta = −40 to 125°C	–	–	120	
Minimum ON Time	$t_{ON3\text{-}min}$		–	60	110	ns
		Ta = −40 to 125°C	–	–	110	
OVER CURRENT PROTECTION						
Cool Down Time	t_{COOL3}	R_{MODE} = 33kΩ or 10kΩ	–	115	–	ms
Output block						
Pch Output ON Resistance	R_{ONP3}	$I_{SW3SOURCE}$ = 0.5A	–	0.5	0.7	Ω
Nch Output ON Resistance	R_{ONN3}	$I_{SW3SINK}$ = 0.5A	–	0.25	0.4	Ω
Switching Current Limit	I_{LIM3}		1.2	1.5	1.8	A
Switch Leak Current (High-Side)	I_{LEAKH3}	$V_{EN/SYNC}$ = 0V, V_{VIN2_1}=V_{VIN2_2}= 5.5V, V_{SW3} = 0V Ta = −40 to 125°C	–	–	5	µA
Switch Leak Current (Low-Side)	I_{LEAKL3}	V_{SW3} = 5.5V Ta = −40 to 125°C	–	–	5	µA

Ch.3(LDO MODE) (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VIN2_1}=V_{VIN2_2} = 3.3V, R_{MODE} = Open or 10 kΩ, Ta = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Reference Voltage	V_{B3}	V_{FB3} = 0.5V	-1.0%	0.6	+1.0%	V
		V_{FB3} = 0.5V Ta = −40 to 125°C	-2.0%	–	+2.0%	
Output Current	I_{OUT3}	V_{OUT3} × 0.9, V_{OUT3}=1.8V	200	600	–	mA
		V_{OUT3} × 0.9, V_{OUT3}=1.8V Ta = −40 to 125°C	200	–	–	
Load Regulation	ΔV_{OUT3} /I_{OUT3}	I_{OUT3} = 1mA to 150mA V_{OUT3} =1.8V	-	11	33	mV /mA
		I_{OUT3} = 1mA to 150mA Ta = −40 to 125°C	-	-	72	
Ripple Rejection	RR3	ein = 50mVrms, f = 1kHz V_{OUT3} = 2.5V, I_{OUT3} = 150mA	–	50	–	dB
Dropout Voltage	ΔV_{IO3}	I_{OUT3} = 150mA	–	0.2	0.3	V
		I_{OUT3} = 150mA Ta = −40 to 125°C	–	–	0.4	
Average Temperature Coefficient of Output Voltage	ΔV_{OUT3} /Ta	I_{OUT3} = 150mA Ta = −40 to 125°C	–	±50	–	ppm/°C

Ch.4(Low voltage LDO) (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VINLDO} = 3.3V, Ta = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Reference Voltage	V_{B4}	V_{FB4} = 0.5V	-1.0%	0.6	+1.0%	V
		V_{FB4} = 0.5V Ta = −40 to 125°C	-2.0%	–	+2.0%	
Output Current	I_{OUT4}	V_{OUT4} × 0.9 V_{OUT4}=1.8V	200	600	–	mA
		V_{OUT4} × 0.9 V_{OUT4}=1.8V Ta = −40 to 125°C	200	–	–	
Load Regulation	ΔV_{OUT4} /I_{OUT4}	I_{OUT4} = 1mA to 150mA	-	11	33	mV /mA
		I_{OUT4} = 1mA to 150mA Ta = −40 to 125°C	–	–	72	
Ripple Rejection	RR4	ein = 50mVrms, f = 1kHz V_{OUT4} = 2.5V, I_{OUT4} = 150mA	–	50	–	dB
Dropout Voltage	ΔV_{IO4}	I_{OUT4} = 150mA	–	0.2	0.3	V
		I_{OUT4} = 150mA Ta = −40 to 125°C	–	–	0.4	
Average Temperature Coefficient of Output Voltage	ΔV_{OUT4} /Ta	I_{OUT4} = 150mA Ta = −40 to 125°C	–	±50	–	ppm/°C

General Characteristics (V_{VIN1} = $V_{EN/SYNC}$ = 12V, V_{VIN2_1} = V_{VIN2_2} = V_{VINLDO} = 3.3V, Ta = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
Quiescent Current1 (VIN1)	I_{DD1}	R_L = no load, V_{FB1} = 0.9V	-	3.6	5.5	mA
		R_L = no load, V_{FB1} = 0.9V Ta = −40 to 125°C	-	-	5.5	
Quiescent Current2 (VIN2_1, VIN2_2)	I_{DD2}	R_L = no load, V_{FB2} = 0.9V, V_{FB3} = 0.9 V	-	1.2	2.0	mA
		R_L = no load, V_{FB2} = 0.9V, V_{FB3} = 0.9V Ta = −40 to 125°C	-	-	2.0	
Quiescent Current3 (LDOVIN)	I_{DDLDO}	R_L = no load, V_{FB4} = 0.9V	–	0.1	0.2	mA
		R_L = no load, V_{FB4} = 0.9V Ta = −40 to 125°C	–	–	0.2	
Standby Current1 (VIN1)	I_{DD_STB1}	$V_{EN/SYNC}$ = 0V	–	–	3	µA
		$V_{EN/SYNC}$ = 0V Ta = −40 to 125°C	–	–	6	
Standby Current2 (VIN2_1, VIN2_2)	I_{DD_STB2}	$V_{EN/SYNC}$ = 0V	–	–	2	µA
		$V_{EN/SYNC}$ = 0V Ta = −40 to 125°C	–	–	6	
Standby Current3 (LDOVIN1)	I_{DD_STBLDO}	$V_{EN/SYNC}$ = 0V	–	–	15	µA
		$V_{EN/SYNC}$ = 0V Ta = −40 to 125°C	–	–	20	
Power Good						
High Level Detection Reference Voltage	V_{THH_PG}	Rising	0.63	–	0.69	V
		Rising, Ta=-40°C to 125°C	0.63	–	0.69	
Low Level Detection Reference Voltage	V_{THL_PG}	Rising	0.51	–	0.57	V
		Rising, Ta=-40°C to 125°C	0.51	–	0.57	
Hysteresis Voltage	V_{HYS_PG}		–	12	–	mV
Power Good ON Resistance	R_{ON_PG}	I_{PG1} = 1mA	-	100	-	Ω
OFF Leak current	I_{LEAK_PG}	V_{PG} = 5.5V T_a = 25°C	-	-	0.1	µA
		V_{PG} = 5.5V	-	-	0.1	
EN/SYNC control						
High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC}$ = L → H T_a = 25°C	1.6	-	20	V
		$V_{EN/SYNC}$ = L → H	1.6	-	20	
Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC}$ = H → L T_a = 25°C	0	-	0.4	V
		$V_{EN/SYNC}$ = H → L	0	-	0.4	
Input Bias Current	$I_{EN/SYNC}$	$V_{EN/SYNC}$ = 5V T_a = 25°C	-	1	3	µA
		$V_{EN/SYNC}$ = 5V	-	-	5	µA

■ DESCRIPTION OF BLOCK FEATURES

1. Mode Settings

By connecting the resistor between the MODE pin and GND, the operation mode of Ch.3 and protection type of over-current protection mode are selected.

Table 1 NP8700 Operating Modes and Set Resistors

MODE	Setting resistor R_{MODE}(±5%)		Ch.3	over-current protection mode	MODE Pin Voltage (±5%)
	Min	Max			
1	open		LDO	Latch	2.5V
2	82kΩ	110kΩ	SW reg.	Latch	1.4V
3	27kΩ	39kΩ	SW reg.	Hiccup(SW reg.) Foldback(LDO)	1.2V
4	6.8kΩ	15kΩ	LDO	Hiccup(SW reg.) Foldback(LDO)	1.0V

The mode setting can be set only at power on timing, and the state of the mode can be checked by pin voltage.

2. Power on sequence setting and HS-SWITCH mode setting for Ch.4

By connecting the following resistors between the SEQ pin and GND, it is possible to select the power on sequence of Ch.2 to Ch.4 from three patterns: SEQ=1,2,3. Please refer to the timing chart.
In addition, the Ch.4 can be operated as an HS-SWITCH by setting the resistor from 6.8kΩ to 15kΩ.
Power on sequence settings is effective in the following cases:

- By a high level at the EN/SYNC pin.
- By releasing the UVLO on Ch.1.
- Recovery from over current protection(latch)
- By releasing thermal shutdown

Sequence control shutdown is enabled by a low level at the EN/SYNC pin.

Table 2 NP8700 Power on Sequence and Set Resistors

SEQ	Setting resistor R_{SEQ}(±5%)		The power on sequence is from Ch.1 (left) to each Ch. (right). (Shutdown is in reverse order.)			
	Min	Max				
1	open		Ch.1	Ch.2	Ch.3	Ch.4
2	82kΩ	110kΩ	Ch.1	Ch.3	Ch.4	Ch.2
3	27kΩ	39kΩ	Ch.1	Ch.4	Ch.2	Ch.3
HS-SWITCH (Ch.4)	6.8kΩ	15kΩ	Ch.1	Ch.2	Ch.3	Ch.4

Only the SEQ set before powering on is valid.

■ DESCRIPTION OF BLOCK FEATURES (continued)

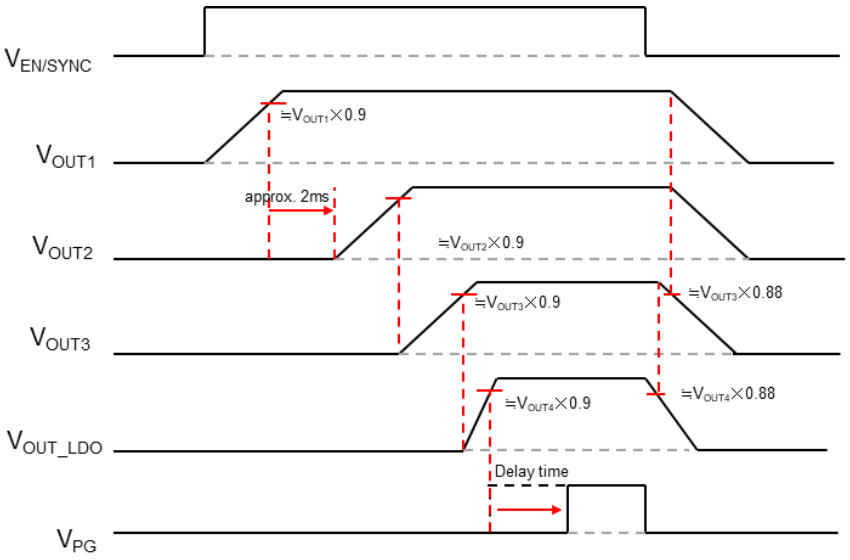


Fig.1 Example timing chart of Ch.1~Ch.4 (when SEQ1 is selected)

● HS-SWITCH mode

The high-side switch mode uses the output transistor of the LDO installed in Ch.4 as a high-side switch.

This makes it possible to supply the output voltage of Ch.1, which is usually initiated, after power on Ch.2,3. Connect V_{OUT1} to the LDOVIN pin and the output voltage is supplied from the LDOVOUT pin.

However, please note that a voltage drop occurs due to the ON resistance (approximately 0.6 Ω) of the output transistor depending on the load current, and there is no over-current protection.

The conditions for transitioning to high-side switch mode are as follows:

- R_{SEQ}: 6.8kΩ~15kΩ connection and FB4>0.85V during Ch.1 power on. (V_{OUT1} is supplied to FB4 or supplied from an external power supply)

Application circuit examples and timing charts are below.

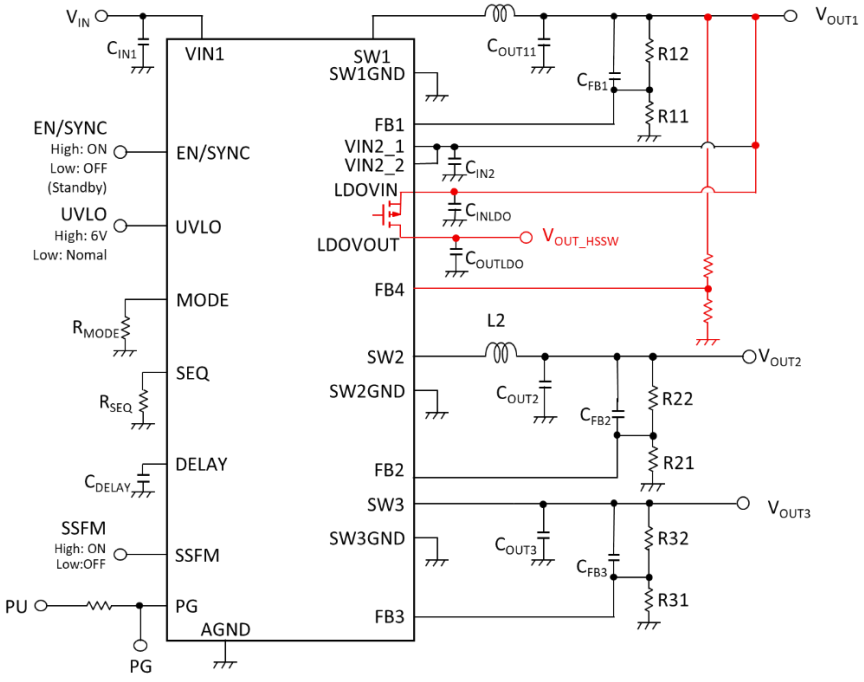


Fig.2 Example of HS-SWITCH mode application circuit

■ DESCRIPTION OF BLOCK FEATURES (continued)

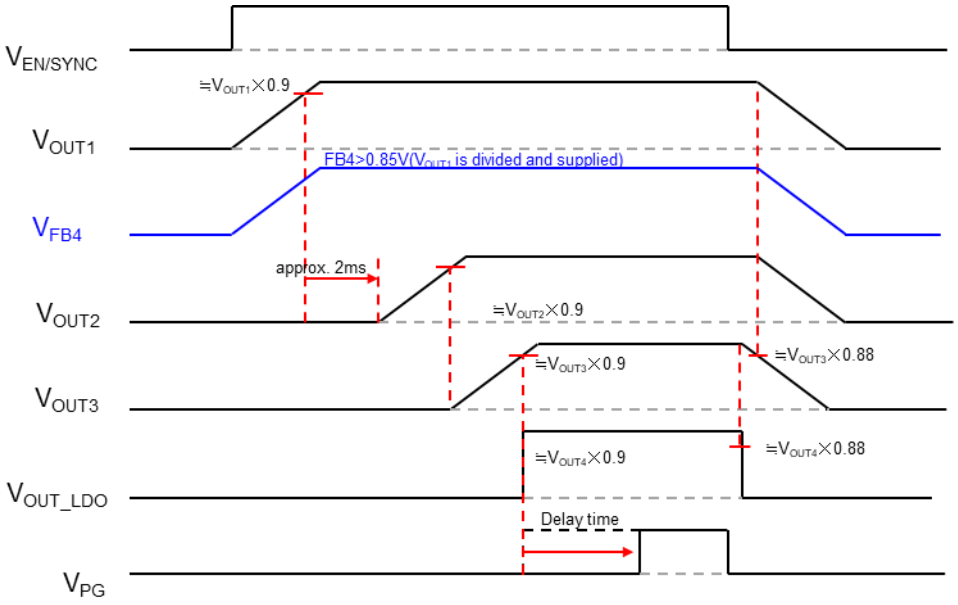


Fig.3 Example of timing chart for Ch.1~Ch.4 (when HS-SWITCH mode is selected)

● Setting of Unused Ch. in Sequence Control.

If the unused Ch. is included in the power on sequence, the FB pin of the unused Ch. can be set to the following voltage setting:

It is possible to disable the corresponding Ch and proceed to start the next Ch.

< FB pin settings for unused Ch>

FBx >0.85V during power on Ch.1 (V_{OUT1} is divided and supplied to FBx or supplied from an external power supply)

Application circuit examples and timing charts are below.

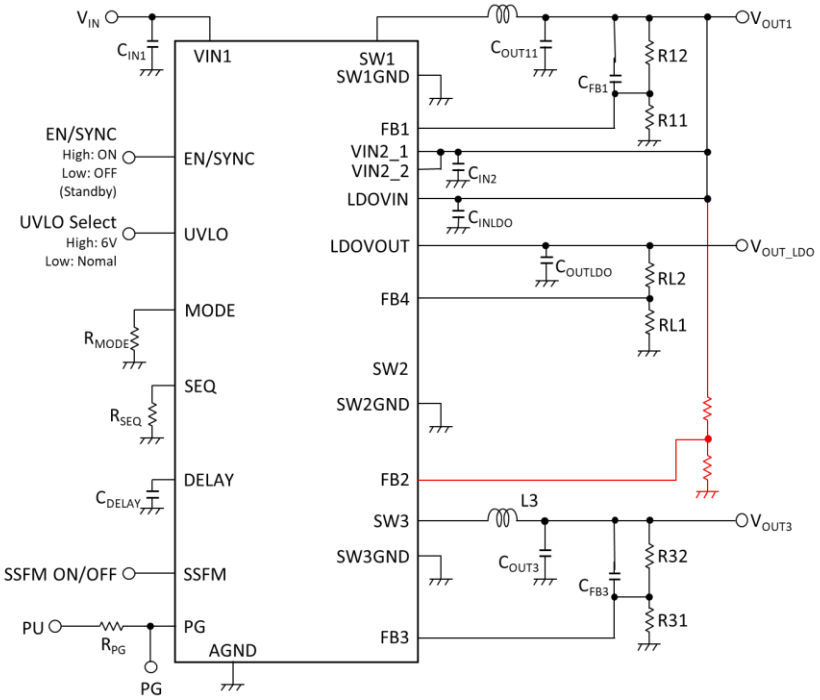


Fig.4 Application circuit example when Ch.2 is not used

■ DESCRIPTION OF BLOCK FEATURES (continued)

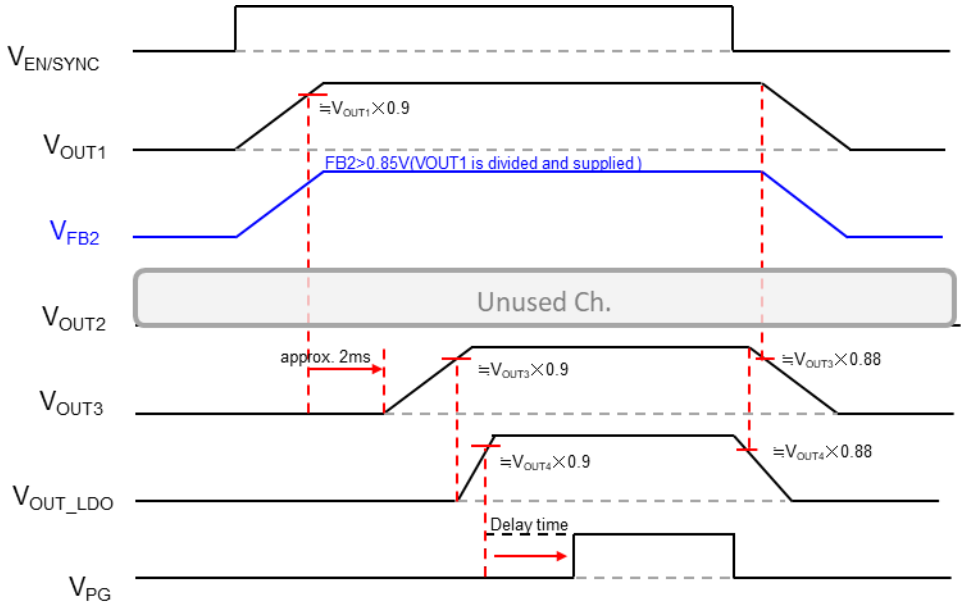


Fig. 5 Example of timing chart of Ch.1 to Ch.4 without Ch.2

3. Basic functions of switching regulators (Ch.1, 2 and Ch.3)

● Error Amplifier Section

0.6V±1% precise reference voltage is connected to the non-inverted input of this section.
The output voltage can be set by dividing the output of the converter and connecting to the inverted input (FB pin)

● Oscillator Circuit (OSC), PWM Comparator

NP8700 operates on a fixed-frequency current mode control scheme. The frequency is set to 2MHz typ.
The PWM comparator outputs a PWM signal via feedback of the output voltage and slope-compensated switching current.
The maximum duty ratio is set at 100% to minimize the potential difference between input and output.
There is a limit to the minimum ON and OFF time of the NP8700. See Electrical Characteristics.
The ON and OFF times are determined by the following formula:

$$t_{ON}=\frac{(V_{OUT}+V_{SWL})}{(V_{IN}-V_{SWH}+V_{SWL})\times f_{OSC}}\ [s] \qquad t_{OFF}=\frac{1}{f_{OSC}}-t_{ON}\ [s]$$

V_{IN}: Input Voltage
V_{OUT}: Output Voltage
V_{SWH}: High-Side Switched Saturation Voltage
V_{SWL}: Low-Side Switched Saturation Voltage

Please note that if the ON time is less than ton-min and the OFF time is less than toff-min, there may be a shift in duty or pulse skipping operation to keep the output voltage constant.

● Power MOSFETs

The power is stored in the inductor by the switch operation of built-in power MOSFET. The switching current is limited by the overcurrent protection.

● Power supply, GND pin (VIN, GND)

Current flows into the IC according to drive frequency in a switching element. When impedance of a power supply line is high, power supply will be unstably, and the performance of the IC can't be drawn out sufficiently. Therefore, since the impedance of the power supply path needs to be lowered, connecting a capacitor (CIN) near the IC pin between VIN1, VIN2_1/2, LDOVIN and GND is required.

■ DESCRIPTION OF BLOCK FEATURES (continued)

4. Switching Regulator Protection Function and Additional Functions (Ch.1,2 and Ch.3)

● Under voltage lockout (UVLO)

The UVLO circuit stops the IC operation in a low power supply voltage case, and when a power supply voltage becomes higher than threshold voltage, then the IC operation starts. The threshold voltage has a hysteresis voltage on rising and falling. Repeats of detection and release of UVLO is prevented by Hysteresis.

NP8700 is equipped with a function to switch the threshold voltage of UVLO to VIN1.

Table 3 shows the threshold settings for UVLO.

If the UVLO pin is at a low level (0.4 V or less) or open, the UVLO threshold voltage is set low, and if the high level (1 V or more) is a high threshold voltage.

Table 3 Threshold Voltage Settings for UVLO

V_{UVLO}	UVLO threshold voltage
0.4V or less or open	V_{T_ON1L}(TYP:3.75V) / V_{T_OFF1L}(TYP:3.20V)
1V or more	V_{T_ON1H}(TYP:5.80V) / V_{T_OFF1H}(TYP:5.25V)

● Soft Start Function

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 4ms (max.) and is defined as the time it takes for the FBx pin voltage to reach 0.55V. (Fig. 6)

Soft start of each Ch. functions under the following conditions:

Ch.1: The UVLO for Ch.1 is released and $V_{EN/SYNC} \geq V_{THH\_EN/SYNC}$

Ch.2: The UVLO for Ch.1 and Ch.2 is released.

Ch.3: The UVLO for Ch.1 and Ch.3 is released.

When recovering from overcurrent protection.

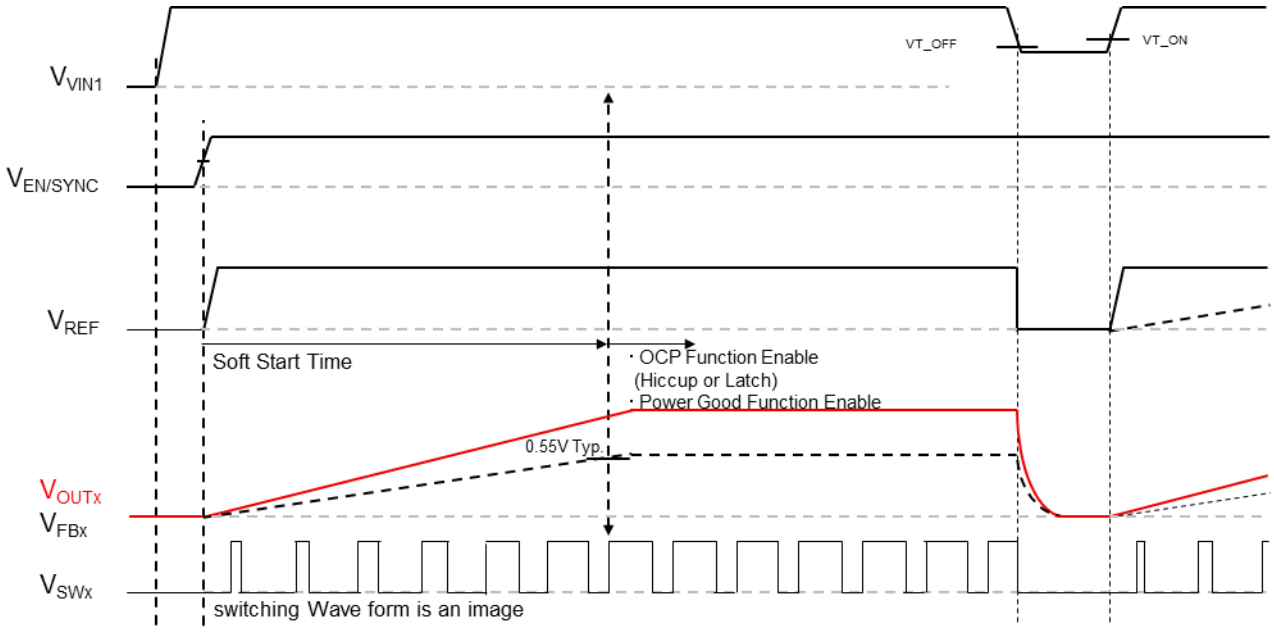


Figure 6 Soft Start Timing Chart

■ DESCRIPTION OF BLOCK FEATURES (continued)

● Over current Protection (OCP) (Ch.1,2 and Ch.3)

NP8700 switching regulator has two types selectable over current protections.

1. Hiccup method (Fig. 7):

   If an overcurrent is detected and the inductor current is limited for 1/fosc × 240 seconds, the corresponding Ch. is latched off.

   Alternatively, if the inductor current is limited and an overcurrent is detected for 7 consecutive cycles from VFB≦0.35V, the corresponding Ch. is latched off, too. After that, a restart is attempted every 115 ms, and if the load is smaller than the overcurrent detection value, NP8700 automatically recovers using a soft start.

2. Latch method (Fig. 8):

   If an overcurrent is detected and the inductor current is limited for 1/fosc × 240 seconds, all channels will be latched off. Alternatively, if the inductor current is limited and an overcurrent is detected for 7 consecutive cycles with VFB≦0.35V, the output of all channels will be stopped . The latch can be released by setting the EN/SYNC pin low or setting the VIN1 pin below the UVLO detection voltage.

*The Hiccup method is controlled independently for each Ch., and for the Latch method, all IC outputs are stopped.

If an overcurrent is detected during the soft start period (typ. 2.5 ms), the mode will not transition to hiccup/latch, and only the pulse-by-pulse inductor current limit will be activated. If the overcurrent continues even after the soft start period has ended, the mode will transition to hiccup/latch if the above conditions are met.

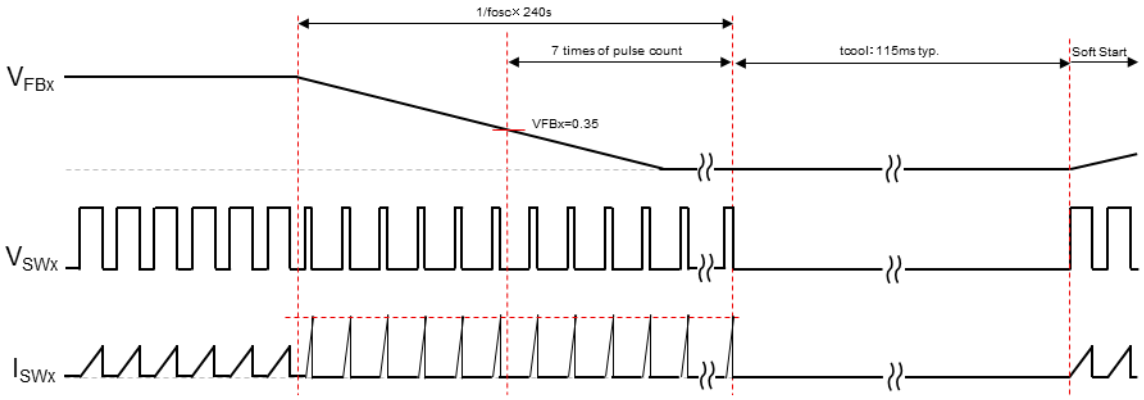


Fig.7 Hiccup mode overcurrent protection detection sequence

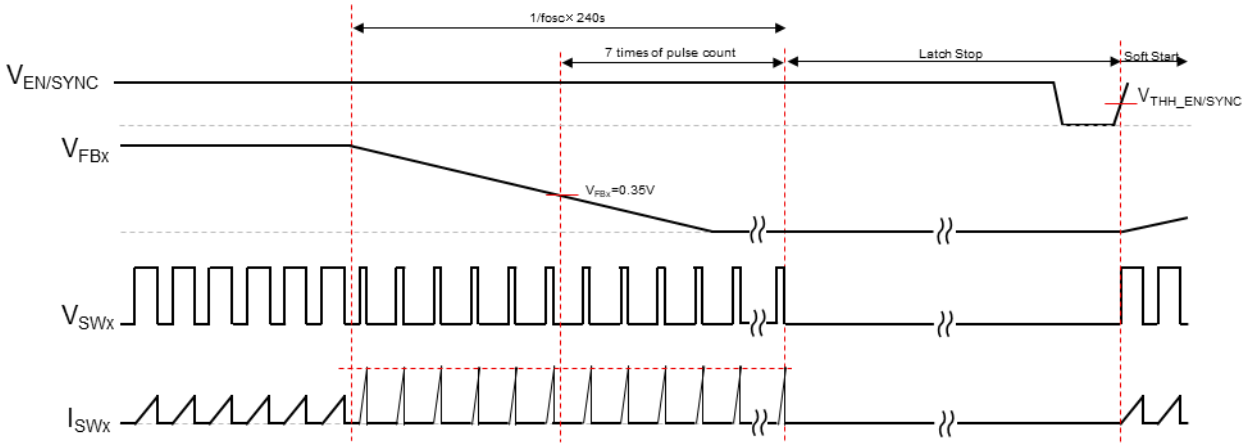


Fig.8 Latch mode overcurrent protection detection sequence

■ DESCRIPTION OF BLOCK FEATURES (continued)

● External clock synchronization (Ch.1,2 and Ch.3)

By inputting a square wave into the EN/SYNC pin, the oscillator of NP8700 can be synchronized to an external signal frequency.
The square wave must meet on the following specification.

Table 4 The input square wave to EN/SYNC pin

	Condition
Input Frequency	1.9 to 2.5MHz
Duty cycle	40% to 60%
Voltage amplitude	1.6V or more (High level) 0.4V or less (Low level)

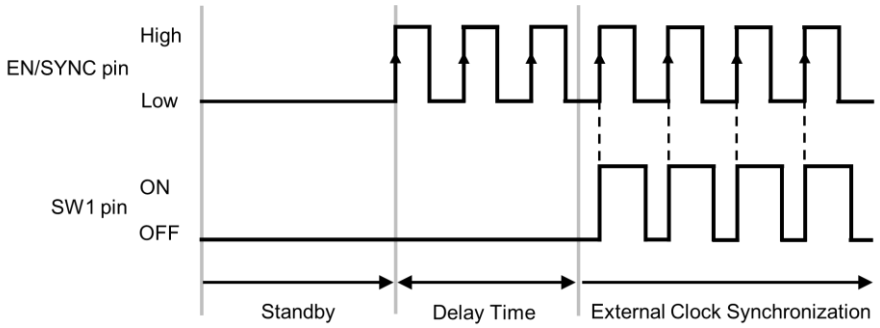


Fig. 9 Switching operation with external synchronization signal

● SSFM Function

To reduce conductive/radiated noise interference, SSFM (Spread Spectrum Frequency Modulation) is used during PWM operation.
SSFM reduces noise peaks at specific frequencies by spreading the oscillating frequency over a wide range.
NP8700's SSFM function can be enabled by setting the SSFM pin to the High level (1V or more). (Table 5)
As for the amount of change in the oscillating frequency it changes in a triangular wave shape in the range of ±5% (Typ.).
The modulation period will be 512/foscx.
However, when an external clock is applied, the SSFM function is disabled and the oscillating frequency is not modulated.

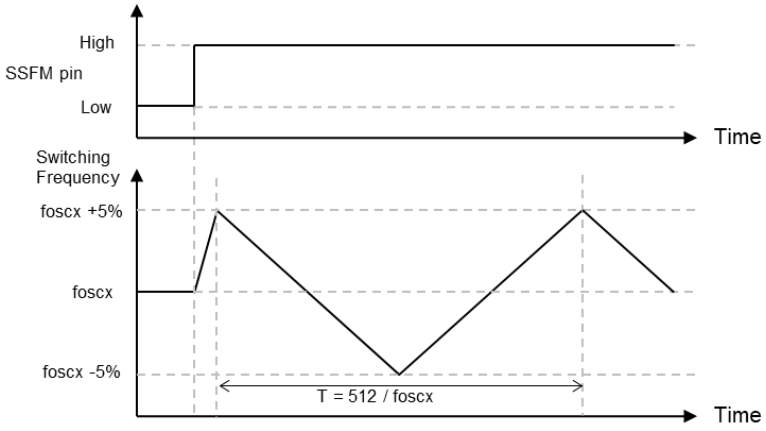


Fig.10 Fluctuation diagram of oscillating frequency by SSFM

Table 5 SSFM Function Settings

V_{SSFM}	SSFM Function
0.4V or less or open	invalid
1V or more	valid

■ DESCRIPTION OF BLOCK FEATURES (continued)

4. LDO Basic Functions (Ch.3LDO Mode, Ch.4)

● Error amplifier section (Error AMP)

0.6V±1% precise reference voltage is connected to the non-inverted input of this section.
The output voltage can be set by dividing the output of the converter and connecting to the inverted input (FB pin).

5. LDO protection function and additional function (Ch.3LDO mode, Ch.4)

● Overcurrent Protection (OCP)

NP8700 LDO has two types selectable over current protections by setting MODE pin.
1. Foldback method: Reduces the output current along with the drop in output voltage. When the load state returns to normal, it will automatically return.
2. Latch method: VFBx≦0.35V condition, stop functioning as a power supply.
Latch is released by setting all EN/SYNC pin to Low or VIN1 pin to 0V.
*The Foldback method controls each Ch. independently, and the Latch method stops all IC outputs.

● Soft Start Function

The soft-start function causes the LDO's output voltage to rise gently to the set voltage.
The soft start time is set at approximately 500 us, defined as the time it takes for the FBx pin voltage to reach 0.55 V.
Soft start works under the following conditions:
・Ch.3 (LDO Mode): When the Ch.1 UVLO is released, VVIN2_1,2 ≥ V_{T_ON3}, and Ch.3 starts up during sequence control.
・Ch.4: When the Ch.1 UVLO is released, and Ch.4 starts up during sequence control.
・When the overcurrent protection (latch) is released.

6. Common protection function, additional function

● Thermal Shutdown Function (TSD)

When junction temperature of the NP8700 exceeds the 160°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation re-start from the soft start operation. The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. Please make sure to operate within the junction temperature range rated (-40°C to 150°C). (* Reference value)

● Standby function

By setting the EN/SYNC pin to 0.4Vmax or less, it moves to a stop sequence and stops the function of each Ch. and puts it into a standby state.
Internally, it is pulled down with a resistor (5 MΩ) and is in standby mode when the EN/SYNC pin are open.
If you do not use the standby function, connect the EN/SYNC pin to the VIN1 pin.

■ DESCRIPTION OF BLOCK FEATURES (continued)

● Power Good Function

All Ch.monitors the output status and outputs a signal from the PG pin in an open-drain configuration.
When the FBx pin of all Ch. is within the range of ±10% of the error amplifier reference voltage, the PG pin will be high impedance, and when it is out of range, the PG pin will be at a low level, i.e. it will notify the status of whether the output voltage is normal or abnormal.
The all Ch. output state of the Low level is normal, and the delay time can be set externally when transitioning from the Low level to the High level.
The setting of the delay time is determined by the capacitance value of the C_{DELAY} connected to the DELAY pin. (Table 6)
The delay time is shortest when the circuit is open. The desired delay time can be calculated using the following formula.

Delay time [ms] = 200 × Cdelay [µF]

Table 6 Estimated DELAY pin Connection Capacitors and Delay Time

C_{DELAY}	0.01µF	0.1µF	1µF
Delay time	Approx. 2ms	Approx. 20ms	Approx. 200ms

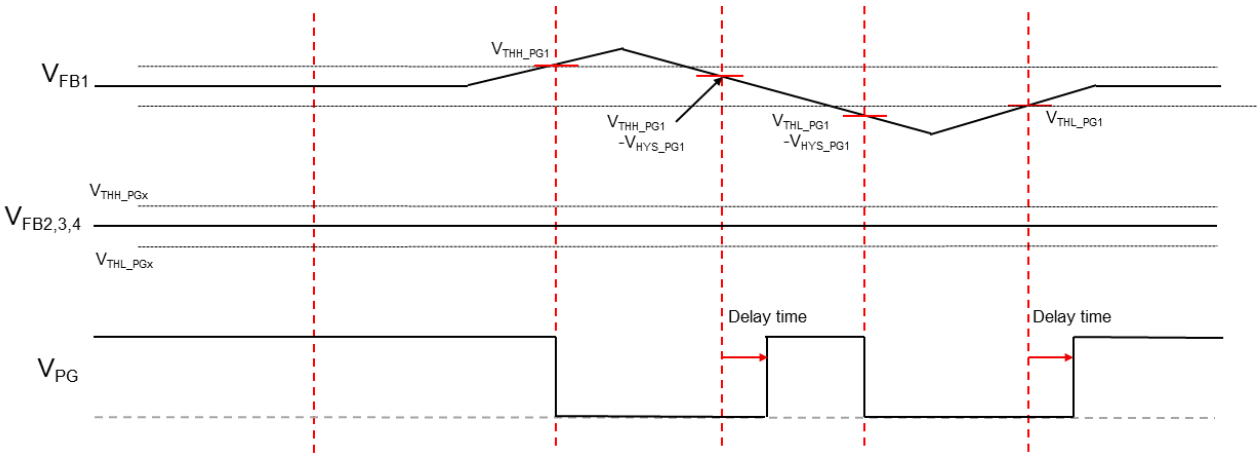
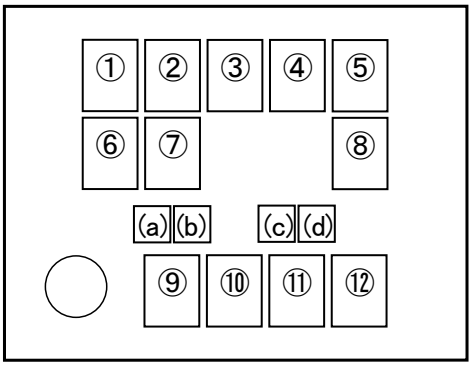


Fig. 11 Power Good in action

■ **Marking specification (QFN2634-26-NC)**

①②③④⑤⑥⑦: Product Code ⋯ Refer to Part Marking List
⑧⑨⑩⑪⑫, (a)(b)(c)(d): Lot Number ⋯ Alphanumeric Serial Number Lot Number



QFN2634-26-NC Marking Diagram

Notes
Package stamping may have differences in character recognition depending on the specifications of the image recognition device. If you wish to use an image recognition device to recognize characters, please contact our dealer or our sales representative in advance.

Part Marking List (QFN2634-26-NC)

Product Name	①	②	③	④	⑤	⑥	⑦
NP8700NCAE2P	P	8	7	0	0	A	P

■Application Information (Switching Regulators)

- Inductor (L)

  Since a large current flows into an inductor, please select an appropriate inductor such as not saturate in the application.
  The NP8700 has built-in phase compensation, and the recommended use range of the L value is determined by the following formula:

Ch.1 : $-0.116 \times V_{IN} + 0.341 \times V_{OUT} < L[\mu H] < 0.553 \times V_{IN} + 0.341 \times V_{OUT}$

Ch.2,3 : $-0.188 \times V_{IN} + 0.552 \times V_{OUT} < L[\mu H] < 0.895 \times V_{IN} + 0.552 \times V_{OUT}$

The maximum output current for the worst condition is determined by the following formula: The peak current is determined by the following formula:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times V_{IN}\times f_{OSC}} [A]$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2} [A]$$

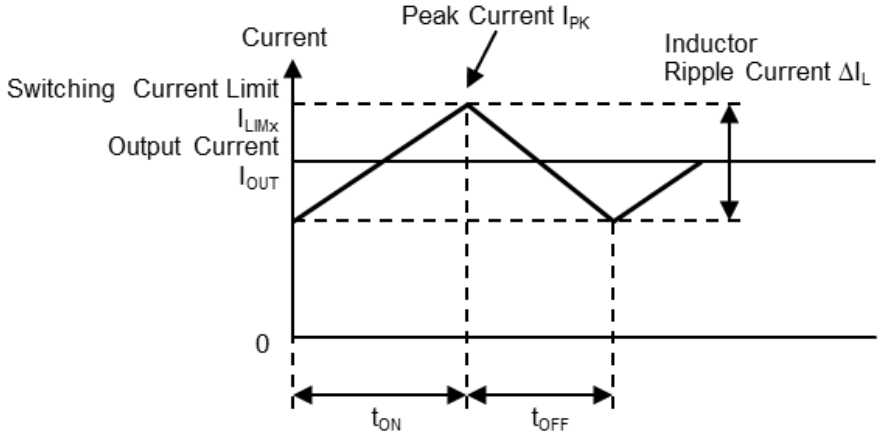


Fig.12 Inductor current state (current continuous mode operation)

- Input Capacitors (CIN)

  For the capacitance value of the input capacitor, refer to the parts list in the application example. Select a capacitor with a capacitance value equal to or greater than the effective value of the capacitor listed in the parts list.

  Transient currents flow through the input section of a switching regulator according to frequency. If the power supply impedance supplied to the power supply circuit is large, this will lead to input voltage fluctuations, preventing the NP8700 from fully utilizing its performance. Therefore, insert the input capacitor as close to the IC as possible.

  Ceramic capacitors are suitable for the NP8700's input capacitor, as they can suppress input ripple current. The input effective current (IRMS) can be calculated using the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}\times(V_{IN}-V_{OUT})}}{V_{IN}} [A_{rms}]$$

The above formula is maximized when VIN = 2× V_{OUT}, and the result at that time is $I_{RMS}=I_{OUT}$(MAX)÷2.

■ Application Information (Switching Regulators)

● Output Capacitors (C_{OUT})

The output capacitor stores power from the inductance and is responsible for stabilizing the supply voltage to the output.
The NP8700 has phase compensation set for use with low ESR output capacitors, and ceramic types are the best choice for output capacitors.
Table 7 shows the recommended values for output capacitors.

Table 7. Recommended Output Capacitors (effective value)

	Output Voltage	Output Capacitor: COUT
Ch.1	ALL	7μF to 18μF
Ch.2,3	0.8V to 2V	7μF to 18μF
	2V or more	4.2μF to 7μF

The selection of output capacitors must take into account the characteristics of ESR (Equivalent Series Resistance), ripple current, and withstand voltage.
Low ESR type capacitors can reduce ripple voltage. The output ripple voltage can be expressed by the following formula.

$$V_{ripple(p\text{-}p)} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right) [V]$$

The effective value (I_{RMS}) of ripple current flowing through a capacitor can be expressed by the following formula:

$$I_{RMS} = \frac{\Delta I_L}{2\sqrt{3}} [A_{rms}]$$

● Output Voltage Setting Resistor

The output voltage VOUT is determined by the resistance ratio of R1 and R2. (Fig. 13)

$$V_{OUT} = \left(\frac{R2}{R1} + 1 \right) \times V_B [V]$$

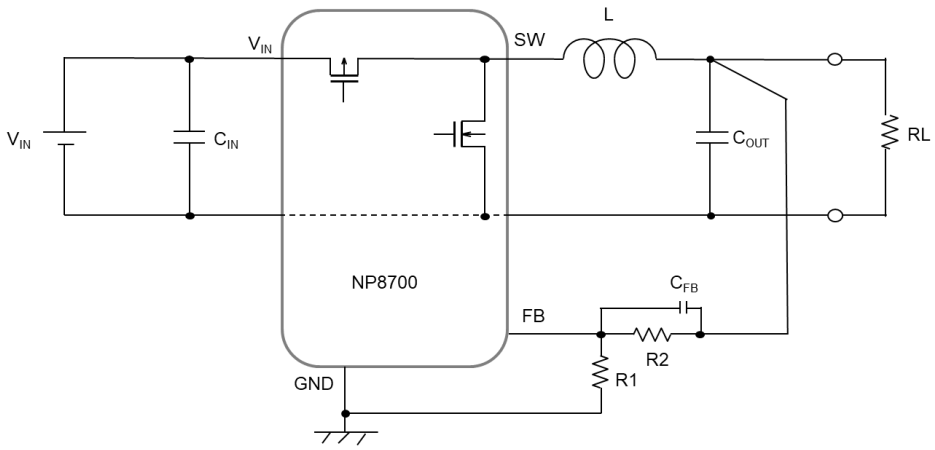


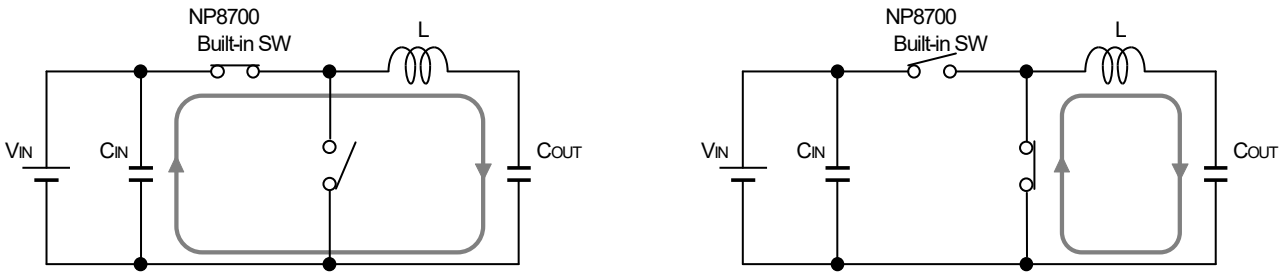
Fig.13 Output voltage setting

■ Application Information (Switching Regulators)

● Board layout

Switching regulators supply power to the output by charging and discharging an inductor. Because current flows according to the oscillating frequency, board layout is an important factor. Lines that carry large current should be kept short and the loop area minimized. Figure 14 shows the current loop in a step-down circuit.

In particular, reducing the loop length of C_{IN} - Hi-side SW - Low-side SW - GND, which involves fast current changes during switching, is effective in reducing spike noise generated by parasitic inductors, so C_{IN} should be mounted as close to the IC as possible.



(a) Buck circuit SW ON state (b) Buck circuit SW OFF state

Fig.14 Current loop in a step-down circuit

It is desirable to have a separate layout of the power and signal systems for the ground line and to connect them at a point where the current on the ground line is less affected.

Also, keep the voltage sense feedback line as far away from the inductor as possible. This line has a high impedance, so it is routed to avoid the effects of noise caused by the leakage magnetic flux from the inductor.

Figure 15 shows the wiring precautions for step-down circuits.

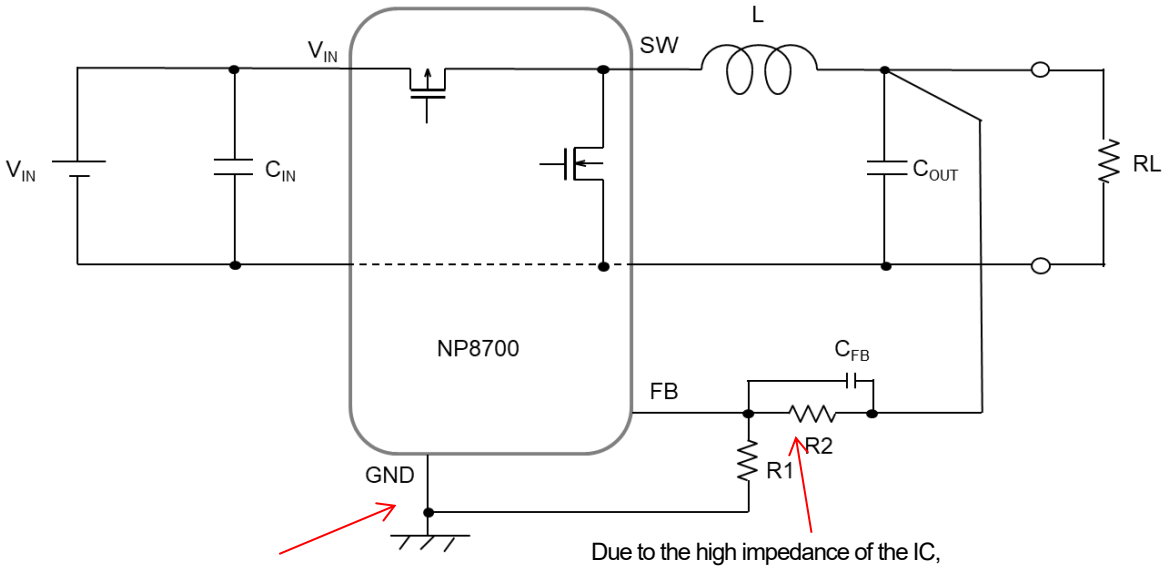


Fig.15 Wiring precautions

CFB is a circuit for phase compensation, but in most cases it is not necessary.
Measure the forwarding capability of the open loop and use CFB to compensate for the phase if the phase margin is insufficient. Configure CFB to have fz between 20 kHz and 30 kHz.

$$f_Z = \frac{1}{2 \times \Pi \times R2 \times C_{FB}} \text{ [Hz]}$$

■Application Information (LDO)

- Output Voltage Setting Resistor

The output voltage VOUT is determined by the resistance ratio of R1 and R2. (Fig. 16)

$$V_{OUT} = \left(\frac{R2}{R1} + 1\right) \times V_B \text{[V]}$$

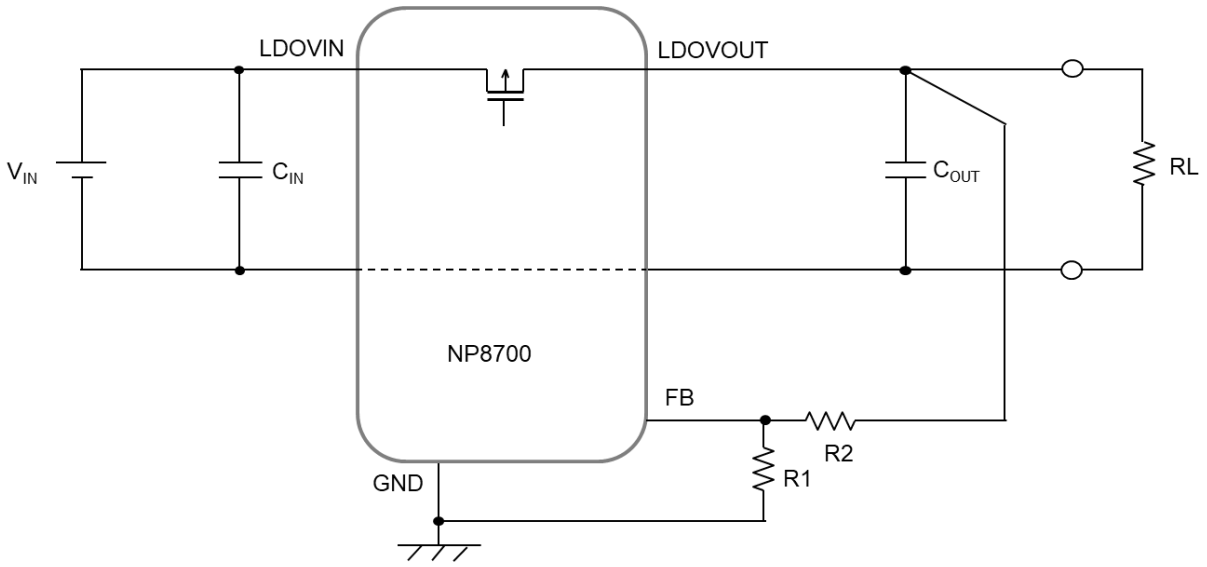


Fig. 16 Output voltage setting (LDO)

- Selection of phase compensation constants.

The NP8700 has a built-in phase compensation circuit, and the external component constants are shown in Table 8, regardless of the output voltage.

Table 8 Phase compensation constants

VOUT	COUT(Ceramic capacitor effective value)	R2
ALL	5μF to 18μF	47kΩ to 68kΩ

■ Calculating Package Power

The loss of the NP8700 is the total loss of all channels..

- In general, the loss of a switching converter and LDO can be calculated as follows:

  Input Power : $P_{IN} = V_{IN} \times I_{IN}$ [W]
  Output power : $P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
  Power consumption : $P_{LOSS} = P_{IN} - P_{OUT}$ [W]

  V_{IN} : Input voltage I_{IN} : Input current
  V_{OUT} : Output voltage I_{OUT}: Output current

  The NP8700's output power can be calculated as the sum of the losses for each channel (VIN2_1 and VIN2_2 are connected to VOUT1):
  $P_{IN} = V_{IN1} \times I_{IN1}$ [W]
  $P_{OUT} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3} + V_{OUT\_LDO} \times I_{OUT\_LDO}$ [W]

  Consider temperature derating for the calculated power consumption PLoss.
  Refer to the "Power Dissipation vs. Ambient Temperature" curve example to confirm that the power dissipation is within the rated limits.

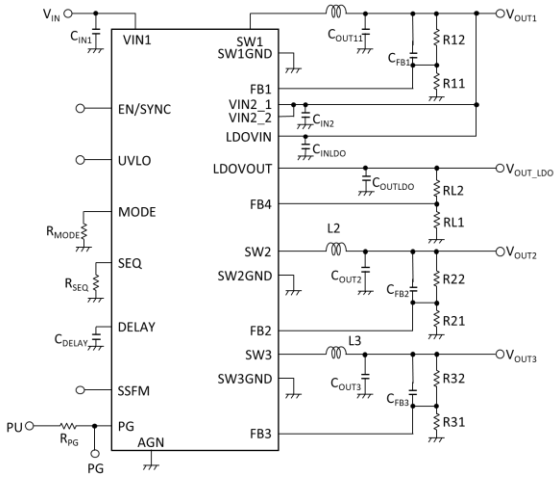
  The conversion efficiency is η determined by the following formula:
  $\eta = (P_{OUT} \div P_{IN}) \times 100$ [%]

  To obtain accurate conversion efficiency, measure the voltage closest to the VIN1 pin for VIN1, and measure the voltage closest to the output capacitor for VOUT1, 2, 3, and VOUT_LDO, and also measure the current value.

■Application examples

output: 3.3V (Ch.1)、1.8V (Ch.2)、1.2V (Ch.3)、2.8V (Ch.4)、 Oscillating Frequency: 2.0MHz

Schematic

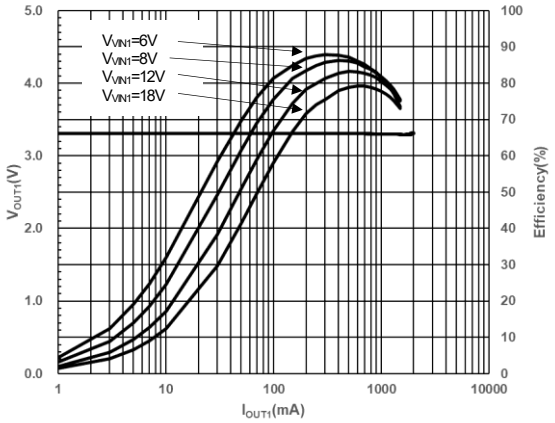


■ Parts List

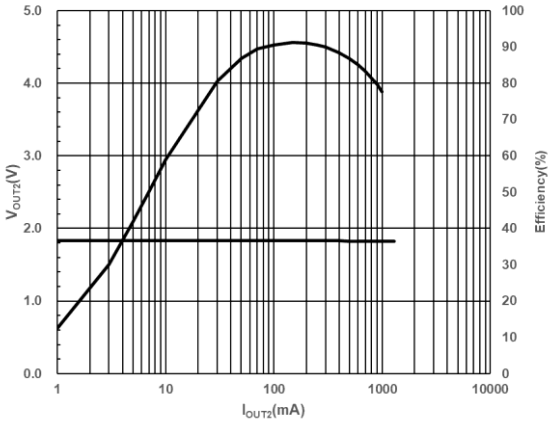
Ref.	Part number	Overview	Manufacture
C_{IN11}	GRM32ER71H106MA12L	Ceramic Capacitor 3225 10μF, 50V	MURATA
C_{IN12}	GRM21BB11H104KA01L	Ceramic Capacitor 2125 0.1μF, 50V	MURATA
C_{OUT11}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
L1	CLF6045NIT2R2	inductor 2.2μH,4.1A	TDK
R11	15kΩ	Resistor 1608 15kΩ, ±1%, 0.1W	Std.
R12	68kΩ	Resistor 1608 68kΩ, ±1%, 0.1W	Std.
C_{FB1}	N/A	N/A	N/A
C_{IN21}	GRM21BB11H104KA01L	Ceramic Capacitor 2125 0.1μF, 50V	MURATA
C_{IN22}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
C_{OUT2}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
L2	CLF6045NIT2R2	inductor 2.2μH,4.1A	TDK
R21	33kΩ	Resistor 1608 33kΩ, ±1%, 0.1W	Std.
R22	68kΩ	Resistor 1608 68kΩ, ±1%, 0.1W	Std.
C_{FB2}	N/A	N/A	N/A
C_{OUT3}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
L3	CLF6045NIT2R2	inductor 2.2μH,4.1A	TDK
R31	47kΩ	Resistor 1608 47kΩ, ±1%, 0.1W	Std.
R32	47kΩ	Resistor 1608 47kΩ, ±1%, 0.1W	Std.
C_{FB3}	N/A	N/A	N/A
C_{INLDO}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
C_{OUTLDO}	GCM32ER71E106KA57L	Ceramic Capacitor 3225 10μF, 25V	MURATA
RL1	15kΩ	Resistor 1608 15kΩ, ±1%, 0.1W	Std.
RL2	56kΩ	Resistor 1608 56kΩ, ±1%, 0.1W	Std.
R_{SEQ}	N/A	N/A	N/A
R_{MODE}	33kΩ	Resistor 1608 33kΩ, ±1%, 0.1W	Std.
C_{DELAY}	N/A	N/A	N/A
R_{PG}	10kΩ	Resistor 1608 10kΩ, ±1%, 0.1W	Std.

■APPLICATION CHARACTERISTICS

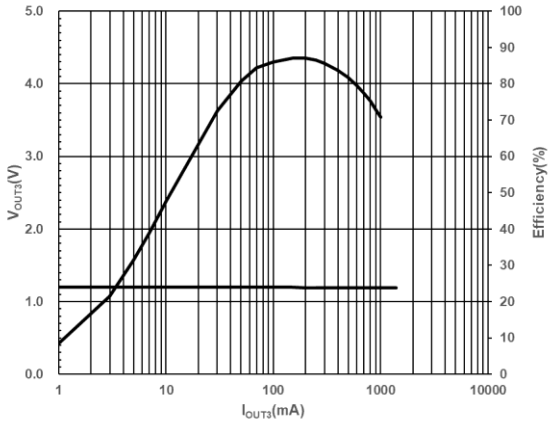
NP8700 Ch.1
Output Voltage, efficiency vs. Output current



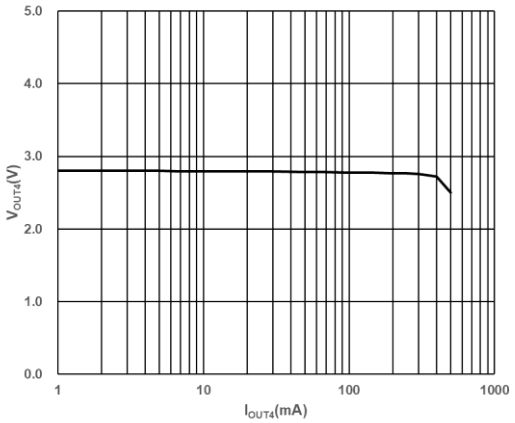
NP8700 Ch.2
Output Voltage, efficiency vs. Output current
$V_{VIN2\_1/2}$=3.3V



NP8700 Ch.3
Output Voltage, efficiency vs. Output current
$V_{VIN2\_1/2}$=3.3V

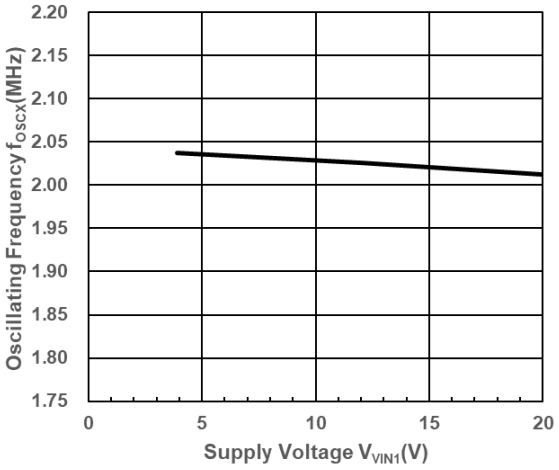


NP8700 Ch.4
Output Voltage vs. Output current
V_{LDOVIN}=3.3V

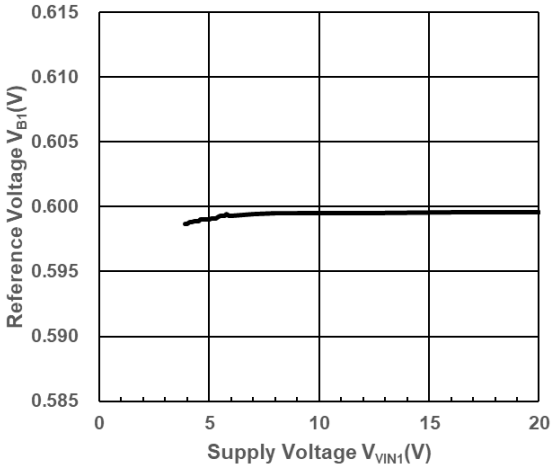


■APPLICATION CHARACTERISTICS

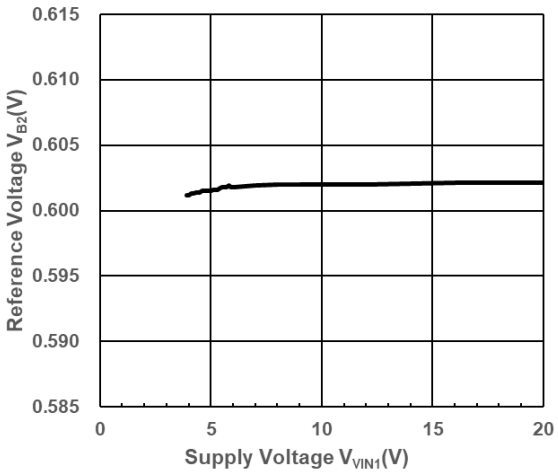
Oscillating Frequency vs. Supply Voltage
Ta=25℃



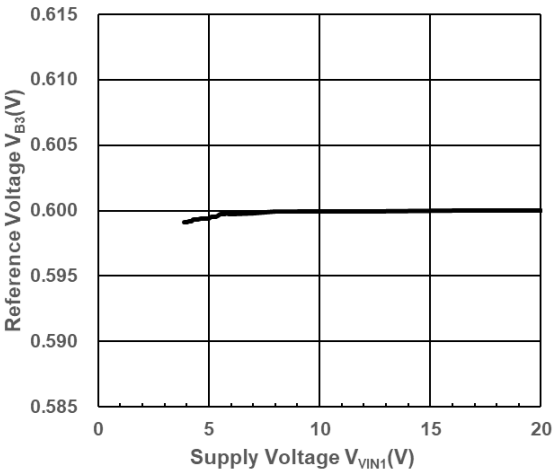
Ch.1 Reference Voltage vs. Supply Voltage
Ta=25℃



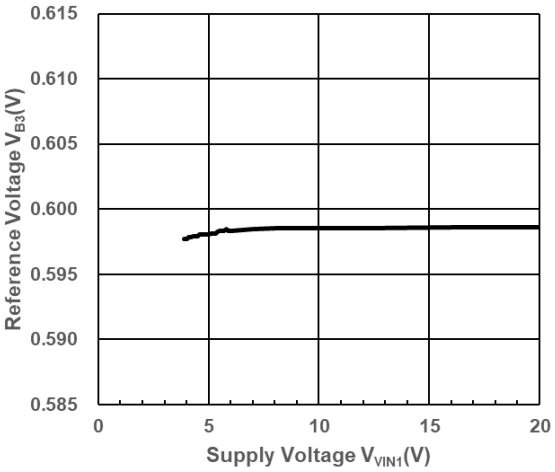
Ch.2 Reference Voltage vs. Supply Voltage
Ta=25℃



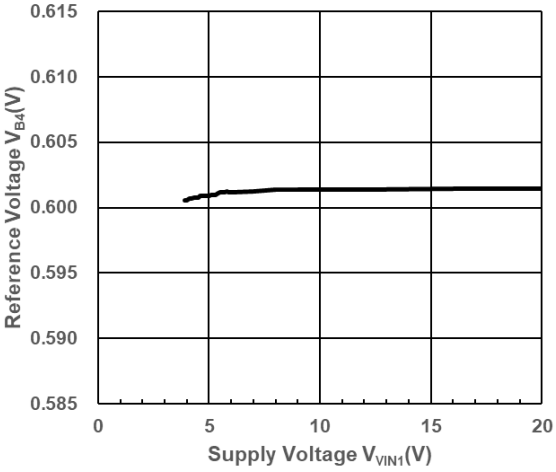
Ch.3 Reference Voltage vs. Supply Voltage
Ta=25℃



Ch.3 Reference Voltage vs. Supply Voltage
Ta=25℃, R_{MODE}=10kΩ,
V_O=1.8V(R1=33kΩ, R2=68kΩ)

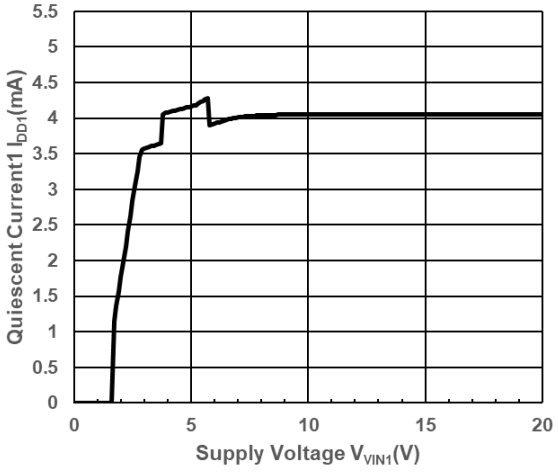


Ch.4 Reference Voltage vs. Supply Voltage
Ta=25℃,Vo=1.8V(R1=33kΩ, R2=68kΩ)

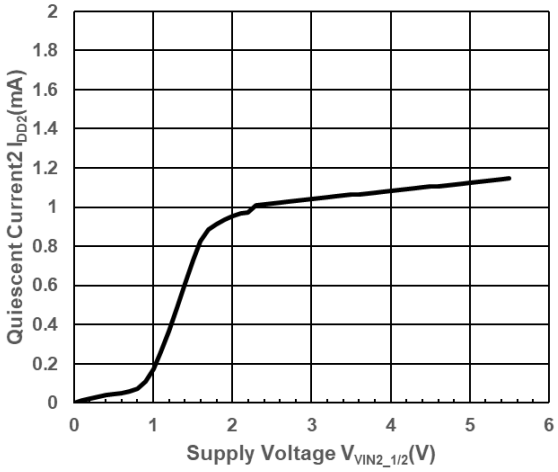


■APPLICATION CHARACTERISTICS

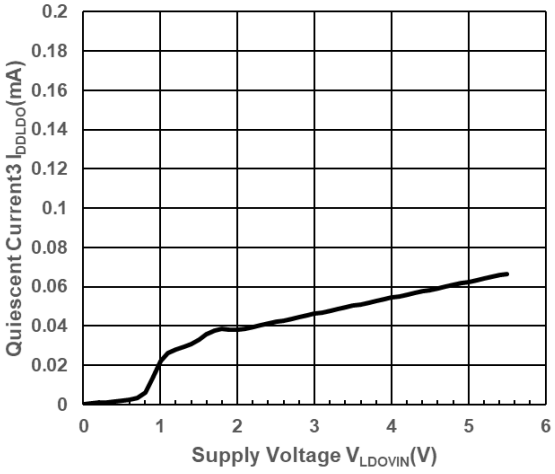
Quiescent Current1 vs. Supply Voltage
R_L=No Load, V_{FB1}=0.9V



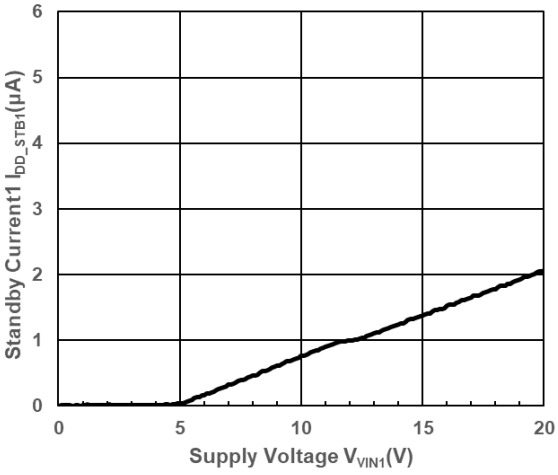
Quiescent Current2 vs. Supply Voltage
R_L=No Load, V_{FB2}=V_{FB3}=0.9V



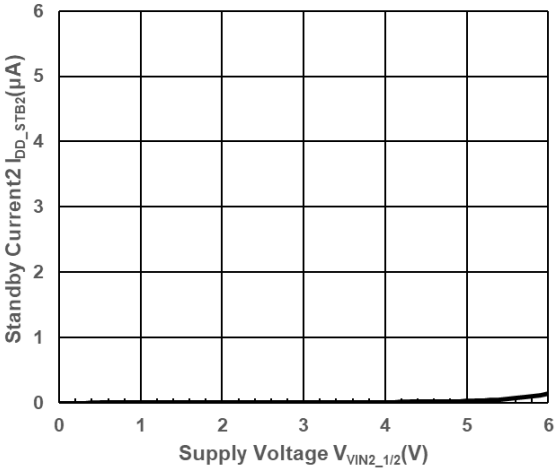
Quiescent Current3 vs. Supply Voltage
R_L=No Load, V_{FB4}=0.9V



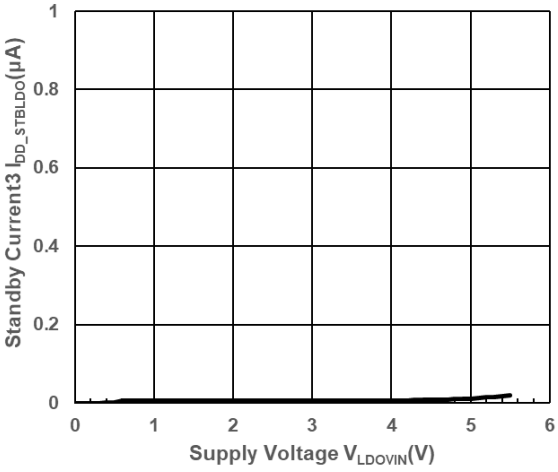
Standby Current1 vs. Supply Voltage
$V_{EN/SYNC}$=0V



Standby Current2 vs. Supply Voltage
$V_{EN/SYNC}$=0V

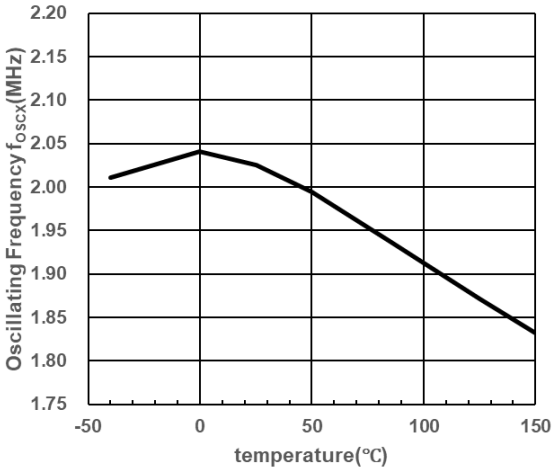


Standby Current3 vs. Supply Voltage
$V_{EN/SYNC}$=0V

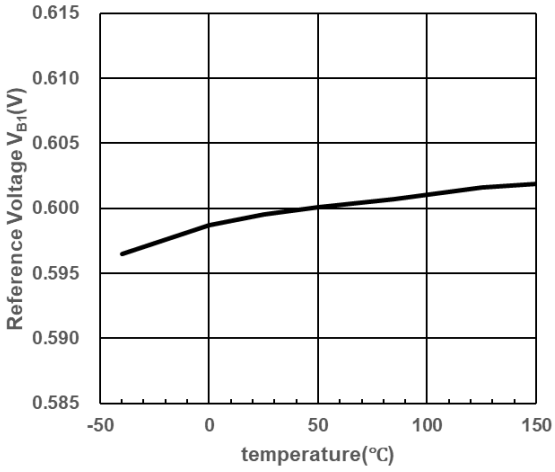


■APPLICATION CHARACTERISTICS

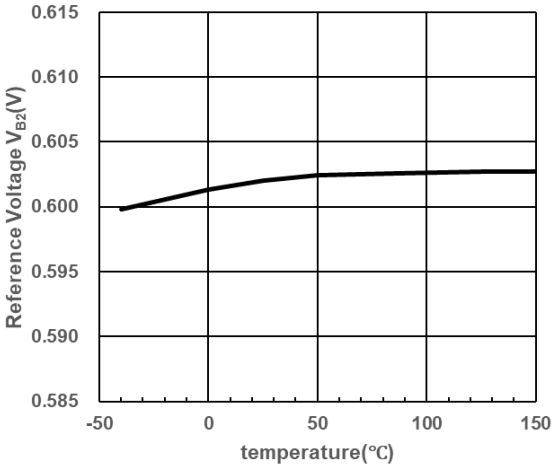
Oscillating Frequency vs. Temperature
V_{VIN1}=12V



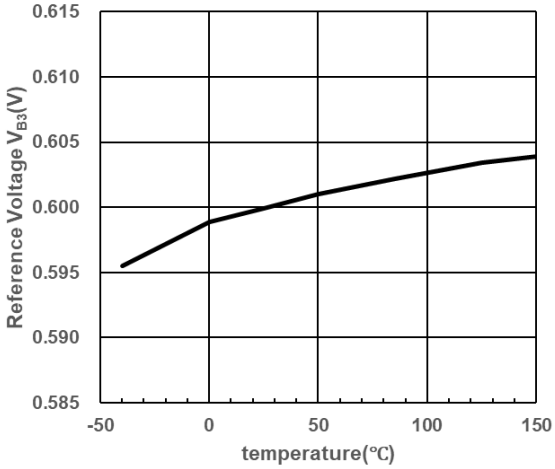
Ch.1 Reference Voltage vs. Temperature
V_{VIN1}=12V



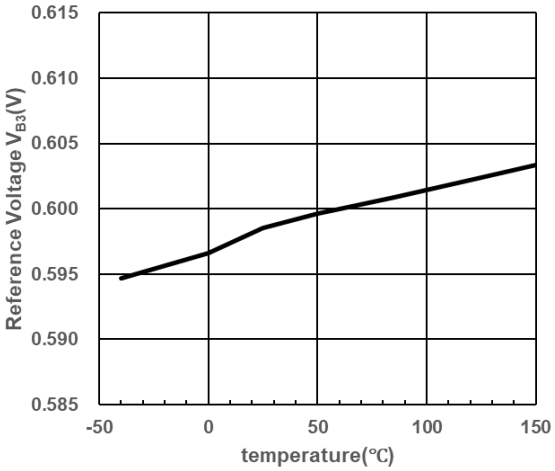
Ch.2 Reference Voltage vs. Temperature
V_{VIN1}=12V



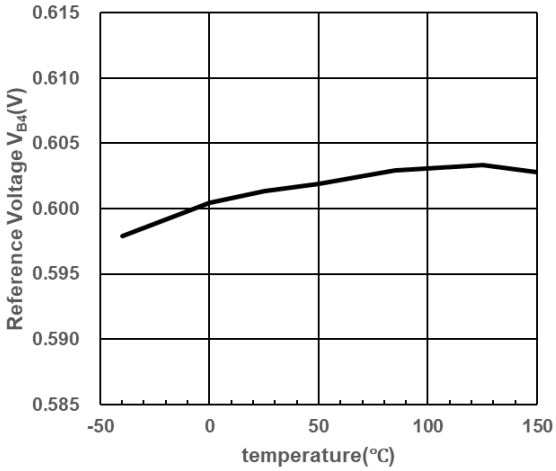
Ch.3 Reference Voltage vs. Temperature
V_{VIN1}=12V , R_{MODE}=33kΩ



Ch.3 Reference Voltage vs. Temperature
V_{VIN1}=12V , R_{MODE}=10kΩ

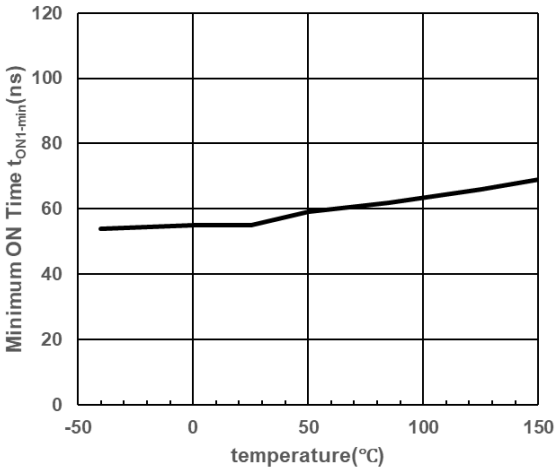


Ch.4 Reference Voltage vs. Temperature
V_{VIN1}=12V

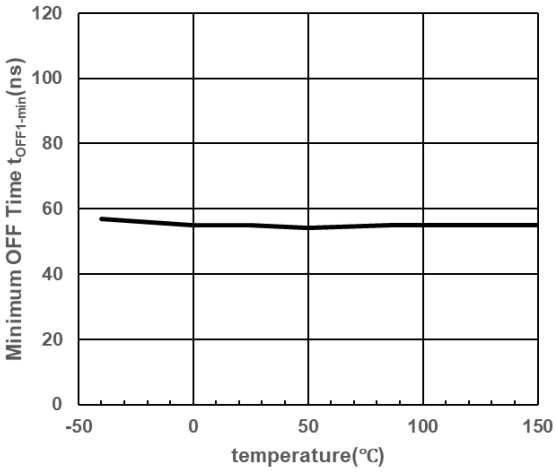


■APPLICATION CHARACTERISTICS

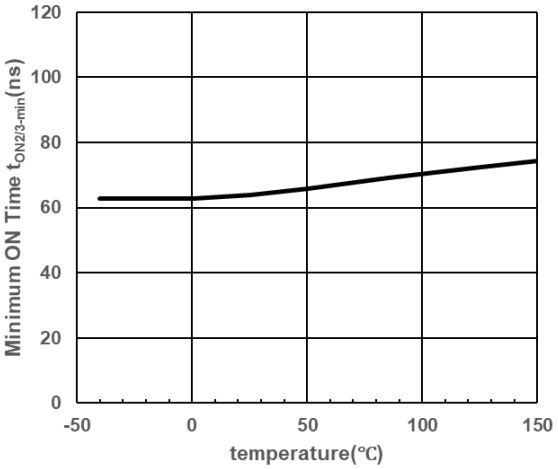
Ch.1 Minimum ON Time vs. Temperature
V_{VIN1}=12V



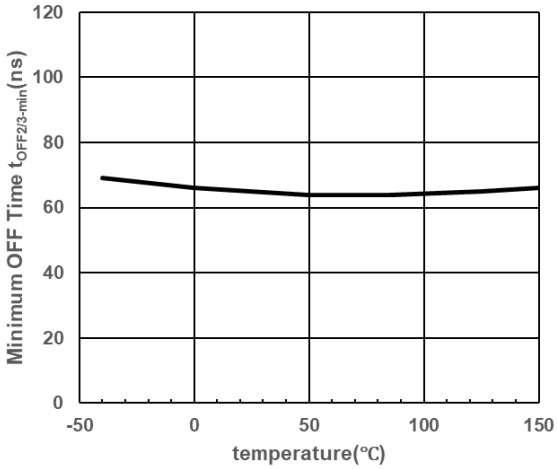
Ch.1 Minimum OFF Time vs. Temperature
V_{VIN1}=12V



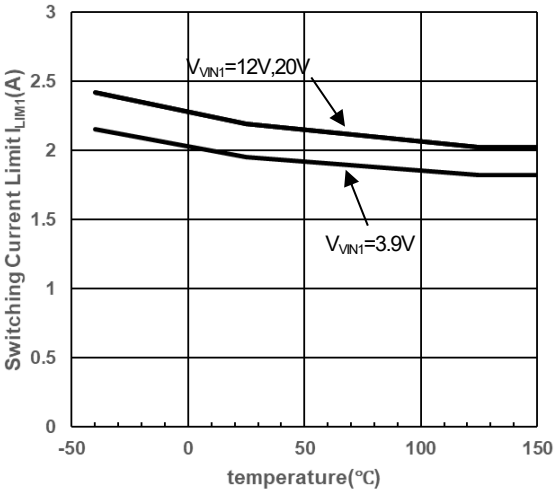
Ch.2/3 Minimum ON Time vs. Temperature
$V_{VIN2\_1/2}$=3.3V



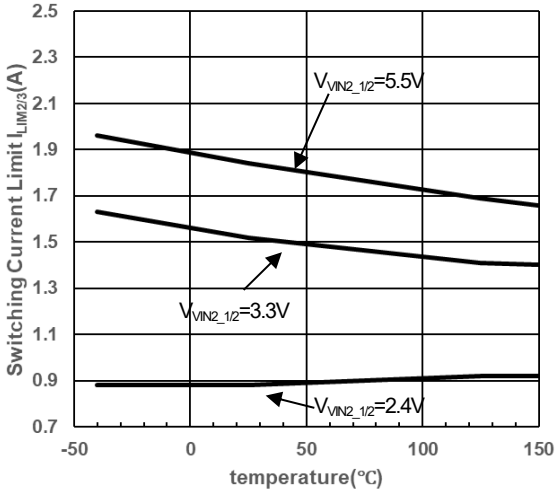
Ch.2/3 Minimum OFF Time vs. Temperature
$V_{VIN2\_1/2}$=3.3V



Ch.1 Switching Current Limit vs. Temperature

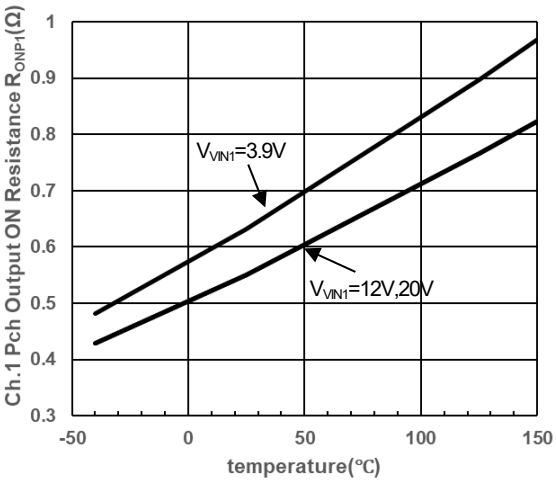


Ch.2/3 Switching Current Limit vs. Temperature

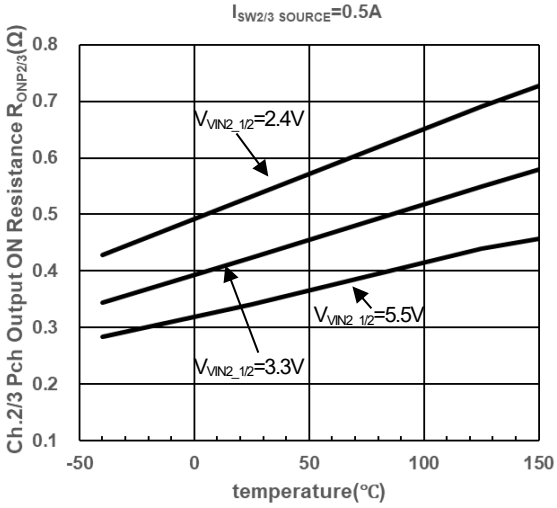


■APPLICATION CHARACTERISTICS

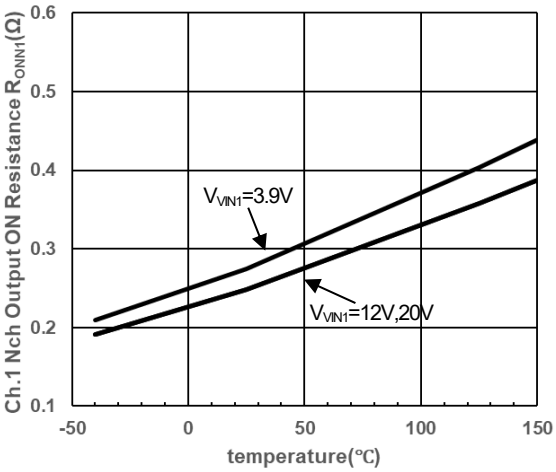
Ch.1 Pch Output ON Resistance vs. Temperature
$I_{SW1\ SOURCE}$=0.8A



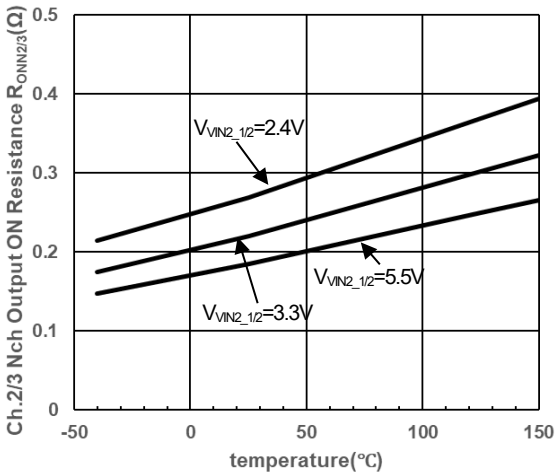
Ch.2/3 Pch Output ON Resistance vs. Temperature
$I_{SW2/3\ SOURCE}$=0.5A



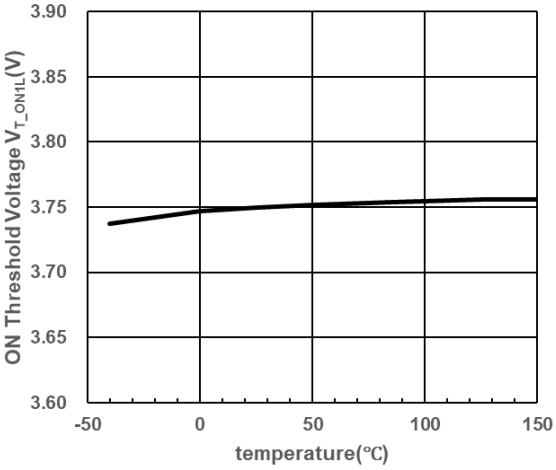
Ch.1 Nch Output ON Resistance vs. Temperature
$I_{SW1\ SINK}$=0.8A



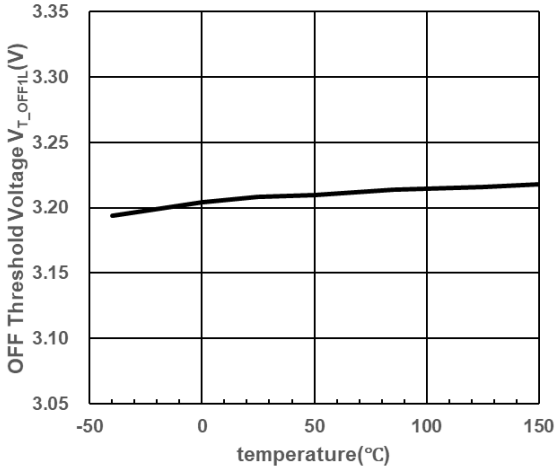
Ch.2/3 Nch Output ON Resistance vs. Temperature
$I_{SW2/3\ SINK}$=0.5A



Ch.1 ON Threshold Voltage vs. Temperature
V_{VIN1}=L → H

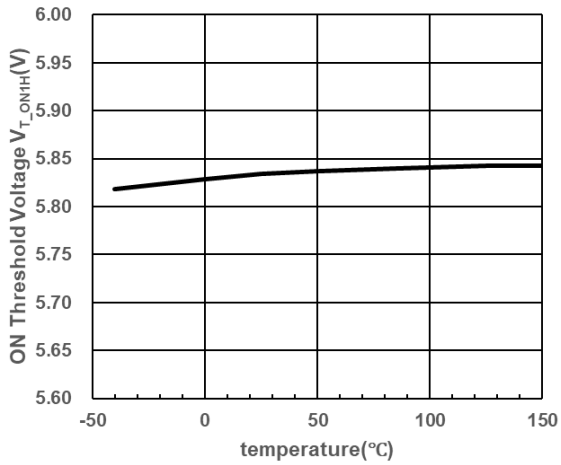


Ch.1 OFF Threshold Voltage vs. Temperature
V_{VIN1}=H → L

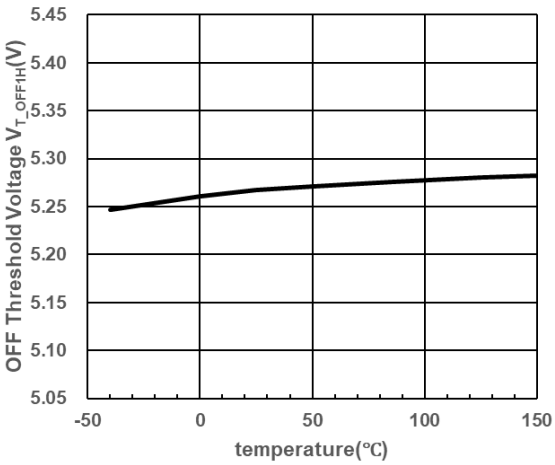


■APPLICATION CHARACTERISTICS

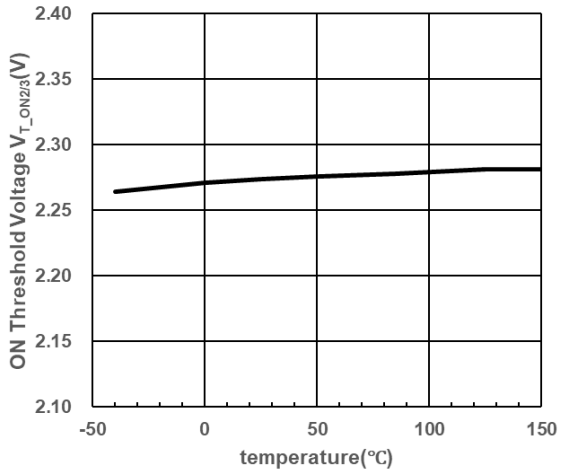
Ch.1 ON Threshold Voltage vs. Temperature
V_{VIN1}=L → H , V_{UVLO}=H



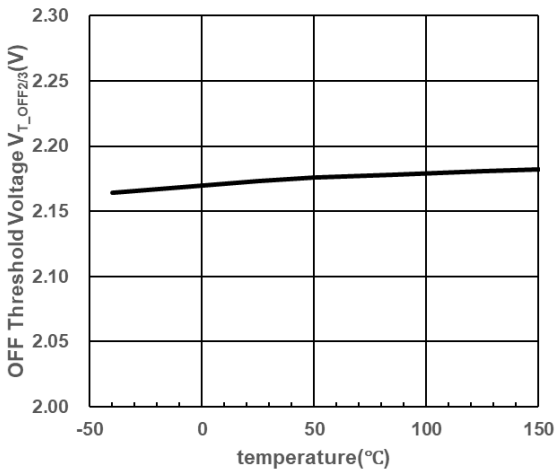
Ch.1 OFF Threshold Voltage vs. Temperature
V_{VIN1}=H → L , V_{UVLO}=H



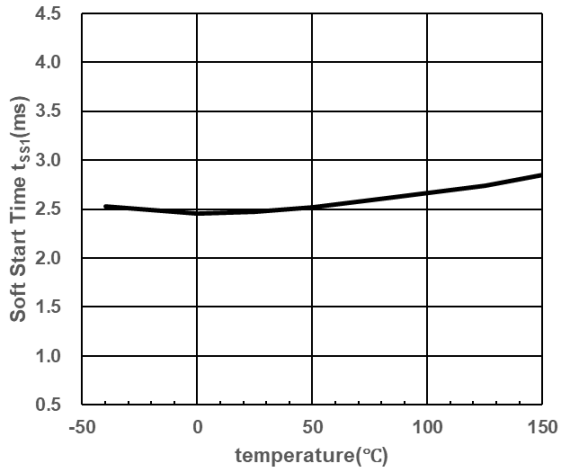
Ch.2/3 ON Threshold Voltage vs. Temperature
$V_{VIN2\_1/2}$=L → H



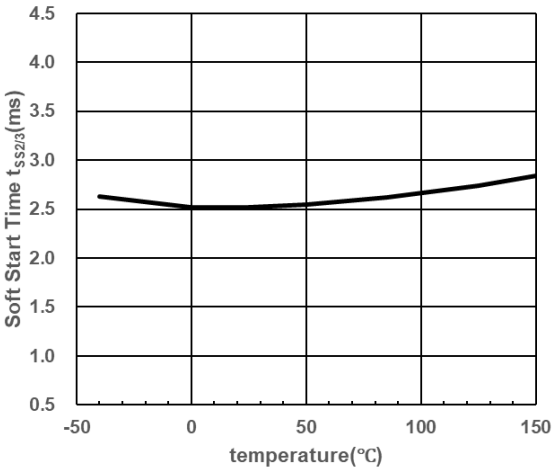
Ch.2/3 OFF Threshold Voltage vs. Temperature
$V_{VIN2\_1/2}$=H → L



Ch.1 Soft Start Time vs. Temperature
V_{FB1}=0.55V

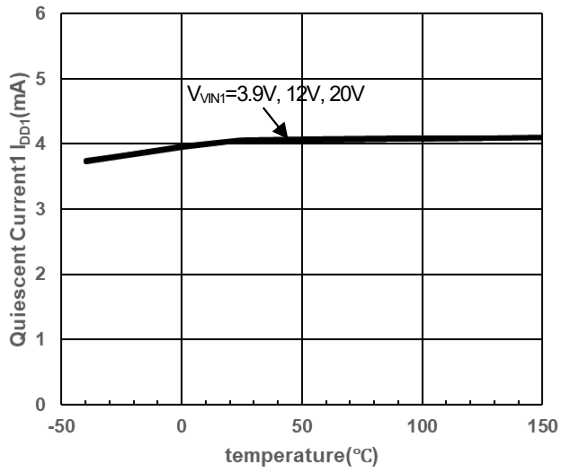


Ch.2/3 Soft Start Time vs. Temperature
$V_{FB2/3}$=0.55V

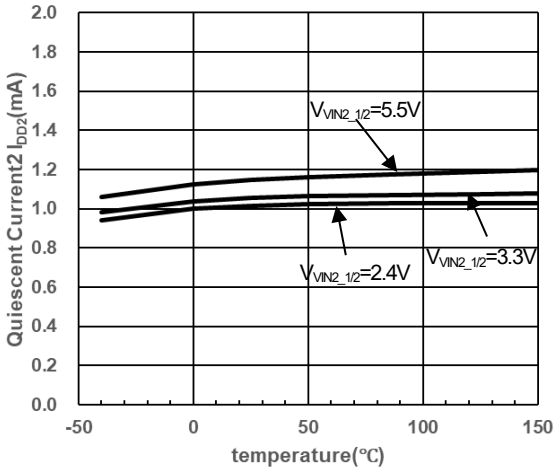


■APPLICATION CHARACTERISTICS

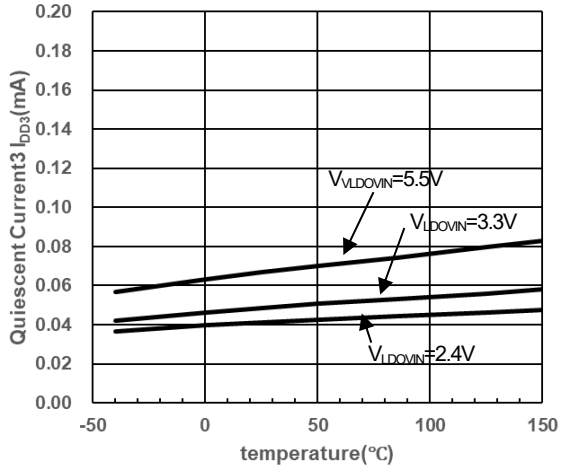
Quiescent Current1 vs. Temperature
R_L=No Load, V_{FB1}=0.9V



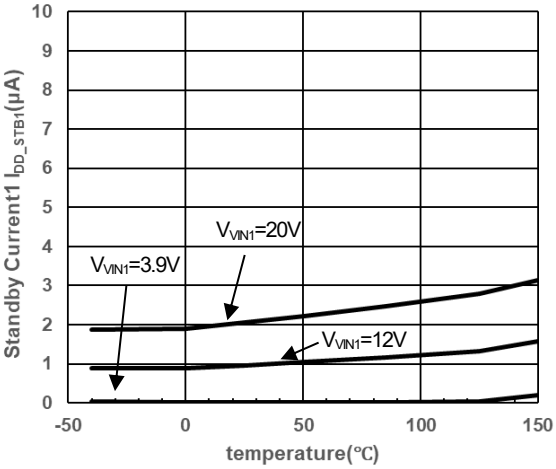
Quiescent Current2 vs. Temperature
R_L=No Load, V_{FB2}=0.9V, V_{FB3}=0.9V



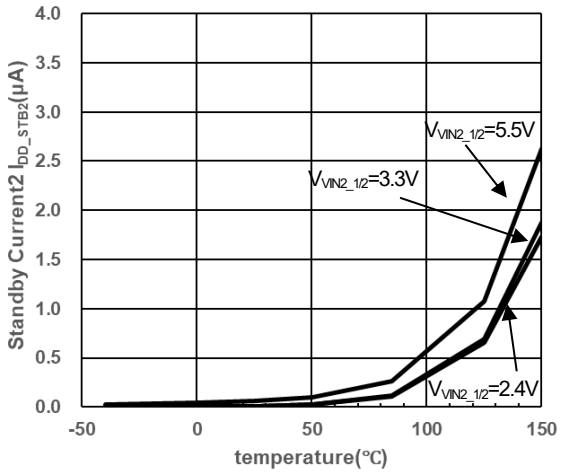
Quiescent Current3 vs. Temperature
R_L=No Load, V_{FB4}=0.9V



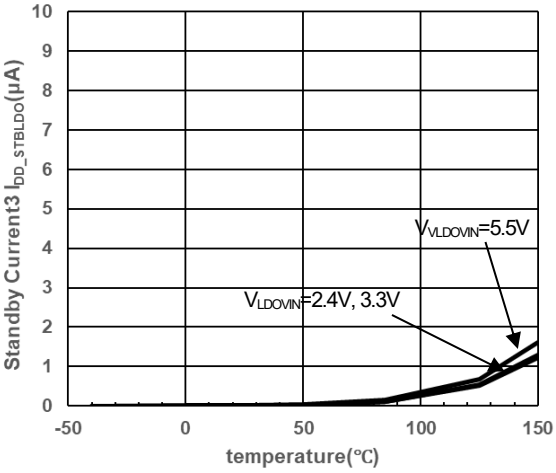
Standby Current1 vs. Temperature
$V_{EN/SYNC}$=0V



Standby Current2 vs. Temperature
$V_{EN/SYNC}$=0V

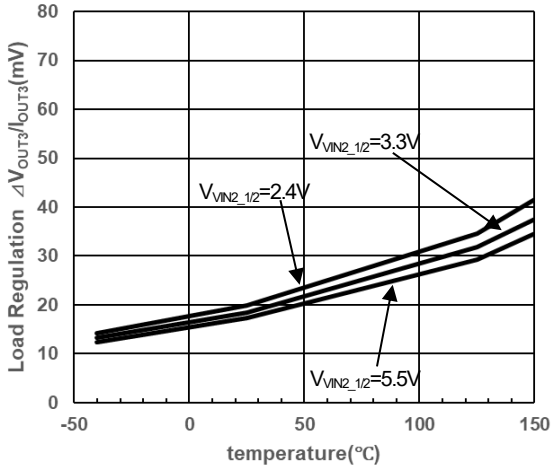


Standby Current3 vs. Temperature
$V_{EN/SYNC}$=0V

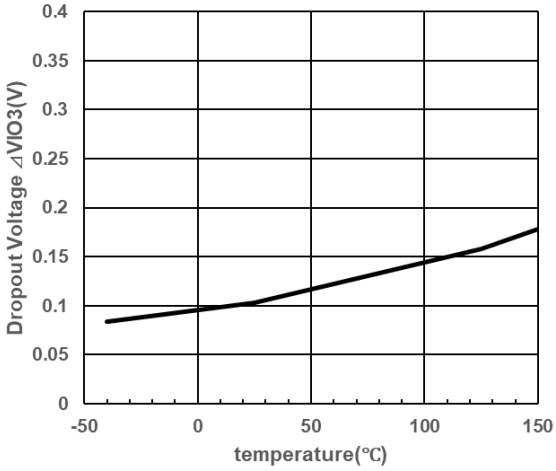


■APPLICATION CHARACTERISTICS (LDO)

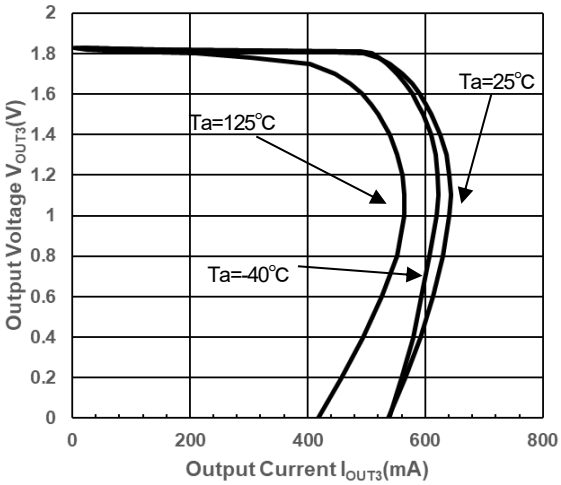
Ch.3 Load Regulation vs. Temperature
I_{OUT3}=1mA to 150mA, R_{MODE}=Open or 10kΩ



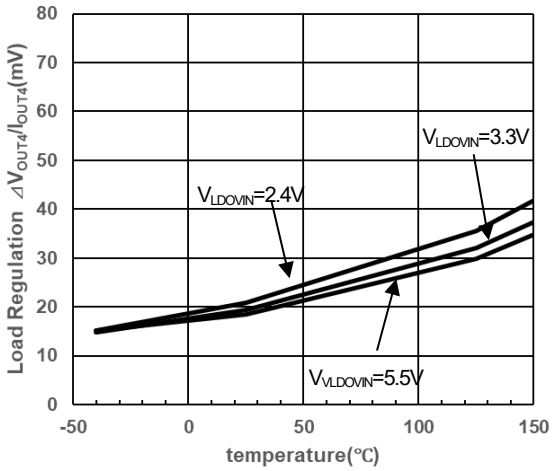
Ch.3 Dropout Voltage vs. Temperature
$V_{VIN2\_1/2}$=3.3V, I_{OUT3}=150mA



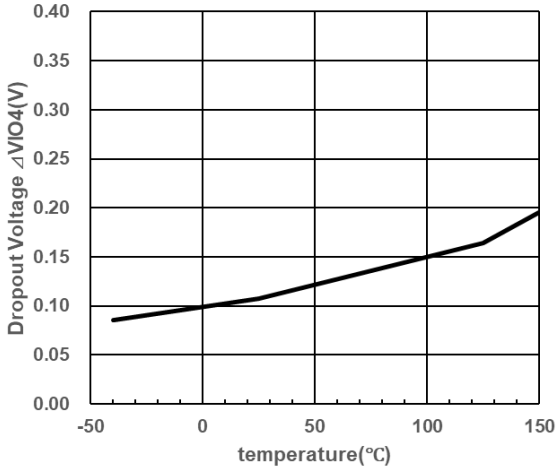
Ch.3 Output Voltage vs. Output Current
V_{OUT3}=1.8V, $V_{VIN2\_1/2}$=3.3V



Ch.4 Load Regulation vs. Temperature
I_{OUT4}=1mA to 150mA

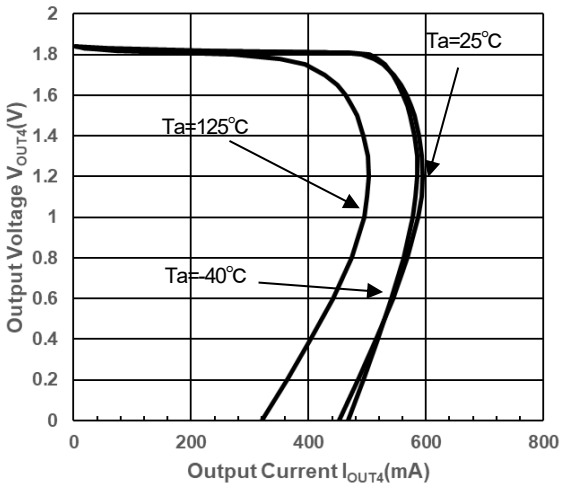


Ch.4 Dropout Voltage vs. Temperature
V_{VINLDO}=3.3V, I_{OUT4}=150mA

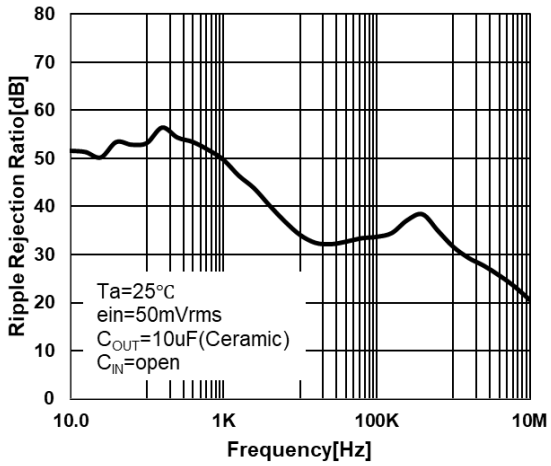


■APPLICATION CHARACTERISTICS (LDO)

Ch.4 Output Voltage vs. Output Current
V_{OUT4}=1.8V, V_{LDOVIN}=3.3V



Ch.3,4 RippleRejection vs. Frequency
V_{OUT}=2.5V, V_{LDOVIN}=3.3V, I_{OUT}=150mA



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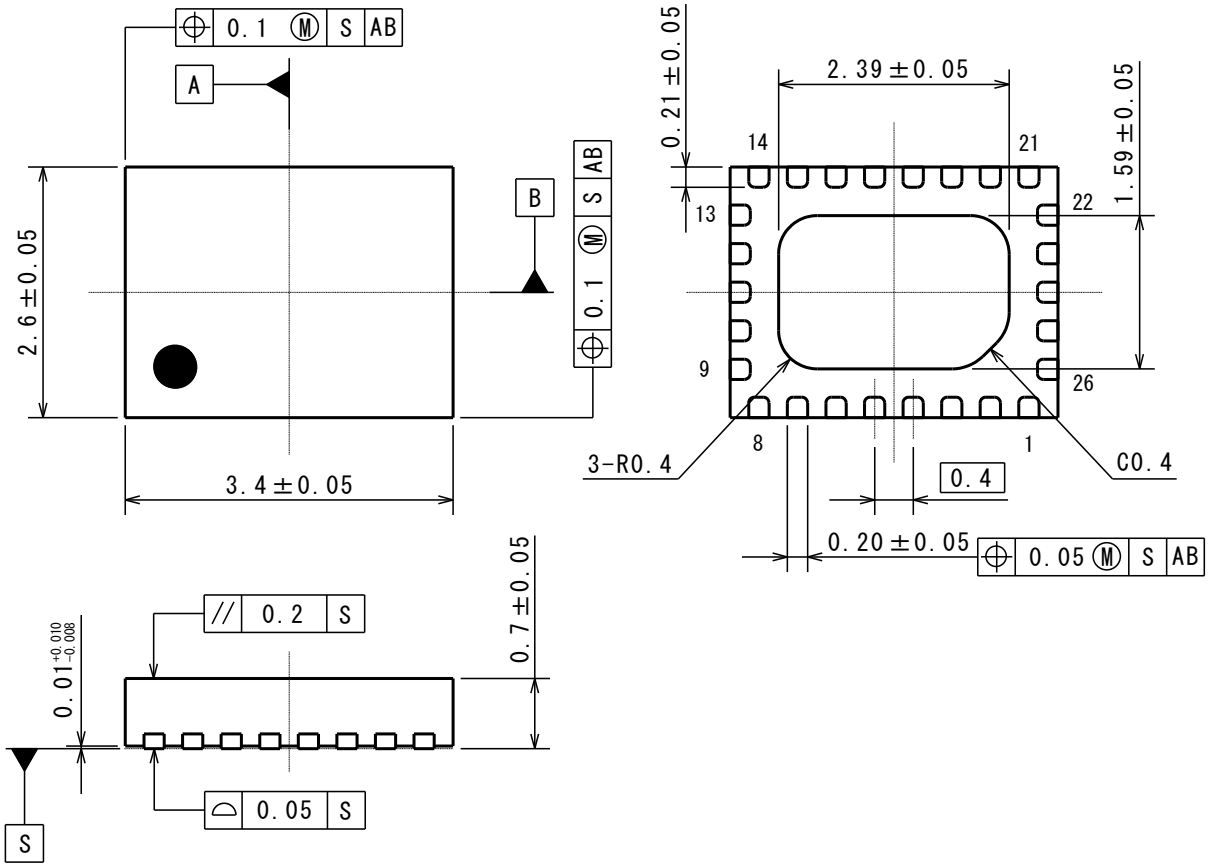
QFN2634-26-NC

PI-QFN2634-26-NC-E-A

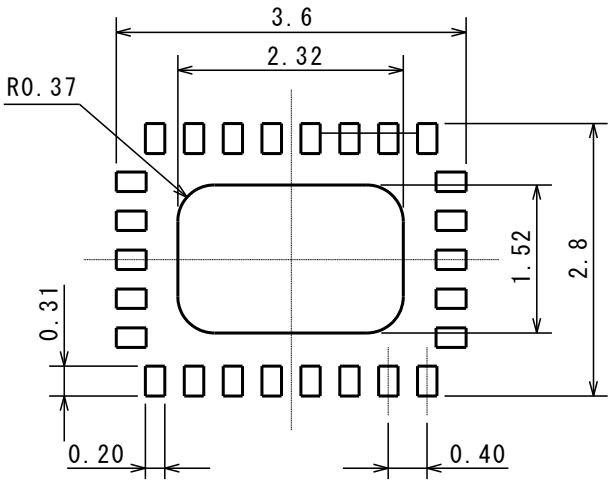
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



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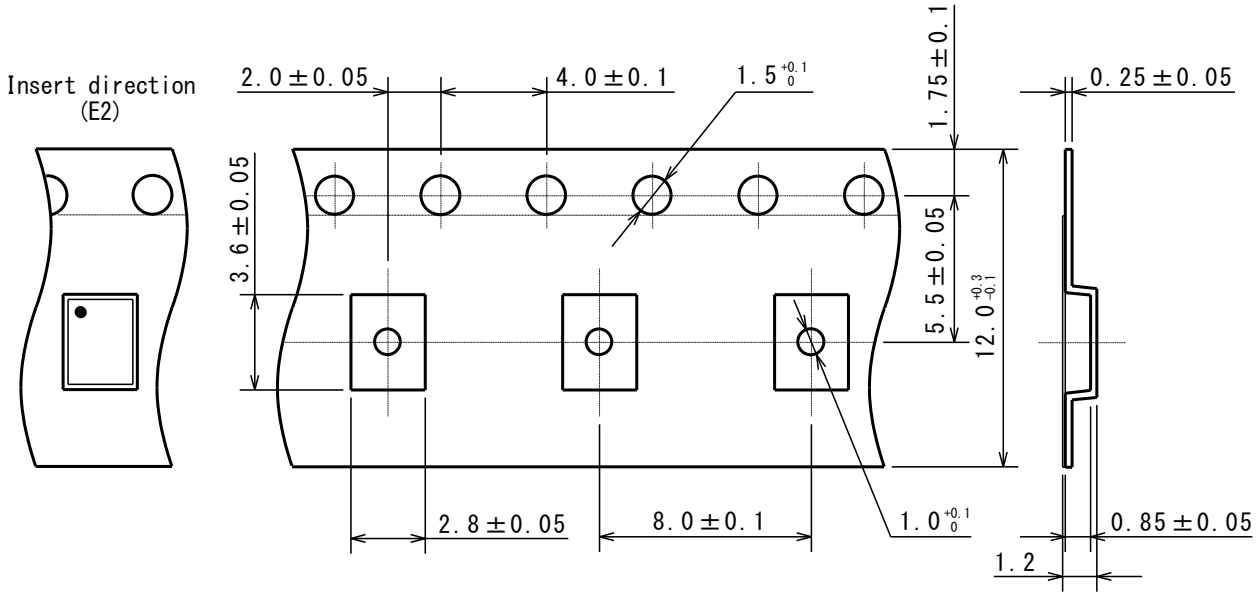
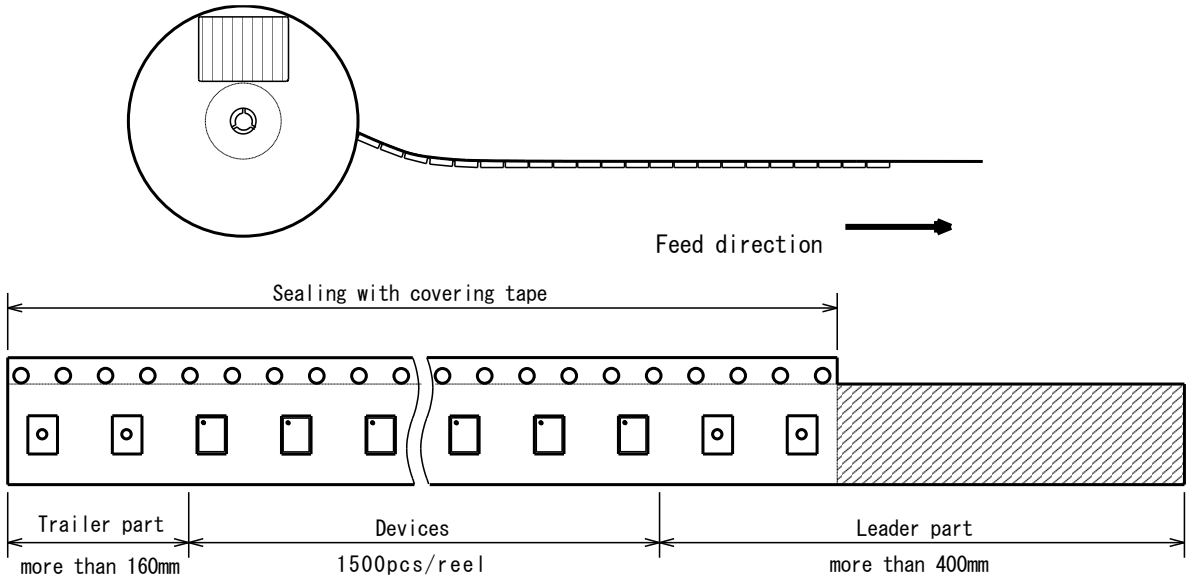
■ PACKING SPEC

UNIT: mm

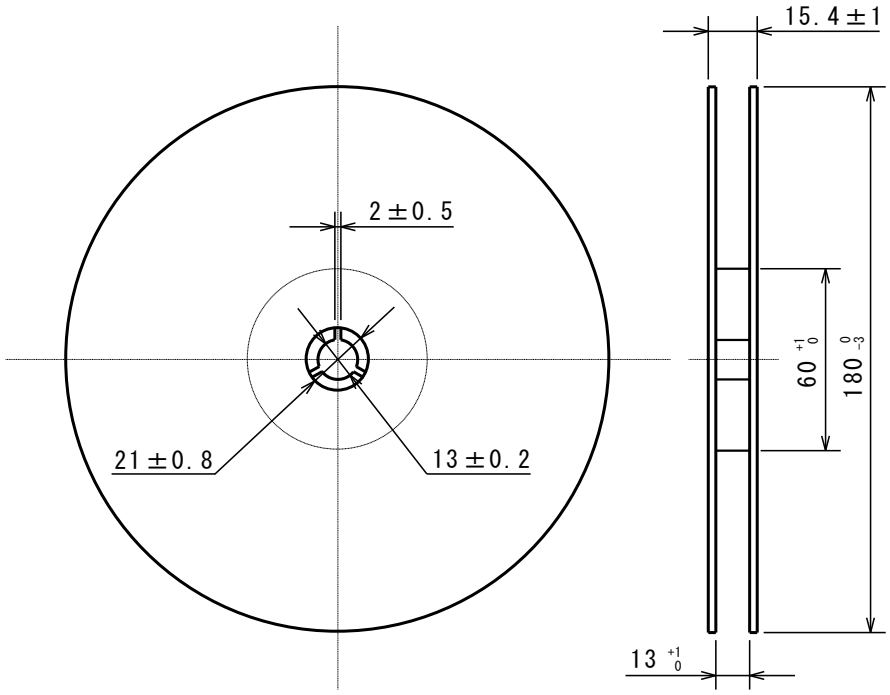
(1) Taping dimensions / Insert direction



(2) Taping state



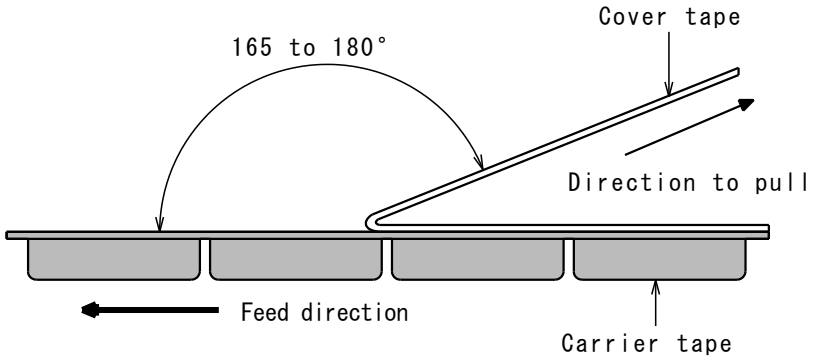
(3) Reel dimensions



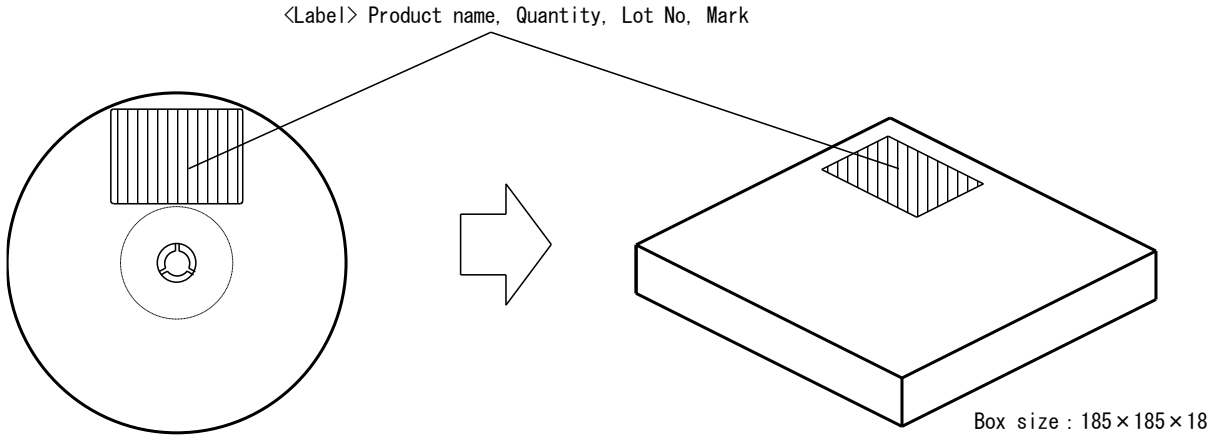
(4) Peeling strength

Peeling strength of cover tape

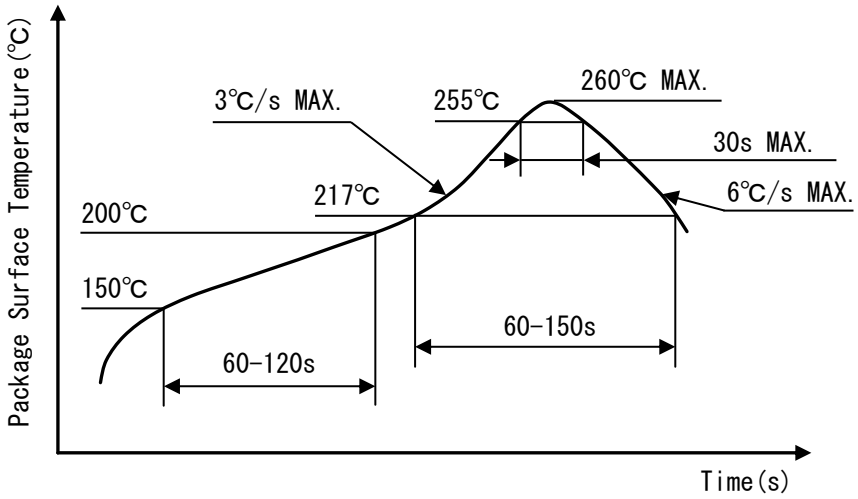
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ HEAT-RESISTANCE PROFILES



Reflow profile

Revision History

Date	Revision	Changes
September 30, 2025	Ver. 1.0	Initial release

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