

74LVC1G97-Q100

Low-power configurable multiple function gate

Rev. 1 — 22 March 2019

Product data sheet

1. General description

The 74LVC1G97-Q100 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- $\pm 24\text{ mA}$ output drive ($V_{CC} = 3.0\text{ V}$)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM ANSI/ESDA/Jedec JS-001 exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pf}$, $R = 0\text{ }\Omega$)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC1G97GW-Q100	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G97GW-Q100	YV

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

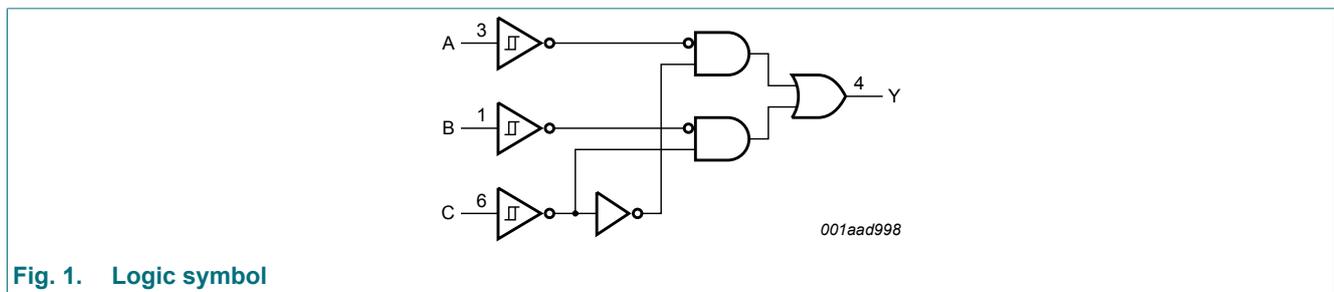


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

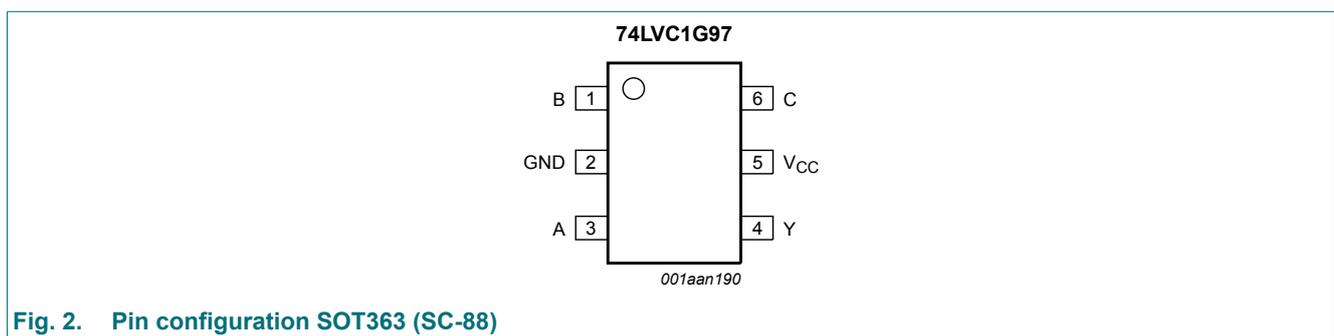


Fig. 2. Pin configuration SOT363 (SC-88)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX	see Fig. 3
2-input AND	see Fig. 4
2-input OR with one input inverted	see Fig. 5
2-input NAND with one input inverted	see Fig. 5
2-input AND with one input inverted	see Fig. 6
2-input NOR with one input inverted	see Fig. 6
2-input OR	see Fig. 7
Inverter	see Fig. 8
Buffer	see Fig. 9

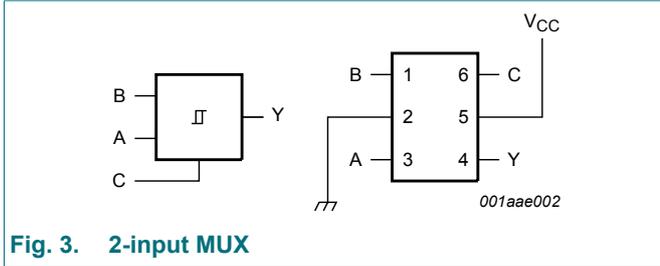


Fig. 3. 2-input MUX

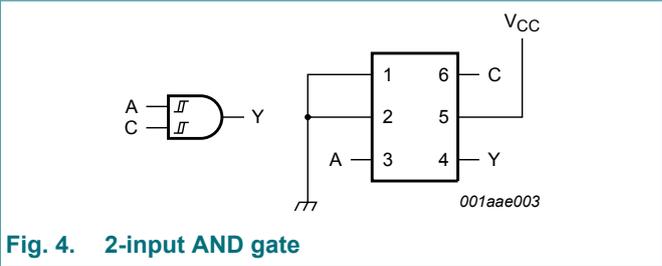


Fig. 4. 2-input AND gate

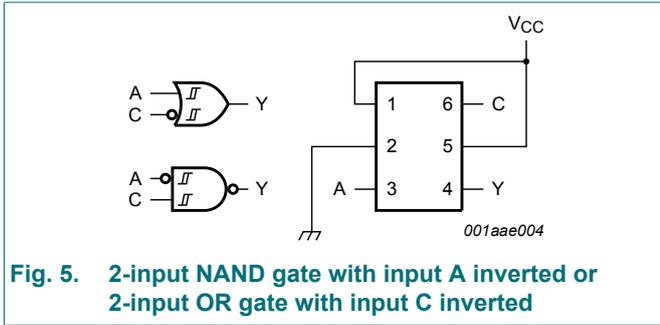


Fig. 5. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

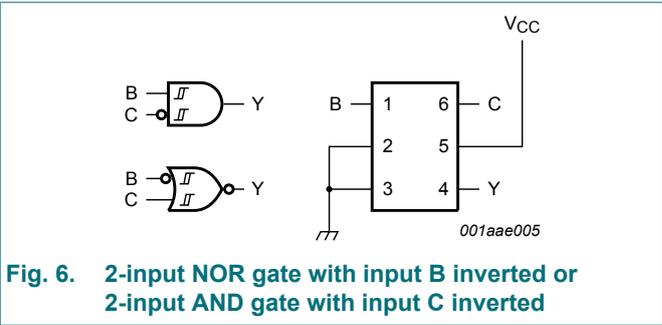


Fig. 6. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

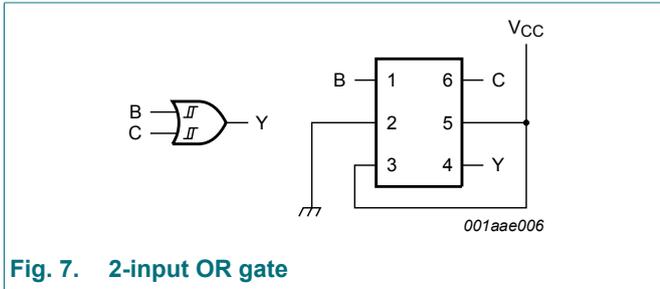


Fig. 7. 2-input OR gate

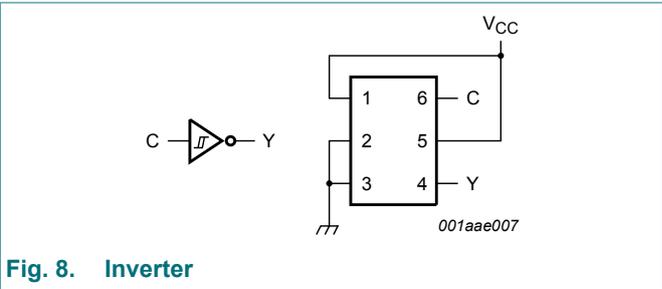


Fig. 8. Inverter

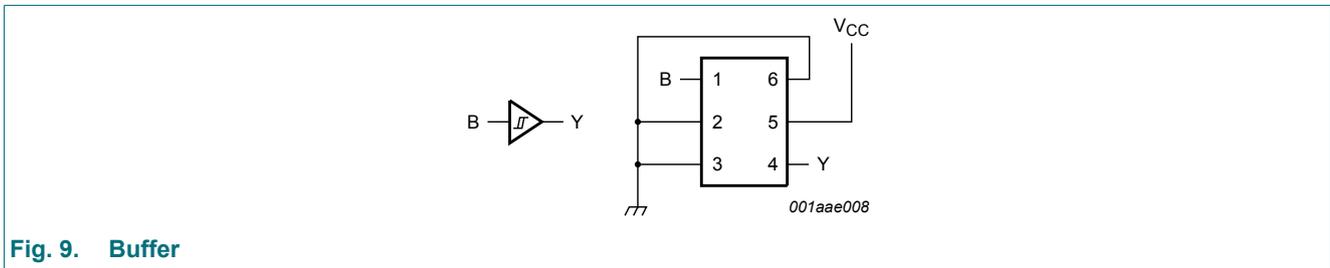


Fig. 9. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode	[1] -0.5	+6.5	V
		$V_{CC} = 0$ V; Power-down mode	[1] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SC-88 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{CC} or GND						
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.7	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{CC} or GND						
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V _{CC} - 0.1	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	-	-	3.4	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	-	500	µA
C _I	input capacitance		-	2.5	-	-	-	pF

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V _{CC} = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C _{PD}	power dissipation capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC} [3]	-	22	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit

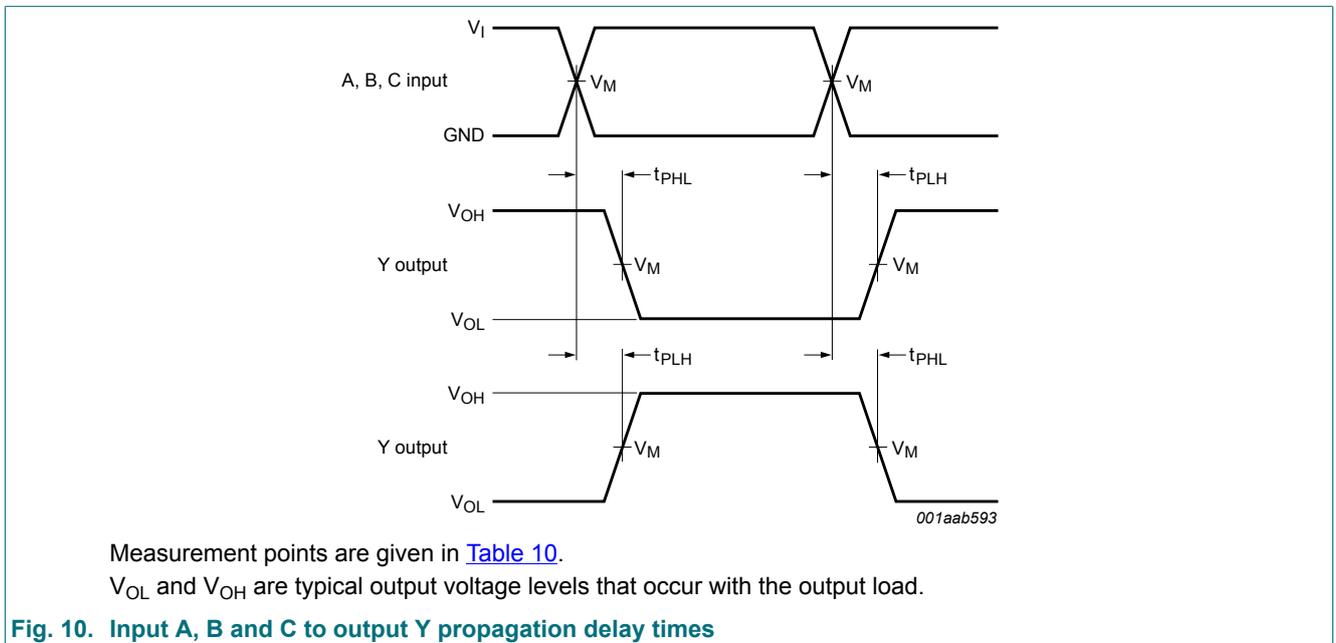
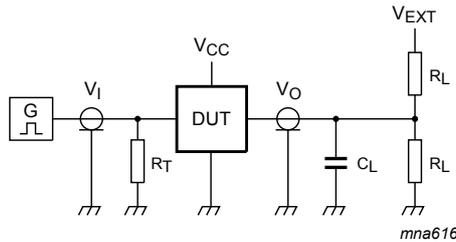


Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$



Measurement points are given in [Table 11](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 11. Test circuit for measuring switching times

Table 11. Measurement points

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Transfer characteristics

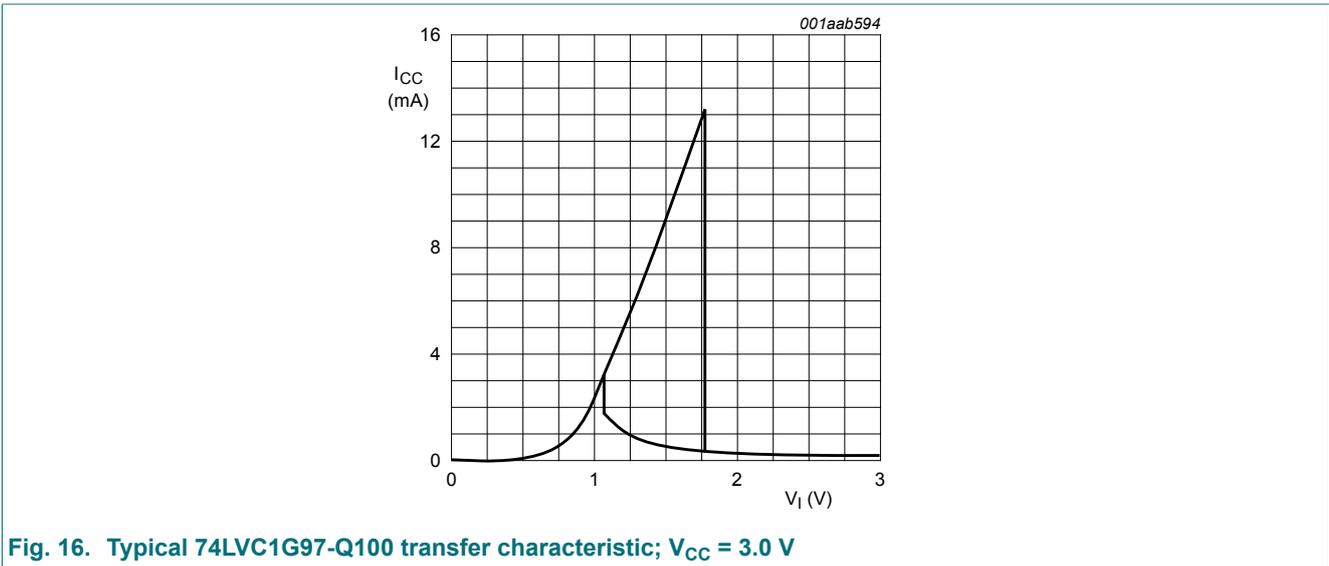
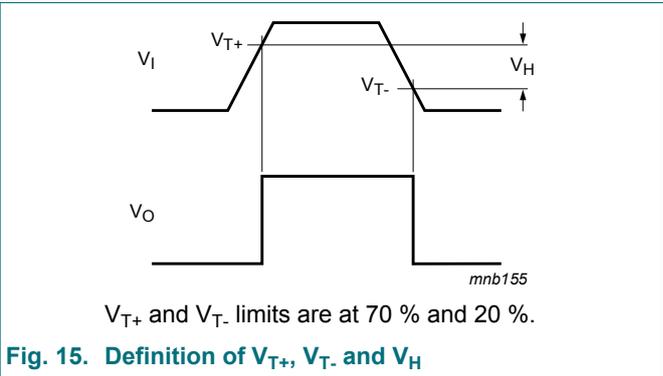
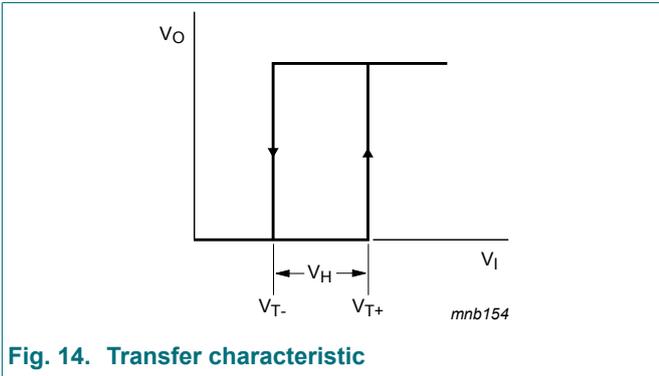
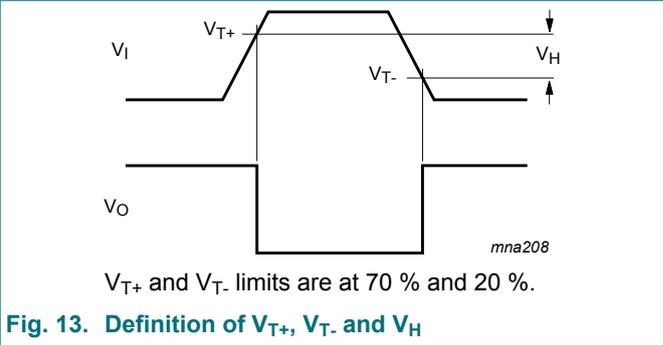
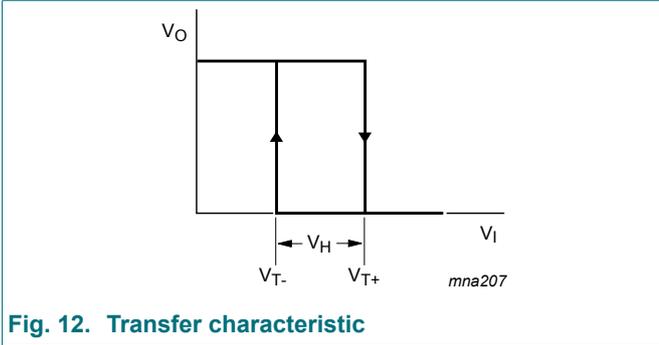
Table 12. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{T+}	positive-going threshold voltage	See Fig. 12 , Fig. 13 , Fig. 14 and Fig. 15						
		V _{CC} = 1.8 V	0.70	1.02	1.20	0.67	1.20	V
		V _{CC} = 2.3 V	1.11	1.42	1.60	1.08	1.60	V
		V _{CC} = 3.0 V, see Fig. 16	1.50	1.79	2.00	1.47	2.00	V
		V _{CC} = 4.5 V	2.16	2.52	2.74	2.13	2.74	V
		V _{CC} = 5.5 V	2.61	2.99	3.33	2.58	3.33	V
V _{T-}	negative-going threshold voltage	See Fig. 12 , Fig. 13 , Fig. 14 and Fig. 15						
		V _{CC} = 1.8 V	0.30	0.53	0.72	0.30	0.75	V
		V _{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V _{CC} = 3.0 V, see Fig. 16	0.80	1.04	1.30	0.80	1.33	V
		V _{CC} = 4.5 V	1.21	1.55	1.90	1.21	1.93	V
		V _{CC} = 5.5 V	1.45	1.86	2.29	1.45	2.32	V
V _H	hysteresis voltage	(V _{T+} - V _{T-}). See Fig. 12 , Fig. 13 , Fig. 14 and Fig. 15						
		V _{CC} = 1.8 V	0.30	0.48	0.62	0.23	0.62	V
		V _{CC} = 2.3 V	0.40	0.64	0.80	0.34	0.80	V
		V _{CC} = 3.0 V, see Fig. 16	0.50	0.75	1.00	0.44	1.00	V
		V _{CC} = 4.5 V	0.71	0.97	1.20	0.65	1.20	V
		V _{CC} = 5.5 V	0.71	1.13	1.40	0.65	1.40	V

[1] Typical values are measured at T_{amb} = 25 °C.

12.1. Waveforms transfer characteristics



13. Package outline

Plastic surface-mounted package; 6 leads

SOT363

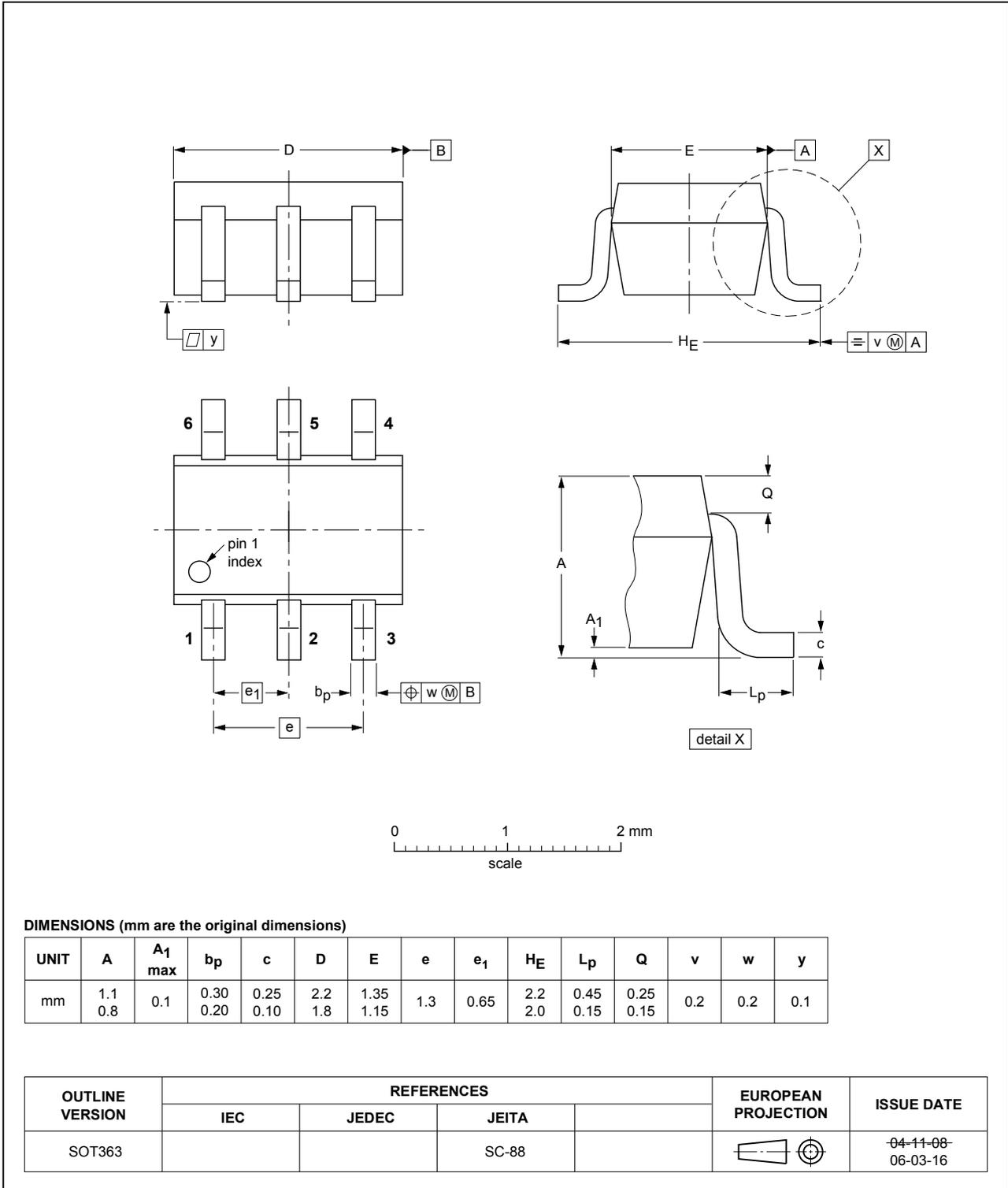


Fig. 17. Package outline SOT363 (SC-88)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G97_Q100 v.1	20190322	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[74HC32S14-13](#) [74LS133](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [NLV74HC14ADR2G](#) [NLV74HC20ADR2G](#) [NLVVHC1G09DFT1G](#)
[NLX2G86MUTCG](#) [74LVC2G02HD4-7](#) [NLU1G00AMUTCG](#) [74LVC2G32RA3-7](#) [74LVC2G00HD4-7](#) [NL17SG02P5T5G](#) [74LVC2G00HK3-](#)
[7](#) [74LVC2G86HK3-7](#) [NLX1G99DMUTWG](#) [NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#) [NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#)
[NLV27WZ86USG](#) [NLV27WZ00USG](#) [NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#) [NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#)
[74AUP2G00RA3-7](#) [NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#) [NL17SG86P5T5G](#) [NL17SZ05P5T5G](#) [NLV74VHC00DTR2G](#)
[NLVVHC1G02DFT1G](#) [NL17SZ38DBVT1G](#) [NLV18SZ00DFT2G](#)