MPQ4481

36V, 3A, Step-Down Converter with Programmable Frequency and Single USB Charging Port Supporting EN_USB, Fault Indication for Automotive, AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ4481 integrates a monolithic, step-down, switch-mode converter with a single USB current-limit switch and Type-C 5V @ 3A mode configuration channel for the USB port. The MPQ4481 achieves 3A of output current with excellent load and line regulation over a wide input supply range.

The output of the USB switch is current-limited. The USB port supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and USB Type-C 5V @ 3A DFP mode without the need for outside user interaction.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4481 requires a minimal number of readily available, standard, external components and is available in a QFN-26 (5mmx5mm) package.

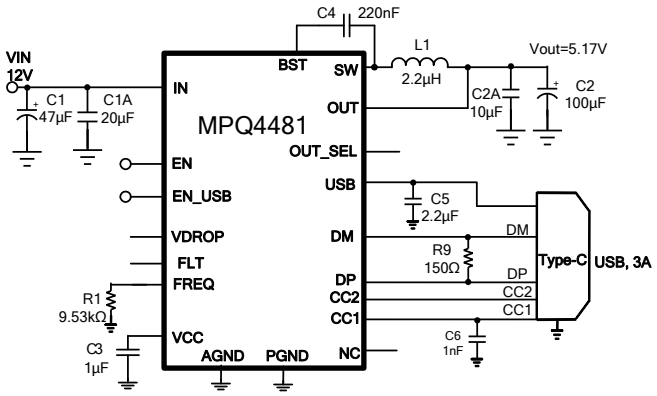
FEATURES

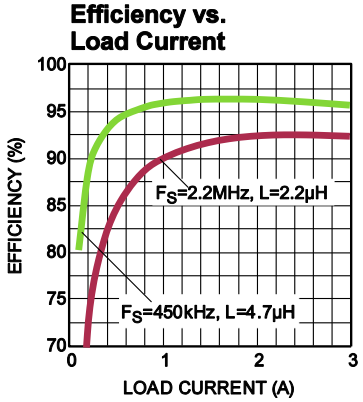
- Supports DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- Wide 6V to 36V Operating Input Range
- Selectable V_{OUT}: 5.1V, 5.17V, and 5.3V
- Programmable Line Drop Compensation
- Accurate USB Output Current Limit
- Low Dropout Mode
- 25mΩ/20mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- 15mΩ Low $R_{DS(ON)}$ Internal USB Power MOSFETs
- Up to 2.2MHz Operation Frequency
- Forced Continuous Conduction Mode (CCM) Operation
- Load Shedding versus Temperature
- EN Control for USB
- Fault Indication for USB
- ±8kV HBM ESD Rating for USB, DP, DM
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB-Dedicated Charging Ports (DCP)
- USB Type-C Charging Port

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4481GU-AEC1	QFN-26 (5mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ4481GU-AEC1–Z)

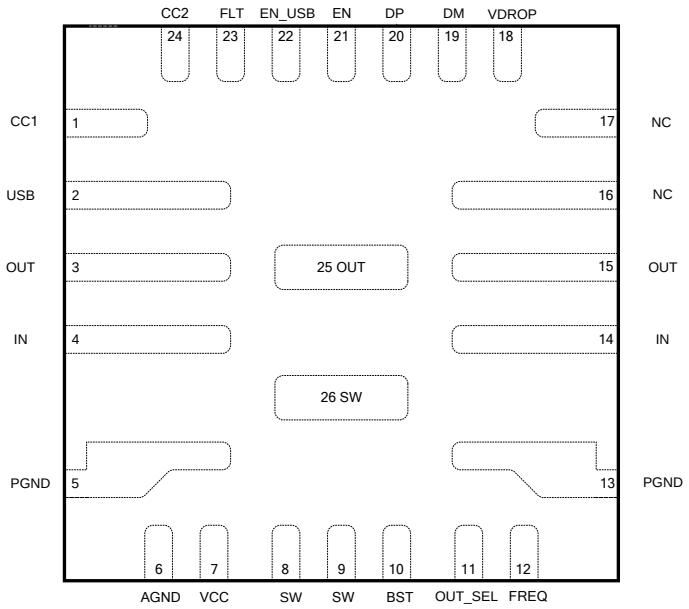
TOP MARKING

MPSYYWW
MP4481
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4481: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (5mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.4V to +40V
V_{SW} ..... -0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} ..... -0.3V to +10V (2)
V_{OUT}, V_{USB} ..... -0.3V to +6.5V
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (3)
QFN-26 (5mmx5mm) 6.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range ..... 6V to 36V
Output current ..... 3A for USB
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
JESD51-7 (5)	44	9	°C/W
50mmx50mm 4-Layer PCB	20	2	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS Max rating, please refer to the EN Control section on page 12.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 = 5.1kΩ, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		10	18	μA
Supply current (quiescent)	I_{Q1}	No switching		0.7	1.7	mA
	I_{Q2}	CC floating		400	800	μA
EN rising threshold	V_{EN_Rising}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
EN pull-up current	I_{EN}		4	8	12	μA
Thermal shutdown (7)	T_{TSD}			165		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C
VCC regulator	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		4.6	5.0	5.4	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			700		mV
HS switch on resistance	R_{DSON_HS}			25	40	mΩ
LS switch on resistance	R_{DSON_LS}			20	30	mΩ
Output voltage	V_{OUT}	OUT_SEL = low	-2%	5.1	+2%	V
		OUT_SEL = float, T_J = +25°C	-1%	5.17	+1%	
		OUT_SEL = float, T_J = -40°C to +125°C	-2%	5.17	+2%	
		OUT_SEL = high	-2%	5.3	+2%	
Output over-voltage protection	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	V_{OVP_F}		5.4	5.7	6.1	V
Low-side current limit (7)	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = +25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = -40°C to +125°C			5	
High-side current limit (7)	I_{LIMIT}	V_{OUT} = 0V	4.5	7	9.5	A
Oscillator frequency	F_{SW1}	Pull R_{FREQ} to GND	170	235	300	kHz
	F_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	
	F_{SW3}	R_{FREQ} = 9.53kΩ	1800	2200	2600	
	F_{SW4}	R_{FREQ} = float	350	440	530	
Maximum duty cycle	D_{MAX}	FREQ = 440kHz		95		%
Minimum off time	T_{OFF_MIN}			110		ns
Minimum on time (7)	T_{ON_MIN}			130		ns
Soft-start time	T_{SS}	Output from 10% to 90%	1	2	3.4	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 = 5.1kΩ, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Switch						
Under-voltage lockout threshold rising	V_{USB_UVR}		3.7	4	4.3	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			15	35	mΩ
USB OVP clamp	V_{USB_OV}		5.45	5.75	6.05	V
Current limit	I_{Limit1}	V_{OUT} drops 10%, Type-C mode, T_J = +25°C	-6%	3.45	6%	A
	I_{Limit2}	V_{OUT} drops 10%, Type-A mode, T_J = +25°C	2.6	2.75	2.9	A
Line drop compensation	V_{DROP_COM1}	Max load 2.4A, V_{DROP} = VCC	270	370	470	mV
	V_{DROP_COM2}	Max load 2.4A, V_{DROP} = 0	40	90	140	mV
VDROP logic high voltage	V_{HIGH}		1.2			V
VDROP logic low voltage	V_{LOW}				0.8	V
VDROP to ground resistance	R_{DROP}			1		MΩ
V_{BUS} soft-start time	T_{SS}	Output from 10% to 90%	1	2	3	ms
Hiccup mode on time	T_{HICP_ON2}	OC, V_{OUT} drops 10%, T_J = +25°C	3.5	5	6.5	ms
		OC, V_{OUT} drops 10%, T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	T_{HICP_OFF}	V_{OUT} connected to GND	1	2	3	s
EN_USB, logic high input	V_{ENSW_H}		1.2			V
EN_USB, logic low input	V_{ENSW_L}				0.8	V
FLT output low voltage	V_{FLT_Low}	Fault condition, sink 1mA			150	mV
FLT leakage	I_{FLT_LKG}	V_{FAULT} = 5V			1	μA
FLT deglitch time	T_{FLT_DEG}	Over-current	3	5	7	ms
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C		85	160	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		85	165	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$		2.55	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = +25°C	17	25	33	kΩ
		T_J = -40°C to +125°C	15	25	37	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 = 5.1kΩ, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = +25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = +25°C	70	115	150	kΩ
		T_J = -40°C to +125°C	60	115	160	
USB Type-C 5V@3A Mode – CC1, CC2						
CC resistor to disable Type-C mode	R_A	CC1, for Type-C mode applications, add a 1nF capacitor on CC1	70		90	kΩ
CC voltage to enable VCONN	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}		0.9		2.45	V
CC detach threshold	V_{OPEN}		2.75			V
CC voltage falling debounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	144	200	ms
CC voltage rising debounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	VCONN comes from buck output with some series resistance	1			W

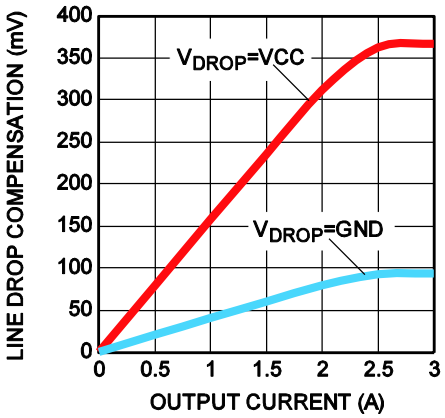
NOTES:

6) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.
7) Guaranteed by design and characterization test.

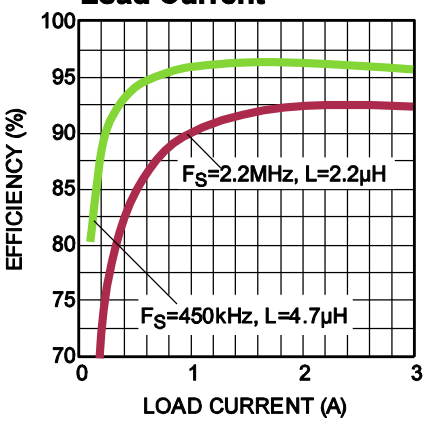
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, L = 2.2µH, F_S = 2.2MHz, T_A = 25°C, unless otherwise noted.

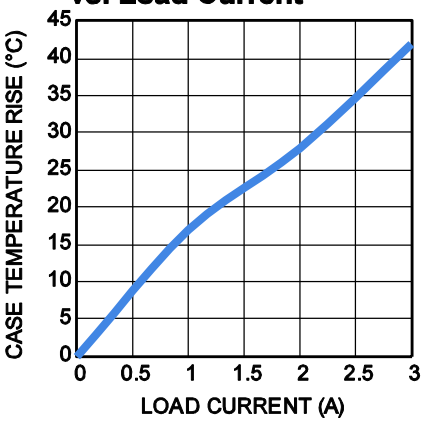
Line Drop Compensation



Efficiency vs. Load Current



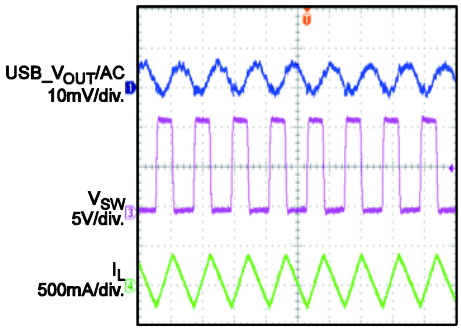
Case Temperature Rise vs. Load Current



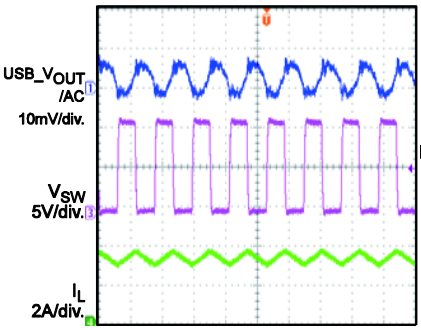
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 2.2µH, F_S = 2.2MHz, T_A = 25°C, unless otherwise noted.

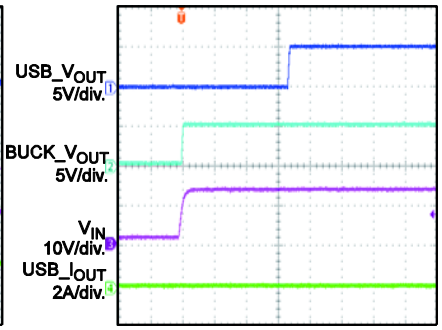
Output Ripple
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0A



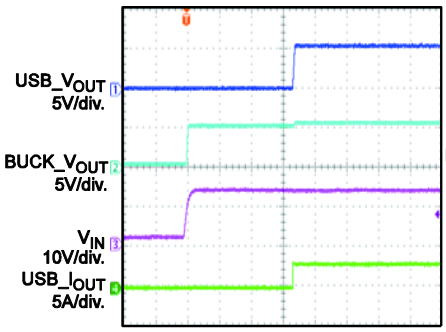
Output Ripple
V_{IN}=12V, V_{OUT}=5.17V,
USB_I_{OUT}=3A



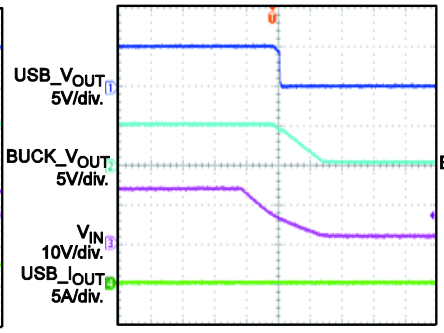
Power Start-Up
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0A



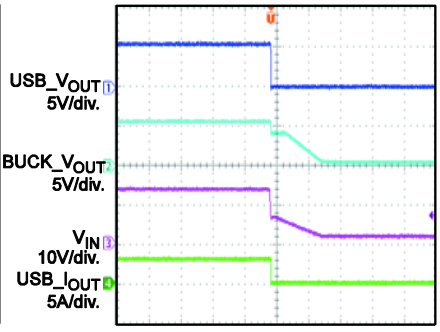
Power Start-Up
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=3A



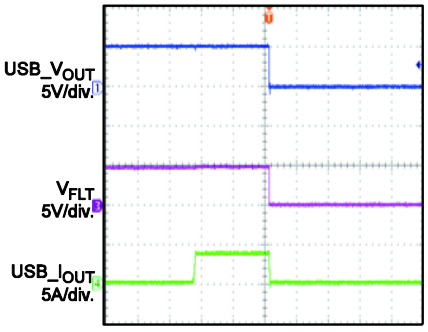
Power Shutdown
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0A



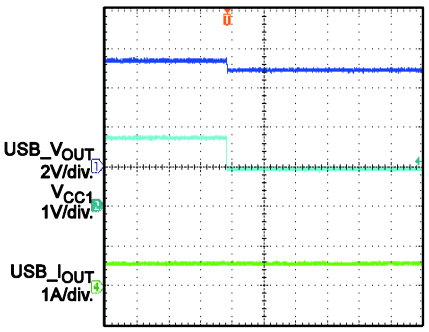
Power Shutdown
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=3A



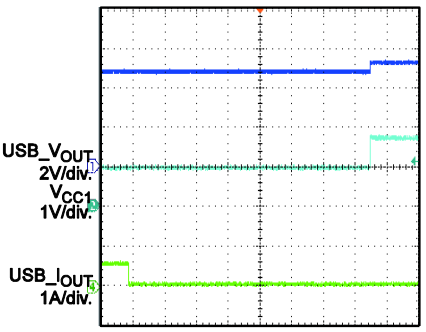
USB Over-Current Protection



Load Shedding Entry
V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0.5A



Load Shedding Recovery
V_{IN}=12V, V_{OUT}=5.17V,
USB Load Current from 0.5A to 0A

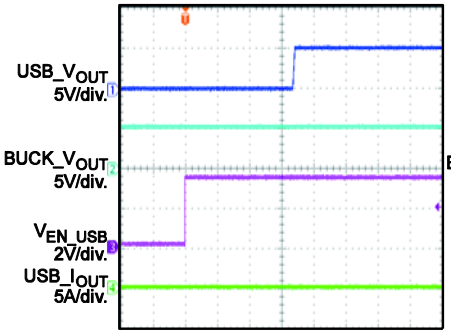


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 2.2µH, F_S = 2.2MHz, T_A = 25°C, unless otherwise noted.

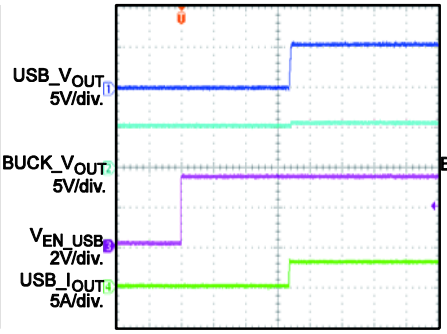
EN_USB Start-Up

V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0A



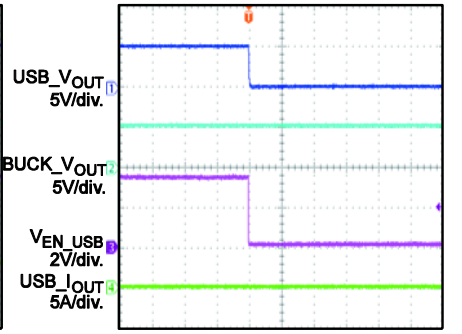
EN_USB Start-Up

V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=3A



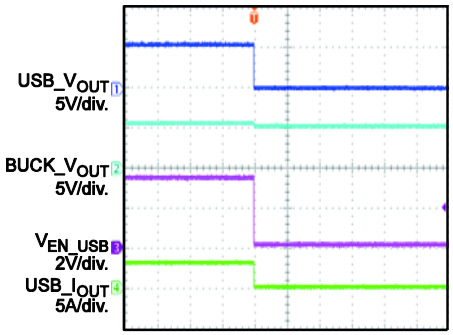
EN_USB Shutdown

V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=0A



EN_USB Shutdown

V_{IN}=12V, V_{OUT}=5.17V, USB_I_{OUT}=3A



PIN FUNCTIONS

QFN 5x5 Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
2	USB	**USB output.**
3, 15, 25	OUT	**Buck output.** OUT is the power input for the USB.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device and provides power to the the entire chip. The MPQ4481 operates from a 6V to 36V input voltage. A capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. Connect PGND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple VCC with a 1µF capacitor.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
10	BST	**Bootstrap.** A 0.22µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	OUT_SEL	**Buck output voltage set.** By setting OUT_SEL to low, float, or high, three different output voltages can be achieved: 5.1V, 5.17V, or 5.3V.
12	FREQ	**Switching frequency program input.** Connect a resistor from FREQ to GND to set the switching frequency. Float FREQ or connect FREQ to VCC for the default 450kHz frequency. Connect FREQ to ground for a 235kHz internal frequency.
16, 17	NC	**No connection.** Leave NC floating.
18	VDROP	**Line drop compensation selection.** Refer to EC table for detailed specifications.
19	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
20	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.
21	EN	**Chip on/off control input.** An internal 8µA pull-up current source pulls up EN automatically.
22	EN_USB	**USB on/off control input.** By default, EN_USB is pulled to VCC by an internal 1MΩ resistor.
23	FLT	**Fault indication of USB.** FLT indicates over-current or over-temperature conditions. FLT is an open drain for normal conditions. Pull FLT low during a fault condition.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

BLOCK DIAGRAM

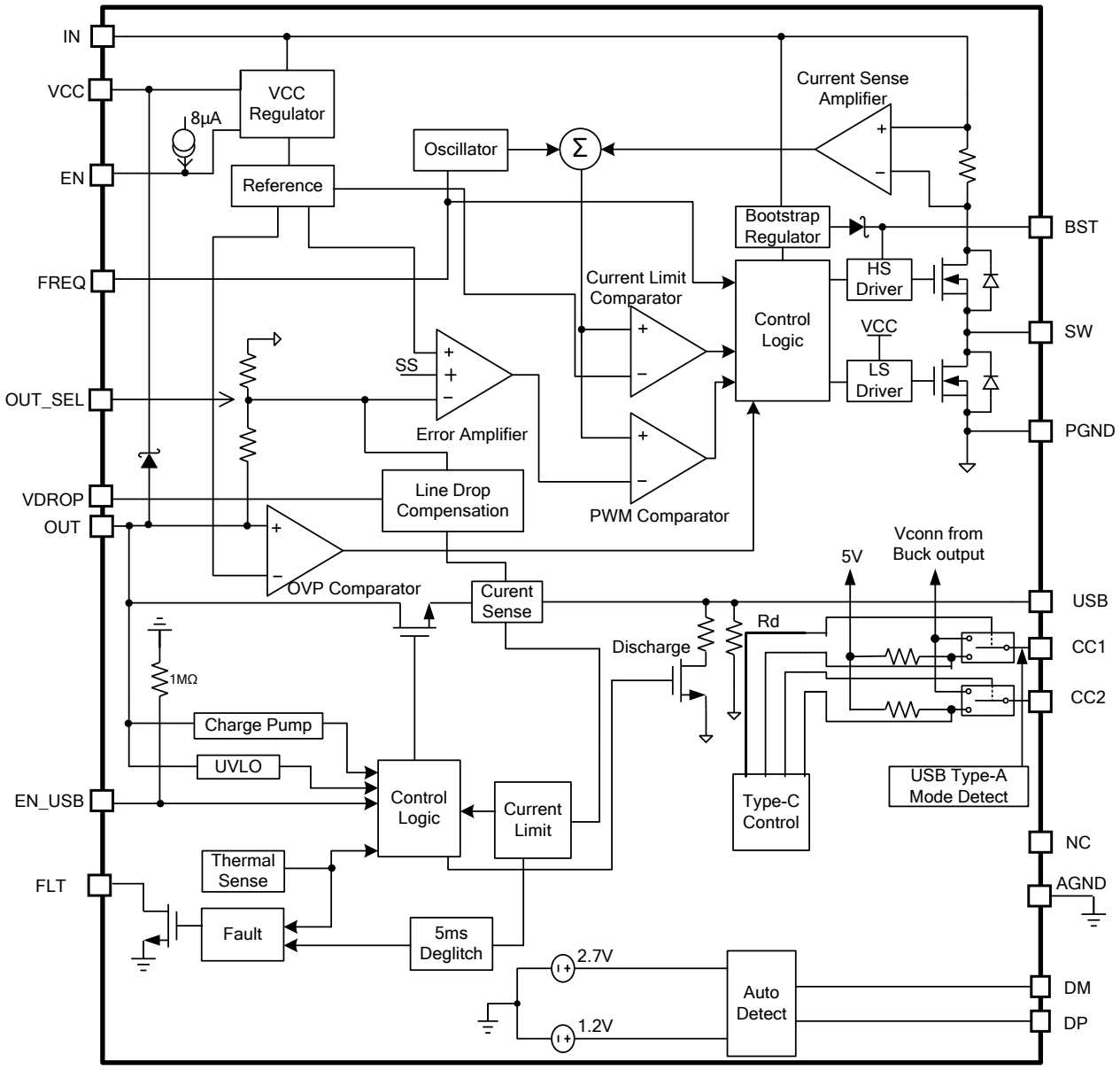


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER SECTION

The MPQ4481 integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and a single USB current-limit switch with charging port auto-detection. The MPQ4481 offers a compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ4481 operates in a fixed-frequency, peak-current-mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (REF) and outputs V_{COMP}. This V_{COMP} controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 4.6V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.6V, the output of the regulator is in full regulation. If V_{IN} is less than 4.6V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the buck output starts up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

Enable Control (EN)

The MPQ4481 has an enable control pin (EN). An internal 8µA pull-up current allows EN to be floated for automatic start-up. Pull EN high or float EN to enable the IC. Pull EN low to disable the IC. Once EN is pulled high, the buck output is enabled regardless of the status of EN_USB, CC1, and CC2.

EN is clamped internally using a 7.6V series Zener diode and a 10V breakdown voltage of the ESD cell.

Connect EN through a pull-up resistor to V_{IN} to enhance the EN pull-up current ability. This requires limiting the amplitude of the EN voltage source below 10V or limiting the EN input current below 500µA if the EN pull-up voltage is larger than 10V.

For example, if connecting EN to V_{IN} = 36V, then R_{PULLUP} ≥ (36V - 10V) / 500µA = 52kΩ.

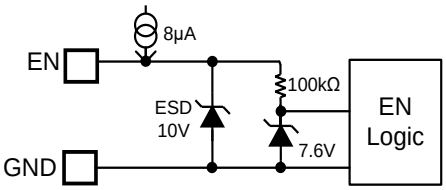


Figure 2: Zener Diode between EN and GND

Setting the Frequency

Connect a resistor from FREQ to ground to set the switching frequency (see Table 1). The value of the frequency can be calculated approximately with Equation (1):

$$FREQ(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(K\Omega) + 53.7} \quad (1)$$

The frequency vs. R_{FREQ} is shown in Figure 3.

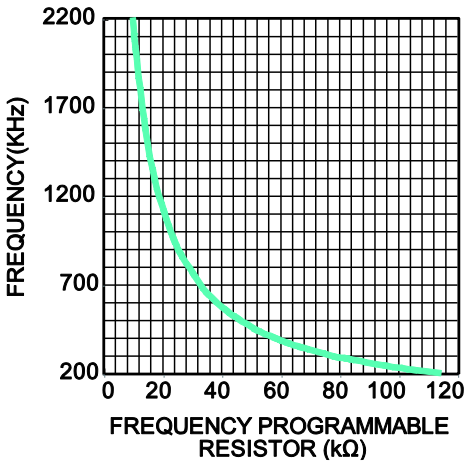


Figure 3: Switching Frequency vs. R_{FREQ}

Table 1: Recommended Resistor Values for Typical Switching Frequencies

R_{FREQ} (kΩ)	F_S (kHz)
0	235
66.5	350
NS	450
45.8	500
22.3	1000
14.6	1500
9.53	2200

Two internal comparators monitor FREQ's logic voltage to enable FREQ to float or short to GND. During power-up, there is another internal source current on FREQ. The frequency is locked at an internal fixed 450kHz when a voltage greater than 2V is sensed on FREQ for longer than 8μs. The frequency is locked at an internal fixed 235kHz when a voltage greater than 0.1V is sensed on FREQ for longer than 8μs. Leave FREQ floating or connect FREQ to VCC to achieve the 450kHz default switching frequency. Short FREQ to ground to achieve a 235kHz frequency (see Figure 4).

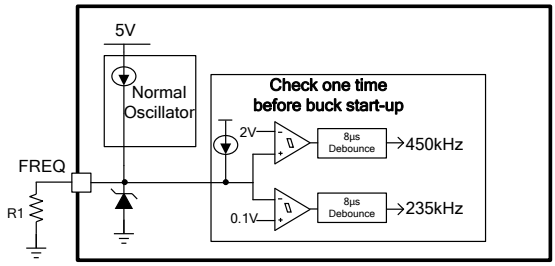


Figure 4: Switching Frequency Functional Block

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5.0V, and its falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 2ms internally. If the output of the MPQ4481 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Forced CCM Operation

The MPQ4481 works in forced continuous conduction mode (CCM) continuously. The MPQ4481 operates with a fixed switching frequency regardless of whether it is operating in light load or full load. The advantage of CCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charge time, but it also has low efficiency at light-load condition. A proper inductance should be selected to avoid triggering the low-side switch's negative current limit (typically 2A, from SW to GND). If the negative current limit is triggered, the low-side switch turns off, and the high-side switch turns on when the internal clock begins.

Buck Over-Current Protection (OCP)

The MPQ4481 has a cycle-by-cycle over-current limit when the inductor peak current exceeds the current-limit threshold, and the FB voltage drops below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPQ4481 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current greatly, alleviates thermal issues, and protects the regulator. The MPQ4481 exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MPQ4481 has output over-voltage protection (OVP). If the output is higher than 5.85V, the high-side switch stops turning on. The low-side switch turns on to discharge the output voltage until the output decreases to 5.7V. Then the chip resumes normal operation.

Low Dropout Operation

When the input voltage is close to the output voltage and the min off time is triggered, the operation frequency decreases automatically until the maximum on time is triggered (typically 8μs). This achieves a low dropout voltage.

Switching Frequency Foldback Mode

The MPQ4481 introduces foldback mode when the input voltage is larger than 15V and the setting frequency is larger than 1.4MHz. When V_{IN} is larger than 15V and Fs is larger than 1.4MHz, the buck frequency is reduced smoothly until the frequency is half of the setting frequency.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 6). The BST capacitor (C4) voltage is charged up quickly by VCC through M1. The 2.5μA input to the BST current source can also charge the BST capacitor when the low-side switch does not turn on.

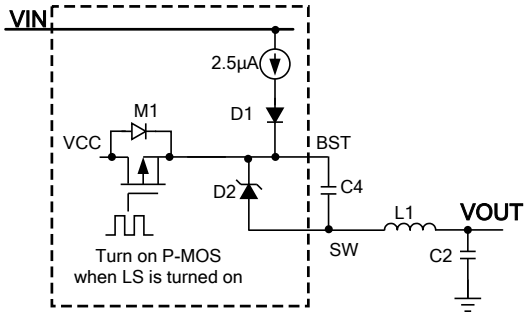


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, IN low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

USB CURRENT-LIMIT SWITCH SECTION

Current-Limit Switch

The MPQ4481 integrates a single USB current-limit switch. The MPQ4481 provides built-in soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

When the load current reaches the current-limit threshold, the USB power MOSFET works in a constant current-limit mode (see Figure 6). If the over-current limit condition lasts longer than 5ms (V_{OUT} does not drop too low), the USB channel enters hiccup mode with 5ms of on time and 2s of off time. The buck output still works normally.

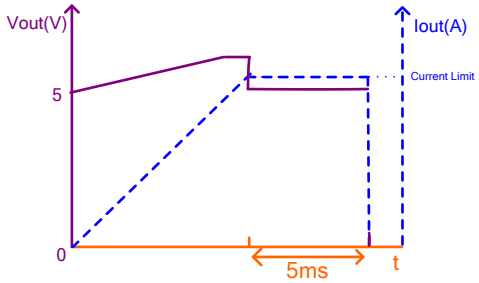


Figure 6: Over-Current Limit

After the soft-start finishes, if the USB output voltage is lower than 3.5V and lasts longer than 50μs, the MPQ4481 enters hiccup mode without having to wait 5ms (see Figure 7). This can prevent an abnormal thermal rise during the constant resistor (CR) load over-current case.

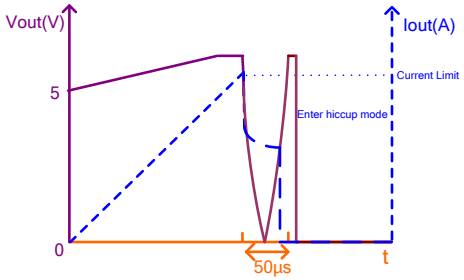


Figure 7: Over-Current Limit for CR Load

Fast Response for Short-Circuit Protection

If the load current increases rapidly due to short-circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 7A secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET.

This can help limit the peak current through the switch, keeping the buck output voltage from dropping too much. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MPQ4481 regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4481 can compensate for an output-voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

Since the trace resistance varies for different cables, the MPQ4481 provides selectable line drop compensation through VDROP. The line drop compensation amplitude increases linearly as the load current increases and also has an upper limitation.

Connect VDROP to VCC to achieve a 370mV line drop compensation. Float VDROP or connect VDROP to GND to achieve a 90mV line drop compensation. VDROP has an internal 1MΩ pull-down resistor.

USB Output Over-Voltage Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage is higher than the OVP threshold, the output voltage is clamped at 5.75V.

USB Output Discharge and Impedance

The USB switch has a fast discharge path that can discharge the external output capacitor's energy quickly during a power shutdown. This function is active when the CC pins are released or the USB is disabled (input voltage is under UVLO, EN off, or EN_USB off). The discharge path is turned off when the USB output voltage is discharged below 50mV. After the fast discharge path turns off, there is only a high impedance resistor (typically 600kΩ) from the USB to ground.

USB Enable On/Off Control (EN_USB)

EN_USB is the USB switch's on/off control input pin. The USB switch is active when EN is pulled high. Float or pull the EN voltage to logic low to shut down the USB switch with an output discharge. EN_USB is pulled low by an internal 1MΩ resistor to ground. Connect EN_USB to VCC through a 100kΩ resistor for automatic start-up.

Fault Indication (FLT)

FLT is the fault indication pin for the USB switch. FLT is in an open-drain state during shutdown, start-up, or normal condition. FLT asserts (logic low) on the USB switch during an over-current or over-temperature condition. FLT asserts low until the fault condition is removed and the USB output voltage rises high again. There is a 5ms deglitch timer during the over-current condition to prevent FLT from triggering falsely. If the over-current condition lasts for 5ms, the USB switch enters hiccup mode and FLT goes low. The FLT signal is not deglitched during the over-temperature condition.

Auto-Detection

The MPQ4481 integrates a USB-dedicated charging port auto-detect function. This function recognizes most mainstream portable devices and supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple divider mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode

The auto-detect function is a state machine that supports all of the DCP charging schemes above. Connect DP and DM with a 150Ω resistor for DCP mode.

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins (CC1 and CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp)

and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up and pull-down resistor (see Figure 8).

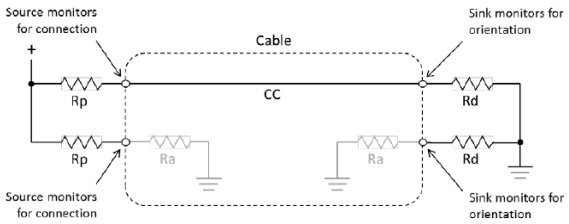


Figure 8: Current Source/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes Ra (typically 1kΩ) on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it may simply be the load.

The source must be able to differentiate between the presence of Rd and Ra to know whether there is a sink attached and where to apply VCONN. The source is not required to source VCONN unless Ra is detected.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode and Rd/Rd for debug accessory mode (see Figure 9 and Table 2). In Type-C debug mode and audio adapter accessory mode, two Ra resistors pull down CC1 and CC2, or two Rd resistors pull down CC1 and CC2. The MPQ4481's V_{BUS} is not enabled.

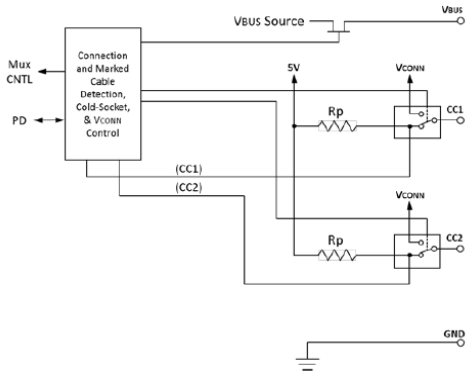


Figure 9: CC Pin Functional Block

A port that behaves as a source has the following functional characteristics.

1. The source uses a MOSFET to enable or disable the power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a sink. The presence of an Rd pull-down resistor on either CC1 or CC2 indicates that a sink is being attached. The value of Rp indicates the initial USB Type-C current level supported by the host. The MPQ4481 default Rp is 10kΩ, which represents a 3A current level.
3. The source uses the CC pin pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when Ra is discovered).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source can adjust the value of Rp dynamically to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures, the MPQ4481 changes Rp to 22kΩ to indicate a 1.5A current ability.
6. The source monitors the continued presence of Rd to detect a sink detach. When a detach event is detected, the source is removes, and V_{BUS} and VCONN return to step 2.

Disable Type-C Mode (Type-A Mode)

During the MPQ4481 initial start-up, the IC discharges CC1 first and sources 10μA of current for 20μs on CC1. If the CC1 voltage falls into a 400mV to 1.2V voltage range, the USB channel is latched at Type-A mode unless the part is re-enabled. Type-C mode is disabled, so CC is attached, the detach logic is disabled, and V_{BUS} is always enabled. The current limit changes to a Type-A spec. To trigger this mode, the external pull-down resistor should be 70 - 90kΩ. Do not connect an extra capacitor on CC1. In normal Type-C mode applications, a 1nF capacitor should be added on CC1 to avoid falsely triggering Type-A mode.

Load Shedding vs. Temperature

The MPQ4481 monitors the die temperature and changes its output current capability dynamically.

If the die temperature is higher than 125°C, the USB port's CC pin pull-up resistance (Rp) changes to 22kΩ to indicate that its source capability has changed to 1.5A. Meanwhile, V_{BUS} changes to 4.77V.

If the die temperature recovers to less than 100°C for 16 seconds, V_{BUS} reverts back to the normal voltage set by OUT_SEL. Meanwhile, the USB Type-C current capability changes back to 3A (Rp = 10kΩ). The current limit threshold remains at 3.45A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 145°C), the chip is enabled.

Table 2: CC Logic Truth Table

EN	EN_USB	CC	Buck	VCONN	USB
0	X	X	Disabled	Disabled	Disabled
1	0	X	Enabled	Disabled	Disabled
1	1	AUDIO	Enabled	Disabled	Disabled
		DEBUG	Enabled	Disabled	Disabled
		“A” (8)	Enabled	Disabled	Enabled
		Rd, Ra	Enabled	Enabled	Enabled
		Open	Enabled	Disabled	Disabled

NOTE:

8) "A" means Type-A mode. CC1 is requested to be pulled down by a 80.6kΩ resistor to enter this mode.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductor value can be derived with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 47µF electrolytic and 20µF ceramic capacitors are recommended in automotive applications at a 450kHz switching frequency.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

A 100µF capacitor with an ESR less than 50mΩ (e.g.: polymer capacitor or tantalum capacitors) and one 10µF ceramic capacitor are recommended in the application (see Table 3).

Table 3: Recommended External Components

Switching Frequency	Inductor	Input Capacitor	Buck Output Capacitor
2.2MHz	2.2µH	20µF ceramic cap + 47µF E-cap	10µF ceramic cap + 100µF Polymer cap
450kHz	4.7µH	20µF ceramic cap + 47µF E-cap	10µF ceramic cap + 100µF Polymer cap

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ4481 features high ESD protection up to ±8kV human body model on the USB pin, DP, and DM, and ±5.5kV human body model on CC1 and CC2. The ESD structures can withstand high ESD both in normal operation and when the device is powered off. To further extend the DP and DM's ESD level for covering complicated application environments, additional resistors and capacitors can be added (see Figure 10).

Similar R-C networks cannot be added on CC1 or CC2 since the CC line must be able to support 200mA of current and 300kHz of signaling. Additional ESD diodes can be added on the CC pins.

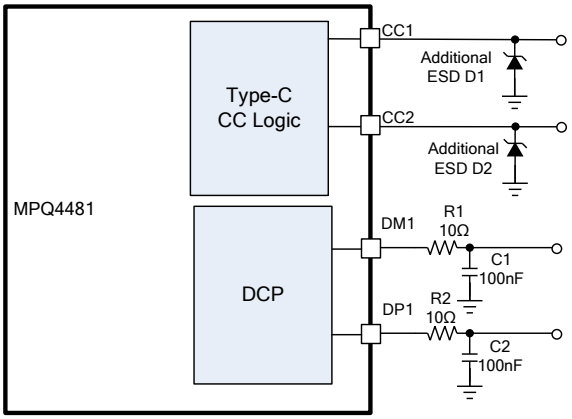


Figure 10: Recommended I/O Pins ESD Enhancing

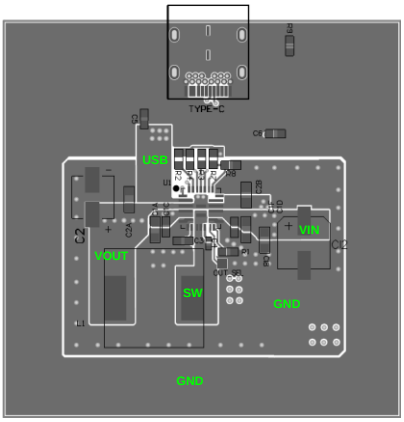
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation, thermal dissipation, and conduction EMI improvement. For best results, refer to Figure 11 and follow the guidelines below.

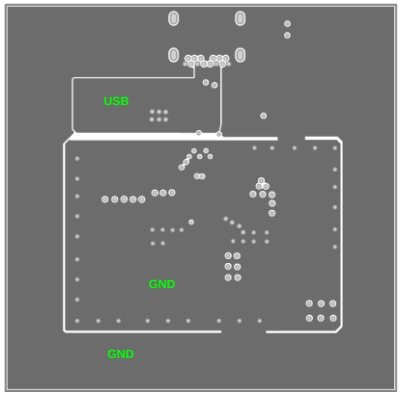
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place the output ceramic capacitor on two sides of the IC near OUT.
5. Use a large copper plane for PGND.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Use a large copper plane for SW and USB.
9. Route the USB trace on both PCB layers.
10. Add multiple vias.
11. Place two ceramic input decoupling capacitors as close as possible to IN and PGND. To improve EMI performance.
12. Place symmetrical C_{IN} capacitors on each side of the IC.
13. Place the BST capacitor close to BST and SW pins.
14. Add an input LC filter at the bottom side of PCB to pass the conduction EMI test.
15. Place the input V_{IN} and PGND copper on the inner layer isolated from the top layer and bottom layer ground.
16. Place the VCC decoupling capacitor as close to VCC as possible.

NOTE:

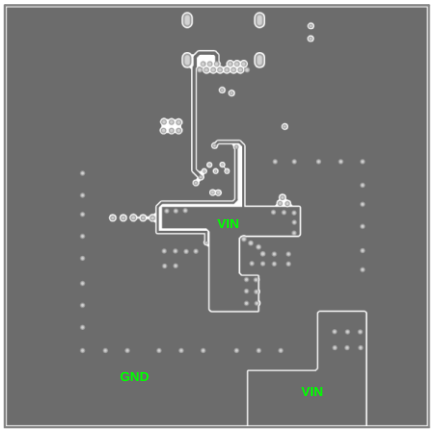
9) The recommended layout is based on the Typical Application Circuits in Figure 12 and Figure 13.



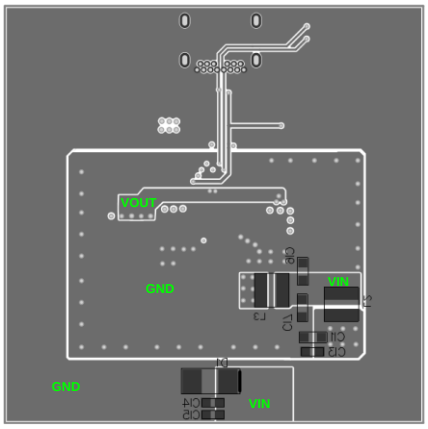
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 11: Recommended Layout

TYPICAL APPLICATION CIRCUITS

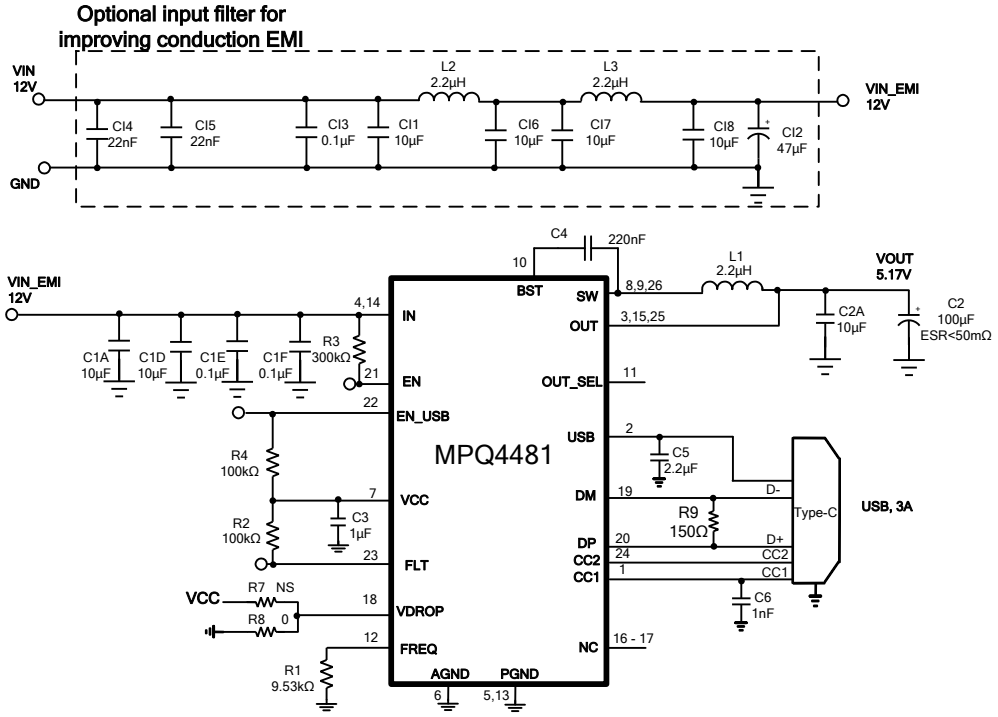


Figure 12: USB Type-C 5V/3A DFP Port (10)

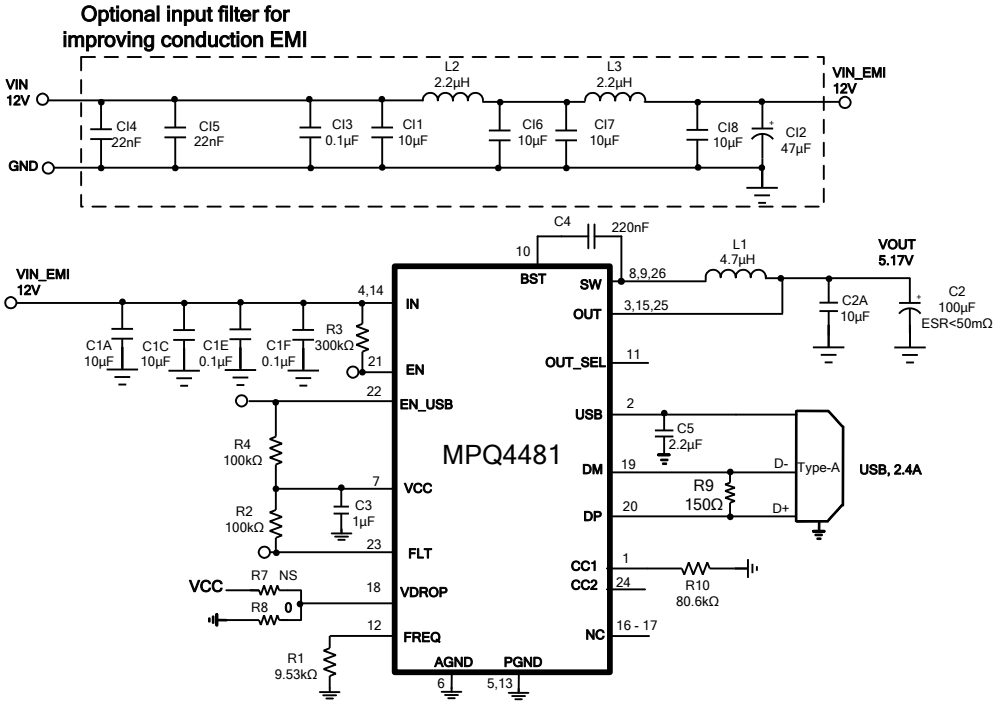


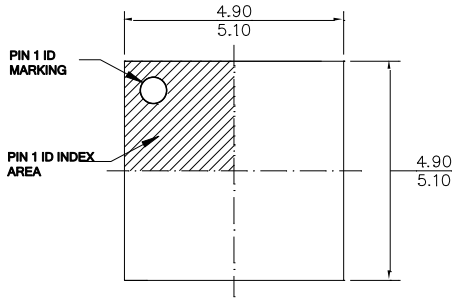
Figure 13: USB Type-A 5V/2.4A Port (10)

NOTE:

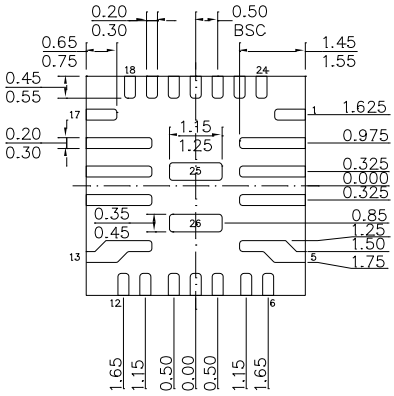
10) See Figure 10 for the CC pins' ESD protection enhancing details.

PACKAGE INFORMATION

QFN-26 (5mmx5mm)

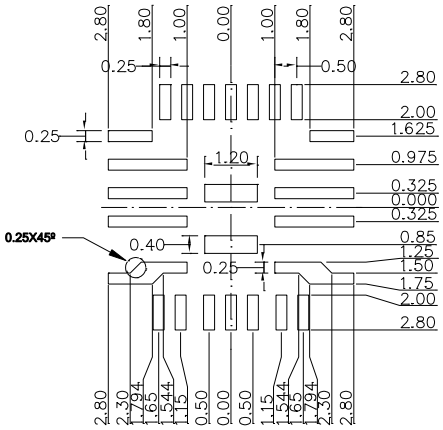


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN 2~4 AND 14~16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.

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