# MP2696A

## I²C-Controlled, Single-Cell Switching Charger with Power-Path Management and 3.6A Boost Output

## DESCRIPTION

The MP2696A is a highly integrated, flexible, switch-mode battery-charging, power-path management device designed for a single-cell Li-ion and Li-polymer battery to be used in a wide range of portable applications.

The MP2696A integrates three battery-charging phases: pre-charge, constant-current, and constant-voltage charge. This device also manages the input power source through input current limit regulation and minimum input voltage regulation.

The MP2696A can switch to boost mode to generate the system power output from the battery.

The MP2696A has an integrated IN to SYS pass-through path to pass the input voltage to the system.

Using an I²C interface, the host can flexibly program the charge and boost parameters. The device operating status can also be read in the registers.

Safety features include SYS short-circuit protection, input over-voltage protection, battery under-voltage protection, thermal shutdown, and JEITA battery temperature monitoring.

The MP2696A is available in a QFN-21 (3mmx3mm) package.

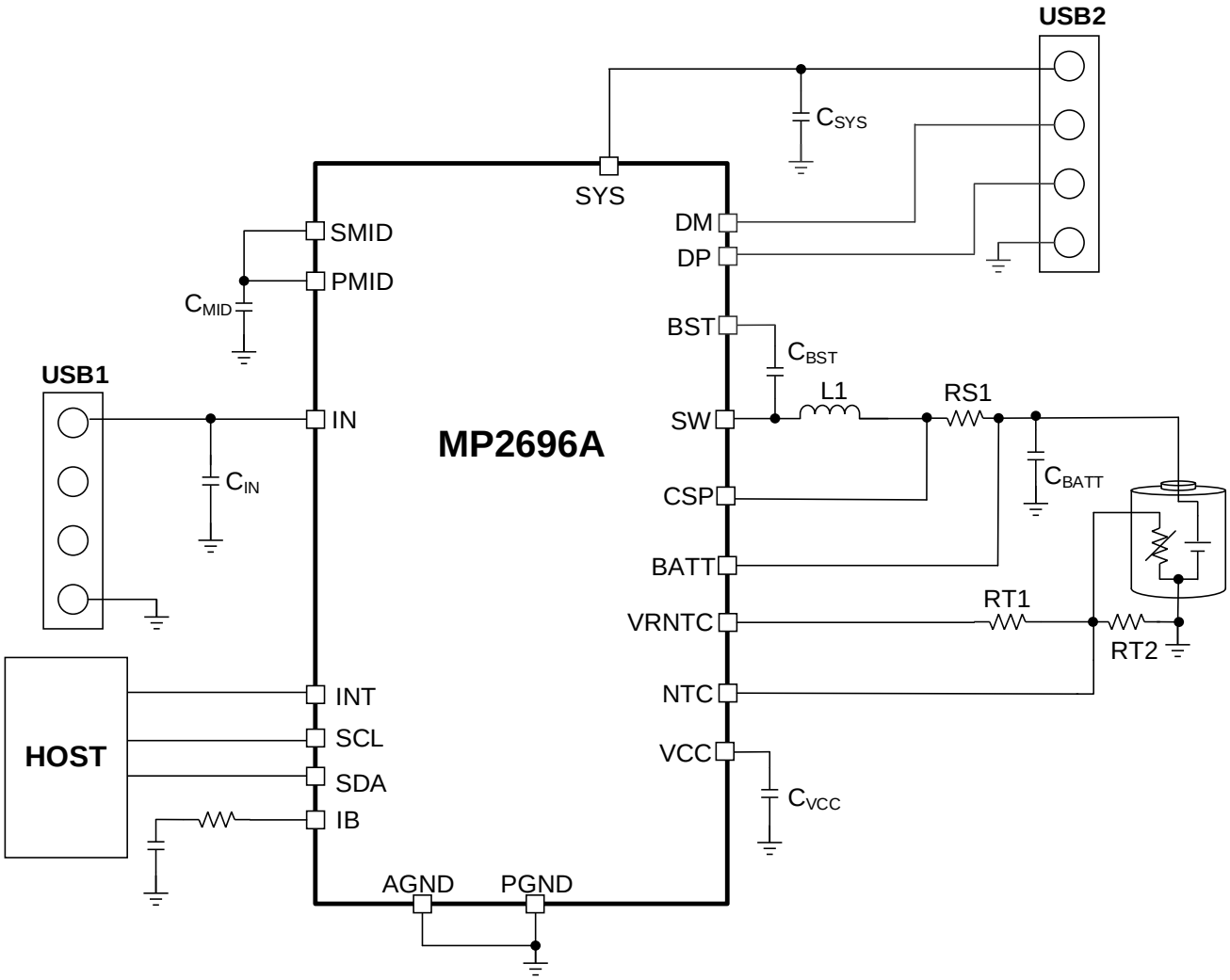
## FEATURES

- 4.0V to 11V Operation Voltage Range
- Up to 16V Sustainable Input Voltage
- 500mA to 3.6A Programmable Charge Current
- 3.6V to 4.45V Programmable Charge Regulation Voltage with ±0.5% Accuracy
- 100mA to 3A Programmable Input Current Limit with ±10% Accuracy
- Minimum Input Voltage Loop for Maximum Adapter Power Tracking
- Ultra-Low 25μA Battery Discharge Current in Idle Mode
- Boost Converter w/ Up to 3.6A Output Current:
  - Programmable Output Current Limit Loop
  - Programmable Boost Output Voltage
  - USB Output Cable Compensation
  - Programmable Inductor Peak Current Limiting
- Comprehensive Safety Features
  - Fully-Customizable JEITA Profile with Programmable Temperature Threshold
  - Charge Safety Timer
  - Input Over-Voltage Protection
  - Thermal Shutdown
  - SYS Over-Current and Short Protection
- Analog Voltage Output IB Pin for Battery Current Monitoring
- SYS Plug-In Detection
- SYS No Load Detection
- SYS DP/DM Interface for BC1.2 and Non-Standard Adapters
- Status and Fault Monitoring
- Available in a QFN-21 (3mmx3mm) Package

## APPLICATIONS

- Sub-Battery Applications
- Power Bank Applications for Smartphone, Tablet, and Other Portable Devices

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2696AGQ-0000** | QFN-21 (3mmx3mm) | *See Below* |
| EVKT-MP2696A | Evaluation kit | |

* For Tape & Reel, add suffix -Z (e.g. MP2696AGQ-xxxx-Z).

**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "xxxx" value.

## TOP MARKING

BKZY

LLL

BKZ: Product code of MP2696AGQ
Y: Year code
LLL: Lot number

## EVALUATION KIT EVKT-MP2696A

EVKT-MP2696A kit contents (items below can be ordered separately):

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EV2696A-Q-00B | MP2696A evaluation board | 1 |
| 2 | EVKT-USBI2C-02 bag | Includes one USB to I²C communication interface, one USB cable, and one ribbon cable | 1 |
| 3 | Online resources | Include datasheet, user guide, product brief, and GUI | 1 |

**Order directly from MonolithicPower.com or our distributors.**

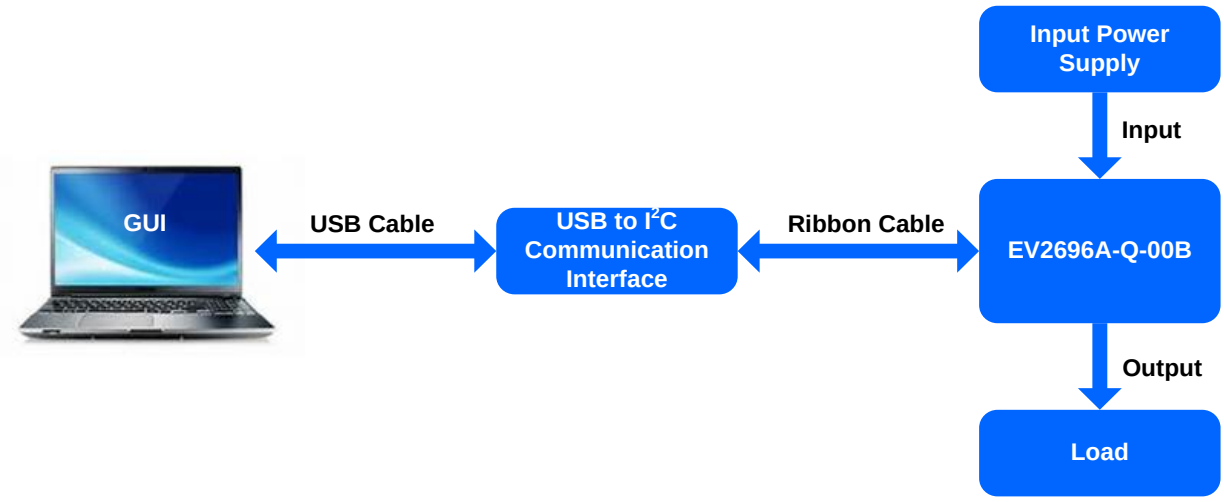
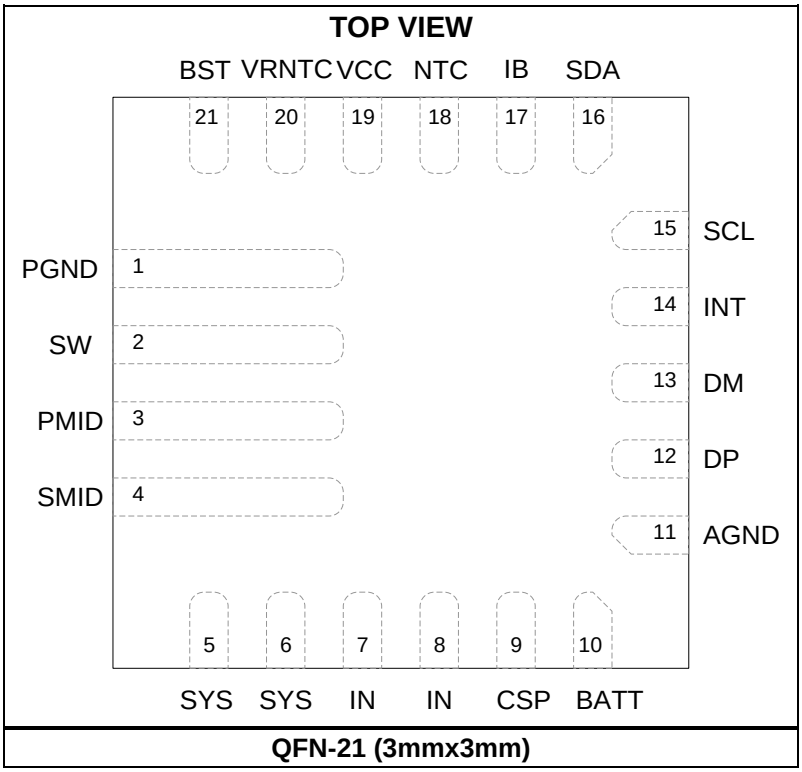



**Figure 1: EVKT-MP2696A Evaluation Kit Set-Up**

# PACKAGE REFERENCE




QFN-21 (3mmx3mm)

## PIN FUNCTIONS

| Pin # | Name | I/O | Description |
|---|---|---|---|
| 1 | PGND | Power | **Power ground.** |
| 2 | SW | Power | **Switching output node.** Connect SW to the inductor. |
| 3 | PMID | Power | **Drain of the high-side switching MOSFET.** Bypass PMID with ceramic capacitors from PMID to PGND, placed as close to the IC as possible. This pin cannot carry an external load. |
| 4 | SMID | Power | **Connected to the drain of Q1 and Q2.** Short SMID to PMID on the PCB. |
| 5,6 | SYS | Power | **System power output.** Place ceramic capacitors from SYS to PGND. |
| 7,8 | IN | Power | **Power input of the IC.** Place ceramic capacitors from IN to PGND. |
| 9 | CSP | I | **Battery current sense positive input.** |
| 10 | BATT | I | **Battery positive terminal**. |
| 11 | AGND | Power | **Analog ground.** Short to PGND on the PCB. |
| 12 | DP | I/O | **Positive port of the USB data for the output.** High ESD rating. |
| 13 | DM | I/O | **Negative port of the USB data for the output.** High ESD rating. |
| 14 | INT | O | **Open-drain interrupt output.** Connect INT to the logic rail through a 10kΩ resistor. |
| 15 | SCL | I | **I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor. |
| 16 | SDA | I/O | **I²C interface data**. Connect SDA to the logic rail through a 10kΩ resistor. |
| 17 | IB | O | **Battery current indicator.** The voltage at IB indicates the charge current to the battery in charge mode, and the discharge current of the battery in boost mode. |
| 18 | NTC | I | **Temperature sense input.** Connect NTC to a negative temperature coefficient thermistor. Program the temperature window with a resistor divider from VRNTC to NTC to GND. Programmable JEITA thresholds are supported. |
| 19 | VCC | Power | **Internal circuit and switch driver power supply.** Bypass to AGND with a ceramic capacitor as close to the IC as possible. For the external load capacity, see the VCC Power Supply section on page 16. |
| 20 | VRNTC | Power | **Reference voltage output for powering up NTC.** |
| 21 | BST | Power | **Bootstrap.** Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the high-side power switch driver. |

## ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, SMID, SYS to PGND ... -0.3V to +16V
SW to PGND ..... -0.3V (-2V for 20ns) to ..... +14V (16V for 20ns)
BST to PGND..... SW to SW + 5V
All other pins to AGND..... -0.3V to +5V
Continuous power dissipation ($T_A$ = 25°C) (2) .....2.5W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage Temperature.....-65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 4V to 11V
Input current ($I_{IN}$)..... Up to 3A
System current ($I_{SYS}$)..... Up to 3.6A
Charge current ($I_{CC}$) ..... Up to 3.6A
Battery voltage ($V_{BATT}$) ..... Up to 4.5V
Operating junction temp ($T_J$) .... -40°C to +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

QFN-21 (3mmx3mm) ..... 50 ..... 12 ... °C/W

## *ESD Ratings*

DP, DM pins:
Human body model (HBM) (5) ..... 8000V
Charged device model (CDM) (6) ..... 800V
All other pins:
Human body model (HBM) (5) ..... 2000V
Charged device model (CDM) (6) ..... 250V

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Per ANSI/ESDA/JEDEC JS-001.
6) Per JESD22-C101.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, RS1 = 10mΩ, $T_A$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Quiescent Current** | | | | | | |
| Battery discharge current in IDLE mode | $I_{BATT\_IDLE}$ | Idle mode | | 25 | 36 | μA |
| Input quiescent current without switching | $I_{IN\_Q}$ | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{IN}$ > $V_{BATT}$ + $V_{HDRM}$, charge disabled, float SYS | | 0.6 | 1 | mA |
| Input quiescent current when switching | $I_{IN\_QSW}$ | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{IN}$ > $V_{BATT}$ + $V_{HDRM}$, charge enabled, float BATT and SYS | | 1 | | mA |
| Battery discharge current in boost mode | $I_{BOOST\_Q}$ | $I_{SYS}$ = 0, VBOOST[2:0] = 5.15V, boost enabled, $V_{BATT}$ = 4.2V | | 2 | | mA |
| **Power On/Off** | | | | | | |
| IN operating range | $V_{IN\_OP}$ | Converter switching | 4 | | 11 | V |
| Input under-voltage lockout | $V_{IN\_UV}$ | $V_{IN}$ falling | 2.95 | 3.10 | 3.25 | V |
| Input under-voltage lockout hysteresis | | $V_{IN}$ rising | | 305 | | mV |
| Input vs. battery headroom | $V_{HDRM}$ | $V_{IN}$ rising | | 200 | 310 | mV |
| | | $V_{IN}$ falling | 10 | 80 | | mV |
| Battery under-voltage lockout | $V_{BATT\_UV}$ | During boost | 2.4 | 2.5 | 2.6 | V |
| | | Before boost starts | 2.8 | 2.9 | 3.0 | V |
| VCC LDO output voltage | $V_{VCC}$ | $V_{IN}$ = 5V, $I_{VCC}$ = 30mA | 3.3 | 3.55 | 3.8 | V |
| VCC under-voltage lockout | $V_{CC\_UV}$ | VCC rising | 1.9 | 2.1 | 2.3 | V |
| VCC under-voltage lockout hysteresis | | | | 80 | | mV |
| **Power Path** | | | | | | |
| IN to PMID FET (Q1) on resistance | $R_{ON\_Q1}$ | | | 25 | | mΩ |
| PMID to SYS FET (Q2) on resistance | $R_{ON\_Q2}$ | | | 15 | | mΩ |
| High-side FET (Q3) on resistance | $R_{ON\_HS}$ | | | 15 | | mΩ |
| Low-side FET (Q4) on resistance | $R_{ON\_LS}$ | | | 14 | | mΩ |
| Peak current limit for high-side FET in buck mode | $I_{HS\_PK}$ | CC charge mode | | 6.5 | | A |
| | | Pre-charge mode | | 1.3 | | A |
| Peak current limit for low-side FET in boost mode | $I_{LS\_PK}$ | BST_IPK[1:0] = 6.5A | 5.9 | 6.6 | 7.3 | A |
| | | BST_IPK[1:0] = 5A | 4.1 | 4.8 | 5.5 | A |
| Switching frequency | $f_{SW}$ | SW_FREQ = 700kHz | | 720 | | kHz |
| | | SW_FREQ = 1200kHz | | 1200 | | kHz |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, RS1 = 10mΩ, $T_A$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Charge Mode** | | | | | | |
| Charge voltage regulation | $V_{BATT\_REG}$ | BATT_REG range (7) | 3.6 | | 4.45 | V |
| | | BATT_REG[2:0] = 3.6V | 3.582 | 3.6 | 3.618 | V |
| | | BATT_REG[2:0] = 4.1V | 4.080 | 4.1 | 4.120 | V |
| | | BATT_REG[2:0] = 4.2V | 4.179 | 4.2 | 4.221 | V |
| | | BATT_REG[2:0] = 4.3V | 4.279 | 4.3 | 4.321 | V |
| | | BATT_REG[2:0] = 4.35V | 4.328 | 4.35 | 4.372 | V |
| | | BATT_REG[2:0] = 4.4V | 4.378 | 4.40 | 4.422 | V |
| | | BATT_REG[2:0] = 4.45V | 4.428 | 4.45 | 4.472 | V |
| Fast charge current | $I_{CC}$ | ICC[4:0] = 3A | 2.7 | 3 | 3.4 | A |
| | | ICC[4:0] = 1.5A | 1.35 | 1.5 | 1.7 | A |
| | | ICC[4:0] = 0.5A | 0.41 | 0.5 | 0.6 | A |
| Charge termination current | $I_{TERM}$ | ITERM[1:0] = 100mA | 40 | 100 | 160 | mA |
| | | ITERM[1:0] = 200mA | 100 | 200 | 300 | mA |
| Recharge threshold below $V_{BATT\_REG}$ | $V_{RECH}$ | $V_{BATT}$ falling | 100 | 200 | 320 | mV |
| Pre-charge to fast charge threshold | $V_{BATT\_PRE}$ | $V_{BATT}$ rising | 2.9 | 3.0 | 3.1 | V |
| Pre-charge to fast charge hysteresis | | $V_{BATT}$ falling | | 290 | | mV |
| Pre-charge current | $I_{PRE}$ | IPRE[1:0] = 150mA, $V_{BATT}$ = 1.8V | | 150 | | mA |
| | | IPRE[1:0] = 350mA, $V_{BATT}$ = 1.8V | | 350 | | mA |
| Safety timer for charging cycle | | | | 20 | | hours |
| **Input Regulation** | | | | | | |
| Input minimum voltage regulation | $V_{IN\_MIN}$ | VINMIN[2:0] = 4.5V | 4.41 | 4.51 | 4.61 | V |
| | | VINMIN[2:0] = 4.65V | 4.56 | 4.66 | 4.76 | V |
| Input current limit | $I_{IN\_LIM}$ | IINLIM[2:0] = 3A | 2.7 | 2.85 | 3 | A |
| | | IINLIM[2:0] = 1.5A | 1.3 | 1.4 | 1.5 | A |
| | | IINLIM[2:0] = 0.5A | 0.4 | 0.45 | 0.5 | A |
| **Boost Mode** | | | | | | |
| Boost output voltage at PMID | $V_{PMID\_BST}$ | VBOOST[2:0] = 5.15V, $I_{SYS}$ = 10mA | 5.05 | 5.13 | 5.21 | V |
| | | VBOOST[2:0] = 5.225V, $I_{SYS}$ = 10mA | 5.13 | 5.21 | 5.29 | V |
| Boost output current limit | $I_{BST\_LMT}$ | IOLIM[3:0] = 3.6A | 3.55 | 3.7 | 3.85 | A |
| | | IOLIM[3:0] = 2.8A | 2.7 | 2.8 | 2.9 | A |
| | | IOLIM[3:0] = 2.1A | 1.9 | 2.05 | 2.15 | A |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, RS1 = 10mΩ, $T_A$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Analog Control** | | | | | | |
| SYS no load current threshold | $I_{BST\_OFF}$ | NOLOAD_THR[1:0] = 30mA | | 30 | | mA |
| | | NOLOAD_THR[1:0] = 50mA | | 50 | | mA |
| | | NOLOAD_THR[1:0] = 75mA | | 75 | | mA |
| | | NOLOAD_THR[1:0] = 100mA | | 100 | | mA |
| SYS plug-in detection threshold | $V_{PLUG\_IN}$ | SYS falling, percentage of $V_{BATT}$ | 70 | 75 | 80 | % |
| Discharge dummy load at IN | $R_{IN\_DUM}$ | | | 250 | | Ω |
| Discharge dummy load at SYS | $R_{SYS\_DUM}$ | | | 30 | | Ω |
| **Protection** | | | | | | |
| Battery over-voltage threshold | $V_{BATT\_OVP}$ | | 102 | 104 | 106 | % |
| BATT over-voltage hysteresis | | | | 1.5 | | % |
| IN over-voltage protection | $V_{IN\_OVP}$ | $V_{IN}$ rising, VIN_OVP = 6V | 5.8 | 6 | 6.2 | V |
| | | $V_{IN}$ rising, VIN_OVP = 11V | 10.6 | 11 | 11.4 | V |
| IN over-voltage protection hysteresis | | $V_{IN}$ falling | | 300 | | mV |
| **Thermal Shutdown and Temperature Control** | | | | | | |
| Thermal shutdown rising threshold (7) | $T_{J\_SHDN}$ | $T_J$ rising | | 150 | | °C |
| Thermal shutdown hysteresis (7) | | | | 20 | | °C |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, RS1 = 10mΩ, $T_A$ = 25°C, unless otherwise noted.**

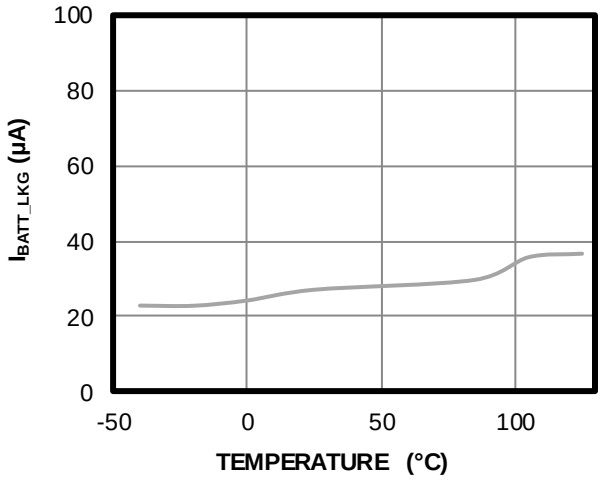
| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VRNTC voltage | $V_{VRNTC}$ | $V_{IN}$ = 5V, $I_{VRNTC}$ = 100μA | | 3.5 | | V |
| NTC low temp rising threshold | $V_{COLD}$ | As percentage of $V_{VRNTC}$, VCOLD[1:0] = 72% | 72 | 73.1 | 74.3 | % |
| NTC low temp rising threshold hysteresis | | As percentage of $V_{VRNTC}$ | | 1.6 | | % |
| NTC cool temp rising threshold | $V_{COOL}$ | As percentage of $V_{VRNTC}$, VCOOL[1:0] = 60% | 59.7 | 61 | 62.2 | % |
| NTC cool temp rising threshold hysteresis | | As percentage of $V_{VRNTC}$ | | 1.6 | | % |
| NTC warm temp falling threshold | $V_{WARM}$ | As percentage of $V_{VRNTC}$, VWARM[1:0] = 40% | 39.4 | 40.6 | 42 | % |
| NTC warm temp falling threshold hysteresis | | As percentage of $V_{VRNTC}$ | | 1.6 | | % |
| NTC hot temp falling threshold | $V_{HOT}$ | As percentage of $V_{VRNTC}$, VHOT[1:0] = 36% | 35.3 | 36.6 | 37.9 | % |
| NTC hot temp falling threshold hysteresis | | As percentage of $V_{VRNTC}$ | | 1.6 | | % |
| **SYS DP/DM Signaling** | | | | | | |
| DP/DM source voltage 2V7 | $V_{SRC\_2V7}$ | | 2.6 | 2.7 | 2.8 | V |
| DP/DM source resistance | $R_{SRC}$ | | 23 | 30 | 37 | kΩ |
| DP/DM comparator threshold 2.9V | $V_{TH\_2V9}$ | | 2.75 | 2.9 | 3.1 | V |
| DP/DM comparator threshold 2.1V | $V_{TH\_2V1}$ | | 1.95 | 2.1 | 2.25 | V |
| Deglitch time for exiting non-standard adapter | | | 8 | 10 | 12 | ms |
| DP/DM short resistance | $R_{SHORT}$ | | | 100 | | Ω |
| Pull-down resistor on DP pin | $R_{PULL\_DWN}$ | | | 300 | | kΩ |
| Timer for DCP to enter non-standard adapter | | | | 2 | | s |
| **I²C Interface** | | | | | | |
| Input high threshold level | | SDA and SCL | 1.3 | | | V |
| Input low threshold level | | SDA and SCL | | | 0.4 | V |
| Output low threshold level | | $I_{SINK}$ = 5mA | | | 0.3 | V |
| I²C clock frequency | $f_{SCL}$ | | | | 400 | kHz |
| **Battery Current Indicator** | | | | | | |
| IB voltage output | | $I_{CC}$ = 1A in charge mode | 0.33 | 0.35 | 0.37 | V |
| | | $I_{DSCHG}$ = 1A in boost mode | 0.15 | 0.16 | 0.17 | V |

**Notes:**

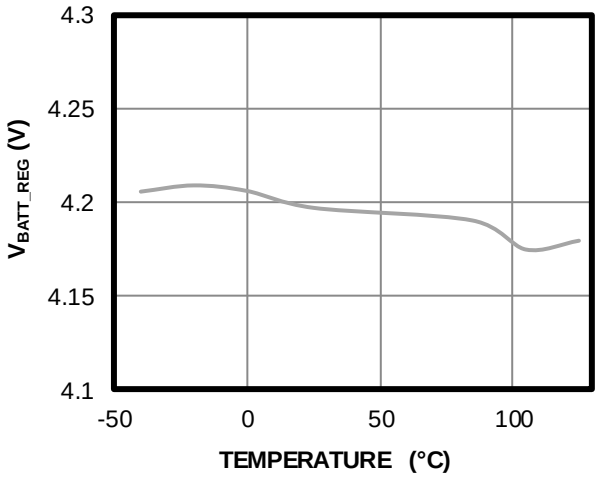
7) Guaranteed by design.

## TYPICAL CHARACTERISTICS

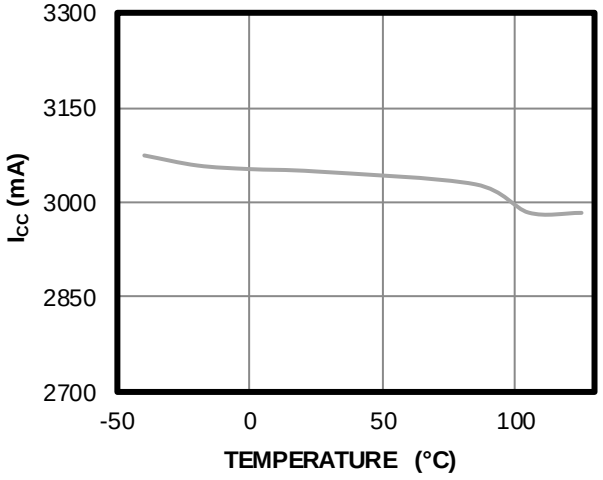
**$I_{BATT\_LKG}$ @ BATT = 5V vs. Junction Temperature**



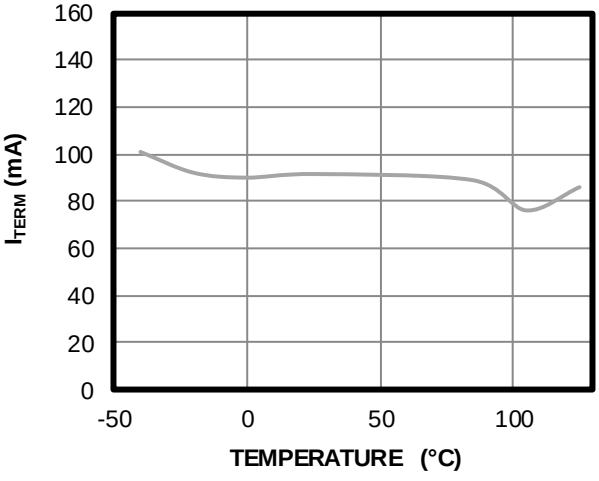

**$V_{BATT\_REG}$ = 4.2V vs. Junction Temperature**



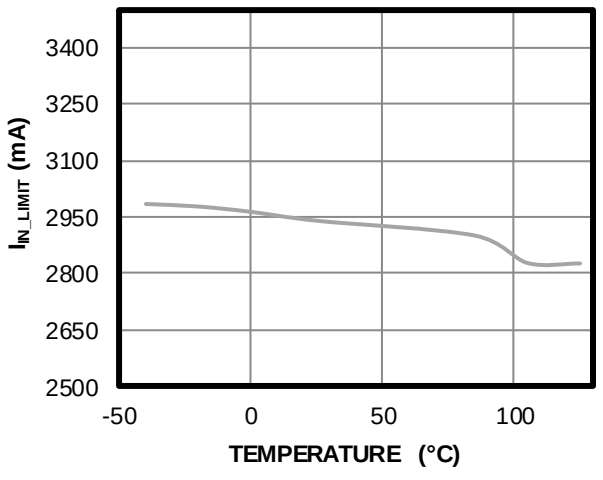

**$I_{CC}$ = 3A vs. Junction Temperature**



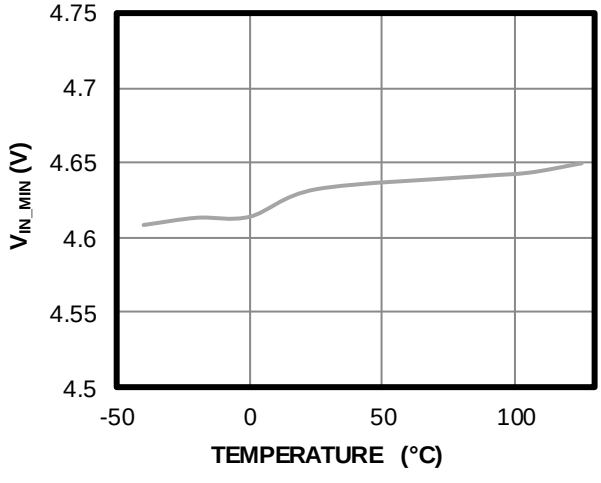

**$I_{TERM}$ = 100mA vs. Junction Temperature**




**$I_{IN\_LIMIT}$ = 3A vs. Junction Temperature**

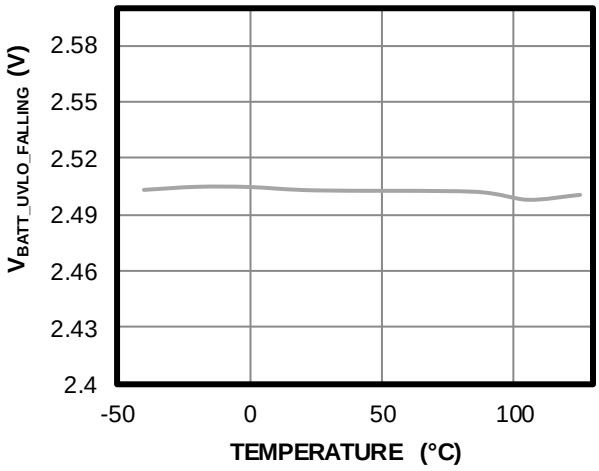



**$V_{IN\_MIN}$ = 4.65V vs. Junction Temperature**

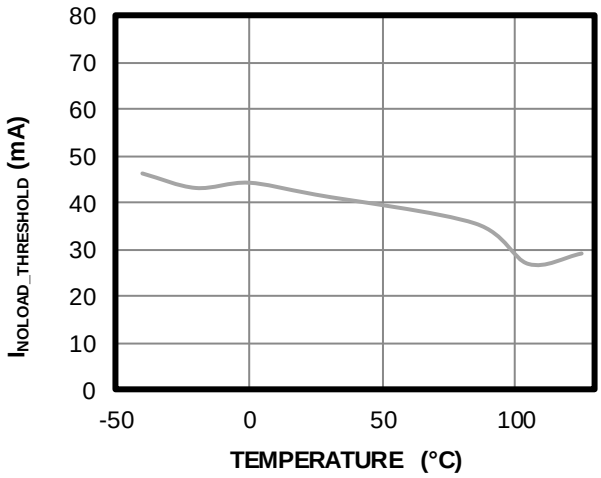


## TYPICAL CHARACTERISTICS *(continued)*

**$V_{BATT\_UVLO\_FALLING}$ vs. Junction Temperature**




**$I_{NOLOAD\_THRESHOLD}$ = 30mA vs. Junction Temperature**

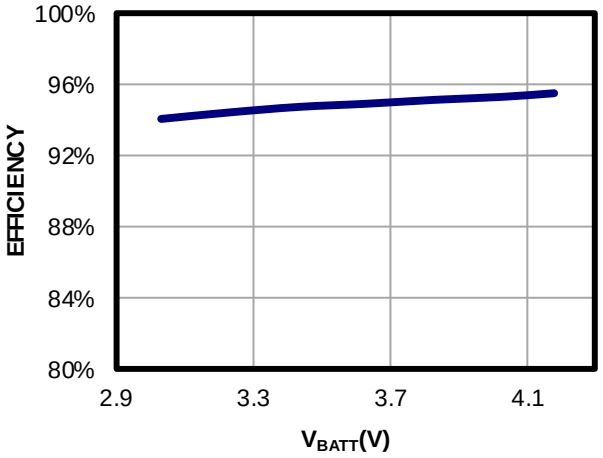


# TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, battery simulator load, unless otherwise noted.**

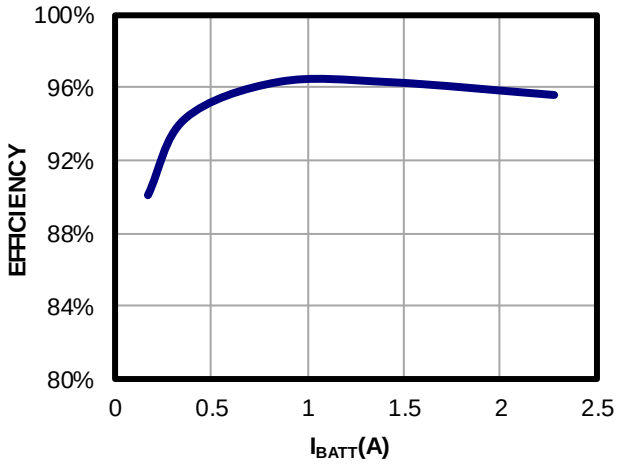
### Constant Current Charge Efficiency

$V_{IN}$ = 5V, $I_{CHG}$ = 2.5A, DCR = 6.5mΩ



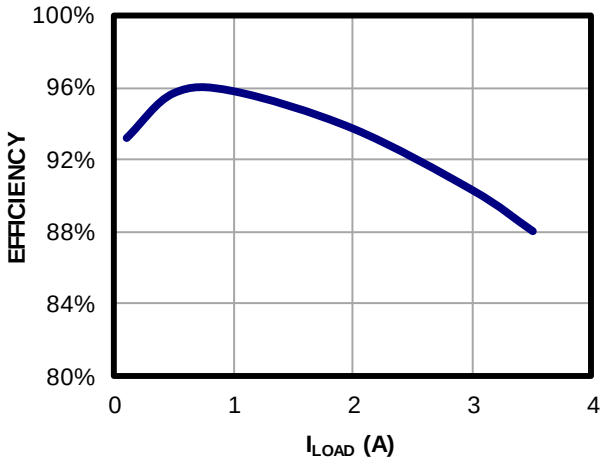

### Constant Voltage Charge Efficiency

$V_{IN}$ = 5V, $V_{BATT}$ = 4.2V, DCR = 6.5mΩ



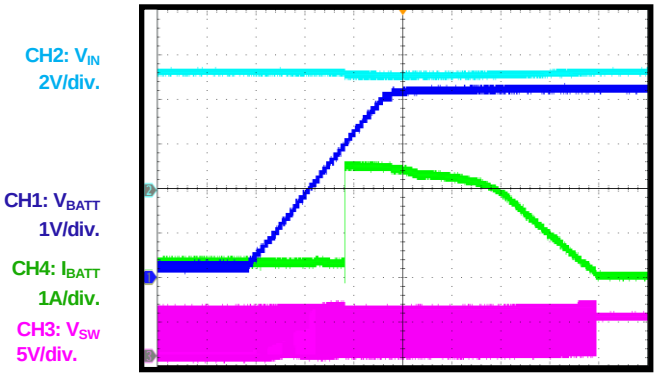

### Boost Mode Efficiency

$V_{BATT}$ = 3.5V, $V_{SYS}$ = 5.15V, DCR = 6.5mΩ




### Battery Charge Curve

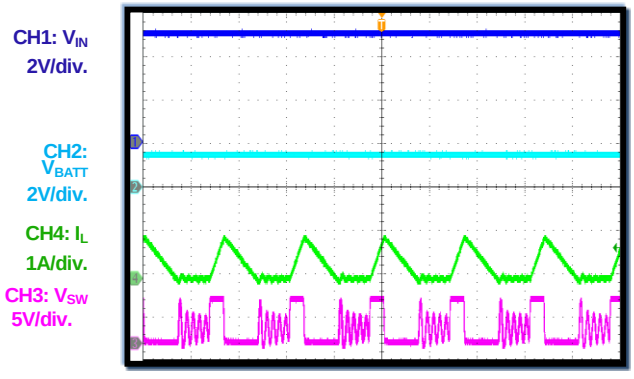
$V_{IN}$ = 5V




4s/div.

### Pre-Charge Steady State

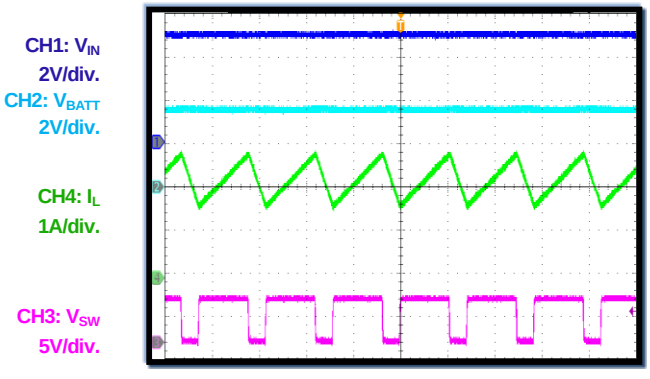
$V_{IN}$ = 5V, $V_{BATT}$ = 1.5V, $I_{PRE}$ = 150mA




1µs/div.

### CC Charge Steady State

$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, $I_{CC}$ = 2A



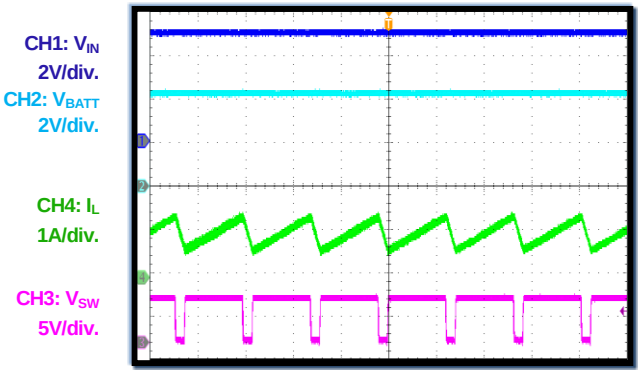

1µs/div.

## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$T_A$ = 25°C, battery simulator load, unless otherwise noted.**

### CV Charge Steady State

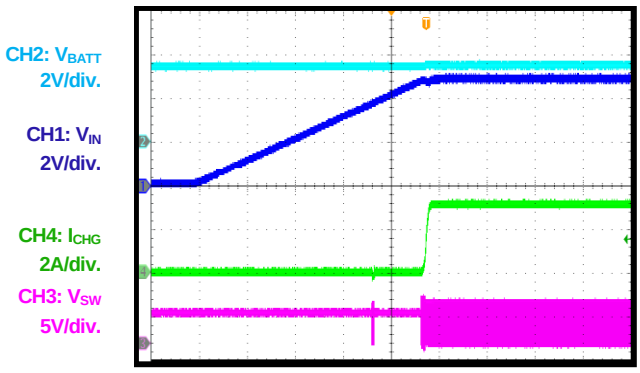
$V_{IN}$ = 5V, $V_{BATT}$ = 4.2V




1µs/div.

### Power-On, CC Charge Mode

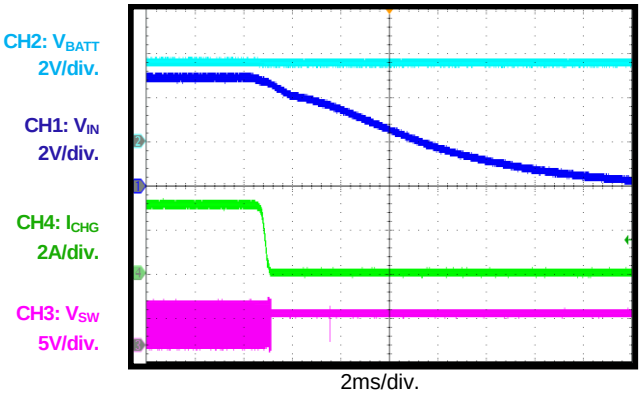
$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, $I_{CC}$ = 3A




2ms/div.

### Power-Off, CC Charge Mode

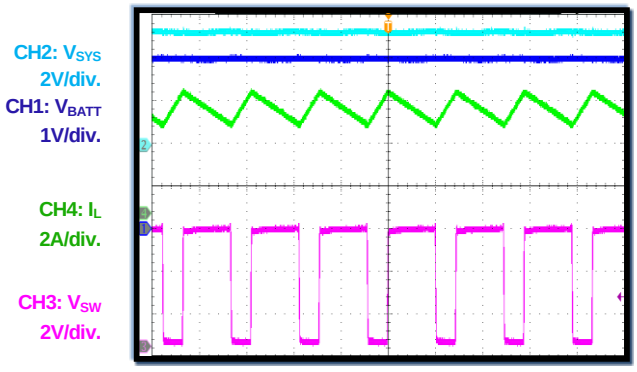
$V_{IN}$ = 5V, $V_{BATT}$ = 3.5V, $I_{CC}$ = 3A




2ms/div.

### Boost Steady State

$V_{BATT}$ = 4V, $I_{SYS}$ = 3.5A




1µs/div.

# FUNCTIONAL BLOCK DIAGRAM

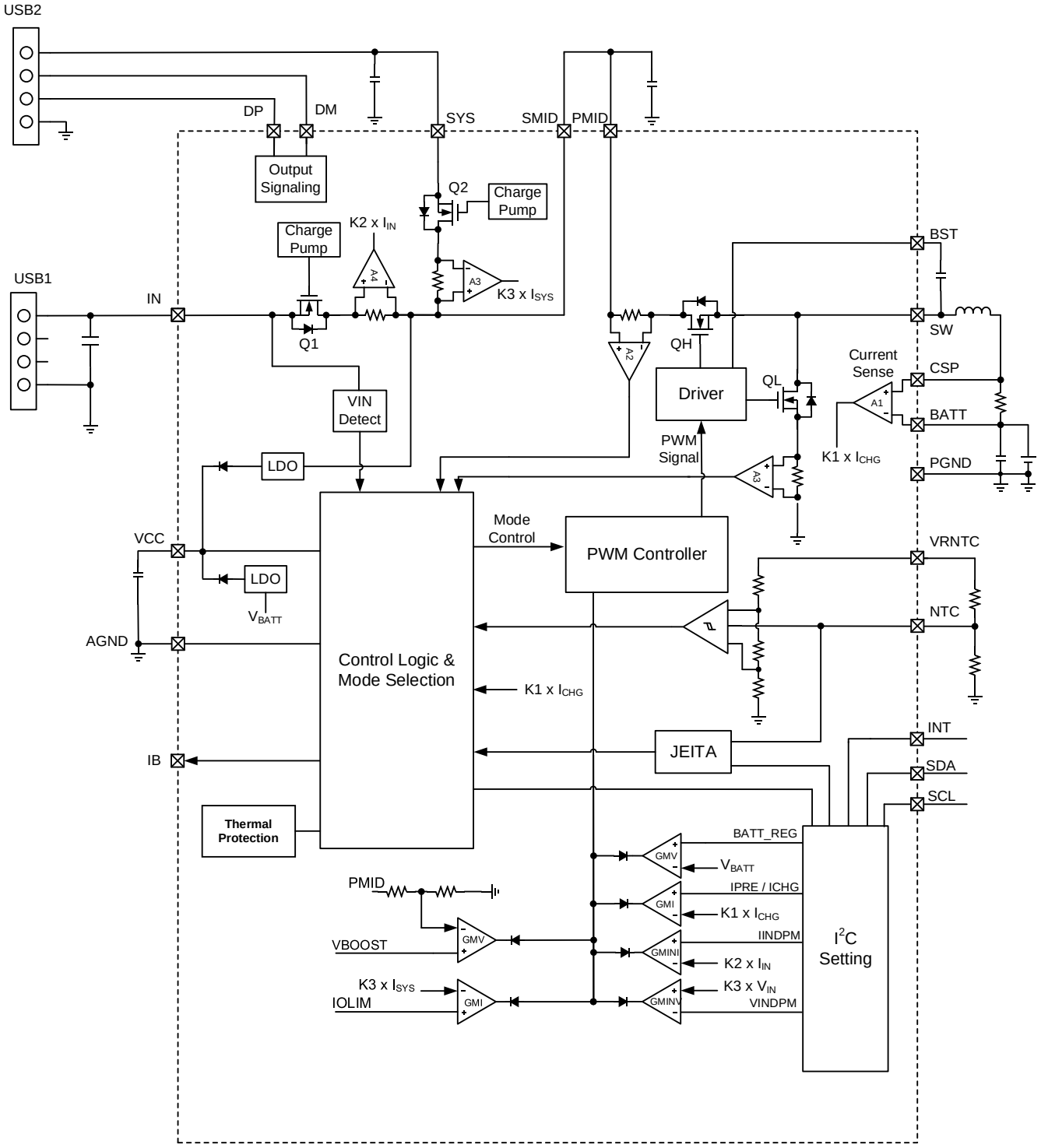



**Figure 2: Functional Block Diagram**

# OPERATION

## Introduction

The MP2696A is an I²C-controlled switching charger with bidirectional operation that can step up the battery voltage ($V_{BATT}$) to power the system. Depending on the input and output status, it operates in one of the three modes: charge mode, boost mode, or idle mode. In charge mode, the IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, the IC boosts $V_{BATT}$ to a regulated voltage at SYS for powering the load. In idle mode, the IC stops charging or boosting and operates at a low current from the input or the battery to reduce the power consumption when the IC is not operating.

## VCC Power Supply

VCC provides power for the internal bias circuit, as well as the low-side switch driver. VCC is powered from whichever voltage is the highest between PMID and BATT. When the VCC voltage rises above the $V_{VCC\_UV}$ threshold, the I²C interface is ready for communication, and all the registers are reset to the default value. When the device is switching, VCC can provide up to 30mA for the external load.

# CHARGER MODE OPERATION

## Battery Charging Profile

The IC can run a charging cycle autonomously without host involvement. Also, the host can control the charge operations and parameters via the registers.

A new charge cycle can start when the following conditions are valid:

- $V_{IN}$ is above $V_{IN\_UV}$
- $V_{IN}$ is below $V_{IN\_OVP}$
- $V_{IN}$ is above $V_{BATT}$ + $V_{HDRM}$
- The NTC voltage is in the proper range (if the NTC_STOP bit is set to 1)
- No charge timer fault
- Charging is enabled (CHG_EN=1)
- No battery over-voltage

After the charge is done, unplug and re-insert VIN or toggle the CHG_EN bit to start a new charge cycle.

## Charge Cycle

The IC checks the battery voltage to provide three main charging phases: pre-charge, constant-current (CC) charge, and constant-voltage (CV) charge.

The IC regulates the voltage drop on the current-sense resistor (RS1) for the battery pre-charge and constant-current charge current. Table 1 shows the default value for a 10mΩ resistor.

**Table 1: Charge Current vs. Battery Voltage (RS1 = 10mΩ)**

| Battery Voltage | Charge Current | Default Value | CHG_STAT |
|---|---|---|---|
| BATT < 3V | IPRE[1:0] | 150mA | 01 |
| BATT > 3V | ICC[4:0] | 1A | 10 |

The charge current can be scaled by implementing different current-sense resistor values. The fast-charge current ($I_{CC}$) can be calculated with Equation (1):

$$I_{CC} = \frac{ICC[4:0] * 10m\Omega}{RS1} \quad (1)$$

The pre-charge current ($I_{PRE}$) can be calculated with Equation (2):

$$I_{PRE} = \frac{IPRE[4:0] * 10m\Omega}{RS1} \quad (2)$$

Note that the soldering tin for the current-sense resistor has resistance, which needs to be compensated.

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as the input current limit or the input voltage limit.

## Charge Termination

Charging terminates if all the following conditions are met:

- The charge current is below the termination threshold for 20ms
- The IC works in a constant-voltage charge loop
- The IC is not in the input current loop or input voltage loop

After termination, the status register CHG_STAT is set to 11, and an INT pulse is generated.

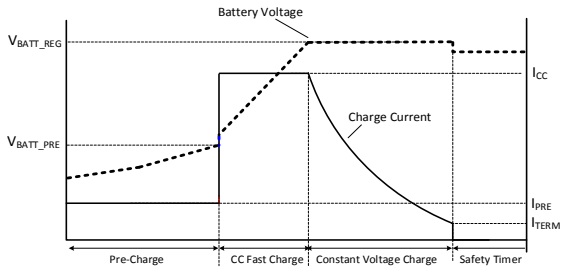



**Figure 3: Battery Charge Profile**

## Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When $V_{BATT}$ is discharged below the recharge threshold ($V_{BATT\_REG}$ - 200mV), the IC starts a new charging cycle automatically if the input power is valid. The timer resets when the auto-recharge cycle begins.

## Safety Timer

The IC provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer feature can be disabled via the I²C. The safety timer does not operate in boost mode.

The safety timer resets at the beginning of a new charging cycle. Two actions can restart the safety timer: a new charge cycle starting, or the EN_TIMER bit being toggled.

If the safety timer expires before the charge is done, then an INT pulse is generated, the charge cycle stops, and CHG_FAULT[1:0] becomes 11 (signaling a safety timer expiration). To clear this fault, unplug and reinsert VIN once the safety timer expires.

## Input Voltage Based and Input Current Based Power Management

The IC features both input current and input voltage based power management by monitoring the input current and input voltage continuously.

When the input current reaches the limit set by IINLIM[2:0], the charge current tapers off to keep the input current from increasing further.

If the preset input current limit is higher than the adapter rating, the backup input voltage based power management also works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold set by VINMIN[2:0] due to the heavy load, the charge current is also reduced to keep the input voltage from dropping further.

An INT pulse is generated once the device enters a VINPPM or INPPM condition.

## Thermistor Qualification

VRNTC is driven to be the same as the VCC voltage when the IC is in charge/boost mode. The IC monitors the battery's temperature continuously by measuring the voltage at the NTC pins. The NTC function can be disabled by setting EN_NTC = 0.

When NTC_STOP is set to 1, the NTC voltage should be within the $V_{HOT}$ to $V_{COLD}$ range for both charge and boost operation. The IC resumes switching when the NTC voltage returns to the $V_{HOT}$ to $V_{COLD}$ range.

When NTC_STOP is set to 0, the IC only generates an interrupt (INT) signal and reports the NTC pin status if the NTC_FAULT[2:0] bits have any changes.

JEITA profile is supported when the JEITA_DIS bit is set to 0.

At a cool temperature ($V_{COLD}$ to $V_{COOL}$) range, the charge current is reduced according to the JEITA_ISET[1:0] setting (see Figure 4).

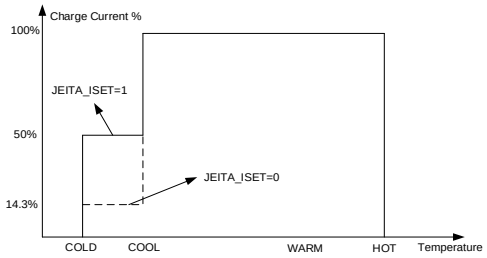



**Figure 4: JEITA Profile – Charge Current**

At a warm temperature ($V_{WARM}$ to $V_{HOT}$) range, the charge voltage is reduced according to the JEITA_VSET[1:0] setting (see Figure 5).

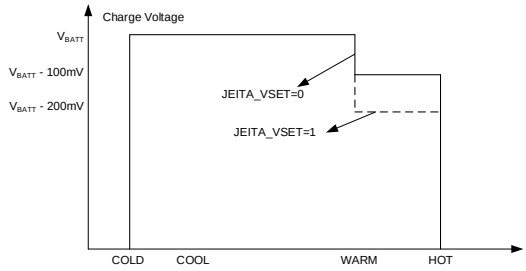



**Figure 5: JEITA Profile – Charge Voltage**

The HOT and COLD thresholds have two options in the register. The WARM and COOL thresholds have four options in the register, which offers accurate and flexible JEITA control.

### Interrupt to Host (INT)

A 50μs interrupt pulse is generated on the open-drain INT pin when any of the events below occur:

- A good input source is detected
- A USB2 plug-in is detected
- Status register 05h changes
- Fault register 06h changes

### Battery Over-Voltage Protection (OVP)

If $V_{BATT}$ exceeds 104% of $V_{BATT\_REG}$, then the IC stops charging, BATT_OVP is set to 1, and an INT pulse is generated. An 800μA current source discharges the battery until it returns to the normal range.

Battery over-voltage protection (OVP) can be disabled by setting BATT_OVP_DIS to 1.

### Input Over-Voltage Protection (OVP)

If IN senses a voltage above the VIN_OVP threshold, then the DC/DC converter shuts down.

The input OVP threshold can be 6V, 11V, or set via VIN_OVP.

## BOOST MODE OPERATION

The IC can supply a regulated 5V output at SYS to power the system. If $V_{BATT}$ is below 2.9V, then the IC does not operate in boost mode to avoid draining the battery. In order to enable boost mode, $V_{IN}$ must be below 2V.

The boost output current limit can be set between 2.1A and 3.6A. If $V_{SYS} > V_{BATT}$, then boost mode has an output current limit loop.

In boost mode, the IC first boosts PMID to the preset voltage, and then the block FET (Q2) turns on linearly. Once $V_{SYS}$ exceeds 4.2V within 3ms, Q2 is turned on completely. Otherwise, Q2 turns off and tries to restarts again after 300ms.

### Boost Power Limitation

During boost operation, the peak inductor current in each switching cycle is limited by the peak current limit of the low-side switch (Q4) BST_IPK[1:0] bits. This limits the maximum battery discharge current.

### Battery Under-Voltage Lockout (UVLO) Protection

Once $V_{BATT}$ drops below 2.5V during boost operation, boost mode stops and BATT_UVLO is set to 1. Boost mode recovers once $V_{BATT}$ exceeds 2.9V. BATT_UVLO does not reset until the input source plug-in and battery is charged again.

### SYS Over-Current and Short Protection

In boost mode, the MP2696A monitors the current flowing through Q2. If the SYS output current exceeds the preset boost output current limit, then the output current loop takes control and both the PMID voltage ($V_{PMID}$) and SYS voltage ($V_{SYS}$) decrease. If $V_{SYS}$ drops to $V_{BATT}$ + 200mV, then Q2 turns off. Q2 tries to restart again after 300ms.

The IC also features fast SYS over-current protection (OCP) in both boost mode and pass-through mode. If the Q2 current exceeds 8A, then Q2 turns off. Q2 tries to restart again after 300ms.

### Impedance Compensation for Boost Output

The Q2 intrinsic resistance and the USB2 output wire voltage drop can be compensated by adjusting the boost output voltage according to the system load current. The PMID voltage ($V_{PMID}$) can be calculated with Equation (3):

$$V_{PMID} = V_{BOOST} + (I_{SYS} \times R_{SYS\_CMP}) \quad (3)$$

Where $V_{BOOST}$ is the boost regulation voltage set by VBOOST[2:0], $I_{SYS}$ is the real-time SYS load current during operation, and $R_{SYS\_CMP}$ is the line resistance compensation set by RSYS_CMP[2:0].

### USB2 Plug-In Detection

If USB2_EN_PLUG is on in standby mode, then SYS is pulled up to BATT. Detection starts once $V_{SYS}$ reaches 90% of $V_{BATT}$. If the system voltage drops to 75% of $V_{BATT}$, then the USB2 plug-in is detected, USB2_PLUG_IN is set to 1, and an INT pulse signal is generated.

The host responds to the INT signal and enables boost mode/Q2.

**For the next detection, the host must clear USB2_PLUG_IN and toggle USB2_EN_PLUG. Writing 1 to USB2_PLUG_IN clears it to 0.**

### No Load Detection

Q2 current is monitored in boost mode and pass-through mode. If the Q2 current is below NOLOAD_THR[1:0], then NO_LOAD is set to 1

and an INT pulse is generated. The host can monitor NO_LOAD and decide whether boost mode/Q2 should be turned off.

### Thermal Shutdown

The IC monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the IC's junction temperature exceeds the threshold value (typically 150°C), then the converter shuts down. If the junction temperature drops to about 120ºC, the MP2696A resumes normal operation.

### Battery Current Analog Output

The IC has an IB pin to monitor the real-time battery current in both charge mode and boost mode. The IB voltage ($V_{IB}$) is a fraction of the battery current. It indicates the current flowing in and out of the battery during charge mode and boost mode.

If using a 10mΩ current-sense resistor in charge mode, the IB voltage ($V_{IB}$) can be calculated with Equation (4):

$$V_{IB} = I_{CHG} \times 0.36(V) \quad (4)$$

If using a 10mΩ current-sense resistor in boost mode, the IB voltage ($V_{IB}$) can be calculated with Equation (5):

$$V_{IB} = I_{DSCHG} \times 0.16(V) \quad (5)$$

Note that scaling the current-sense resistor also scales the IB gain.

### Idle Mode

If the input power source is not present and boost mode is disabled, then the IC goes into idle mode. In idle mode, all the FETs and most of the internal circuits are turned off to minimize leakage and extend the battery runtime.

### SYS DP/DM Signaling

For a nonstandard adapter imitation, the DP and DM pins are initially biased at 2.7V, with a 30kΩ internal resistance.

The IC operates in DCP mode when the DP or DM pin is outside of the 2.1V to 2.9V range for 10ms. The 2.7V reference is disconnected, and DP and DM are tied together via a 100Ω resistor.

If DP is less than 0.35V for 2s in DCP mode, then the IC returns to nonstandard adapter mode with a DP/DM biased at 2.7V.

### Series Interface

The IC uses an I²C interface for setting the charging parameters and device status reporting. The I²C is a two-wire serial interface with two bus lines: a serial data line (SDA) and serial clock line (SCL). Both SDA and SCL are open drains that must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device (e.g. a micro-controller). SCL is driven by the master device. The I²C interface supports both standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s).

All transactions begin with a start (S) command and are terminated by a stop (P) command. The start and stop commands are generated by the master. A start command is defined as a high to low transition on SDA while SCL is high. A stop command is defined as a low to high transition on SDA while SCL is high. Figure 6 shows the start and stop commands.

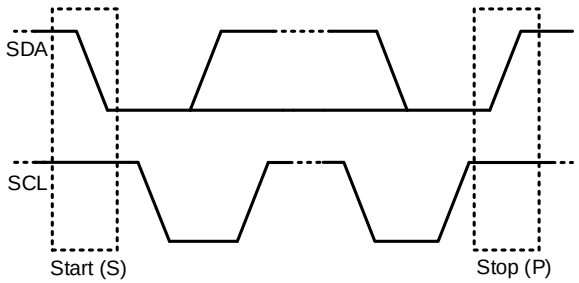



**Figure 6: Start and Stop Conditions**

For data validity, the data on SDA must be stable during the high clock period. The SDA high and low states only change if the clock signal on SCL is low. Every byte on SDA must be 8 bits long. The number of bytes transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

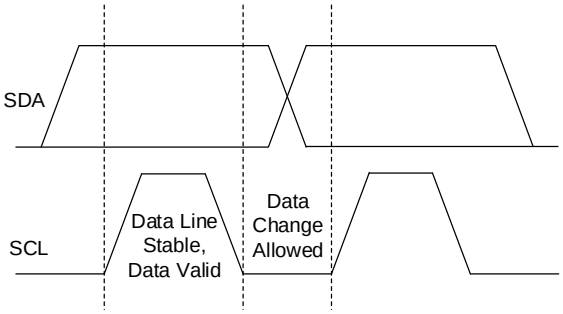



**Figure 7: Bit Transfer on the I²C Bus**

To signal that a byte was successfully received by the transmitter, each byte has to be followed by an acknowledge (ACK) bit generated by the receiver.

The ACK signal is defined as follows: The transmitter releases SDA during the ACK clock pulse and the receiver pulls SDA low. SDA remains low during the 9th clock's high period.

If SDA is high during the 9th clock, then the signal is defined as a not acknowledged (NACK) signal. The master then generates either a stop to abort the transfer or a repeated start to begin a new transfer.

After the start signal, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (bit R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 8 shows the address arrangement.

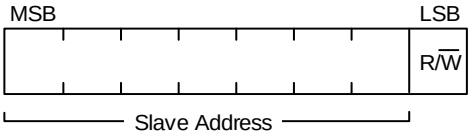



**Figure 8: 7-Bit Addressing**

See Figure 9, Figure 10, Figure 11, Figure 12, and Figure 13 for detailed signal sequences.

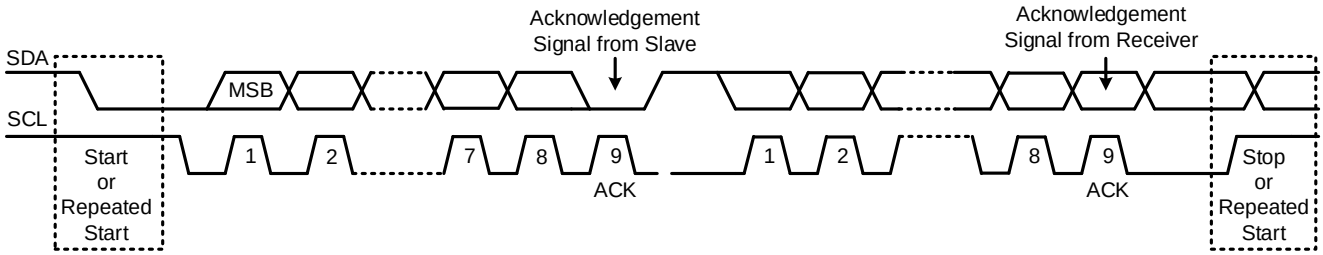



**Figure 9: Data Transfer on the I²C Bus**

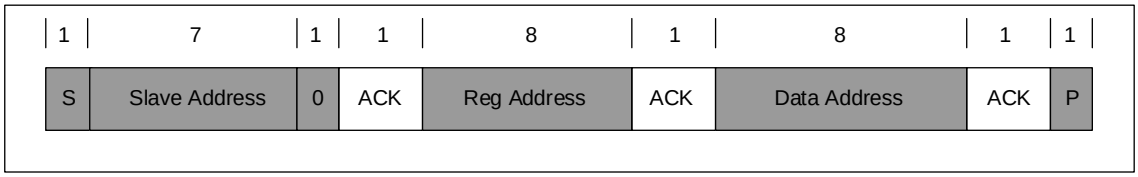



**Figure 10: Single-Write**

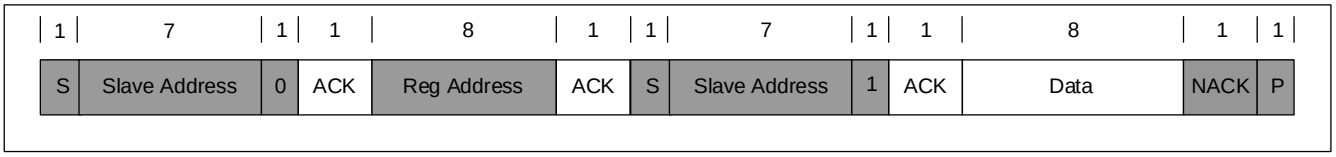



**Figure 11: Single-Read**

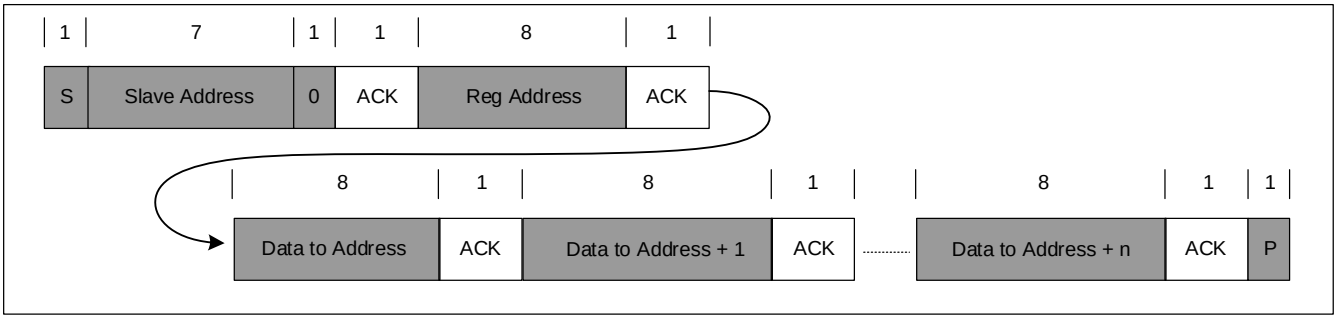



**Figure 12: Multi-Write**


**Figure 13: Multi-Read**

# I²C REGISTER MAP

## IC Address: 6Bh

| Register Name | Address | R/W | Description |
|---|---|---|---|
| REG00h | 0x00 | R/W | Input voltage regulation setting and input current limit setting. |
| REG01h | 0x01 | R/W | Charge current setting and pre-charge current setting. |
| REG02h | 0x02 | R/W | Battery regulation voltage and termination current setting. |
| REG03h | 0x03 | R/W | Boost output current limit setting and cable impedance compensation. |
| REG04h | 0x04 | R/W | Boost output voltage setting and boost control. |
| REG05h | 0x05 | R | Status register. |
| REG06h | 0x06 | R | Fault register. |
| REG07h | 0x07 | R/W | Boost no load setting and miscellaneous control. |
| REG08h | 0x08 | R/W | JEITA control. |

## REG 00h

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | REG_RST | 0 | Y | R/W | 0: Keeps current setting<br>1: Reset | Resets all registers to default. After reset, this bit returns to 0. |
| 6 | EN_TIMER | 1 | Y | R/W | 0: Disabled<br>1: Enabled (default) | Enables the safety timer. |
| 5 | VINMIN[2] | 1 | Y | R/W | 200mV (default) | Sets the input voltage dynamic regulation.<br>Offset: 4.45V<br>Range: 4.45V to 4.8V<br>Default: 4.65V (200mV) |
| 4 | VINMIN[1] | 0 | Y | R/W | 100mV | |
| 3 | VINMIN[0] | 0 | Y | R/W | 50mV | |
| 2 | IINLIM[2] | 0 | Y | R/W | 000: 100mA<br>001: 500mA (default)<br>010: 1000mA<br>011: 1500mA<br>100: 1800mA<br>101: 2100mA<br>110: 2400mA<br>111: 3000mA | Sets the input current limit. |
| 1 | IINLIM[1] | 0 | Y | R/W | | |
| 0 | IINLIM[0] | 1 | Y | R/W | | |

### REG 01h

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | ICC[4] | 0 | Y | R/W | 1600mA | Sets the charge current for the 10mΩ current-sense resistor.<br>Offset: 500mA<br>Range: 500mA to 3.6A<br>Default: 1A<br>A scaling current-sense resistor scales the setting at the same ratio. |
| 6 | ICC[3] | 0 | Y | R/W | 800mA | |
| 5 | ICC[2] | 1 | Y | R/W | 400mA | |
| 4 | ICC[1] | 0 | Y | R/W | 200mA | |
| 3 | ICC[0] | 1 | Y | R/W | 100mA | |
| 2 | EN_NTC | 1 | Y | R/W | 0: Disabled<br>1: Enabled (default) | |
| 1 | IPRE[1] | 0 | Y | R/W | 01: 150mA (default)<br>10: 250mA<br>11: 350mA | Sets the pre-charge current for the 10mΩ current-sense resistor.<br>Range: 150mA to 350mA |
| 0 | IPRE[0] | 1 | Y | R/W | | |

### REG 02h

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | BATT_OVP_DIS | 0 | Y | R/W | 0: Enabled (default)<br>1: Disabled | Enables OVP battery function. |
| 6 | BATT_REG[2] | 0 | Y | R/W | 000: 3.6V<br>001: 4.1V<br>010: 4.2V (default)<br>011: 4.3V<br>100: 4.35V<br>101: 4.4V<br>110: 4.45V | Sets the charge voltage regulation. |
| 5 | BATT_REG[1] | 1 | Y | R/W | | |
| 4 | BATT_REG[0] | 0 | Y | R/W | | |
| 3 | JEITA_DIS | 1 | Y | R/W | 0: Enabled<br>1: Disabled (default) | Enables JEITA.<br>0: JEITA enabled, NTC warm/cool decreases ICC or $V_{BATT\_REG}$<br>1: JEITA disabled, NTC warm/cool only reports status and INT |
| 2 | ITERM[1] | 0 | Y | R/W | 200mA | Sets the charge termination current for the 10mΩ current-sense resistor.<br>Offset: 100mA<br>Range: 100mA to 400mA |
| 1 | ITERM[0] | 0 | Y | R/W | 100mA | |
| 0 | CHG_EN | 1 | Y | R/W | 0: Disabled<br>1: Enabled (default) | Enables charge mode. |

### REG 03h

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | IOLIM[1] | 1 | Y | R/W | 800mA | Sets the SYS output current limit.<br>Offset: 2.1A<br>Range: 2.1A to 3.6A<br>Default: 3A |
| 6 | IOLIM[0] | 0 | Y | R/W | 400mA | |
| 5 | IOLIM[1] | 0 | Y | R/W | 200mA | |
| 4 | IOLIM[0] | 1 | Y | R/W | 100mA | |
| 3 | RSYS_CMP[2] | 0 | Y | R/W | 80mΩ | Sets the SYS cable voltage drop compensation.<br>Default: 60mΩ |
| 2 | RSYS_CMP[1] | 1 | Y | R/W | 40mΩ | |
| 1 | RSYS_CMP[0] | 1 | Y | R/W | 20mΩ | |
| 0 | NO_LOAD | 0 | Y | R | 0: Q2 normal load<br>1: Q2 no load | |

### REG 04h

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | VBOOST[2] | 0 | Y | R/W | -100mV | Sets the PDIM pin's boost regulation voltage.<br>Offset: 5.2V<br>Range: 5.05V to 5.225V<br>Default: 5.15V |
| 6 | VBOOST[1] | 1 | Y | R/W | -50mV | |
| 5 | VBOOST[0] | 0 | Y | R/W | 25mV | |
| 4 | BST_EN | 0 | Y | R/W | 0: Disabled (default)<br>1: Enabled | Enables boost mode. Boost mode can only be enabled once $V_{IN}$ < 2V. |
| 3 | Q2_EN | 0 | Y | R/W | 0: Off (default)<br>1: On | Turns Q2 on. |
| 2 | SYS_DSC | 0 | Y | R/W | 0: Disabled<br>1: Enabled | Enables the SYS to GND discharge resistance (25Ω). |
| 1 | USB2_EN_PLUG | 1 | Y | R/W | 0: Disabled<br>1: Enabled | Enables the USB2 plug-in detection circuit. Toggle this bit for new detection. |
| 0 | USB2_PLUG_IN | 0 | Y | R/W | 0: USB2 is not plugged in<br>1: USB2 plug-in detected | If SYS exceeds 90% of $V_{BATT}$, then plug-in detection begins. If SYS drops to 75% of $V_{BATT}$, then the USB2 plug-in signal is asserted.<br>Write 1 to reset this bit to 0. This bit should be cleared manually after read to enable the next detection. |

**REG 05h**

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | CHIP_STAT[1] | 0 | Y | R | 00: Idle<br>01: Charge mode<br>10: Boost mode<br>11: Power path and charge mode | |
| 6 | CHIP_STAT[0] | 0 | Y | R | | |
| 5 | CHG_STAT[1] | 0 | Y | R | 00: Not charging<br>01: Pre-charge mode<br>10: CC or CV charge mode<br>11:Charge complete | |
| 4 | CHG_STAT[0] | 0 | Y | R | | |
| 3 | VPPM_STAT | 0 | Y | R | 0: Does not enter $V_{IN\_LIM}$ loop<br>1: Enters $V_{IN\_LIM}$ loop | |
| 2 | IPPM_STAT | 0 | Y | R | 0: Does not enter $I_{IN\_LIM}$ loop<br>1: Enters $I_{IN\_LIM}$ loop | |
| 1 | USB1_PLUG_IN | 0 | Y | R | 0: USB1 is not plugged in<br>1: USB1 is plugged in | If ($V_{IN\_UV}$, $V_{BATT}$ + $V_{HDRM}$) < $V_{IN}$ < $V_{IN\_OVP}$, then this bit is set to 1. |
| 0 | RESERVED | 0 | Y | R | | |

An interrupt signal is asserted when any bit in this register changes.

**REG 06h**

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | BATT_UVLO | 0 | Y | R | 0: No Battery ULVO<br>1: Battery UVLO | If $V_{BATT}$ is below the UVLO threshold, then this bit is set to 1.<br>Once the battery is charged again, this bit resets to 0. |
| 6 | SYS_SHORT | 0 | Y | R | 0: Normal<br>1: SYS short circuit | |
| 5 | BST_LMT | 0 | Y | R | 0: Normal<br>1: Boost mode works in Q2 current limit | |
| 4 | CHG_FAULT[1] | 0 | Y | R | 00: Normal<br>01: USB1 UV<br>10: USB1 OV<br>11: Safety timer expiration | |
| 3 | CHG_FAULT[0] | 0 | Y | R | | |
| 2 | NTC_FAULT[2] | 0 | Y | R | 000: Normal<br>001: Warm<br>010: Cool<br>011: Cold<br>100: Hot | |
| 1 | NTC_FAULT[1] | 0 | Y | R | | |
| 0 | NTC_FAULT[0] | 0 | Y | R | | |

An interrupt signal is asserted when any bit in this register changes.

**REG 07h**

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | NOLOAD_THR[1] | 0 | Y | R/W | 00: 30mA (default)<br>01: 50mA<br>10: 75mA<br>11:100mA | Sets the SYS no load current threshold. |
| 6 | NOLOAD_THR[0] | 0 | Y | R/W | | |
| 5 | BATT_OVP | 0 | Y | R | 0: Battery normal<br>1: Battery OVP | |
| 4 | NTC_STOP | 1 | Y | R/W | 0: NTC out of window, only reports in register<br>1: NTC out of window, suspends the charge and boost operation | |
| 3 | VIN_OVP | 0 | Y | R/W | 0: 6V<br>1: 11V | |
| 2 | SW_FREQ | 0 | Y | R/W | 0: 700kHz (default)<br>1: 1200kHz | |
| 1 | BST_IPK[1] | 1 | Y | R/W | 00: 5A<br>01: 5.5A<br>10: 6A<br>11: 6.5A (default) | Low-side switch peak current limit in boost mode. |
| 0 | BST_IPK[0] | 1 | Y | R/W | | |

**REG 08h**

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | JEITA_VSET | 1 | Y | R/W | 0: $V_{BATT\_REG}$ - 100mV<br>1: $V_{BATT\_REG}$ - 200mV | Default: $V_{BATT\_FULL}$ - 200mV |
| 6 | JEITA_ISET | 1 | Y | R/W | 0: 14.3% of $I_{CC}$<br>1: 50% of $I_{CC}$ (default) | |
| 5 | VHOT | 1 | Y | R/W | 0: 34%<br>1: 36% (default) | Sets the hot threshold. |
| 4 | VWARM[1] | 0 | Y | R/W | 00: 44%<br>01: 40% (default)<br>10: 38%<br>11: 36% | Sets the warm threshold. |
| 3 | VWARM[0] | 1 | Y | R/W | | |
| 2 | VCOOL[1] | 1 | Y | R/W | 00: 72%<br>01: 68%<br>10: 64%<br>11: 60% (default) | Sets the cool threshold. |
| 1 | VCOOL[0] | 1 | Y | R/W | | |
| 0 | VCOLD | 0 | Y | R/W | 0: 72% (default)<br>1: 68% | Sets the cold threshold. |

## REG 0Ah (8)

| Bit | Name | POR | Reset by REG_RST | R/W | Description | Comment |
|---|---|---|---|---|---|---|
| 7 | TMR | 0 | N/A | N/A | 0: 20hr charge timer (default)<br>1: 10hr charge timer | |
| 6 | RESERVED | N/A | N/A | N/A | N/A | |
| 5 | RESERVED | N/A | N/A | N/A | N/A | |
| 4 | RESERVED | N/A | N/A | N/A | N/A | |
| 3 | VPRE | 0 | N/A | N/A | 0: 3V pre-charge threshold (default)<br>1: 2.5V pre-charge threshold | |
| 2 | RESERVED | N/A | N/A | N/A | N/A | |
| 1 | RESERVED | N/A | N/A | N/A | N/A | |
| 0 | RESERVED | N/A | N/A | N/A | N/A | |

**Note:**

8) Register 0Ah is for OTP only and is not accessible to users.

## OTP MAP

| # | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| 0x02 | N/A | BATT_REG: 3.6V to 4.45V | | | N/A | N/A | N/A | N/A |
| 0x07 | NOLOAD_THR | | N/A | NTC_STOP | VIN_OVP | N/A | N/A | N/A |
| 0x0A | TMR | N/A | N/A | N/A | VPRE | N/A | N/A | N/A |

## OTP DEFAULT

| OTP Items | Default |
|---|---|
| BATT_REG[2:0] | 4.2V |
| NOLOAD_THR[1:0] | 30mA |
| NTC_STOP | 1: NTC out of window, suspends charge and boost operation |
| VIN_OVP | 0: VIN_OVP is 6V |
| TMR | 0: 20hr charge timer |
| VPRE | 0: 3V pre-charge threshold |

# APPLICATION INFORMATION

## NTC Function

JEITA profile is supported for battery temperature management. For a given NTC thermistor, select an appropriate $R_{T1}$ and $R_{T2}$ to set the NTC window. $R_{T1}$ can be calculated with Equation (6):

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (6)$$

$R_{T2}$ can be calculated with Equation (7):

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC\_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC\_HOT}} \quad (7)$$

Where $R_{NTC\_HOT}$ is the value of the NTC resistor at the upper bound of its operating temperature range, and $R_{NTC\_COLD}$ is its lower bound. $V_{HOT}$ is the hot temperature threshold percentage, which can be selected as 34% or 36%. $V_{COLD}$ is the cold temperature threshold percentage, which can be selected as 72% or 68%.

The warm temperature threshold ($V_{WARM}$) can be calculated with Equation (8):

$$V_{WARM} = \frac{R_{T2} // R_{NTC\_WARM}}{R_{T1} + R_{T2} // R_{NTC\_WARM}} \quad (8)$$

The cool temperature threshold ($V_{COOL}$) can be calculated with Equation (9):

$$V_{COOL} = \frac{R_{T2} // R_{NTC\_COOL}}{R_{T1} + R_{T2} // R_{NTC\_COOL}} \quad (9)$$

Choose the nearest warm/cool threshold in REG08h using the results from the calculations above.

If no external NTC is available, connect $R_{T1}$ and $R_{T2}$ to keep the voltage on NTC within the valid NTC window (e.g. $R_{T1}$ = $R_{T2}$ = 10kΩ).

## Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A lower inductance value means a smaller size, but results in greater current ripple, greater magnetic hysteretic losses, and greater output capacitance. A higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in greater inductor DC resistance (DCR) loss. Table 2 shows recommended values with which to choose an inductor.

**Table 2: Inductance Selection Guide**

| RS1 (mΩ) | Max $I_{CC}$ (A) | L (µH) |
|---|---|---|
| 10 | 3.6 | 1 |
| 20 | 1.8 | 2.2 |
| 30 | 1.2 | 3.3 |
| 50 | 0.72 | 4.7 |

Choose an inductor that does not saturate under the worst-case load condition.

## Selecting the PMID Capacitor ($C_{PMID}$)

Select $C_{PMID}$ based on the demand of the PMID current ripple for the mode being used.

In charge mode, $C_{PMID}$ acts as the input capacitor of the buck converter in charge mode. The input current ripple ($I_{RMS\_MAX}$) can be calculated with Equation (10):

$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (10)$$

In boost mode, $C_{PMID}$ is the output capacitor of the boost converter. $C_{PMID}$ keeps the system voltage ripple small and ensures feedback loop stability. The system current ripple ($I_{RMS\_MAX}$) can be calculated with Equation (11):

$$I_{RMS\_MAX} = I_{BATT} \times \frac{\sqrt{V_{BATT} \times (V_{SYS} - V_{BATT})}}{V_{SYS}} \quad (11)$$

Select the PMID capacitors based on the ripple current temperature rise, not exceeding 10°C. For best results, use ceramic capacitors with X5R dielectrics because of their low ESR and small temperature coefficients.

## Compensate the Current-Sense Resistor

The soldering tin has resistance. For a 10mΩ resistor soldered on the PCB, the total resistance between resistor pads is about 11mΩ to 12mΩ. One compensation method is to apply a resistor divider for the CSP/BATT pins (see Figure 14 on page 30). After the PCB is assembled, apply a 2A DC current source between SW and BATT, measure the voltage drop across the current-sense resistor on its PCB pads ($V_{CS}$). Then R1 can be calculated using Equation (12):

$$R1 = \frac{V_{CS} - 2 \times RS1}{2 \times RS1} \times 10\Omega \quad (12)$$

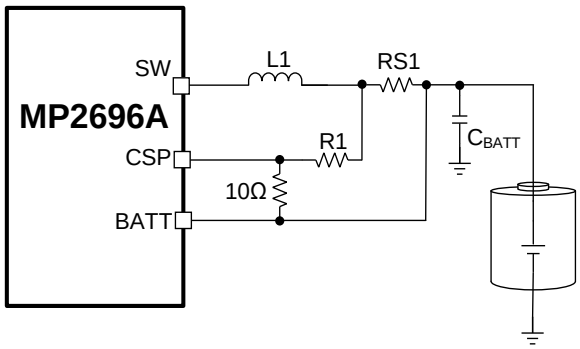



**Figure 14: Current-Sense Compensation**

## PCB Layout Guidelines

Efficient PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best results, follow the guidelines below:

1. Place the PMID capacitor as close as possible to PMID and PGND. The PMID capacitor should have a return to the IC's PMID and PGND pins that is as short as possible.
2. Connect AGND to the ground of the PMID capacitor.
3. Keep the switching node short.
4. The power pads for VIN, PMID, SYS, and PGND should be connected to as many coppers planes on the board as possible to improve thermal performance by conducting heat to the PCB.

## TYPICAL APPLICATION CIRCUIT

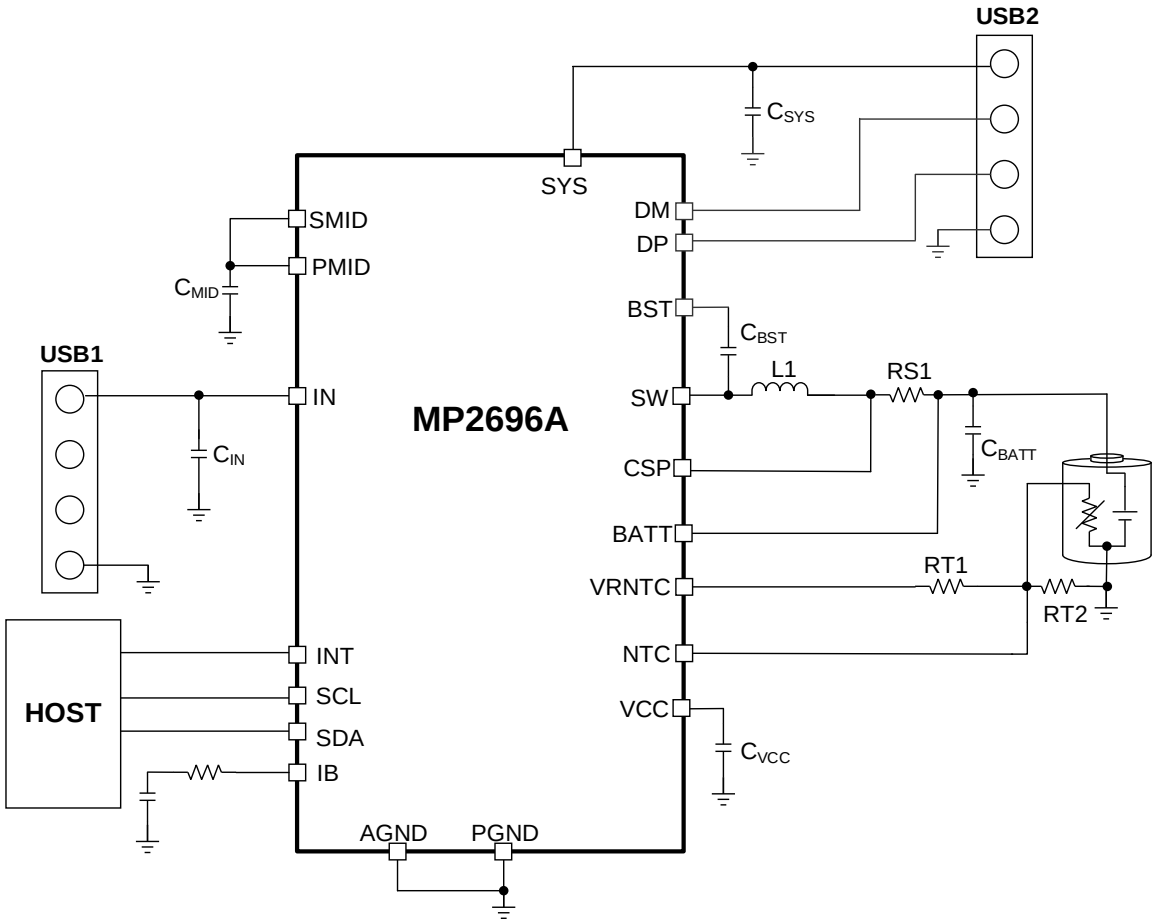


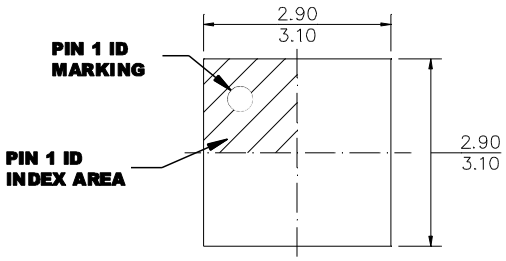

**Figure 15: Typical Application Circuit for Power Bank**

**Table 3: Key BOM for Figure 15**

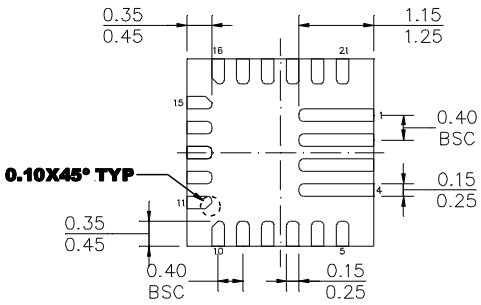
| Qty | Ref | Value | Description | Package | Manufacture |
|---|---|---|---|---|---|
| 1 | $C_{IN}$ | 1μF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | $C_{MID}$ | 10μF | Ceramic capacitor, 16V, X5R or X7R | 0805 | Any |
| 2 | $C_{SYS}$ | 10μF | Ceramic capacitor, 16V, X5R or X7R | 0805 | Any |
| 1 | $C_{BATT}$ | 22μF | Ceramic capacitor, 10V, X5R or X7R | 0805 | Any |
| 1 | $C_{VCC}$ | 2.2μF | Ceramic capacitor, 6.3V, X5R or X7R | 0603 | Any |
| 1 | $C_{BST}$ | 470nF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | L1 | 1μH | Inductor, 1μH, low DCR | SMD | Any |
| 1 | RS1 | 10mΩ | Film resistor, 1% | 1206 | Any |

# PACKAGE INFORMATION

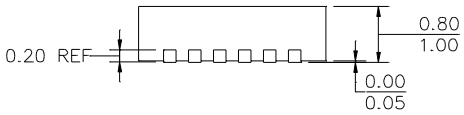
## QFN-21 (3mmx3mm)



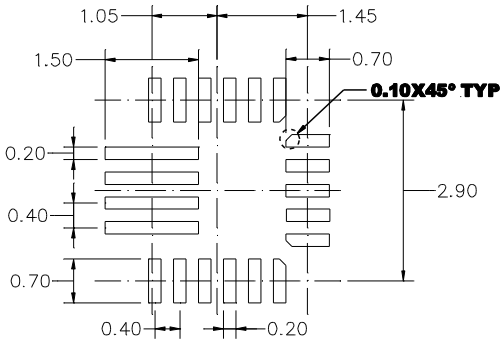

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 07/02/2019 | Initial Release | - |
| 1.01 | 01/15/2020 | Updated the evaluation board part number from “EV2696A-Q-00A” to “EV2696A-Q-00B” in the Evaluation Kit EVKT-MP2696A section | 3 |
| 1.02 | 07/20/2020 | Updated the IB pin I/O description | 5 |
| | | Added comment in the PMID pin description about not carrying current | |
| 1.1 | 04/28/2021 | Updated the I/O property of the IB, SCL, VRNTC, and BST pins in the Pin Functions table | 5 |
| | | Changed the supply voltage range in the Recommended Operating Conditions section from “4.5V to +11V” to “4V to 11V” for consistency | 6 |
| | | Changed IN OVP symbol in the Electrical Characteristics table from “$V_{IN\_OV}$” to “$V_{IN\_OVP}$” for consistency | 9 |
| | | Updated graphs titles | 11–12 |
| | | Changed “$V_{IN\_OV}$” to “$V_{IN\_OVP}$” for consistency; added abbreviation for battery voltage ($V_{BATT}$); updated the ICC default value in Table 1; updated descriptions for Equation 1 and Equation 2 | 16 |
| | | Updated the Safety Timer section; added abbreviation for interrupt (INT) | 17 |
| | | Updated description for Equation 3 | 18 |
| | | Updated descriptions for Equation 4 and Equation 5 | 19 |
| | | Updated I²C sections | 18–21 |
| | | Updated I²C Register Map section | 22–28 |
| | | Updated descriptions for Equations 6 through 12 | 29 |
| | | Updated Package Information | 32 |
| | | Formatting updates and clerical updates; like updated Figure numbers; changed “current-sensing” to “current-sense”; changed “adaptor” to “adapter” | All |

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