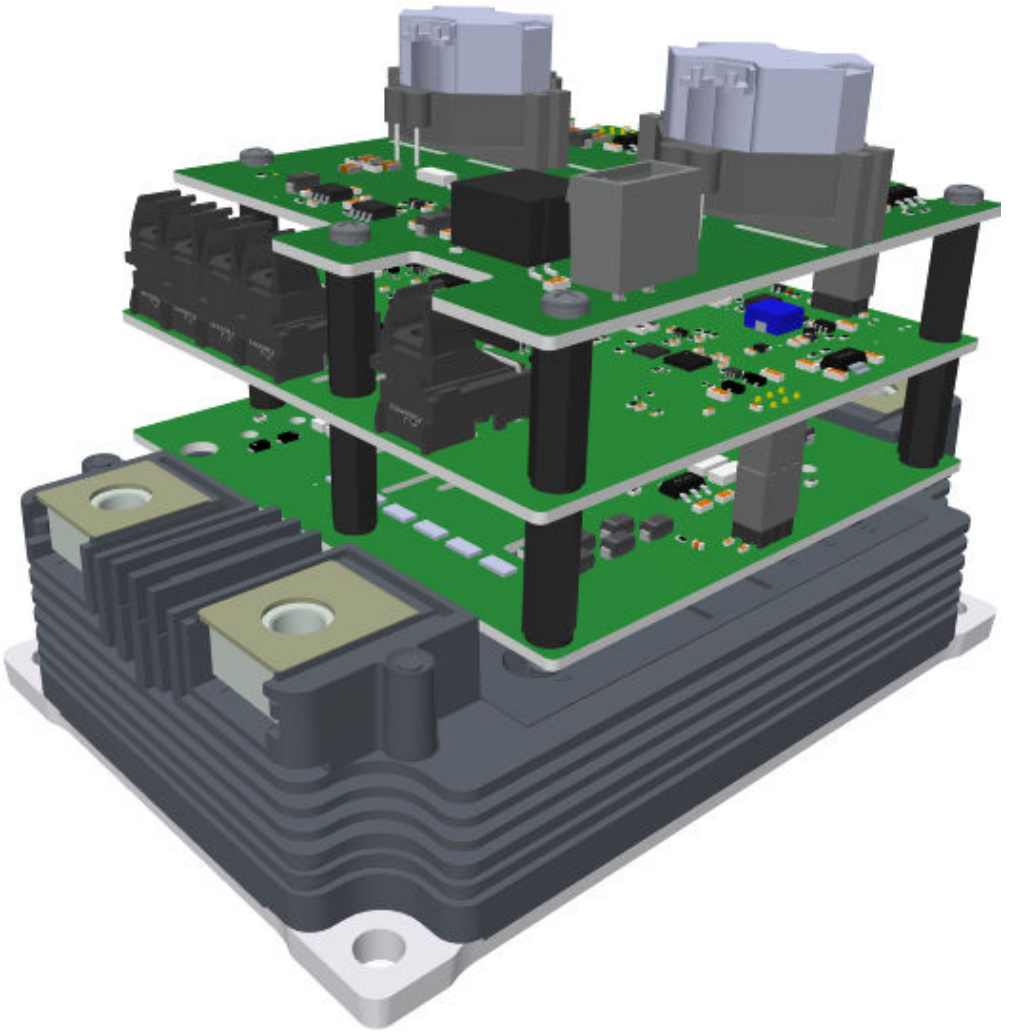
XIFM Intelligent Plug-and-Play 3.3 kV Gate Driver

Product Overview

Microchip XIFM plug-and-play mSiC™ gate driver is designed to drive 3.3 kV SiC modules in High-Voltage (HV) packages such as HV LinPak, HV100 XHP™, or equivalent. It features Augmented Switching™ to enhance the control of the SIC MOSFET-based power systems in normal operation and in fault conditions, such as over-current. The driver includes isolated High (HI) and Low (LO) side DC/DC converters and complies with key rail specifications—EN 50155.

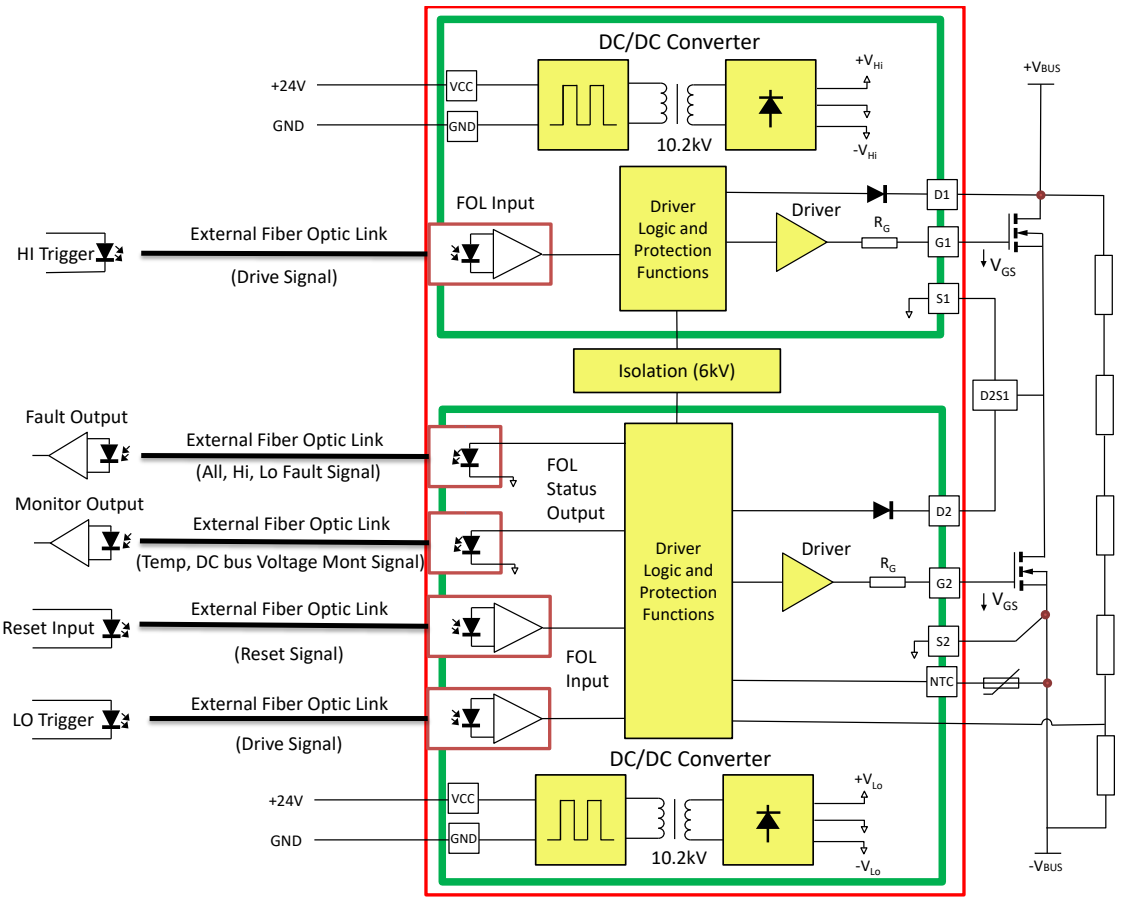
The following figure shows a representative stack-up of the gate driver, which is subject to change without notice.

Figure 1. XIFM Gate Driver—3D View



The following figure shows the basic topology of the XIFM gate driver.

Figure 2. Basic Schematic of the XIFM Gate Driver



The following table lists the fiber optic interface for XIFM gate driver.

Table 1. Fiber Optic Interface

Interface	Description	Part Number
HI trigger input—J5	Fiber optic receiver	FR05DVCR HFBR-2531ETZ[1]
LO trigger input—J4	Fiber optic receiver	
Reset input—J1	Fiber optic receiver	
All fault output—J3	Fiber optic transmitter	FT05MVNR HFBR-1531ETZ[1]
HV/Temp. monitor output—J2	Fiber optic transmitter	

Note:

1. This part number is used in the assembly on special request.

The following table lists the electrical connector for XIFM gate driver.

Table 2. Electrical Connector

Interface	Description	Part Number
J1	24V On-board connector	231-132/001-000

Features

The following sections describes the features of the XIFM gate driver.

1.1 Software Programmable Features

The XIFM gate driver has the following software programmable features:

- Augmented switching
- Power supply Under-Voltage Lockout (UVLO)
- Desaturation detection settings
- Fault lockout settings
- Automatic reset settings
- Positive and negative gate voltage biasing
- Negative Temperature Coefficient (NTC) based measurement settings

1.2 Key Switch Driver Features

The XIFM gate driver has the following key switch driver features:

- Compatible with HV LinPak, HV100 XHP, or any equivalent package
- 10.2 kV primary-to-secondary isolation voltage
- Isolated temperature and DC link monitoring
- 2 × 10W output power
- 15A peak source/sink current
- Configurable gate output voltages
- Compact three boards stack on-board isolated solution
- Soft shutdown time and voltage level

Applications

The XIFM gate driver has the following applications:

- High-speed trains, traction, and hybrid trains
- Railway/Transportation
- Grid
- DC/DC

Standards Compliance Targets

The XIFM gate driver has the following standards compliance targets:

- Railway application compliant to EN50155
- Electromagnetic Compatibility (EMC) compliant to EN 50121-3-2 and EN 61000-6-4
- Shock and vibration to EN 61373
- Fire hazard level—HL2

1. Electrical Specifications

The following sections describes the electrical specifications of the XIFM intelligent plug-and-play 3.3 kV gate driver.

1.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the XIFM gate driver.

Table 1-1. Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
Supply voltage	V_{CC} to GND	0	28	V
Peak gate current	Peak current allowed only for fast charge C_{GS}	−15	15	A
Output power per gate	—	—	10	W
Isolation voltage	Primary-to-secondary, V_{AC} RMS, 1 min	—	10200	V
	Secondary-to-secondary, V_{AC} RMS, 1 min	—	6700	
Clearance distance	Primary-to-secondary side	22	—	mm
	Secondary-to-secondary side	12.5	—	
Creepage distance	Primary-to-secondary side	41	—	
	Secondary-to-secondary side	25	—	
Common Mode Transient Immunity (CMTI)	Rate of change from input to output	100	—	kV/µs
Operating temperature	Ambient operating temperature	−40	85	°C
Storage temperature	—	−40	85	
Voltage measurement	Voltage monitoring on drain of the High-Side (HS) switch against source of the Low-Side (LS) switch	0	2500	V
Temperature measurement	NTC thermistor-based monitoring[1]	−40	150	°C

Note:

1. Software configurable parameter.

1.2 Electrical Characteristics

The following table lists the electrical characteristics of the XIFM gate driver.
Note: Conditions: V_{SUP} = 24V and MOSFET = SiC module 5SFG 0500Z330100.

Table 1-2. Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Power Supply					
Supply voltage	V_{CC} to GND	22	24	27	V
Supply current	Without load	80	85	90	mA
	With load[1]	—	—	340	
Over-Voltage Lockout (OVLO) threshold	Primary side	—	27.5	28	V
OVLO level—HI and LO	Secondary side high voltage detect fault level	—	26.5	—	V
UVLO level—HI and LO	Secondary side low voltage detect fault level	—	16.5	—	V
Coupling capacitance	Primary to secondary	—	11	12	pF
Positive biasing V_{GS} voltage[4]	—	15	—	21	—
Negative biasing V_{GS} voltage[4]	—	−10	—	0	
Signal I/O					
Gate output voltage low[2, 4]	—	—	−10	—	V
Gate output voltage high[2, 4]	—	—	20	—	V

.....continued					
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
Fault output (optical signal output)	Open signal output[8]	—	1 (High on fault)	—	Logic
Turn-on gate resistance	R_{GON}[6]	—	1.1	—	Ω
Turn-off gate resistance	R_{GOFF}[6]	—	1.1	—	Ω
Gate-emitter capacitance	C_{GS}	—	0	—	nF
HV/Temperature monitor output	Open signal output[3]	0.5	—	10	kHz
Temperature range	−40 °C to 150 °C[2]	0.5	—	10	kHz
HV range	0 to 2500V	2.5	—	10	kHz
MOSFET Short Protection					
Desaturation (DSAT) monitor voltage	Between drain and source[2]	—	8.7	—	V
Desaturation Time (T_{DSAT})	DSAT blanking time[2, 7]	—	1	—	µs
Response time after fault	—	—	—	5000	ns

Notes:

1. The preceding SiC MOSFET dependent conditions assume SiC MOSFET module 5SFG 0500Z330100 with C_{iss} = TBD nF; Q_g = 100 nF operating at 20 kHz.
2. Software configurable parameter.
3. Shared between HV and temperature signals. One of them can be selected.
4. Total (+/− V_{GS} voltage threshold must not exceed 27V).
5. Recommended to use ferrite core at supply input lines (Wurth Elektronik P/N 74270031 or 742700381) and shielded cable.
6. Can be configured as per user requirement or application dependent.
7. Hardware blanking time is set to the present value.
8. Software configurable output fault can be set as High or Low on fault, as per requirement.

2. Standard Compliance

The following table lists the standard compliance of the XIFM gate driver.

Table 2-1. Standard Compliance

Test	Description	Test Standard
Dielectric test	10.2 kV_{RMS} AC, 50 Hz, 1 min, primary to secondary	Type test
	6.7 kV_{RMS} AC, 50 Hz, 1 min secondary to secondary	Type test
Impulse test	18 V_{PK} 1.2/50 µs, primary to secondary	Type test (EN 50124-1)
Partial discharge	<10 pC at 2.6 kV_{RMS} extinction, primary to secondary	Type test
Radiated immunity	20 $V/m_{(RMS)}$, 80 MHz to 800 MHz, AM (80%, 1kHz), performance criteria A	EN 61000-4-3
Fast transients immunity	±2 kV, 5/50 ns, 5 kHz, performance criteria A	EN 61000-4-4
Surges immunity	±2 kV, 42Ω, 0.5 µF, 1.2/50 µs, performance criteria B	EN 61000-4-5
Conducted immunity	10 V_{RMS}, AM (80%, 1kHz), performance criteria A	EN 61000-4-6
Radiated emission	30 MHz to 230 MHz / 52 dB(µV/m) to 52 dB(µV/m) quasi-peak at 3m 230 MHz to 1GHz / 52dB quasi-peak at 3m	EN 61000-6-4
Conducted emission	150 kHz to 500 kHz / 99 dBµV quasi-peak 500 kHz to 30 MHz/ 93 dBµV quasi-peak	EN 55016–2–1
Cold test	T_{TEST} = -40 °C	Type test (EN 50155)
Dry heat thermal test	T_{TEST} = 85 °C	Type test (EN 50155)
Cycle damp heat test	With relative humidity (90% to 100%)	Type test (EN 50155)
Mechanical vibration	Category 1 Class B (Functional random vibration, simulated long-life)	Type test (EN 50155)
Mechanical shock	Category 1 Class B (Body mounted)	Type test (EN 50155)

3. General Specifications

The following table lists the general specifications of the XIFM gate driver.

Table 3-1. General Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Humidity	Compliant to EN 50155 railways standard[1]	—	85	95	%
Pollution degree	Class 2	—	—	—	—
Environmental compliance	Reach compliant	—	—	—	—
	RoHS compliant	—	—	—	—
Material flammability rating	UL94V-0 rated	—	—	—	—
Fire hazard level	HL2	—	—	—	—

Note:

1. Device used with conformal coating.

4. Physical Specification

The following table lists the physical specifiactions of the XIFM gate driver.

Table 4-1. Physical Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Length[1]	—	—	—	95.5	mm
Width[1]	—	—	—	95	mm
Height[1]	—	—	—	75	mm
Weight	Total weight of the gate driver (all three boards)[2]	—	—	220	g
Screw torque	Torque on the collector, emitter, high and low side gate terminals.	1	—	1.5	Nm

Notes:

1. Dimensions have a tolerance of ±0.5 mm.
2. Weight can have tolerance of ±10g.

5. Timing Diagrams

The following figures show the timing diagrams of the XIFM gate driver.

Figure 5-1. Signal Input/Output Timing Diagram for Normal Operation

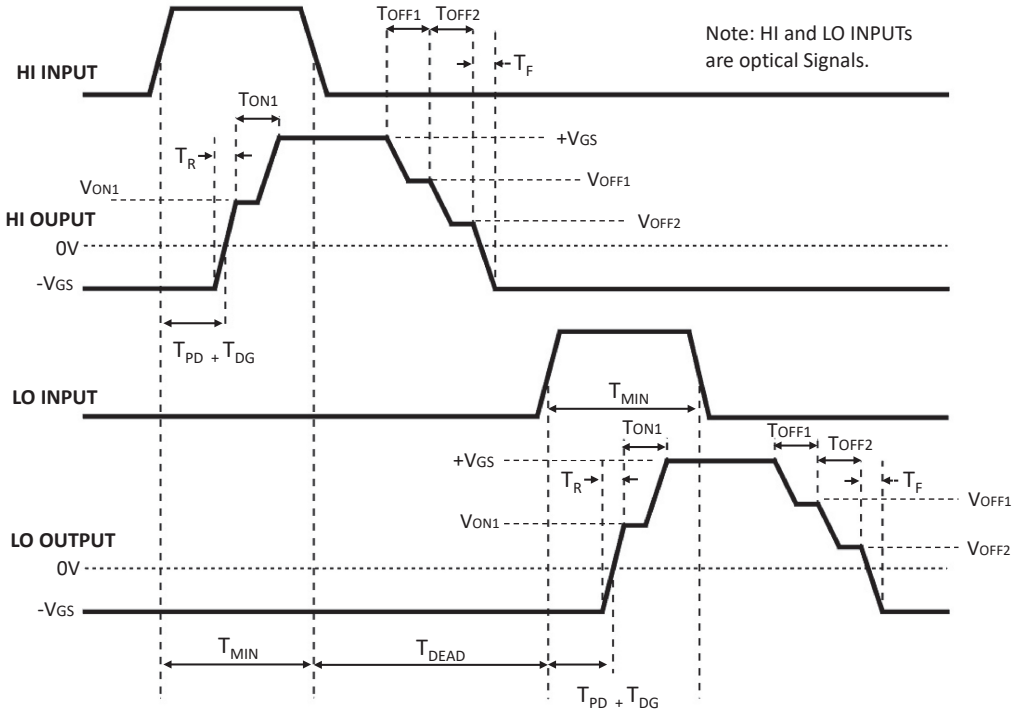
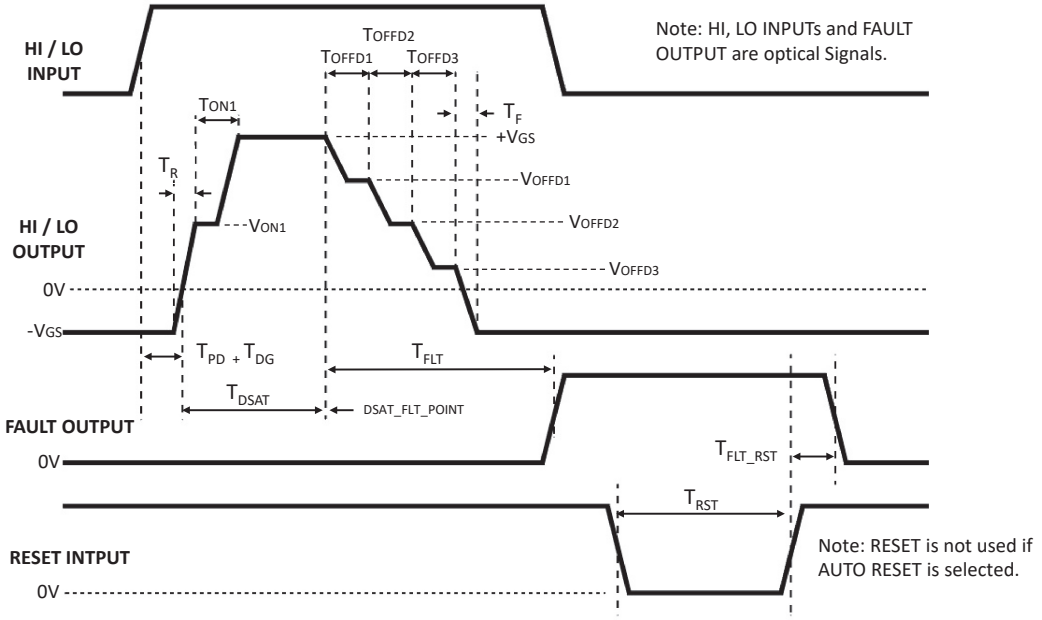


Figure 5-2. Signal Desaturation and Fault Timing Diagram



5.1 Timing Diagram Values

The following table lists the timing diagram values of the XIFM gate driver.

Note: Condition V_{SUP} = 24V, Temp. = 0 °C to 85 °C.

Table 5-1. Timing Diagram Values

Parameter		Description	Min.	Typ.	Max.	Unit
Minimum pulse width		T_{MIN}[8]	—	—	—	ns
Propagation delay		T_{PD}[1, 3]	—	—	280	ns
De-glitch time		T_{DG}[4]	—	200	—	ns
Rise time		T_R[2, 3]	—	35	—	ns
Fall time		T_F[2, 3]	—	30	—	ns
Two-level turn-on	First step turn-on time	T_{ON1}[4]	—	200	—	ns
	First step turn-on voltage	V_{TON1}[4]	—	9.5	—	V
Multi-level turn-off step	First step turn-off time	T_{OFF1}[4]	—	200	—	ns
	First step turn-off voltage	$V_{OFF1,}$[4]	—	9.5	—	V
	Second step turn-off time	T_{OFF2}[4]	—	200	—	ns
	Second step turn-off voltage	V_{OFF2}[4]	—	4.5	—	V
DSAT voltage level		V_{DSAT}[4]	—	8.7	—	V
DSAT blanking time		T_{DSAT}[4, 5]	1000	1100	1200	ns
DSAT de-glitch time		T_{DSAT_DG}[4]	—	0	—	ns
DSAT turn-off steps	First step DSAT turn-off time	T_{OFFD1}[4]	—	250	—	ns
	First step DSAT turn-off voltage	V_{OFFD1}[4]	—	9.5	—	V
	Second step DSAT turn-off time	T_{OFFD2}[4]	—	250	—	ns
	Second step DSAT turn-off voltage	V_{OFFD2}[4]	—	6.5	—	V
	Third step DSAT turn-off time	T_{OFFD3}[4]	—	250	—	ns
	Third step DSAT turn-off voltage	V_{OFFD3}[4]	—	2.5	—	V
Fault time delay		T_{FLT}[7]	—	5000	—	ns
Fault reset		T_{FLT_RST}	—	1000	—	ns
Dead time-input		T_{DEAD}[6]	—	500	—	ns
Reset timing		$T_{RST,}$ Minimum reset time	—	1000	—	ns
Automatic reset (optional)		—	—	5	—	ms

Notes:

1. Measured from 50% to 50% of input trigger and output V_{GS} signal.
2. Measured from 10% to 90% of output V_{GS} signal.
3. Measured without augmented settings and at no load condition.
4. Software configurable depends on user requirements.
5. Hardware blanking time is set to the present value in the table.
6. Death Time must be configured by the user by the host controller.
7. This is fault output delay time, but when DSAT is detected on board gate driver shouts-down trigger within 25 ns.
8. The minimum pulse width is a factor of the multi-level turn-off and two-level turn-on time.

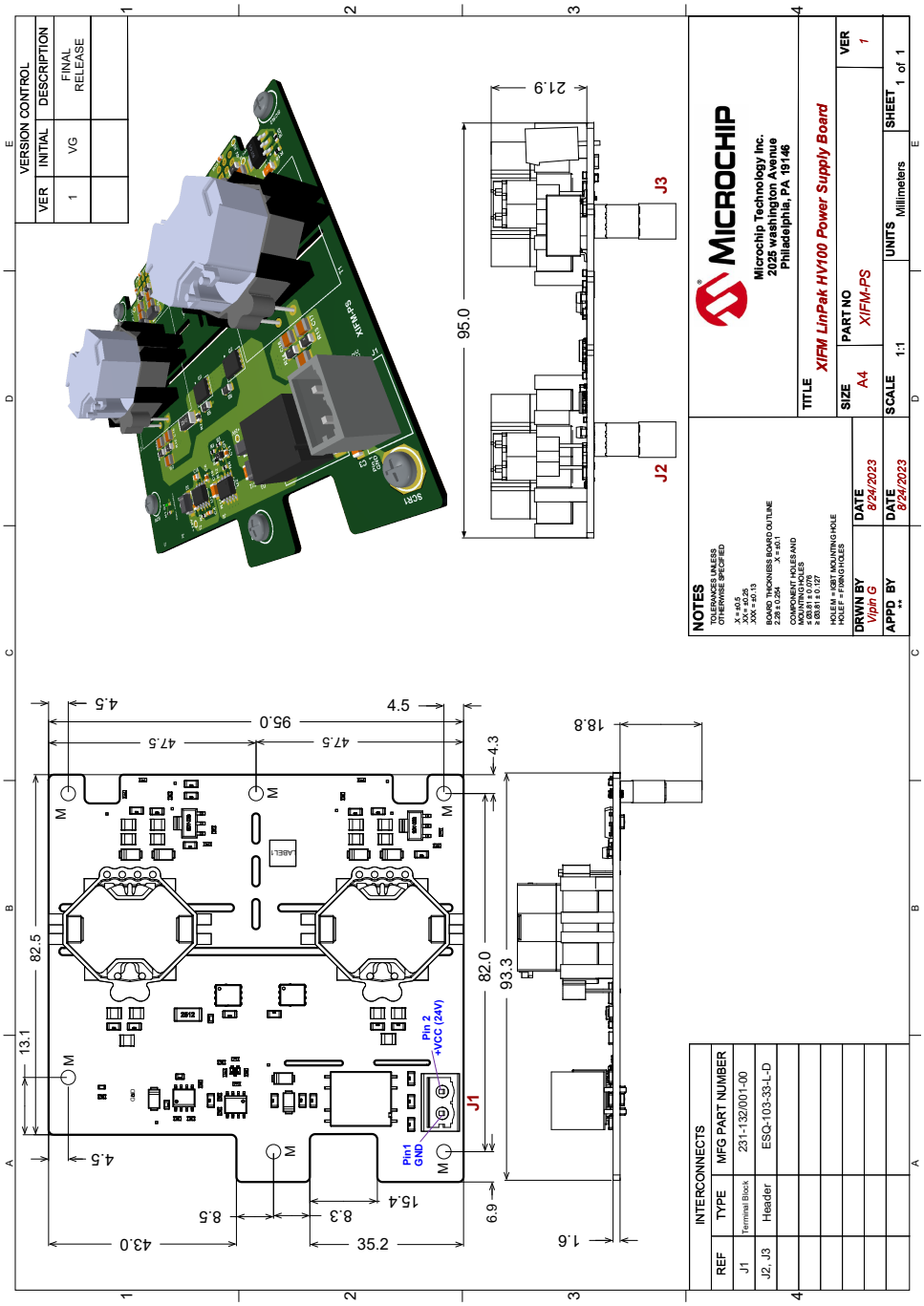
6. Package Specifications

The following section shows the package specification of the XIFM gate driver.

6.1 Package Outline

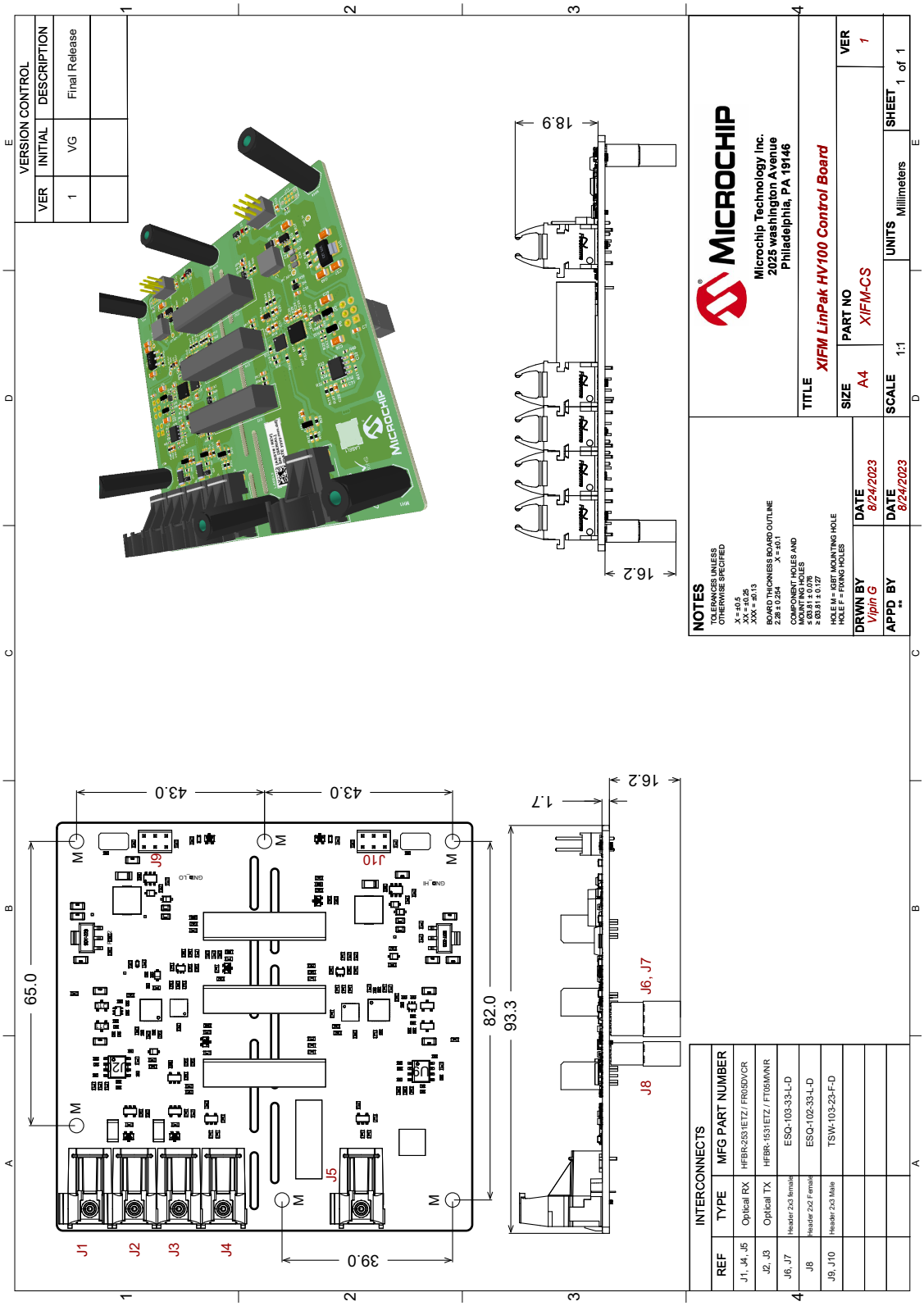
The following figures show the package outline drawing of the XIFM LinPak HV100 power supply board. The dimensions in the following figure are in millimeters.

Figure 6-1. Package Outline Drawing—XIFM LinPak HV100 Power Supply Board



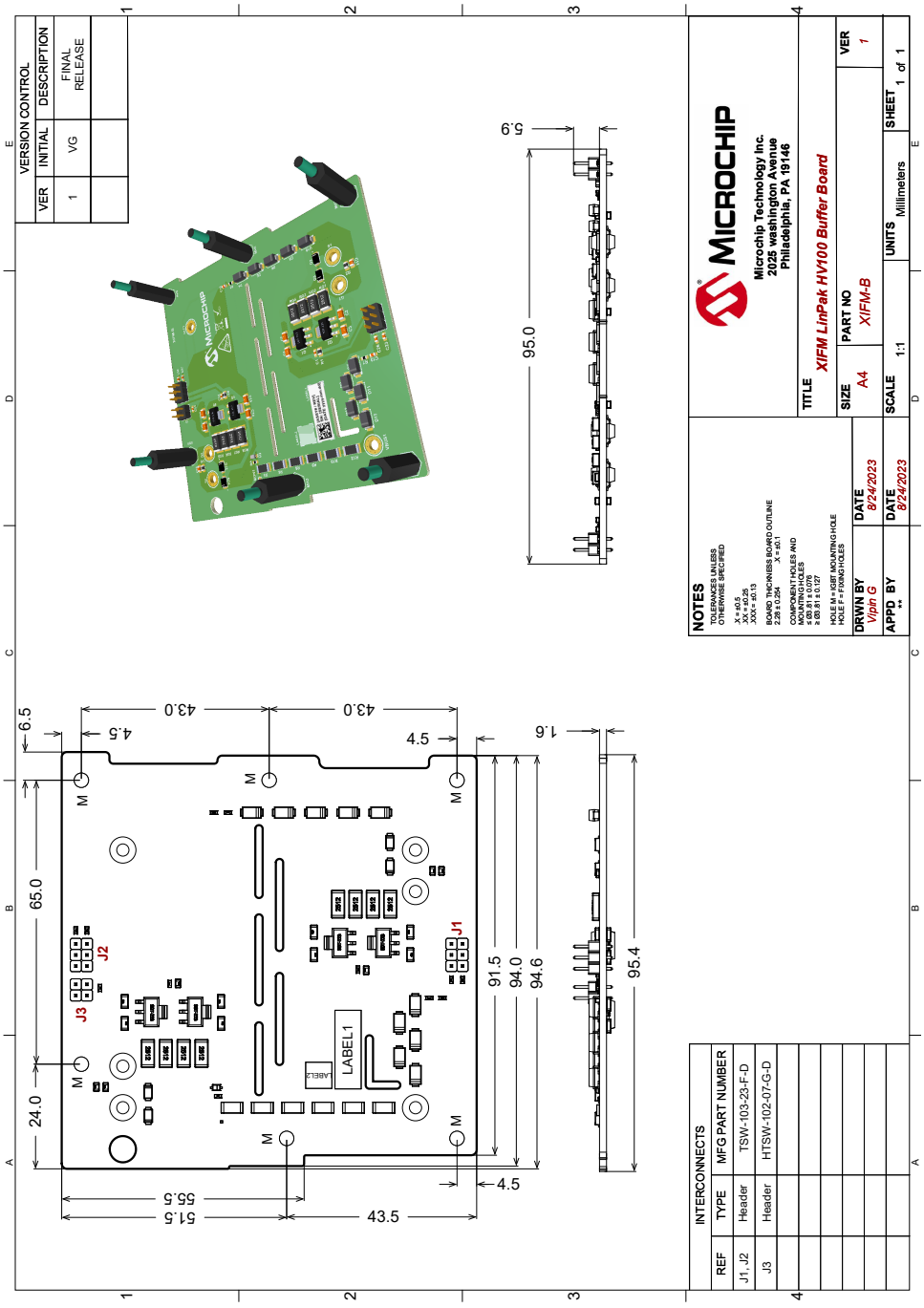
The following figure shows the package outline drawing of the XIFM LinPak HV100 control board. The dimensions in the following figure are in millimeters.

Figure 6-2. Package Outline Drawing—XIFM LinPak HV100 Control Board



The following figure shows the package outline drawing of the XIFM LinPak HV100 buffer board. The dimensions in the following figure are in millimeters.

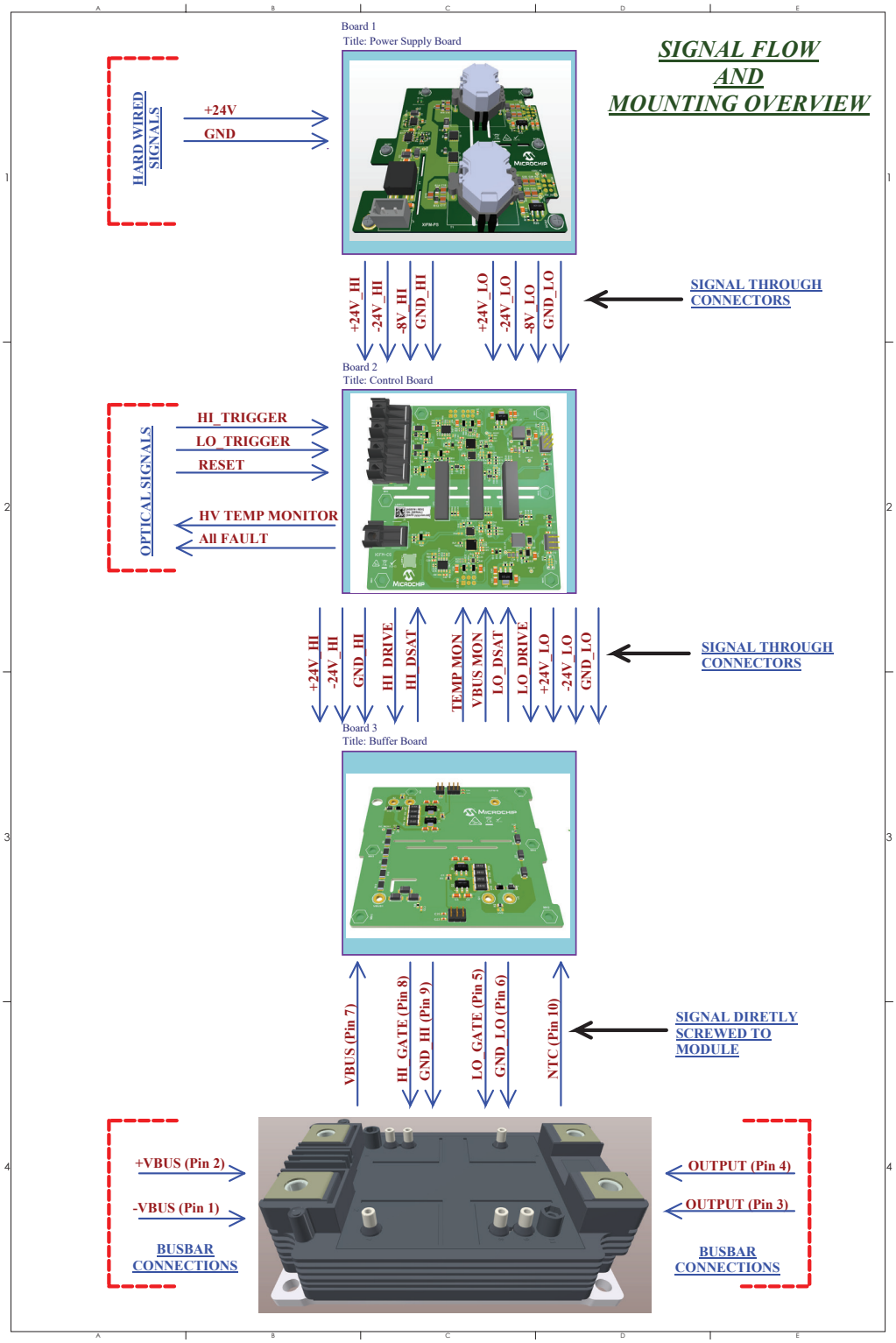
Figure 6-3. Package Outline Drawing—XIFM LinPak HV100 Buffer Board



6.2 Signal Flow and Mounting Overview

The following figure shows the signal flow and mounting overview of the XIFM gate driver.

Figure 6-4. Signal Flow and Mounting Overview



7. Important Precautions

⚠WARNING Handling devices with high voltages involves risk to life. It is imperative to comply with all respective precautions and safety regulations.

Microchip assumes that the gate drive board is mounted on the SiC MOSFET prior to start-up testing. It is recommended that the user check that the SiC MOSFET power modules are operating inside the Specified Operating Area (SOA) as specified by the module manufacturer, including short circuit testing under very low load conditions.

8. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
D	11/2023	The following changes are made in this revision of the document: • Updated values in Table 1-1 and Table 1-2. • Added 2. Standard Compliance, 3. General Specifications, 4. Physical Specification, and 5. Timing Diagrams. • Updated Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4.
C	02/2023	• Updated part numbers in Table 1. • Updated values in Table 1-1 and Table 1-2. • Updated Figure 6-3, Figure 6-2, Figure 6-1, and Figure 6-4.
B	12/2022	Updated Table 1, Table 1-1, and Table 1-2.
A	10/2022	Initial revision.

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ISBN: 978-1-6683-3519-2

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