LAN91C110 REV. B

FEAST Fast Ethernet Controller for PCMCIA and Generic 16-Bit Applications

Product Features

- Dual Speed CSMA/CD Engine (10 Mbps and 100 Mbps)
- Compliant with IEEE 802.3 100BASE-T Specification
- Supports 100BASE-TX, 100BASE-T4
- 16 Bit Wide Data Path (into Packet Buffer Memory)
- Generic 16-bit System Level Interface Easily Adaptable to ISA, PCMCIA (16-bit CardBus), and Various CPU System Interfaces
- Support for 16 and 8 Bit CPU Accesses
- Asynchronous Bus Interface
- 128 Kbyte External Memory
- Built-in Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- IEEE-802.3 MII (Media Independent Interface) Compliant MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- IEEE-802.3u Full Duplex Capability
- 144 Pin TQFP lead-free RoHS Compliant package (1.0 Millimeter Height)

ORDER NUMBER(S):

LAN91C110-PU for 144 pin TQFP lead-free RoHS Compliant package

DATASHEET

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table Of Contents

List of Figures

List of Tables

Chapter 1 General Description

The LAN91C110 is designed to facilitate the implementation of second generation Fast Ethernet PC Card adapters and other non-PCI connectivity products. The LAN91C110 is a digital device that implements the Media Access Control (MAC) portion of the CSMA/CD protocol at 10 and 100 Mbps, and couples it with a lean and fast data and control path system architecture to ensure that the CPU to packet RAM data movement does not cause a bottleneck at 100 Mbps.

The LAN91C110 implements a generic 16-bit host interface which is adaptable to a wide range of system buses and CPUs. This makes the LAN91C110 ideal for 10/100 Fast Ethernet implementations in systems based on system buses other than PCI.

Total memory size is 128 Kbytes, equivalent to a total chip storage (transmit plus receive) of 64 outstanding packets. The LAN91C110 is software compatible with the LAN9000 family of products in the default mode and can use existing LAN9000 drivers (ODI, IPX, and NDIS) with minor modifications in 16 and 32 bit Intel X86 based environments.

Memory management is handled using a unique patented MMU (Memory Management Unit) architecture and an internal 32-bit wide data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions. The total memory size is 128 Kbytes (external), equivalent to a total chip storage (transmit and receive) of 64 outstanding packets.

FEAST provides a flexible slave interface for easy connectivity with industry-standard buses. The host interface is “ISA-like” and is easily adapted to a wide range of system and CPU buses such as ISA, PCMCIA, etc.

An IEEE-802.3 compliant Media Independent Interface (MII) provided on the network side of the LAN91C110. The MII interface allows the use of a wide range of MII compliant Physical Layer (PHY) devices to be used with the LAN91C110. The LAN91C110 also provides an interface to the two-line MII serial management protocol.

Chapter 2 Pin Configuration

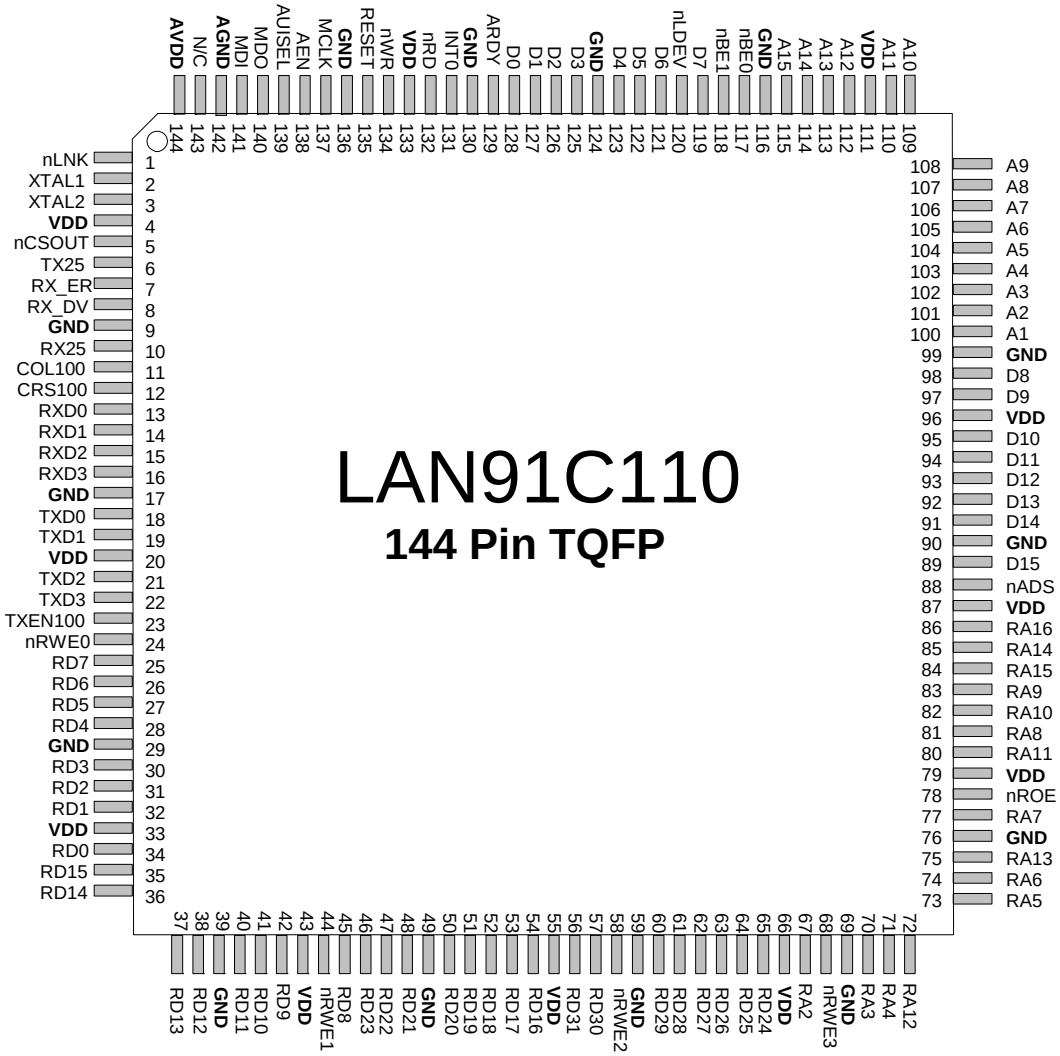

Figure 2.1 – Pin Configuration

Chapter 3 Description of Pin Functions

144 TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
115-112, 110-100	Address	A[15:1]	I	Input. Used by LAN91C110 for internal register selection.
138	Address Enable	AEN	I	Input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
118, 117		nBE[1:0]	I	Input. Used during LAN91C110 register accesses to determine the width of the access and the register(s) being accessed.
89, 91-95, 97-98, 119, 121-123, 125-128	Data Bus	D[15:0]	I/O8	Bidirectional. 16-bit data bus used to access the LAN91C110's internal registers. Data bus has weak internal pullups. Supports direct connection to the system bus without external buffering.
135	Reset	RESET	IS	Input. This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
129	Asynchro-nous Ready	ARDY	OD16	Open drain output. ARDY may be used when interfacing asynchronous buses to extend accesses. Its rising (access completion) edge is controlled by the XTAL1 clock and, therefore, asynchronous to the host CPU or bus clock. Note: Asserted for 100 to 150ns for the appropriate NO WAIT bit state in the Configuration register. See the NO WAIT bit description for complete information.
120	Local Device	nLDEV	O16	Output. Local Device. This active low output is asserted when AEN is low and A4-A15 decode to the LAN91C110 address programmed into the high byte of the Base Address Register. nLDEV* is a combinatorial decode of unlatched address and AEN signals.
88	nAddress Strobe	nADS	IS	Input. Address strobe. For systems that require address latching. The rising edge of nADS indicates the latching moment of A[1:15] and AEN. All LAN91C110 internal functions of A[1:15] and AEN are latched.
131	Interrupt	INTR0	O4	Output. The interrupt output is enabled by selecting the appropriate routing bits (INT SEL 1-0) in the Configuration Register.
132	nRead Strobe	nRD	IS	Input. Used in asynchronous bus interfaces.
134	nWrite Strobe	nWR	IS	Input. Used in asynchronous bus interfaces.

144 TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
56-57, 60-65, 46-48, 50-54, 35-38, 40-42, 45, 25-28, 30-32, 34	RAM Data Bus	RD[31:0]	I/O4 with pullups	Bidirectional. Carries the local buffer memory read and write data. Reads are always 32 bits wide. Writes are controlled individually at the byte level.
86,84,85, 75,72,80, 82-83,81, 77,74-73, 71-70,67	RAM Address Bus	RA[16:2]	O4	Outputs. This bus specifies the buffer RAM doubleword being accessed by the LAN91C110.
78		nROE	O4	Output. Active low signal used to read a doubleword from buffer RAM.
24,44,58, 68		nRWE[3:0]	O4	Outputs. Active low signals used to write any byte, word or dword in RAM.
2 3	Crystal 1 Crystal 2	XTAL1 XTAL2	Iclk	An external 25 MHz crystal is connected across these pins. If a TTL clock is supplied instead, it should be connected to XTAL1 and XTAL2 should be left open.
1	nLink Status	nLNK	I with pullup	Input. General purpose input port used to convey LINK status (EPHSR bit 14).
139	AUI Select	AUISEL	O4	Output. Non volatile output pin. Driven by AUI SELECT (CONFIG bit 8).
23	Transmit Enable MII	TXEN100	O12	Output to MII PHY. Envelope to 100 Mbps transmission.
12	Carrier Sense MII	CRS100	I with pulldown	Input from MII PHY. Envelope of packet reception used for deferral and backoff purposes.
8	Receive Data Valid	RX_DV	I with pulldown	Input from MII PHY. Envelope of data valid reception. Used for receive data framing.
11	Collision Detect MII	COL100	I with pulldown	Input from MII PHY. Collision detection input.
18,19,21, 22	Transmit Data	TXD[3:0]	O12	Outputs. Transmit Data nibble to MII PHY.
6	Transmit Clock	TX25	I with pullup	Input. Transmit clock input from MII. Nibble rate clock (25 MHz).
10	Receive Clock	RX25	I with pullup	Input. Receive clock input from MII PHY. Nibble rate clock.
16-13	Receive Data	RXD[3:0]	I	Inputs. Received Data nibble from MII PHY.
141	Manage-ment Data Input	MDI	I with pulldown	MII management data input.
140	Manage-ment Data Output	MDO	O4	MII management data output.
137	Manage-ment Clock	MCLK	O4	MII management clock.

144 TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
7	Receive Error	RX_ER	I with pulldown	Input. Indicates a code error detected by PHY. Used by the LAN91C110 to discard the packet being received. The error indication reported for this event is the same as a bad CRC (Receive Status Word bit 13).
5	nChip Select Output	nCSOUT	O4	Output. Chip Select provided for mapping of PHY functions into LAN91C110 decoded space. Active on accesses to LAN91C110's eight lower addresses when the BANK SELECTED is 7.
4,20,33,43,55,66,79, 87,96,111,133	Power	VDD		+5V power supply pins.
144	Analog Power	AVDD		+5V analog power supply pins.
9,17,29,39,49,59,69, 76,90,99, 116,124, 130,136,	Ground	GND		Ground pins.
142	Analog Ground	AGND		Analog ground pin.

BUFFER TYPES

O4	OUTPUT BUFFER WITH 2MA SOURCE AND 4MA SINK
O12	Output buffer with 6mA source and 12mA sink
OD16	Open drain buffer with 16mA sink
I/O4	Bidirectional buffer with 2mA source and 4mA sink
I/O8	Bidirectional buffer with 4mA source and 8mA sink
IS	Schmitt Trigger (Hysteresis: 250mV)
I with pullup	Rated at 30mA
I with pulldown	Rated at 30mA

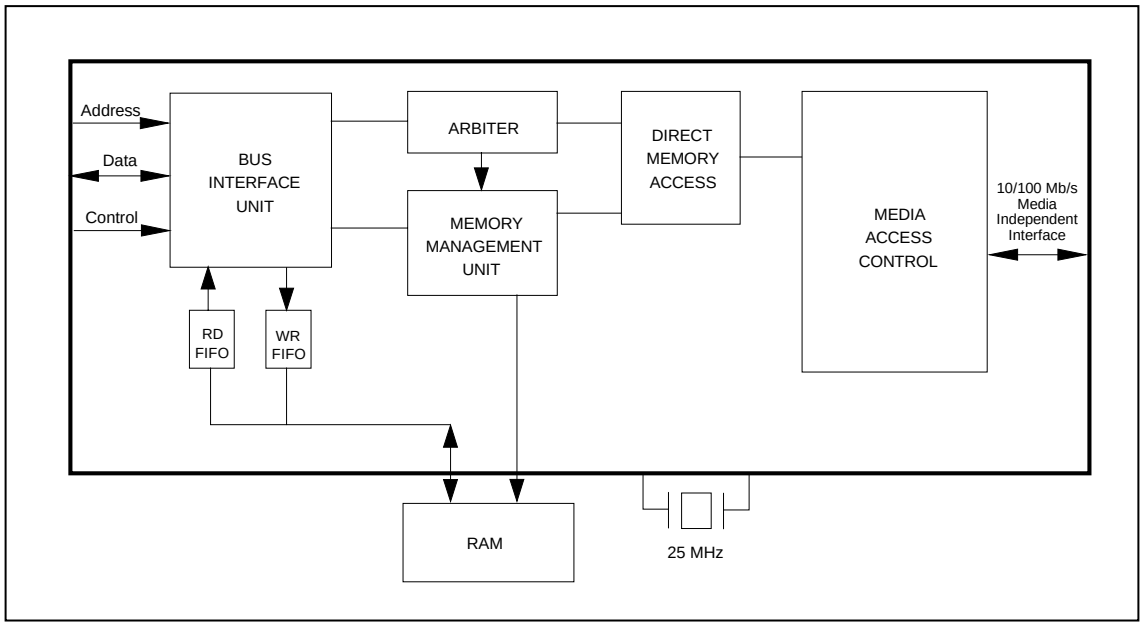

Figure 3.1 - LAN91C110 Block Diagram

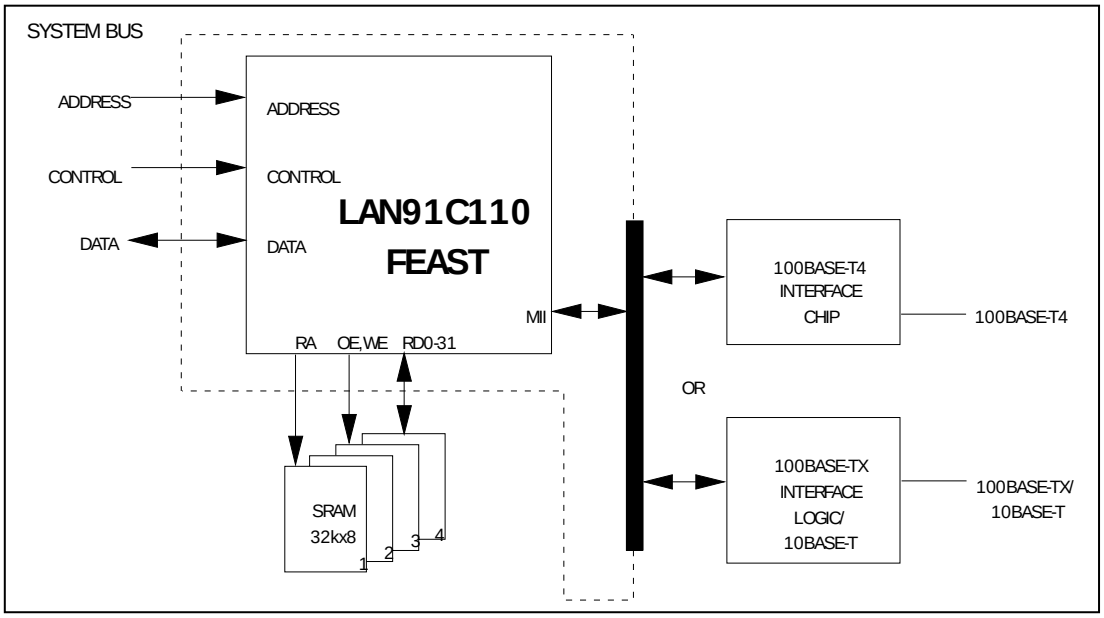

Figure 3.2 - LAN91C110 System Diagram

Chapter 4 Functional Description

4.1 Description of Blocks

4.1.1 Clock Generator Block

1. The XTAL1 and XTAL2 pins are to be connected to a 25 MHz 50 PPM crystal.

2. TX25 is an input clock. It will be the nibble rate of the particular PHY connected to the MII (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

3. RX25 - This is the MII nibble rate receive clock used for sampling received data nibbles and running the receive state machine. (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

4.2 CSMA/CD Block

This is a 16 bit oriented block, with fully- independent Transmit and Receive logic. The data path in and out of the block consists of two 16-bit wide uni-directional FIFOs interfacing the DMA block. The DMA port of the FIFO stores 32 bits to exploit the 32 bit data path into memory, but the FIFOs themselves are 16 bit wide. The Control Path consists of a set of registers interfaced to the CPU via the BIU.

4.2.1 DMA Block

This block accesses packet memory on the CSMA/CD's behalf, fetching transmit data and storing received data. It interfaces the CSMA/CD Transmit and Receive FIFOs on one side, and the Arbiter block on the other. To increase the bandwidth into memory, a 50 MHz clock is used by the DMA block, and the data path is 32 bits wide.

For example, during active reception at 100 Mbps, the CSMA/CD block will write a word into the Receive FIFO every 160ns. The DMA will read the FIFO and accumulate two words on the output port to request a memory cycle from the Arbiter every 320ns.

The DMA machine is able to support full duplex operation. Independent receive and transmit counters are used. Transmit and receive cycles are alternated when simultaneous receive and transmit accesses are needed.

4.2.2 Arbiter Block

The Arbiter block sequences accesses to packet RAM requested by the BIU and by the DMA blocks. BIU requests represent pipelined CPU accesses to the Data Register, while DMA requests represent CSMA/CD data movement. The external memory used is a 25ns SRAM.

The Arbiter is also responsible for controlling the nRWE0-nRWE3 lines as a function of the bytes being written. Read accesses are always 32 bit wide, and the Arbiter steers the appropriate byte(s) to the appropriate lanes as a function of the address.

The CPU Data Path consists of two uni-directional FIFOs mapped at the Data Register location. These FIFOs can be accessed in any combination of bytes, word, or doublewords. The Arbiter will indicate 'Not Ready' whenever a cycle is initiated that cannot be satisfied by the present state of the FIFO.

4.2.3 MMU Block

The Hardware Memory Management Unit allocates memory and transmit and receive packet queues. It also determines the value of the transmit and receive interrupts as a function of the queues. The page size is 2k, with a maximum memory size of 128k. MIR and MCR values are interpreted in 512 byte units.

4.2.4 BIU Block

The Bus Interface Unit can handle synchronous as well as asynchronous buses; different signals are used for each one. Transparent latches are added on the address path using rising nADS for latching.

With ISA, the read and write operations are controlled by the edges of nRD and nWR. ARDY is used for notifying the system that it should extend the access cycle. The leading edge of ARDY is generated by the leading edge of nRD or nWR while the trailing edge of ARDY is controlled by the internal LAN91C110 clock and, therefore, asynchronous to the bus.

The BIU is implemented using the following principles:

1. Address decoding is based on the values of A15-A4 and AEN.
2. Address latching is performed by using transparent latches that are transparent when nADS=0 and nRD=1, nWR=1 and latch on nADS rising edge.
3. Byte, word and doubleword accesses to all registers and Data Path are supported except a doubleword write to offset Ch will only write the BANK SELECT REGISTER (offset Fh).
4. No bus byte swapping is implemented (no eight bit mode).
5. Word swapping as a function of A1 is implemented for 16 bit bus support.
6. The asynchronous interface uses nRD and nWR strobes. If necessary, ARDY is negated on the leading edge of the strobe. The ARDY trailing edge is controlled by CLK.

4.2.5 MAC-PHY Interface Block

For the MII interface, transmit data is clocked out using the TX25 clock input, while receive data is clocked in using RX25.

In 100 Mbps mode, the LAN91C110 provides the following interface signals to the PHY:

- For transmission: TXEN100 TXD0-3 TX25
- For reception: RX_DV RX_ER RXD0-3 RX25
- For CSMA/CD state machines: CRS100 COL100

A transmission begins by TXEN100 going active (high), and TXD0-TXD3 having the first valid preamble nibble. TXD0 carries the least significant bit of the nibble (that is the one that would go first out of the EPH at 100 Mbps), while TXD3 carries the most significant bit of the nibble. TXEN100 and TXD0-TXD3 are clocked by the LAN91C110 using TX25 rising edges. TXEN100 goes inactive at the end of the packet on the last nibble of the CRC.

During a transmission, COL100 might become active to indicate a collision. COL100 is asynchronous to the LAN91C110's clocks and will be synchronized internally to TX25.

Reception begins when RX_DV (receive data valid) is asserted. A preamble pattern or flag octet will be present at RXD0-RXD3 when RX_DV is activated. The LAN91C110 requires no training sequence beyond a full flag octet for reception. RX_DV as well as RXD0-RXD3 are sampled on RX25 rising edges. RXD0 carries the least significant bit and RXD3 the most significant bit of the nibble. RX_DV goes inactive when the last valid nibble of the packet (CRC) is presented at RXD0-RXD3.

RX_ER might be asserted during packet reception to signal the LAN91C110 that the present receive packet is invalid. The LAN91C110 will discard the packet by treating it as a CRC error.

RXD0-RXD3 should always be aligned to packet nibbles, therefore, opening flag detection does not consider misaligned cases. Opening flag detection expects the 5Dh pattern and will not reject the packet on non-preamble patterns.

CRS100 is used as a frame envelope signal for the CSMA/CD MAC state machines (deferral and backoff functions), but it is not used for receive framing functions. CRS100 is an asynchronous signal and it will be active whenever there is activity on the cable, including LAN91C110 transmissions and collisions.

The MII SELECT bit in the CONFIG REGISTER must always be set for proper chip function.

Note that given the modular nature of the MII, TX25 and RX25 cannot be assumed to be free running clocks. The LAN91C110 will not rely on the presence of TX25 and RX25 during reset and will use its own internal clock whenever a timeout on TX25 is detected.

4.2.6 MII Management Interface Block

PHY management through the MII management interface is supported by the LAN91C110 by providing the means to drive a tri-statable data output, a clock, and reading an input. Timing and framing for each management command is to be generated by the CPU.

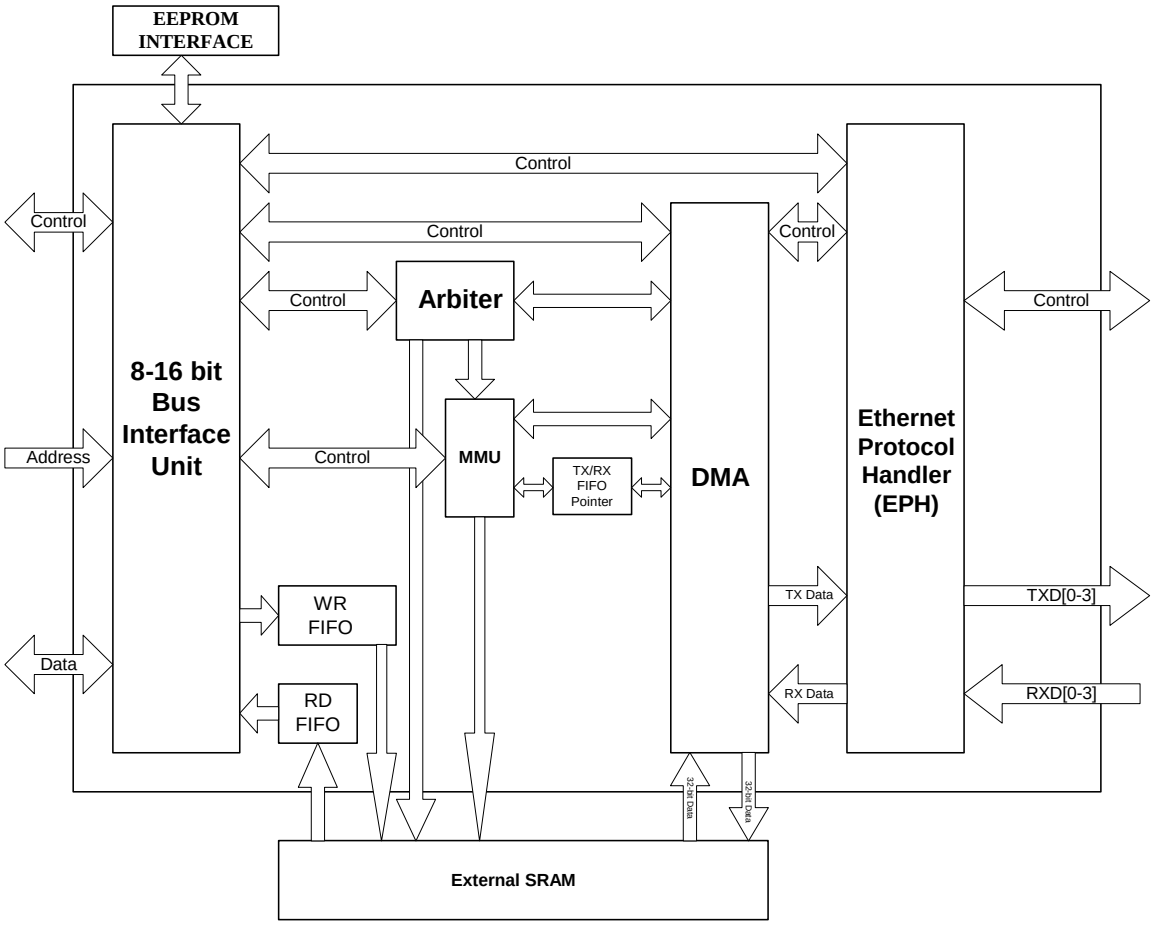

Figure 4.1 - LAN91C110 Internal Block Diagram with Data Path

Chapter 5 Data Structures and Registers

5.1 Packet Format in Buffer Memory

The packet format in memory is similar for the Transmit and Receive areas. The first word is reserved for the status word. The next word is used to specify the total number of bytes, and it is followed by the data area. The data area holds the packet itself.

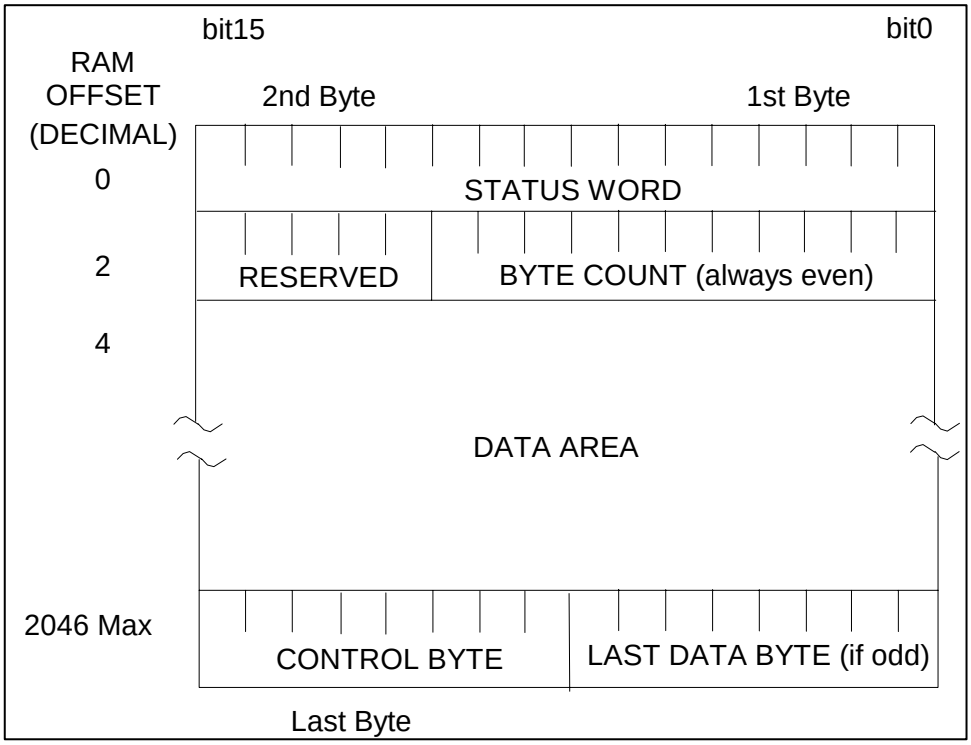

Figure 5.1 – Data Packet Format

	TRANSMIT PACKET	RECEIVE PACKET
STATUS WORD	Written by CSMA upon transmit completion (see Status Register)	Written by CSMA upon receive completion (see RX Frame Status Word)
BYTE COUNT	Written by CPU	Written by CSMA
DATA AREA	Written/modified by CPU	Written by CSMA
CONTROL BYTE	Written by CPU to control odd/even data bytes	Written by CSMA; also has odd/even bit

BYTE COUNT - Divided by two, it defines the total number of words including the STATUS WORD, the BYTE COUNT WORD, the DATA AREA and the CONTROL BYTE.

The receive byte count always appears as even; the ODDFRM bit of the receive status word indicates if the low byte of the last word is relevant.

The transmit byte count least significant bit will be assumed 0 by the controller regardless of the value written in memory.

DATA AREA - The data area starts at offset 4 of the packet structure and can extend up to 2043 bytes.

The data area contains six bytes of DESTINATION ADDRESS followed by six bytes of SOURCE ADDRESS, followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The LAN91C110 does not insert its own source address. On receive, all bytes are provided by the CSMA side.

The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the LAN91C110. It is treated transparently as data both for transmit and receive operations.

CONTROL BYTE - For transmit packets the CONTROL BYTE is written by the CPU as:

X	X	ODD	CRC	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE is not transmitted.

CRC - When set, CRC will be appended to the frame. This bit has only meaning if the NOCRC bit in the TCR is set.

For receive packets the CONTROL BYTE is written by the controller as:

0	1	ODD	0	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE should be ignored.

RECEIVE FRAME STATUS WORD

This word is written at the beginning of each receive frame in memory. It is not available as a register.

HIGH BYTE	ALGN ERR	BROD CAST	BAD CRC	ODD FRM	TOOLNG	TOO SHORT		
LOW BYTE		HASH VALUE						MULT CAST
		5	4	3	2	1	0	

ALGNERR - Frame had alignment error. When MII SEL=1 alignment error is set when BADCRC=1 and an odd number of nibbles was received between SFD and RX_DV going inactive.

BRODCAST - Receive frame was broadcast.

BADCRC - Frame had CRC error, or RX_ER was asserted during reception.

ODDFRM - This bit when set indicates that the received frame had an odd number of bytes.

TOOLNG - Frame length was longer than 802.3 maximum size (1518 bytes on the cable).

TOOSHORT - Frame length was shorter than 802.3 minimum size (64 bytes on the cable).

HASH VALUE - Provides the hash value used to index the Multicast Registers. Can be used by receive routines to speed up the group address search. The hash value consists of the six most significant bits of the CRC calculated on the Destination Address, and maps into the 64 bit multicast table. Bits 5,4,3 of the hash value select a byte of the multicast table, while bits 2,1,0 determine the bit within the byte selected. Examples of the address mapping:

ADDRESS	HASH VALUE 5-0	MULTICAST TABLE BIT
ED 00 00 00 00 00	000 000	MT-0 bit 0
0D 00 00 00 00 00	010 000	MT-2 bit 0
01 00 00 00 00 00	100 111	MT-4 bit 7
2F 00 00 00 00 00	111 111	MT-7 bit 7

MULTCAST - Receive frame was multicast. If hash value corresponds to a multicast table bit that is set, and the address was a multicast, the packet will pass address filtering regardless of other filtering criteria.

I/O SPACE

The base I/O space is specified by the power-up I/O Base Register default. To limit the I/O space requirements to 16 locations, the registers are assigned to different banks. The last word of the I/O area is shared by all banks and can be used to change the bank in use. Registers are described using the following convention:

OFFSET **NAME** **TYPE** **SYMBOL**

HIGH BYTE	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
	X	X	X	X	X	X	X	X
LOW BYTE	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	X	X	X	X	X	X	X	X

OFFSET - Defines the address offset within the IOBASE where the register can be accessed at, provided the bank select has the appropriate value.

The offset specifies the address of the even byte (bits 0-7) or the address of the complete word.

The odd byte can be accessed using address (offset + 1).

Some registers (like the Interrupt Ack., or like Interrupt Mask) are functionally described as two eight bit registers, in that case the offset of each one is independently specified.

Regardless of the functional description, all registers can be accessed as doublewords, words or bytes.

The default bit values upon hard reset are highlighted below each register.

Table 5.1 - Internal I/O Space Mapping

	BANK0	BANK1	BANK2	BANK3
0	TCR	CONFIG	MMU COMMAND	MT0-1
2	EPH STATUS	BASE	PNR	MT2-3
4	RCR	IA0-1	FIFO PORTS	MT4-5
6	COUNTER	IA2-3	POINTER	MT6-7
8	MIR	IA4-5	DATA	MGMT
A	MCR	-	DATA	REVISION
C	RESERVED (0)	CONTROL	INTERRUPT	RCV
E	BANK SELECT	BANK SELECT	BANK SELECT	BANK SELECT

A special BANK (BANK7) exists to support the addition of external registers.

BANK SELECT REGISTER

OFFSET E	NAME BANK SELECT REGISTER	TYPE READ/WRITE	SYMBOL BSR

HIGH BYTE	0	0	1	1	0	0	1	1
	0	0	1	1	0	0	1	1
LOW BYTE						BS2	BS1	BS0
	X	X	X	X	X	0	0	0

BS2, BS1, BS0 Determine the bank presently in use. This register is always accessible and is used to select the register bank in use.

The upper byte always reads as 33h and can be used to help determine the I/O location of the LAN91C110.

The BANK SELECT REGISTER is always accessible regardless of the value of BS0-2.

Note: The bank select register can be accessed as a word at offset 0x0Eh, or as a byte at offset 0x0Fh.
BANK 7 has no internal registers other than the BANK SELECT REGISTER itself. On valid cycles where BANK7 is selected (BS0=BS1=BS2=1), and A3=0, nCSOUT is activated to facilitate implementation of external registers.

Note: BANK7 does not exist in LAN91C9x devices. For backward S/W compatibility BANK7 accesses should be done if the Revision Control register indicates the device is the LAN91C110.

BANK 0

OFFSET	NAME	TYPE	SYMBOL
0	TRANSMIT CONTROL REGISTER	READ/WRITE	TCR

This register holds bits programmed by the CPU to control some of the protocol transmit options.

HIGH BYTE	SWFDUP	Reserved	EPH LOOP	STP SQET	FDUPLX	Reserved	Reserved	NOCRC
	0	0	0	0	0	0	0	0
LOW BYTE	PAD_EN	Reserved	Reserved	Reserved	Reserved	FORCOL	Reserved	TXENA
	0	0	0	0	0	0	0	0

SWFDUP - Enables Switched Full Duplex mode. In this mode, transmit state machine is inhibited from recognizing carrier sense, so deferrals will not occur. Also inhibits collision count, therefore, the collision related status bits in the EPHSR are not valid (CTR_ROL, LATCOL, SQET, 16COL, MUL COL, and SNGL COL). Uses COL100 as flow control, limiting backoff and jam to 1 clock each before inter-frame gap, then retry will occur after IFG. If COL100 is active during preamble, full preamble will be output before jam. When SWFDUP is high, the values of FDUPLX and MON_CSN have no effect. This bit should be low for non-MII operation.

EPH_LOOP - Internal loopback at the EPH block. Serial data is internally looped back when set. Defaults low. When EPH_LOOP is high the following transmit outputs are forced inactive: TXD0-TXD3 = 0h, TXEN100 = TXEN = 0, TXD = 1. The following and external inputs are blocked: CRS=CRS100=0, COL=COL100=0, RX_DV= RX_ER=0.

STP_SQET - Stop transmission on SQET error. If set, stops and disables transmitter on SQE test error. Does not stop on SQET error and transmits next frame if clear. Defaults low.

FDUPLX - When set the LAN91C110 will cause frames to be received if they pass the address filter regardless of the source for the frame. When clear the node will not receive a frame sourced by itself. This bit does not control the duplex mode operation, the duplex mode operation is controlled by the SWFDUP bit.

NOCRC - Does not append CRC to transmitted frames when set. Allows software to insert the desired CRC. Defaults to zero, namely CRC inserted.

PAD_EN - When set, the LAN91C110 will pad transmit frames shorter than 64 bytes with 00. For TX, CPU should write the actual BYTE COUNT before padded by the LAN91C110 to the buffer RAM, excludes the padded 00. When this bit is cleared, the LAN91C110 does not pad frames.

FORCOL - When set, the FORCOL bit will force a collision by not deferring deliberately. This bit is set and cleared only by the CPU. When TXENA is enabled with no packets in the queue and while the FORCOL bit is set, the LAN91C110 will transmit a preamble pattern the next time a carrier is seen on the line. If a packet is queued, a preamble and SFD will be transmitted. This bit defaults low to normal operation. NOTE: The LATCOL bit in the EPHSR, setting up as a result of FORCOL, will reset TXENA to 0. In order to force another collision, TXENA must be set to 1 again.

TXENA - Transmit enabled when set. Transmit is disabled if clear. When the bit is cleared the LAN91C110 will complete the current transmission before stopping. When stopping due to an error, this bit is automatically cleared.

BANK 0

OFFSET	NAME	TYPE	SYMBOL
2	EPH STATUS REGISTER	READ ONLY	EPHSR

This register stores the status of the last transmitted frame. This register value, upon individual transmit packet completion, is stored as the first word in the memory area allocated to the packet. Packet interrupt processing should use the copy in memory as the register itself will be updated by subsequent packet transmissions. The register can be used for real time values (like TXENA and LINK OK). If TXENA is cleared the register holds the last packet completion status.

HIGH BYTE	Reserved	LINK_ OK	Reserved	CTR _ROL	EXC _DEF	Reserved	LATCOL	Reserved
	0	-nLNK pin	0	0	0	0	0	0
LOW BYTE	TX DEFR	LTX BRD	SQET	16COL	LTX MULT	MUL COL	SNGL COL	TX_SUC
	0	0	0	0	0	0	0	0

LINK_OK - General purpose input port driven by nLNK pin inverted. Typically used for Link Test. A transition on the value of this bit generates an interrupt.

CTR_ROL - Counter Roll Over. When set one or more 4 bit counters have reached maximum count (15). Cleared by reading the ECR register.

EXC_DEF - Excessive Deferral. When set last/ current transmit was deferred for more than 1518 * 2 byte times. Cleared at the end of every packet sent.

LATCOL - Late collision detected on last transmit frame. If set a late collision was detected (later than 64 byte times into the frame). When detected the transmitter jams and turns itself off clearing the TXENA bit in TCR. Cleared by setting TXENA in TCR.

TX_DEFR - Transmit Deferred. When set, carrier was detected during the first 6.4 μs of the inter frame gap. Cleared at the end of every packet sent.

LTX_BRD - Last transmit frame was a broadcast. Set if frame was broadcast. Cleared at the start of every transmit frame.

SQET - Signal Quality Error Test. SQET bit is always set after first transmit, except if SWFDUP=1. As a consequence, the STP_SQET bit in the TCR register cannot be set as it will always result in transmit fatal error. Transmission stops and EPH INT is set if STP_SQET is in the TCR is also set when SQET is set. This bit is cleared by setting TXENA high.

16COL - 16 collisions reached. Set when 16 collisions are detected for a transmit frame. TXENA bit in TCR is reset. Cleared when TXENA is set high.

LTX_MULT - Last transmit frame was a multicast. Set if frame was a multicast. Cleared at the start of every transmit frame.

MULCOL - Multiple collision detected for the last transmit frame. Set when more than one collision was experienced. Cleared when TX_SUC is high at the end of the packet being sent.

SNGLCOL - Single collision detected for the last transmit frame. Set when a collision is detected. Cleared when TX_SUC is high at the end of the packet being sent.

TX_SUC - Last transmit was successful. Set if transmit completes without a fatal error. This bit is cleared by the start of a new frame transmission or when TXENA is set high. Fatal errors are:

- 16 collisions (1/2 duplex mode only)
- SQET fail and STP_SQET = 1 (1/2 duplex mode only)
- Late collision (1/2 duplex mode only)

BANK 0

OFFSET	NAME	TYPE	SYMBOL
4	RECEIVE CONTROL REGISTER	READ/WRITE	RCR

HIGH BYTE	SOFT RST	FILT CAR	ABORT_ENB	Reserved	Reserved	Reserved	STRIP CRC	RXEN
	0	0	0	0	0	0	0	0
LOW BYTE	Reserved	Reserved	Reserved	Reserved	Reserved	ALMUL	PRMS	RX_ ABORT
	0	0	0	0	0	0	0	0

SOFT_RST - Software-Activated Reset. Active high. Initiated by writing this bit high and terminated by writing the bit low. The LAN91C110's configuration is not preserved except for Configuration, Base, and IA0-IA5 Registers. EEPROM is not reloaded after software reset.

FILT_CAR - Filter Carrier. When set filters leading edge of carrier sense for 12 bit times (3 nibble times). Otherwise recognizes a receive frame as soon as carrier sense is active. (Does NOT filter RX DV on MII!)

ABORT_ENB - Enables abort of receive when collision occurs. Defaults low. When set, the LAN91C110 will automatically abort a packet being received when the appropriate collision input is This bit has no effect if the SWFDUP bit in the TCR is set.

STRIP_CRC - When set it strips the CRC on received frames. When clear the CRC is stored in memory following the packet. Defaults low.

RXEN - Enables the receiver when set. If cleared, completes receiving current frame and then goes idle. Defaults low on reset.

ALMUL - When set accepts all multicast frames (frames in which the first bit of DA is '1'). When clear accepts only the multicast frames that match the multicast table setting. Defaults low.

PRMS - Promiscuous mode. When set receives all frames. Does not receive its own transmission unless it is in Full Duplex!

RX_ABORT - This bit is set if a receive frame was aborted due to length longer than 2K bytes. The frame will not be received. The bit is cleared by RESET or by the CPU writing it low.

Reserved - Must be 0.

BANK 0

OFFSET	NAME	TYPE	SYMBOL
6	COUNTER REGISTER	READ ONLY	ECR

Counts four parameters for MAC statistics. When any counter reaches 15 an interrupt is issued. All counters are cleared when reading the register and do not wrap around beyond 15.

HIGH BYTE	NUMBER OF EXC. DEFFERED TX				NUMBER OF DEFFERED TX			
	0	0	0	0	0	0	0	0
LOW BYTE	MULTIPLE COLLISION COUNT				SINGLE COLLISION COUNT			
	0	0	0	0	0	0	0	0

Each four bit counter is incremented every time the corresponding event, as defined in the EPH STATUS REGISTER bit description, occurs. Note that the counters can only increment once per enqueued transmit packet, never faster, limiting the rate of interrupts that can be generated by the counters. For example if a packet is successfully transmitted after one collision the SINGLE COLLISION COUNT field is incremented by one. If a packet experiences between 2 to 16 collisions, the MULTIPLE COLLISION COUNT field is incremented by one. If a packet experiences deferral the NUMBER OF DEFERRED TX field is incremented by one, even if the packet experienced multiple deferrals during its collision retries.

The COUNTER REGISTER facilitates maintaining statistics in the AUTO RELEASE mode where no transmit interrupts are generated on successful transmissions.

Reading the register in the transmit service routine will be enough to maintain statistics.

BANK 0

OFFSET	NAME	TYPE	SYMBOL
8	MEMORY INFORMATION REGISTER	READ ONLY	MIR

HIGH BYTE	FREE MEMORY AVAILABLE (IN BYTES * 256 * M)							
	1	1	1	1	1	1	1	1
LOW BYTE	MEMORY SIZE (IN BYTES *256 * M)							
	1	1	1	1	1	1	1	1

FREE MEMORY AVAILABLE - This register can be read at any time to determine the amount of free memory. The register defaults to the MEMORY SIZE upon reset or upon the RESET MMU command.

MEMORY SIZE - This register can be read to determine the total memory size.

All memory related information is represented in 256 * M byte units, where the multiplier M is determined by the MCR upper byte.

These register default to FFh, which should be interpreted as 256.

BANK 0

OFFSET	NAME	TYPE	SYMBOL
A	MEMORY CONFIGURATION REGISTER	Lower Byte - READ/WRITE Upper Byte - READ ONLY	MCR

HIGH BYTE					MEMORY SIZE MULTIPLIER				
	0	0	1	1	0	1	0	1	
LOW BYTE	MEMORY RESERVED FOR TRANSMIT (IN BYTES * 256 * M)								
	0	0	0	0	0	0	0	0	

MEMORY RESERVED FOR TRANSMIT - Programming this value allows the host CPU to reserve memory to be used later for transmit, limiting the amount of memory that receive packets can use. When programmed for zero, the memory allocation between transmit and receive is completely dynamic. When programmed for a non-zero value, the allocation is dynamic if the free memory exceeds the programmed value, while receive allocation requests are denied if the free memory is less or equal to the programmed value. This register defaults to zero upon reset. It is not affected by the RESET MMU command.

The value written to the MCR is a reserved memory space IN ADDITION TO ANY MEMORY CURRENTLY IN USE. If the memory allocated for transmit plus the reserved space for transmit is required to be constant (rather than grow with transmit allocations) the CPU should update the value of this register after allocating or releasing memory.

The contents of the MIR as well as the low byte of the MCR are specified in units of 256 * M bytes, where M is the Memory Size Multiplier. M=2 for the LAN91C110. A value of 04h in the lower byte of the MCR is equal to one 2K page (4 * 256 *2 = 2K); since memory must be reserved in multiples of pages, bits 0 and 1 of the MCR should be written to 1 only when the entire memory is being reserved for transmit (i.e., low byte of MCR = FFh).

BANK1

OFFSET	NAME	TYPE	SYMBOL
0	CONFIGURATION REGISTER	READ/WRITE	CR

The Configuration Register holds bits that define the adapter configuration and are not expected to change during run-time. This register is part of the EEPROM saved setup.

HIGH BYTE	MII SELECT	Reserved		NO WAIT	Reserved	FULL STEP	Reserved	AUI SELECT
	1	0	1	0	0	0	0	0
LOW BYTE	1	Reserved	Reserved			INT SEL1	INT SEL0	
	1	0	1	1	0	0	0	1

MII SELECT - Used to select the network interface port. When set, the LAN91C110 will use its MII port and interface a PHY device at the nibble rate. This bit must always be set for proper chip function.

NO WAIT - When set, does not request additional wait states. An exception to this are accesses to the Data Register if not ready for a transfer. When clear, negates ARDY for two to three clocks on any cycle to the LAN91C110.

FULL STEP - Reserved

AUI SELECT - This bit is a general purpose output port. Its value drives pin AUISEL and can be used as a general purpose non-volatile configuration pin. Defaults low.

Reserved - Must be 0.

INT SEL1-0 - Used to select interrupt pin. The bits must remain 00 for the interrupt pin to be asserted for interrupt indication. All other bit combinations are undefined.

BANK 1

OFFSET	NAME	TYPE	SYMBOL
2	BASE ADDRESS REGISTER	READ/WRITE	BAR

This register holds the I/O address decode option chosen for the LAN91C110. Is not usually modified during run-time.

HIGH BYTE	A15	A14	A13	A9	A8	A7	A6	A5
	0	0	0	1	1	0	0	0
LOW BYTE	Reserved							1
	0	0	0	0	0	0	0	1

A15 - A13 and A9 - A5 - These bits are compared against the I/O address on the bus to determine the IOBASE for the LAN91C110's registers. The 64k I/O space is fully decoded by the LAN91C110 down to a 16 location space, therefore the unspecified address lines A4, A10, A11 and A12 must be all zeros.

The I/O base decode defaults to 300h (namely, the high byte defaults to 18h).

Reserved - Must be 0.

BANK 1

OFFSET	NAME	TYPE	SYMBOL
4 THROUGH 9	INDIVIDUAL ADDRESS REGISTERS	READ/WRITE	IAR

These registers are required to be written by the host following power-up and hardware reset. For PC Card designs, the CIS contains the node address. The S/W driver must load that address into these registers. The registers are modified by the software driver. Bit 0 of Individual Address 0 register corresponds to the first bit of the address on the cable.

LOW BYTE	ADDRESS 0							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 1							
	0	0	0	0	0	0	0	0
LOW BYTE	ADDRESS 2							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 3							
	0	0	0	0	0	0	0	0
LOW BYTE	ADDRESS 4							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 5							
	0	0	0	0	0	0	0	0

BANK 1

OFFSET	NAME	TYPE	SYMBOL
A			

Reserved.

BANK 1

OFFSET	NAME	TYPE	SYMBOL
C	CONTROL REGISTER	READ/WRITE	CTR

HIGH BYTE	Reserved	RCV_ BAD	Reserved	1	AUTO RELEASE	Reserved	1	Reserved
	0	0	0	1	0	0	1	0
LOW BYTE	LE ENABLE	CR ENABLE	TE ENABLE	1	Reserved	Reserved	Reserved	Reserved
	0	0	0	1	0	0	0	0

RCV_BAD - When set, bad CRC packets are received. When clear bad CRC packets do not generate interrupts and their memory is released.

AUTO RELEASE - When set, transmit pages are released by transmit completion if the transmission was successful (when TX_SUC is set). In that case there is no status word associated with its packet number, and successful packet numbers are not even written into the TX COMPLETION FIFO. A sequence of transmit packets will generate an interrupt only when the sequence is completely transmitted (TX EMPTY INT will be set), or when a packet in the sequence experiences a fatal error (TX INT will be set). Upon a fatal error TXENA is cleared and the transmission sequence stops. The packet number that failed, is present in the FIFO PORTS register, and its pages are not released, allowing the CPU to restart the sequence after corrective action is taken.

LE ENABLE - Link Error Enable. When set it enables the LINK_OK bit transition as one of the interrupts merged into the EPH INT bit. Clearing the LE ENABLE bit after an EPH INT interrupt, caused by a LINK_OK transition, will acknowledge the interrupt. LE ENABLE defaults low (disabled).

CR ENABLE - Counter Roll over Enable. When set, it enables the CTR_ROL bit as one of the interrupts merged into the EPH INT bit. Reading the COUNTER register after an EPH INT interrupt caused by a counter rollover, will acknowledge the interrupt. CR ENABLE defaults low (disabled).

TE ENABLE - Transmit Error Enable. When set it enables Transmit Error as one of the interrupts merged into the EPH INT bit. An EPH INT interrupt caused by a transmitter error is acknowledged by setting TXENA bit in the TCR register to 1 or by clearing the TE ENABLE bit. TE ENABLE defaults low (disabled). Transmit Error is any condition that clears TXENA with TX_SUC staying low as described in the EPHSR register.

Reserved 2-0: These reserved bits must always be written to as zero(0).

BANK2

OFFSET	NAME	TYPE	SYMBOL
0	MMU COMMAND REGISTER	WRITE ONLY BUSY Bit Readable	MMUCR

This register is used by the CPU to control the memory allocation, de-allocation, TX FIFO and RX FIFO control. The three command bits determine the command issued as described below:

HIGH BYTE								
LOW BYTE	COMMAND			Reserved	Reserved	N2	N1	N0/BUSY
	X	Y	Z					
								0

COMMAND SET:

xyz

000 0) NOOP - NO OPERATION

001 1) ALLOCATE MEMORY FOR TX - N2, N1, N0 defines the amount of memory requested as (value + 1) * 256 bytes. Namely N2, N1, N0 = 1 will request 2 * 256 = 512 bytes. A shift-based divide by 256 of the packet length yields the appropriate value to be used as N2, N1, N0. Immediately generates a completion code at the ALLOCATION RESULT REGISTER. Can optionally generate an interrupt on successful completion. N2, N1, N0 are ignored by the LAN91C110 but should be implemented in LAN91C110 software drivers for LAN9000 compatibility.

010 2) RESET MMU TO INITIAL STATE - Frees all memory allocations, clears relevant interrupts, resets packet FIFO pointers.

011 3) REMOVE FRAME FROM TOP OF RX FIFO - To be issued after CPU has completed processing of present receive frame. This command removes the receive packet number from the RX FIFO and brings the next receive frame (if any) to the RX area (output of RX FIFO).

100 4) REMOVE AND RELEASE TOP OF RX FIFO - Like 3) but also releases all memory used by the packet presently at the RX FIFO output. The MMU busy time after issuing REMOVE and RELEASE command depends on the time when the busy bit is cleared. The time from issuing REMOVE and RELEASE command on the last receive packet to the time when receive FIFO is empty depends on RX INT bit turning low. An alternate approach can be checking the read RX FIFO register.

101 5) RELEASE SPECIFIC PACKET - Frees all pages allocated to the packet specified in the PACKET NUMBER REGISTER. Should not be used for frames pending transmission. Typically used to remove transmitted frames, after reading their completion status. Can be used following 3) to release receive packet memory in a more flexible way than 4).

110 6) ENQUEUE PACKET NUMBER INTO TX FIFO - This is the normal method of transmitting a packet just loaded into RAM. The packet number to be enqueued is taken from the PACKET NUMBER REGISTER.

111 7) RESET TX FIFOs - This command will reset both TX FIFOs: The TX FIFO holding the packet numbers awaiting transmission and the TX Completion FIFO. This command provides a mechanism for canceling packet transmissions, and reordering or bypassing the transmit queue. The RESET TX FIFOs command should only be used when the transmitter is disabled. Unlike the RESET MMU command, the RESET TX FIFOs does not release any memory.

Note 1: Bits N2,N1,N0 bits are ignored by the LAN91C110 but should be used for command 0 to preserve software compatibility with the LAN91C92 and future devices. They should be zero for all other commands.

Note 2: When using the RESET TX FIFOS command, the CPU is responsible for releasing the memory associated with outstanding packets, or re-enqueuing them. Packet numbers in the completion FIFO can be read via the FIFO ports register before issuing the command.

Note 3: MMU commands releasing memory (commands 4 and 5) should only be issued if the corresponding packet number has memory allocated to it.

COMMAND SEQUENCING

A second allocate command (command 1) should not be issued until the present one has completed. Completion is determined by reading the FAILED bit of the allocation result register or through the allocation interrupt.

A second release command (commands 4, 5) should not be issued if the previous one is still being processed. The BUSY bit indicates that a release command is in progress. After issuing command 5, the contents of the PNR should not be changed until BUSY goes low. After issuing command 4, command 3 should not be issued until BUSY goes low.

BUSY BIT - Readable at bit 0 of the MMU command register address. When set indicates that MMU is still processing a release command. When clear, MMU has already completed last release command. BUSY and FAILED bits are set upon the trailing edge of command.

BANK 2

OFFSET	NAME	TYPE	SYMBOL
2	PACKET NUMBER REGISTER	READ/WRITE	PNR

Reserved	Reserved	PACKET NUMBER AT TX AREA					
0	0	0	0	0	0	0	0

PACKET NUMBER AT TX AREA - The value written into this register determines which packet number is accessible through the TX area. Some MMU commands use the number stored in this register as the packet number parameter. This register is cleared by a RESET or a RESET MMU Command.

OFFSET	NAME	TYPE	SYMBOL
3	ALLOCATION RESULT REGISTER	READ ONLY	ARR

This register is updated upon an ALLOCATE MEMORY MMU command.

FAILED	Reserved	ALLOCATED PACKET NUMBER					
1	0	0	0	0	0	0	0

FAILED - A zero indicates a successful allocation completion. If the allocation fails the bit is set and only cleared when the pending allocation is satisfied. Defaults high upon reset and reset MMU command. For polling purposes, the ALLOC_INT in the Interrupt Status Register should be used because it is synchronized to the read operation. Sequence:

1. Allocate Command
2. Poll ALLOC_INT bit until set
3. Read Allocation Result Register

ALLOCATED PACKET NUMBER - Packet number associated with the last memory allocation request. The value is only valid if the FAILED bit is clear.

Note: For software compatibility with future versions, the value read from the ARR after an allocation request is intended to be written into the PNR as is, without masking higher bits (provided FAILED = 0).

BANK 2

OFFSET	NAME	TYPE	SYMBOL
4	**FIFO PORTS REGISTER**	**READ ONLY**	**FIFO**

This register provides access to the read ports of the Receive FIFO and the Transmit completion FIFO. The packet numbers to be processed by the interrupt service routines are read from this register.

HIGH BYTE	REMPTY	0	RX FIFO PACKET NUMBER					
	1	0	0	0	0	0	0	0
LOW BYTE	TEMPTY	0	TX FIFO PACKET NUMBER					
	1	0	0	0	0	0	0	0

REMPTY - No receive packets queued in the RX FIFO. For polling purposes, uses the RCV_INT bit in the Interrupt Status Register.

TOP OF RX FIFO PACKET NUMBER - Packet number presently at the output of the RX FIFO. Only valid if REMPTY is clear. The packet is removed from the RX FIFO using MMU Commands 3) or 4).

TEMPTY - No transmit packets in completion queue. For polling purposes, uses the TX_INT bit in the Interrupt Status Register.

TX FIFO PACKET NUMBER - Packet number presently at the output of the TX FIFO. Only valid if TEMPTY is clear. The packet is removed when a TX INT acknowledge is issued.

Note: For software compatibility with future versions, the value read from each FIFO register is intended to be written into the PNR as is, without masking higher bits (provided TEMPTY and REMPTY = 0 respectively).

BANK 2

OFFSET	NAME	TYPE	SYMBOL
6	POINTER REGISTER	READ/WRITE NOT EMPTY is a read only bit	PTR

HIGH BYTE	RCV	AUTO INCR.	READ	Reserved	NOT EMPTY	POINTER HIGH		
	0	0	0	0	0	0	0	0
LOW BYTE	POINTER LOW							
	0	0	0	0	0	0	0	0

POINTER REGISTER - The value of this register determines the address to be accessed within the transmit or receive areas. It will auto-increment on accesses to the data register when AUTO INCR. is set. The increment is by one for every byte access, by two for every word access, and by four for every double word access. When RCV is set the address refers to the receive area and uses the output of RX FIFO as the packet number, when RCV is clear the address refers to the transmit area and uses the packet number at the Packet Number Register.

READ - Determines the type of access to follow. If the READ bit is high the operation intended is a read. If the READ bit is low the operation is a write. Loading a new pointer value, with the READ bit high, generates a pre-fetch into the Data Register for read purposes.

Readback of the pointer will indicate the value of the address last accessed by the CPU (rather than the last pre-fetched). This allows any interrupt routine that uses the pointer, to save it and restore it without affecting the process being interrupted. The Pointer Register should not be loaded until the Data Register FIFO is empty. The NOT EMPTY bit of this register can be read to determine if the FIFO is empty. On reads, if IOCHRDY is not connected to the host, the Data Register (ARDY) should not be read before 370ns after the pointer was loaded to allow the Data Register FIFO to fill.

If the pointer is loaded using 8 bit writes, the low byte should be loaded first and the high byte last.

Reserved – Must be 0.

NOT EMPTY - When set indicates that the Write Data FIFO is not empty yet. The CPU can verify that the FIFO is empty before loading a new pointer value. This is a read only bit.

Note: If AUTO INCR. is not set, the pointer must be loaded with a dword aligned value.

BANK 2

OFFSET	NAME	TYPE	SYMBOL
8 THROUGH Bh	DATA REGISTER	READ/WRITE	DATA

DATA HIGH							
X	X	X	X	X	X	X	X
DATA LOW							
X	X	X	X	X	X	X	X

DATA REGISTER - Used to read or write the data buffer byte/word presently addressed by the pointer register.

This register is mapped into two uni-directional FIFOs that allow moving words to and from the LAN91C110 regardless of whether the pointer address is even, odd or dword aligned. Data goes through the write FIFO into memory, and is pre-fetched from memory into the read FIFO. If byte accesses are used, the appropriate (next) byte can be accessed through the Data Low or Data High registers. The order to and from the FIFO is preserved. Byte word accesses can be mixed on the fly in any order.

This register is mapped into two consecutive word locations. The DATA register is accessible at any address in the 8 through Ah range, while the number of bytes being transferred is determined by A1 and nBE0-nBE. The FIFOs are 12 bytes each.

BANK 2

OFFSET	**NAME**	**TYPE**	**SYMBOL**
C	**INTERRUPT STATUS REGISTER**	**READ ONLY**	**IST**

	Reserved	EPH INT	RX_OVRN INT	ALLOC INT	TX EMPTY INT	TX INT	RCV INT
0	0	0	0	0	1	0	0

OFFSET	**NAME**	**TYPE**	**SYMBOL**
C	**INTERRUPT ACKNOWLEDGE REGISTER**	**WRITE ONLY**	**ACK**

	Reserved		RX_OVRN INT		TX EMPTY INT	TX INT	

OFFSET	**NAME**	**TYPE**	**SYMBOL**
D	**INTERRUPT MASK REGISTER**	**READ/WRITE**	**MSK**

	Reserved	EPH INT MASK	RX_OVRN INT MASK	ALLOC INT MASK	TX EMPTY INT MASK	TX INT MASK	RCV INT MASK
0	0	0	0	0	0	0	0

This register can be read and written as a word or as two individual bytes.

The Interrupt Mask Register bits enable the appropriate bits when high and disable them when low. A MASK bit being set will cause a hardware interrupt.

Note: The Bit 7 mask must never be written high (1).

Reserved – Must be 0.

EPH INT - Set when the Ethernet Protocol Handler section indicates one out of various possible special conditions. This bit merges exception type of interrupt sources, whose service time is not critical to the execution speed of the low level drivers. The exact nature of the interrupt can be obtained from the EPH Status Register (EPHSR), and enabling of these sources can be done via the Control Register. The possible sources are:

1. LINK - Link Test transition
2. CTR_ROL - Statistics counter roll over
3. TXENA cleared - A fatal transmit error occurred forcing TXENA to be cleared. TX_SUC will be low and the specific reason will be reflected by the bits:
    3.1) SQET - SQE Error
    3.2) LOST CARR - Lost Carrier
    3.3) LATCOL - Late Collision
    3.4) 16COL - 16 collisions

Any of the above interrupt sources can be masked by the appropriate ENABLE bits in the Control Register. 1) LE ENABLE (Link Error Enable), 2) CR ENABLE (Counter Roll Over), 3) TE ENABLE (Transmit Error Enable)

EPH INT will only be cleared by the following methods:
1. Clearing the LE ENABLE bit in the Control Register if an EPH interrupt is caused by a LINK_OK transition.
2. Reading the Counter Register if an EPH interrupt is caused by statistics counter roll over.
3. Setting TXENA bit high if an EPH interrupt is caused by any of the fatal transmit error listed above (3.1 to 3.5).

RX_OVRN INT - Set when 1) the receiver aborts due to an overrun due to a failed memory allocation, 2) the receiver aborts due to a packet length of greater than 2K bytes, or 3) the receiver aborts due to the RCV DISCRD bit in the RCV register set. The RX_OVRN INT bit latches the condition for the purpose of being polled or generating an interrupt, and will only be cleared by writing the acknowledge register with the RX_OVRN INT bit set.

ALLOC INT - Set when an MMU request for TX ram pages is successful. This bit is the complement of the FAILED bit in the ALLOCATION RESULT register. The ALLOC INT bit is cleared by the MMU when the next allocation request is processed or allocation fails.

TX EMPTY INT - Set if the TX FIFO goes empty, can be used to generate a single interrupt at the end of a sequence of packets enqueued for transmission. This bit latches the empty condition, and the bit will stay set until it is specifically cleared by writing the acknowledge register with the TX EMPTY INT bit set. If a real time reading of the FIFO empty is desired, the bit should be first cleared and then read.

The TX_EMPTY MASK bit should only be set after the following steps:
1. A packet is enqueued for transmission
2. The previous empty condition is cleared (acknowledged)

TX INT - Set when at least one packet transmission was completed or any of the below transmit fatal errors occurs:
1. SQET - SQE Error
2. LOST CARR - Lost Carrier
3. LATCOL - Late Collision
4. 16COL - 16 collisions

The first packet number to be serviced can be read from the FIFO PORTS register. The TX INT bit is always the logic complement of the TEMPTY bit in the FIFO PORTS register. After servicing a packet number, its TX INT interrupt is removed by writing the Interrupt Acknowledge Register with the TX INT bit set.

RCV INT - Set when a receive interrupt is generated. The first packet number to be serviced can be read from the FIFO PORTS register. The RCV INT bit is always the logic complement of the REMPTY bit in the FIFO PORTS register. Receive Interrupt is cleared when RX FIFO is empty.

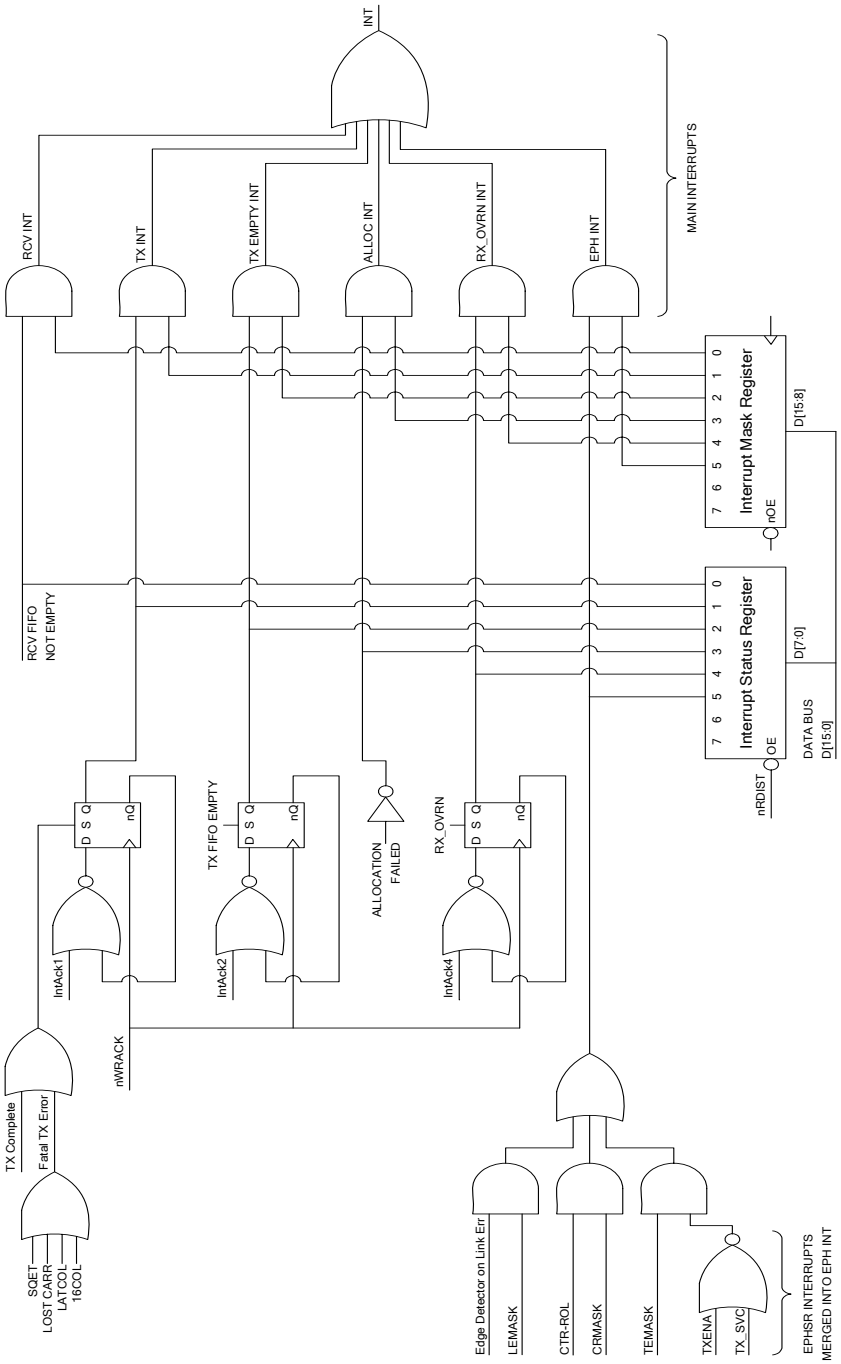

Figure 5.2 – Interrupt Structure

BANK3

OFFSET 0 THROUGH 7	NAME MULTICAST TABLE	TYPE READ/WRITE	SYMBOL MT

LOW BYTE	MULTICAST TABLE 0								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 1								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 2								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 3								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 4								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 5								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 6								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 7								
	0	0	0	0	0	0	0	0	

The 64 bit multicast table is used for group address filtering. The hash value is defined as the six most significant bits of the CRC of the destination addresses. The three msb's determine the register to be used (MT0-MT7), while the other three determine the bit within the register.

If the appropriate bit in the table is set, the packet is received.

If the ALMUL bit in the RCR register is set, all multicast addresses are received regardless of the multicast table values.

Hashing is only a partial group addressing filtering scheme, but being the hash value available as part of the receive status word, the receive routine can reduce the search time significantly. With the proper memory structure, the search is limited to comparing only the multicast addresses that have the actual hash value in question.

BANK 3

OFFSET	NAME	TYPE	SYMBOL
8	MANAGEMENT INTERFACE	READ/WRITE	MGMT

HIGH BYTE	FLTST	MSK_ CRS100						
	0	0	1	1	0	0	1	1
LOW BYTE					MDOE	MCLK	MDI	MDO
	0	0	1	1	0	0	MDI Pin	0

FLTST - Facilitates the inclusion of packet forwarding information on the receive packet memory structure. When 0, RD0-RD7 is always driven. When 1, RD0-RD7 is floated during RECEIVE FRAME STATUS WORD writes (RA2-RA16=0, RCVDMA=1, nRWE0-nRWE3=0).

MSK_CRS100 - Disables CRS100 detection during transmit in half duplex mode (SWFDUP=0).

MDO - MII Management output. The value of this bit drives the MDO pin.
MDI - MII Management input. The value of the MDI pin is readable using this bit.

MDCLK - MII Management clock. The value of this bit drives the MDCLK pin.

MDOE - MII Management output enable. When high pin MDO is driven, when low pin MDO is tri-stated.

The purpose of this interface, along with the corresponding pins is to implement MII PHY management in software.

BANK 3

OFFSET	NAME	TYPE	SYMBOL
A	REVISION REGISTER	READ ONLY	REV

HIGH BYTE								
	0	0	1	1	0	0	1	1
LOW BYTE	CHIP				REV			
	1	0	0	1	0	0	0	0

CHIP - Chip ID. Can be used by software drivers to identify the device used.

REV - Revision ID. Incremented for each revision of a given device.

CHIP ID VALUE	DEVICE
3	LAN91C90/LAN91C92
4	LAN91C94
5	LAN91C95
4*	LAN91C96
7	LAN91C100
8	LAN91C100FD
9	LAN91C110

***Note:** Shares the chip ID with the LAN91C94. Distinction is made by the revision ID. Revision ID of 6 or higher represents the LAN91C96.

OFFSET	NAME	TYPE	SYMBOL
C	RCV REGISTER	READ/WRITE	RCV

HIGH BYTE								
	0	0	0	0	0	0	0	0
LOW BYTE	RCV DISCRD	Reserved	Reserved	MBO	MBO	MBO	MBO	MBO
	0	0	0	1	1	1	1	1

RCV DISCRD - Set to discard a packet being received. Will discard packets only in the process of being received. When set prior to the end of receive packet, bit 4 (RXOVRN) of the interrupt status register will be set to indicate that the packet was discarded. Otherwise, the packet will be received normally and bit 0 set (RCVINT) in the interrupt status register. RCV DISCRD is self clearing.

MBO – Must be 1.

BANK7

OFFSET	NAME	TYPE	SYMBOL
0 THROUGH 7	EXTERNAL REGISTERS		

nCSOUT is driven low by the LAN91C110 when a valid access to the EXTERNAL REGISTER range occurs.

HIGH BYTE	EXTERNAL R/W REGISTER							
LOW BYTE	EXTERNAL R/W REGISTER							

CYCLE	nCSOUT	LAN91C110 DATA BUS
AEN=0 A3=0 A4-15 matches I/O BASE BANK SELECT = 7	Driven low. Transparently latched on nADS rising edge.	Ignored on writes. Tri-stated on reads.
BANK SELECT = 4,5,6	High	Ignore cycle.
Otherwise	High	Normal LAN91C110 cycle.

5.2 Typical Flow of Events for Transmit (Auto Release = 0)

	S/W DRIVER	MAC SIDE
1	ISSUE ALLOCATE MEMORY FOR TX - N BYTES - the MMU attempts to allocate N bytes of RAM.	
2	WAIT FOR SUCCESSFUL COMPLETION CODE - Poll until the ALLOC INT bit is set or enable its mask bit and wait for the interrupt. The TX packet number is now at the Allocation Result Register.	
3	LOAD TRANSMIT DATA - Copy the TX packet number into the Packet Number Register. Write the Pointer Register, then use a block move operation from the upper layer transmit queue into the Data Register.	
4	ISSUE "ENQUEUE PACKET NUMBER TO TX FIFO" - This command writes the number present in the Packet Number Register into the TX FIFO. The transmission is now enqueued. No further CPU intervention is needed until a transmit interrupt is generated.	
5		The enqueued packet will be transferred to the MAC block as a function of TXENA (nTCR) bit and of the deferral process (1/2 duplex mode only) state.
6		a) Upon transmit completion the first word in memory is written with the status word. The packet number is moved from the TX FIFO into the TX completion FIFO. Interrupt is generated by the TX completion FIFO being not empty. b) If a TX failure occurs on any packets, TX INT is generated and TXENA is cleared, transmission sequence stops. The packet number of the failure packet is presented at the TX FIFO PORTS Register.
7	a) SERVICE INTERRUPT - Read Interrupt Status Register. If it is a transmit interrupt, read the TX FIFO Packet Number from the FIFO Ports Register. Write the packet number into the Packet Number Register. The corresponding status word is now readable from memory. If status word shows successful transmission, issue RELEASE	

S/W DRIVER	MAC SIDE
packet number command to free up the memory used by this packet. Remove packet number from completion FIFO by writing TX INT Acknowledge Register.	
b) Option 1) Release the packet. Option 2) Check the transmit status in the EPH STATUS Register, write the packet number of the current packet to the Packet Number Register, re-enable TXENA, then go to step 4 to start the TX sequence again.	

5.3 Typical Flow of Events for Transmit (Auto Release = 1)

	S/W DRIVER	MAC SIDE
1	ISSUE ALLOCATE MEMORY FOR TX - N BYTES - the MMU attempts to allocate N bytes of RAM.	
2	WAIT FOR SUCCESSFUL COMPLETION CODE - Poll until the ALLOC INT bit is set or enable its mask bit and wait for the interrupt. The TX packet number is now at the Allocation Result Register.	
3	LOAD TRANSMIT DATA - Copy the TX packet number into the Packet Number Register. Write the Pointer Register, then use a block move operation from the upper layer transmit queue into the Data Register.	
4	ISSUE "ENQUEUE PACKET NUMBER TO TX FIFO" - This command writes the number present in the Packet Number Register into the TX FIFO. The transmission is now enqueued. No further CPU intervention is needed until a transmit interrupt is generated.	
5		The enqueued packet will be transferred to the MAC block as a function of TXENA (nTCR) bit and of the deferral process (1/2 duplex mode only) state.
6		Transmit pages are released by transmit completion.
7		a) The MAC generates a TXEMPTY interrupt upon a completion of a sequence of enqueued packets. b) If a TX failure occurs on any packets, TX INT is generated and TXENA is cleared, transmission sequence stops. The packet number of the failure packet is presented at the TX FIFO PORTS Register.
8	a) SERVICE INTERRUPT – Read Interrupt Status Register, exit the interrupt service routine. b) Option 1) Release the packet.	

S/W DRIVER	MAC SIDE
Option 2) Check the transmit status in the EPH STATUS Register, write the packet number of the current packet to the Packet Number Register, re-enable TXENA, then go to step 4 to start the TX sequence again.	

5.4 Typical Flow of Events for Receive

	S/W DRIVER	MAC SIDE
1	ENABLE RECEPTION - By setting the RXEN bit.	
2		A packet is received with matching address. Memory is requested from MMU. A packet number is assigned to it. Additional memory is requested if more pages are needed.
3		The internal DMA logic generates sequential addresses and writes the receive words into memory. The MMU does the sequential to physical address translation. If overrun, packet is dropped and memory is released.
4		When the end of packet is detected, the status word is placed at the beginning of the receive packet in memory. Byte count is placed at the second word. If the CRC checks correctly the packet number is written into the RX FIFO. The RX FIFO, being not empty, causes RCV INT (interrupt) to be set. If CRC is incorrect the packet memory is released and no interrupt will occur.
5	SERVICE INTERRUPT - Read the Interrupt Status Register and determine if RCV INT is set. The next receive packet is at receive area. (Its packet number can be read from the FIFO Ports Register). The software driver can process the packet by accessing the RX area, and can move it out to system memory if desired. When processing is complete the CPU issues the REMOVE AND RELEASE FROM TOP OF RX command to have the MMU free up the used memory and packet number.	

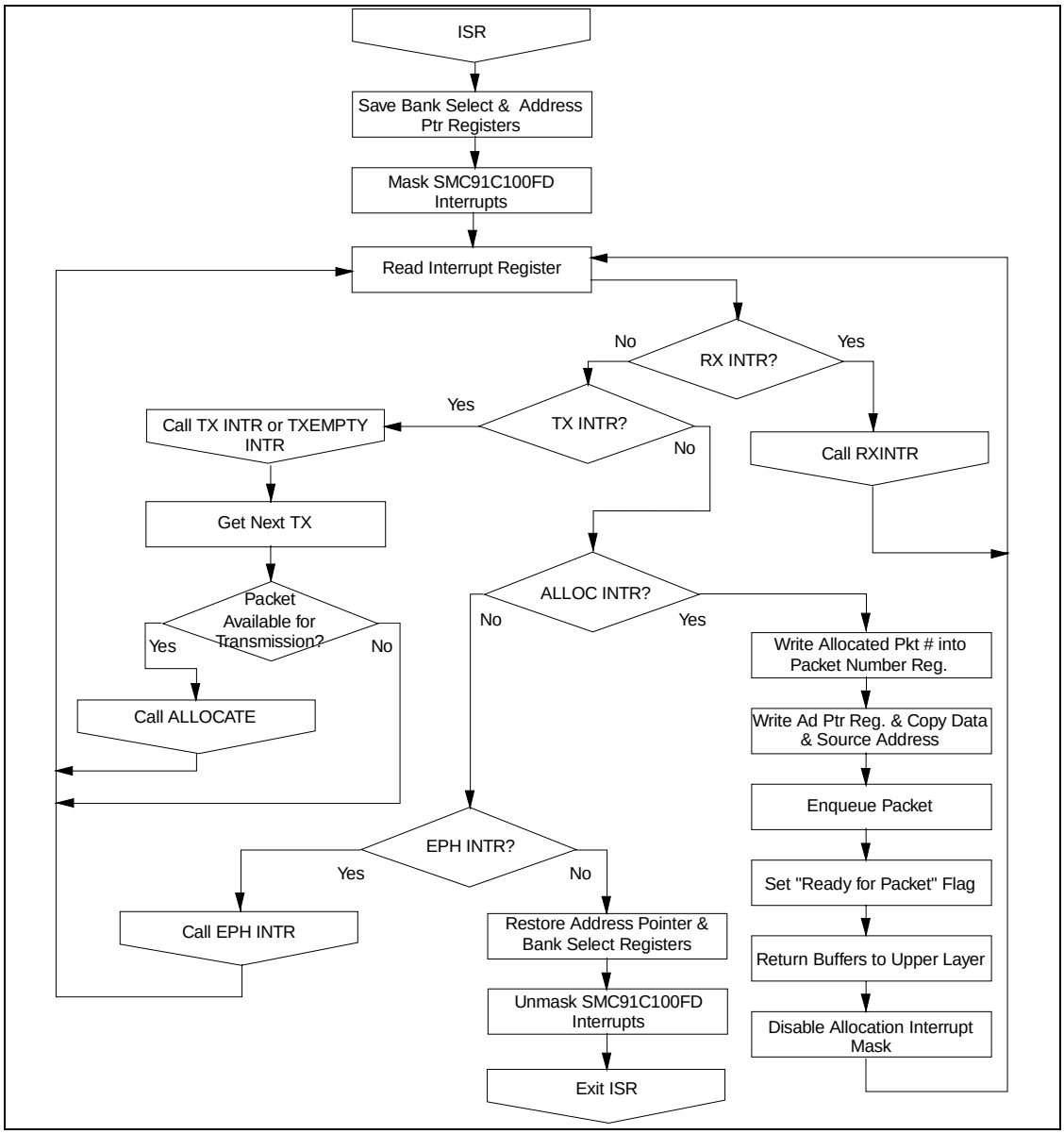

Figure 5.3 – Interrupt Service Routine

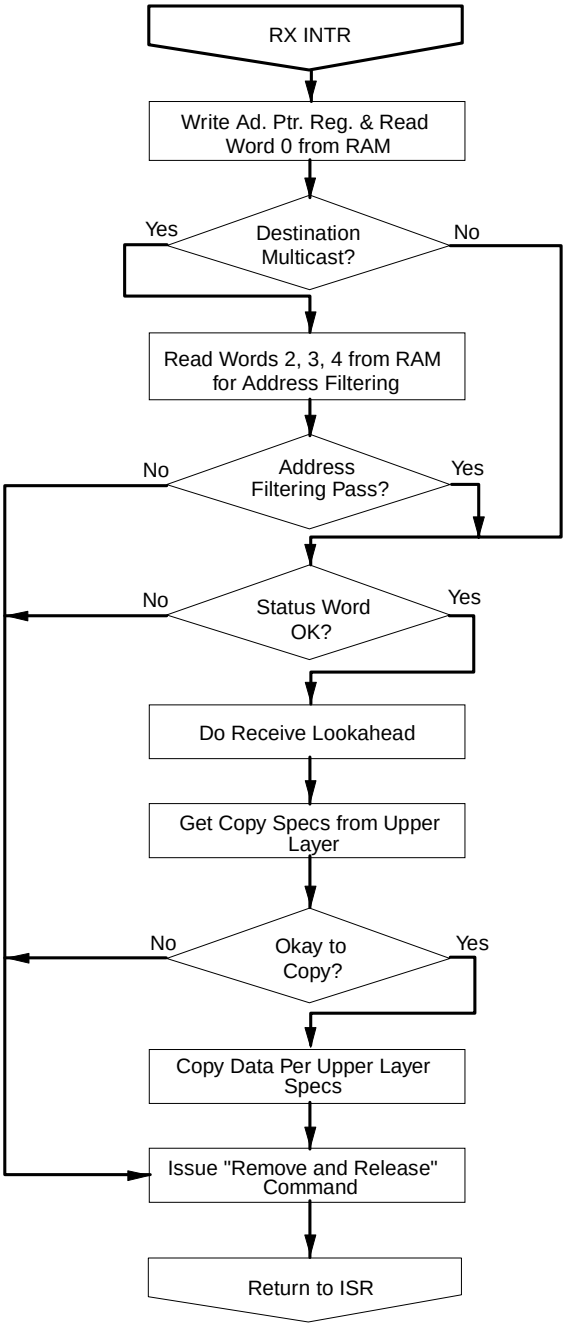

Figure 5.4 - RX INTR

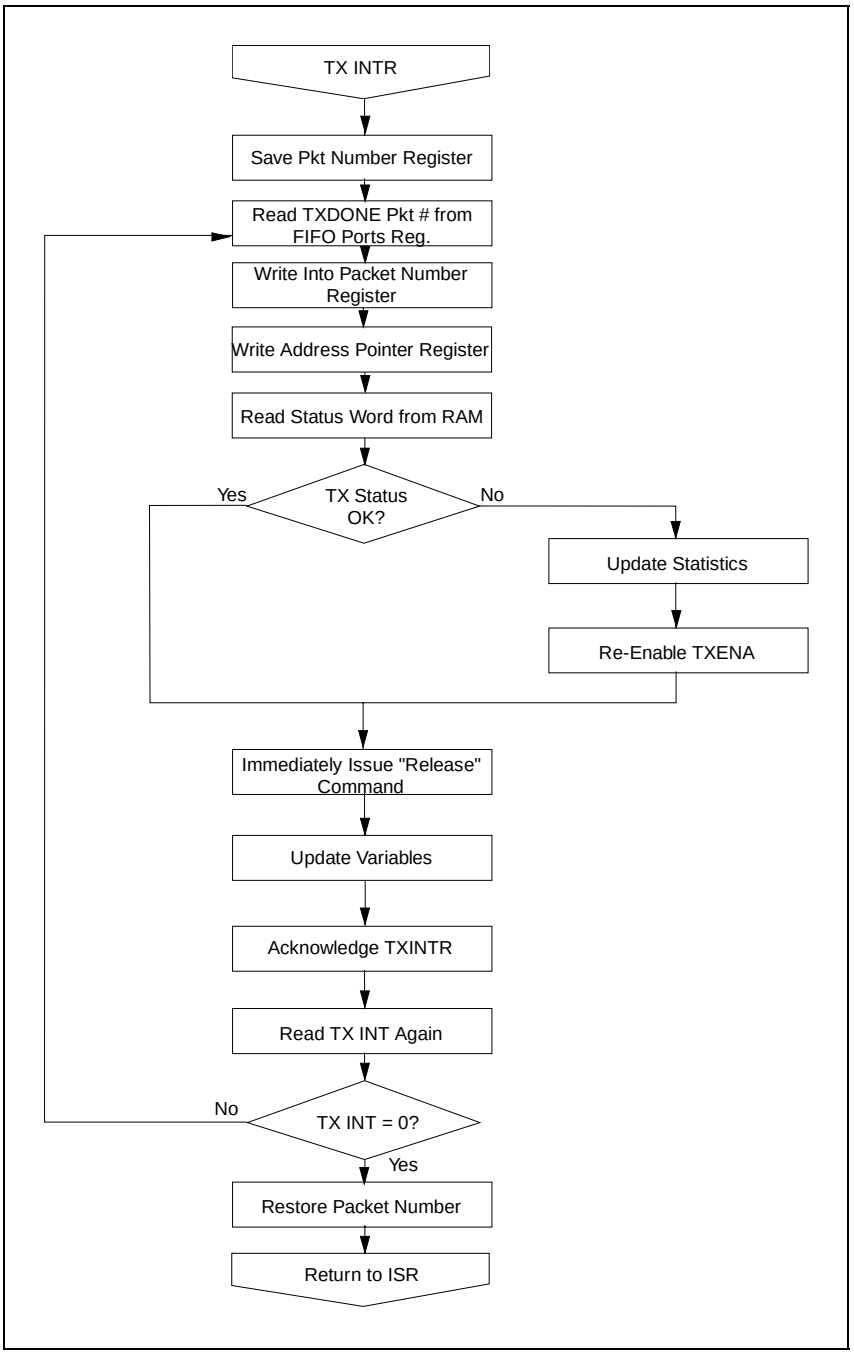

Figure 5.5 - TX INTR

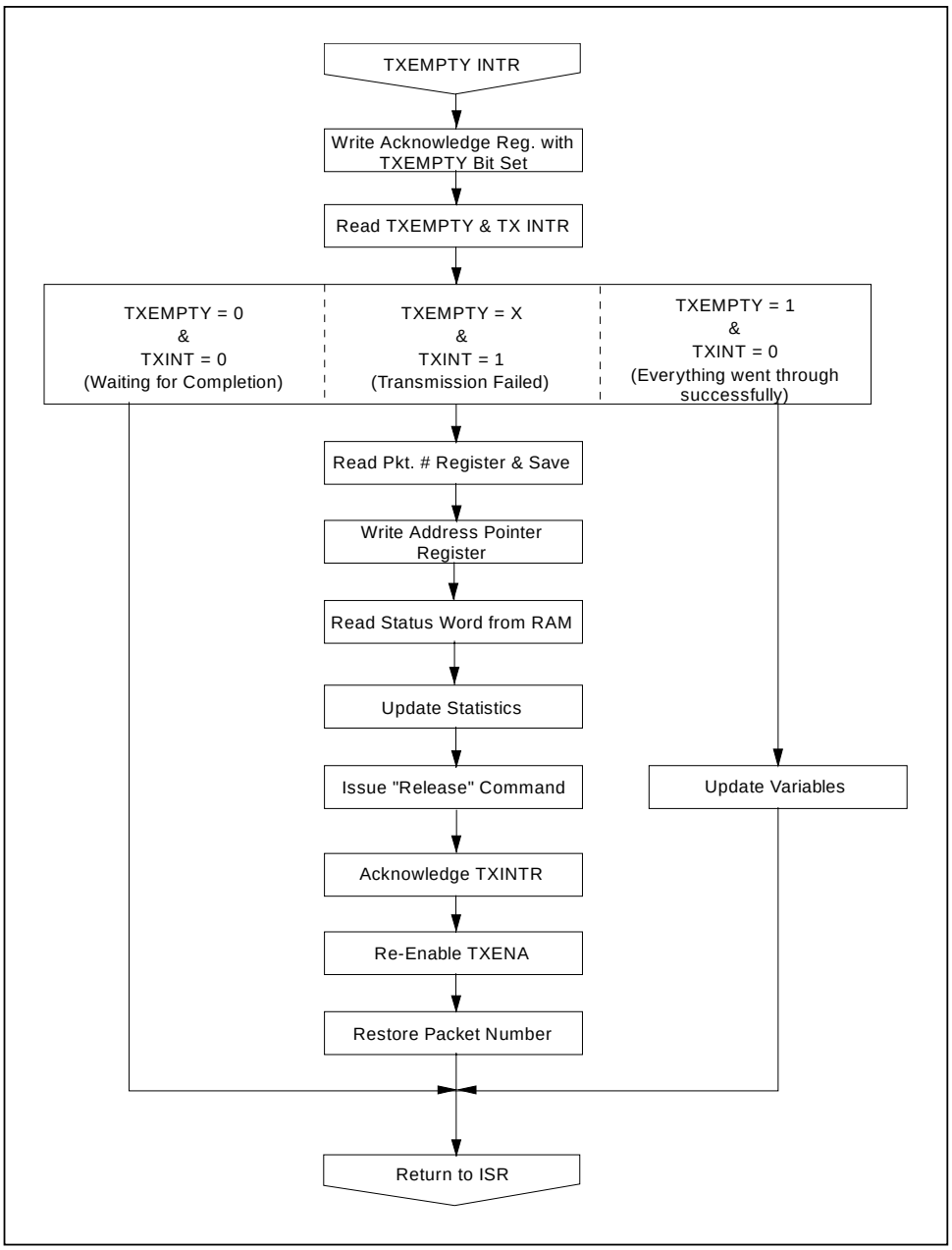

Figure 5.6 - TXEMPTY INTR (Assumes auto release option selected)

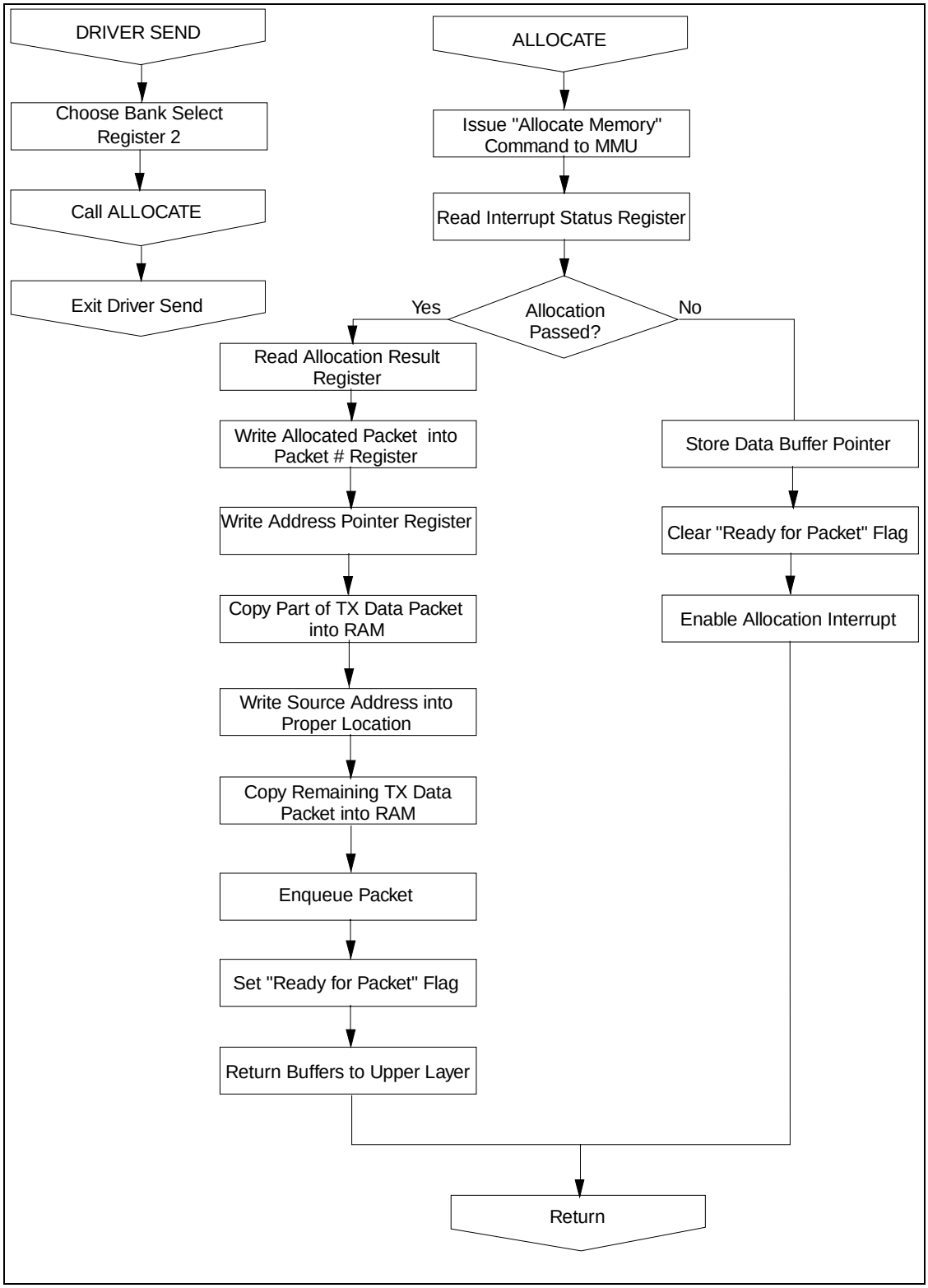

Figure 5.7 - Drive Send and Allocate Routines

5.5 Memory Partitioning

Unlike other controllers, the LAN91C110 does not require a fixed memory partitioning between transmit and receive resources. The MMU allocates and de-allocates memory upon different events. An additional mechanism allows the CPU to prevent the receive process from starving the transmit memory allocation.

Memory is always requested by the side that needs to write into it, that is: the CPU for transmit or the MAC for receive. The CPU can control the number of bytes it requests for transmit but it cannot determine the number of bytes the receive process is going to demand. Furthermore, the receive process requests will be dependent on network traffic, in particular on the arrival of broadcast and multicast packets that might not be for the node, and that are not subject to upper layer software flow control.

In order to prevent unwanted traffic from using too much memory, the CPU can program a "memory reserved for transmit" parameter. If the free memory falls below the "memory reserved for transmit" value, MMU requests from the MAC block will fail and the packets will overrun and be ignored. Whenever enough memory is released, packets can be received again. If the reserved value is too large, the node might lose data which is an abnormal condition. If the value is kept at zero, memory allocation is handled on first-come first-served basis for the entire memory capacity.

Note that with the memory management built into the LAN91C110, the CPU can dynamically program this parameter. For instance, when the driver does not need to enqueue transmissions, it can allow more memory to be allocated for receive (by reducing the value of the reserved memory). Whenever the driver needs to burst transmissions it can reduce the receive memory allocation. The driver program the parameter as a function of the following variables:

1. Free memory (read only register)
2. Memory size (read only register)

The reserved memory value can be changed on the fly. If the MEMORY RESERVED FOR TX value is increased above the FREE MEMORY, receive packets in progress are still received, but no new packets are accepted until the FREE MEMORY increases above the MEMORY RESERVED value.

5.6 Interrupt Generation

The interrupt strategy for the transmit and receive processes is such that it does not represent the bottleneck in the transmit and receive queue management between the software driver and the controller. For that purpose there is no register reading necessary before the next element in the queue (namely transmit or receive packet) can be handled by the controller. The transmit and receive results are placed in memory.

The receive interrupt will be generated when the receive queue (FIFO of packets) is not empty and receive interrupts are enabled. This allows the interrupt service routine to process many receive packets without exiting, or one at a time if the ISR just returns after processing and removing one.

There are two types of transmit interrupt strategies:

1. One interrupt per packet.
2. One interrupt per sequence of packets.

The strategy is determined by how the transmit interrupt bits and the AUTO RELEASE bit are used.

TX INT bit - Set whenever the TX completion FIFO is not empty.

TX EMPTY INT bit - Set whenever the TX FIFO is empty.

AUTO RELEASE - When set, successful transmit packets are not written into completion FIFO, and their memory is released automatically.

1. One interrupt per packet: enable TX INT, set AUTO RELEASE=0. The software driver can find the completion result in memory and process the interrupt one packet at a time. Depending on the completion code the driver will take different actions. Note that the transmit process is working in parallel and other transmissions might be taking place. The LAN91C110 is virtually queuing the packet numbers and their status words.

In this case, the transmit interrupt service routine can find the next packet number to be serviced by reading the TX FIFO PACKET NUMBER at the FIFO PORTS register. This eliminates the need for the driver to keep a list of packet numbers being transmitted. The numbers are queued by the LAN91C110 and provided back to the CPU as their transmission completes.

2. One interrupt per sequence of packets: Enable TX EMPTY INT and TX INT, set AUTO RELEASE=1. TX EMPTY INT is generated only after transmitting the last packet in the FIFO.

TX INT will be set on a fatal transmit error allowing the CPU to know that the transmit process has stopped and therefore the FIFO will not be emptied.

This mode has the advantage of a smaller CPU overhead, and faster memory de-allocation. Note that when AUTO RELEASE=1 the CPU is not provided with the packet numbers that completed successfully.

Note: The pointer register is shared by any process accessing the LAN91C110 memory. In order to allow processes to be interruptable, the interrupting process is responsible for reading the pointer value before modifying it, saving it, and restoring it before returning from the interrupt.

Typically there would be three processes using the pointer:

1. Transmit loading (sometimes interrupt driven)
2. Receive unloading (interrupt driven)
3. Transmit Status reading (interrupt driven).

1) and 3) also share the usage of the Packet Number Register. Therefore saving and restoring the PNR is also required from interrupt service routines.

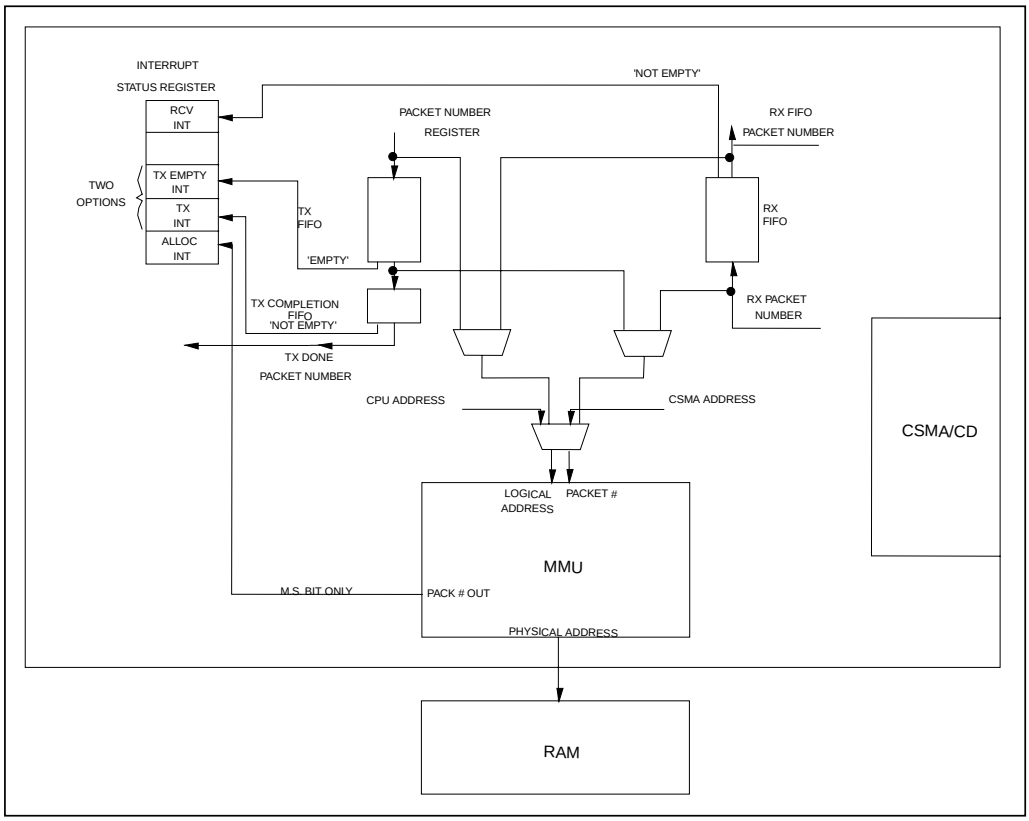

Figure 5.8 – Interrupt Generation for Transmit, Receive, MMU

Chapter 6 Operational Description

6.1 Maximum Guaranteed Ratings*

Operating Temperature Range ..... 0 EC to +70EC
Storage Temperature Range .....-55EC°to + 150EC
Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground .....V_{CC} + 0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

6.2 DC Electrical Characteristics

(T_A = 0EC - 70EC, V_{CC} = +5.0 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	3.0			V	
Input Leakage (All I and IS buffers except pins with pullups/pulldowns)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	$V_{IN} = V_{CC}$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O8 Type Buffer						
Low Output Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD16 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 16 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
Supply Current Active	I_{CC}		60	95	mA	All outputs open.
Supply Current Standby	I_{CSBY}		8		mA	

CAPACITANCE T_A = 25EC; fc = 1MHz; V_{CC} = 5V

PARAMETER	SYMBOL	LIMITS				TEST CONDITION
		MIN	TYP	MAX	UNIT	
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

CAPACITIVE LOAD ON OUTPUTS

ARDY, D0-D15	240 pF
All other outputs	45 pF

Chapter 7 Timing Diagrams

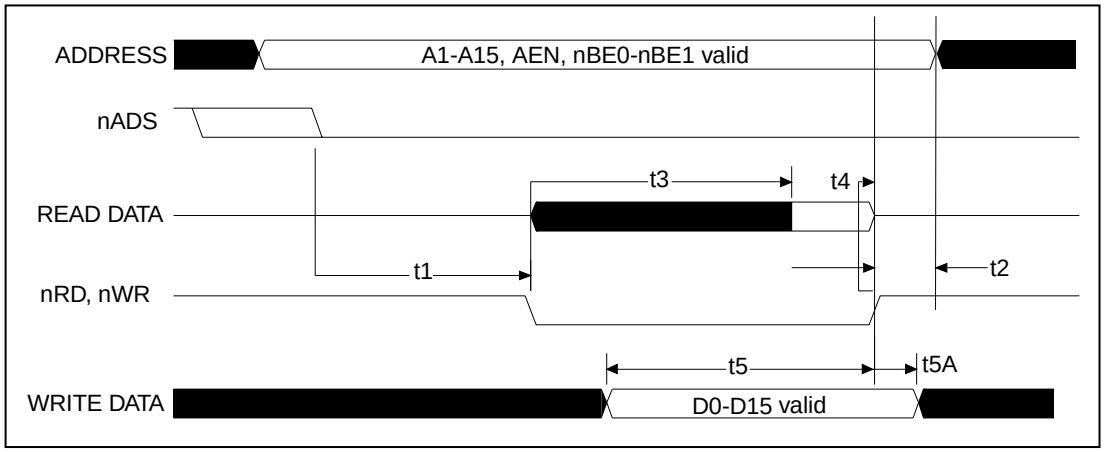

Figure 7.1 - Asynchronous Cycle - nADS=0

	PARAMETER	MIN	TYP	MAX	UNITS
t1	A1-A15, AEN, nBE0-nBE1 Valid and nADS Low Setup to nRD, nWR Active	25			ns
t2	A1-A15, AEN, nBE0-nBE1 Hold After nRD, nWR Inactive (Assuming nADS Tied Low)	20			ns
t3	nRD Low to Valid Data			40	ns
t4	nRD High to Data Floating			30	ns
t5	Data Setup to nWR Inactive	30			ns
t5A	Data Hold After nWR Inactive	5			ns

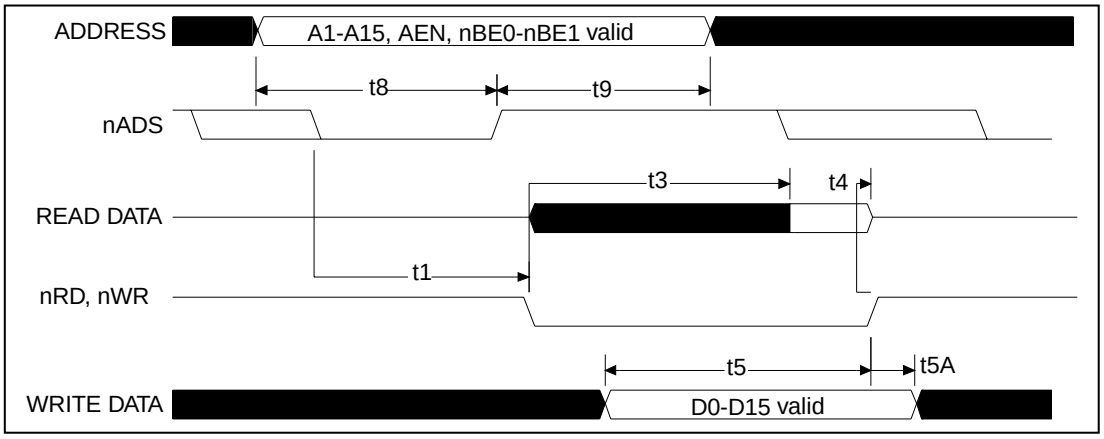

Figure 7.2 - Asynchronous Cycle - USING nADS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	A1-A15, AEN, nBE0-nBE1 Valid and nADS Low Setup to nRD, nWR Active	25			ns
t3	nRD Low to Valid Data			40	ns
t4	nRD High to Data Floating			30	ns
t5	Data Setup to nWR Inactive	30			ns
t5A	Data Hold After nWR Inactive	5			ns
t8	A1-A15, AEN, nBE0-nBE1 Setup to nADS Rising	10			ns
t9	A1-A15, AEN, nBE0-nBE1 Hold after nADS Rising	15			ns

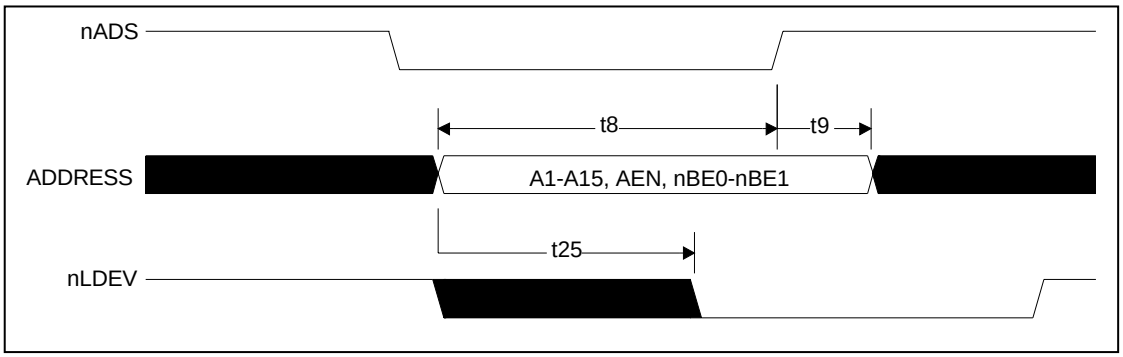

Figure 7.3 – Address Latching for All Modes

	PARAMETER	MIN	TYP	MAX	UNITS
t8	A1-A15, AEN, nBE0-nBE1 Setup to nADS Rising	10			ns
t9	A1-A15, AEN, nBE0-nBE1 Hold After nADS Rising	15			ns
t25	A4-A15, AEN to nLDEV Delay			20	ns

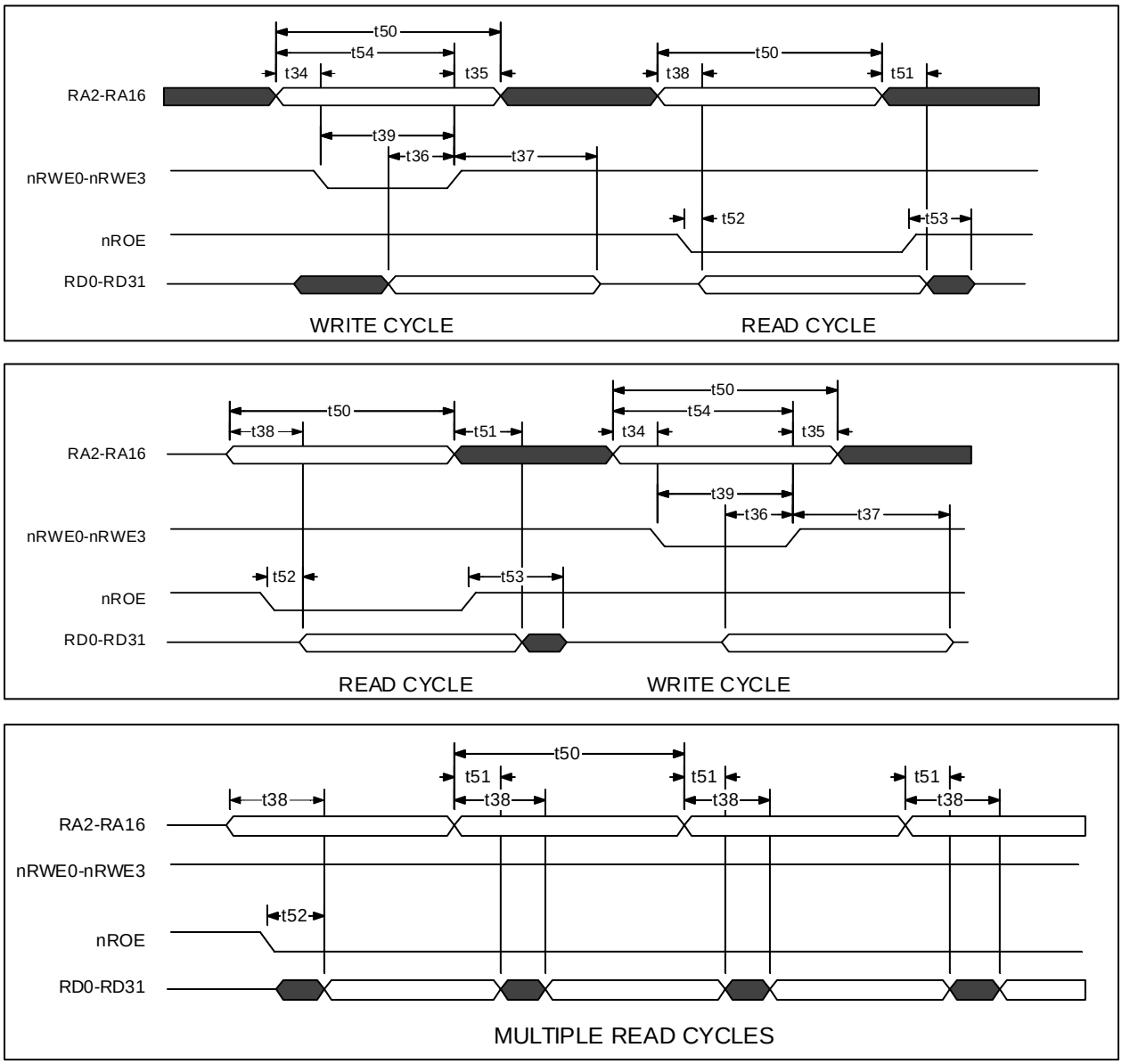

Figure 7.4 - SRAM Interface

	PARAMETER	MIN	TYP	MAX	UNITS
t34	Write – RA2-RA16 Setup to nRWE0-nRWE3 Falling	0			ns
t35	Write – RA2-RA16 Hold after nRWE0-nRWE3 Rising	0			ns
t36	Write – RD0-RD31 Setup to nRWE0-nRWE3 Rising	12			ns
t37	Write – RD0-RD31 Hold after nRWE0-nRWE3 Rising	0			ns
t39	Write – nRWE0-nRWE3 Pulse Width	15			ns
t54	Write – RA2-RA16 Valid to End of Write	12			ns
t38	Read – RA2-RA16 Valid to RD0-RD31 Valid			15	ns
t51	Read – RD0-RD31 Hold after RA2-RA16 Change	3			ns
t52	Read – nROE enable to RD0-RD31 Valid			12	ns
t53	Read – nROE disable to RD0-RD31 Invalid	0		8	ns
t50	Read/Write – Cycle Time	25			ns

APPLICATION NOTE

The following is the list of potential SRAMs and suppliers for the LAN91C110 Rev B. These SRAMs meet all timing requirements for LAN91C110 Rev B. But any other SRAM that meets the specification will also work with the LAN91C110 Rev B.

		Min ≥ 3ns	Max≤15ns	Min≤25ns	Max≤12ns	Max≤8ns	Min≤12ns	Min≤12ns	Min≤15ns
Manufacturer	Part #	t51 Data Hold after Address Change	t38 Address Valid to Data Valid	R/W Cycle	Output Enable to Output Valid	nROE Disable to Output in High Z	Address Valid to End of Write	Data Setup to End of Write	Write Pulse Width
ISSI	IS61C3216-10	3	10	10	5	5	9	5	7
ISSI	IS61C3216-12	3	12	12	5	6	10	6	8
ISSI	IS61C3216-15	3	15	15	7	7	11	7	10
Alliance	AS7C256-12	3	12	12	5	3	8	6	8
Alliance	AS7C256-15	3	15	15	6	4	10	8	9
Winbond	24257AJ-10	3	10	10	5	5	9	6	9
Winbond	24257AJ-12	3	12	12	6	6	10	7	10
Cypress	CY7C199-10VC	3	10	10	5	5	7	5	7
Cypress	CY7C199-12VC	3	12	12	5	5	9	8	8
Cypress	CY7C199-15VC	3	15	15	7	7	10	9	9
Cypress	CY7C1021-10	3	10	10	5	5	7	5	7
Cypress	CY7C1021-12	3	12	12	6	6	8	6	8
Cypress	CY7C1021-15	3	15	15	7	7	10	8	10
IDT	IDT71016S12	4	12	12	7	6	9	7	9
IDT	IDT71016S15	4	15	15	8	6	10	8	10
IDT	IDT71256SA12	3	12	12	6	6	9	6	8
IDT	IDT71256SA15	3	15	15	7	6	10	7	10
SamSung	K6E0808C1E-C10	3	10	10	5	5	8	5	8
SamSung	K6E0808C1E-C12	3	12	12	6	6	9	6	9
SamSung	K6E0808C1E-C15	3	15	15	7	7	10	7	10

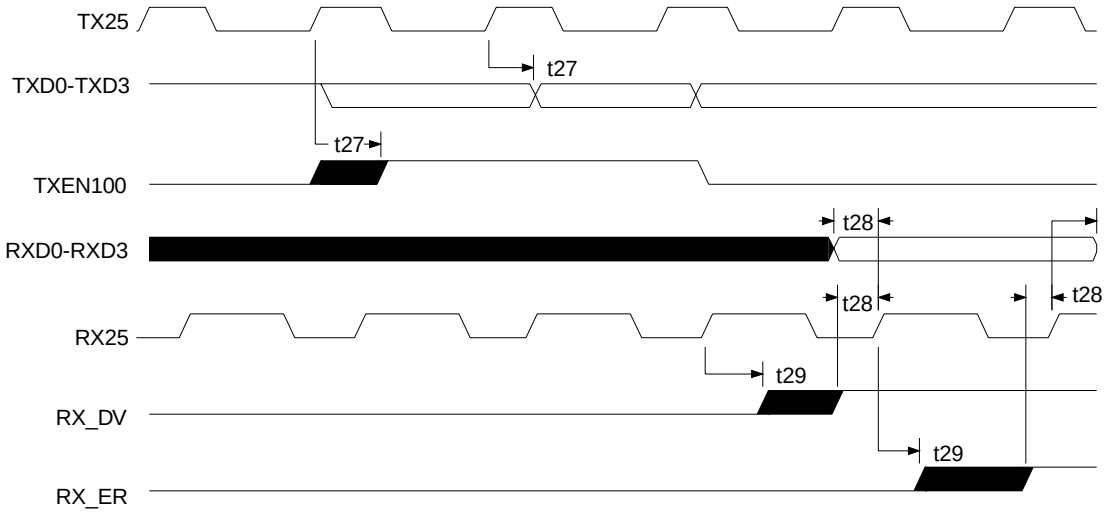

Figure 7.5 - MII Interface

	PARAMETER	MIN	TYP	MAX	UNITS
t27	TXD0-TXD3, TXEN100 Delay from TX25 Rising	0		15	ns
t28	RXD0-RXD3, RX_DV, RX_ER Setup to RX25 Rising	10			ns
t29	RXD0-RXD3, RX_DV, RX_ER Hold After RX25 Rising	10			ns

Chapter 8 Package Outline

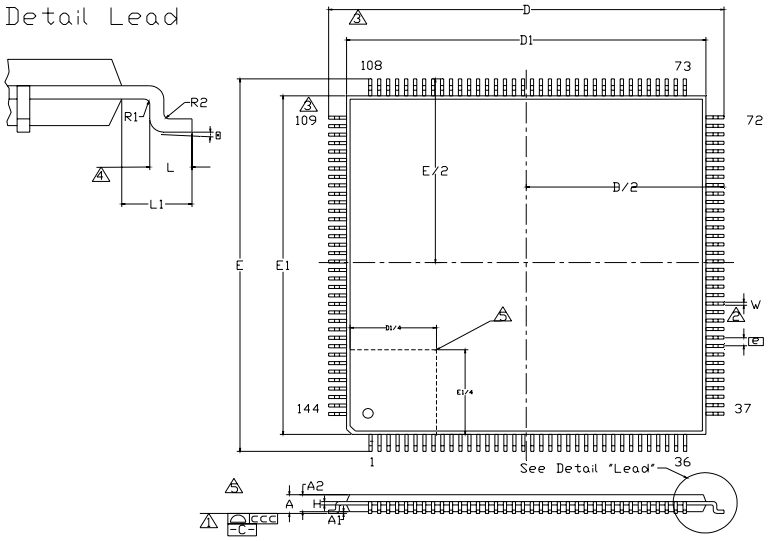

Figure 8.1 - 144 Pin TQFP Package Outlines

Table 8.1 – 144 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	1.0	1.20	Overall Package Height
A1	0.05	0.10	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D	21.80	22.00	22.20	X Span
D/2	10.90	11.00	11.10	$^1/_2$ X Span Measure from Centerline
D1	19.80	20.00	20.20	X body Size
E	21.80	22.00	22.20	Y Span
E/2	10.90	11.00	11.10	$^1/_2$ Y Span Measure from Centerline
E1	19.80	20.00	20.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
	0^o	3.5^o	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Max Coplanarity *(Assemblers)*
ccc	~	~	0.08	Max Coplanarity *(Test House)*

Note 1: Controlling Unit: millimeter
Note 2: Tolerance on the position of the leads is ± 0.04 mm maximum.
Note 3: Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion Is 0.25 mm.
Note 4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.
Note 5: Details of pin 1 identifier are optional but must be located within the zone indicated.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Ethernet ICs ***category:***

Click to view products by Microchip ***manufacturer:***

Other Similar products are found below :

EZFM6324A S LKA5 EZFM6364A S LKA7 12200BS23MM EZFM5224A S LKA3 VSC8522XJQ-02 WGI219LM SLKJ3 JL82599EN S R1ZS EZFM6348A S LKA6 WGI219V SLKJ5 BCM84793A1KFSBG BCM56680B1KFSBLG BCM53402A0KFSBG BCM56960B1KFSBG EZX557AT2 S LKVX BCM56842A1KFTBG BCM56450B1KFSBG EZX557AT S LKW4 RTL8153-VC-CG CH395L BCM56864A1IFSBG WGI219LM SLKJ2 KSZ8462FHLI KSZ8841-16MVLI KSZ9897STXC KSZ8842-16MVLI KSZ8893MQL VSC8244XHG ADIN2111BCPZ FIDO2100BGA128IR0 FIDO5210BBCZ FIDO5200CBCZ ADIN1110BCPZ ADIN1110CCPZ ADIN1100BCPZ ADIN1110CCPZ-R7 ADIN1100CCPZ-R7 DM9000EP DM9161AEP HG82567LM S LAVY LAN9210-ABZJ LAN9221-ABZJ LAN9221I-ABZJ LAN9211-ABZJ EZFM4105F897C S LKAM EZFM4224F1433E S LKAD EZFM4224F1433I S LKAE FBFM2112F897C S LJLS JL82576GB S LJBM JL82576NS S LJBP RC82545GM 855561