SAMA7D65-Curiosity Kit User Guide

EV63J76A

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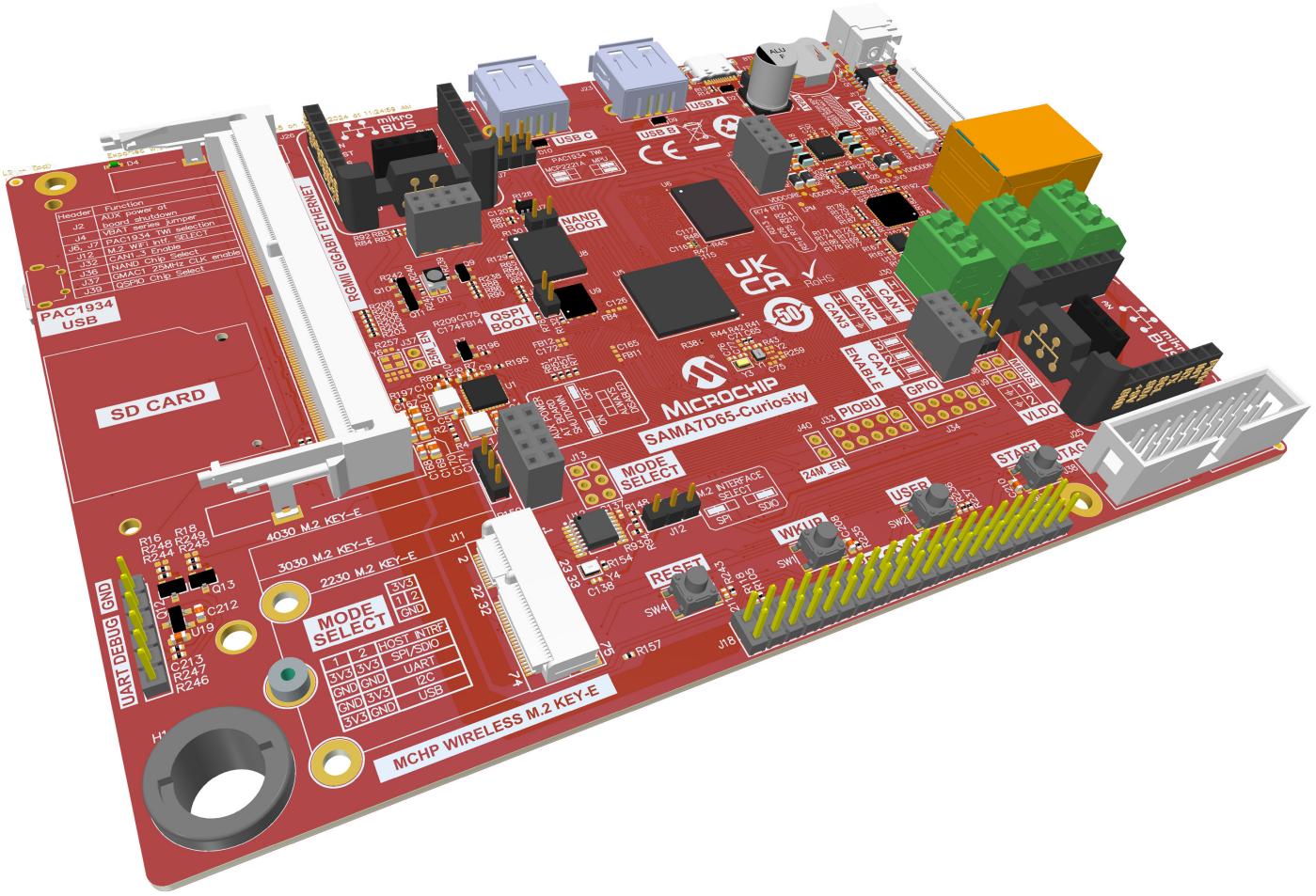
Scope

This user guide provides details on the overall design of the main board of the SAMA7D65-Curiosity Kit (EV63J76A) and describes how to use the kit effectively.

The kit is the evaluation platform for the SAMA7D6 Series MPU devices.

Figure 1. SAMA7D65-Curiosity Board Overview



1. Introduction

1.1 Document Layout

The document is organized as follows:

- Introduction
- Product Overview – Important information about the SAMA7D65-Curiosity board
- Function Blocks – Specifications of the SAMA7D65-Curiosity board and high-level description of the major components and interfaces
- Installation and Operation – Instructions on how to get started with the SAMA7D65-Curiosity board
- Errata
- Appendix: Schematics

1.2 Recommended Reading

The following Microchip document is available on www.microchip.com and recommended as a supplemental reference resource:

- SAMA7D6 Series Data Sheet (Lit. Number DS60001851)

2. Product Overview

2.1 Kit Content

The SAMA7D65-Curiosity Kit includes the following:

- The SAMA7D65-Curiosity board inside an ESD bag
- One USB Type-A to USB Type-C cable
- One 64 GB microSD card with SD adapter
- One QR code coupon pointing to the product web page

2.2 Board Features

Table 2-1. Board Features

Characteristic	Specification	Featured Components
Processor	SoC 343-ball TFBGA, 14x14 mm, 0.65 mm pitch	Microchip SAMA7D65-V/4HB-SL3
External clock	24-MHz crystal for MPU main clock 32.768-KHz crystal for MPU slow clock 32.768-KHz clock generator for M.2 interface 25-MHz crystal for on-board ETH RGMII	ECS-240-10-37B2-JTN-TR FC-12M 32.7680KA-A3 ASAK-32.768KHZ-LRS-T ECS-250-10-37B-CTN-TR
Memory	8-Gbit DDR3L 64-Mbit QSPI NOR Flash with EUI-48 4-Gbit SLC NAND Flash 2-Kbit EEPROM with EUI-48	AS4C512M16D3LA-10BIN Microchip SST26VF064BEUI-104I/MF MX30LF4G28AD-XKI Microchip 24AA025E48
SD/MMC	One 4-bit SD card socket One M.2 radio module interface, SDIO I/F multiplexed with an SPI interface	- -
USB	One device USB Type-C connector Two host USB Type-A connectors	Microchip MIC2026-1YM
Ethernet	One 10/100/1000 RGMII on board One 10/100/1000 RGMII SODIMM add-on slot	Microchip LAN8840-V/PSA -
Display	One MIPI DSI® 34-pin FPC connector One LVDS 30-pin FPC connector	-
Debug port	One UART debug connector One JTAG interface	- -
User interaction	One RGB (Red, Green, Blue) LED Four push button switches	- -
CAN-FD	Three on-board CAN-FD transceivers Two interfaces available on mikroBUS™ slots	Microchip MCP2542FDT-E/MF
Expansion	Raspberry Pi[note] 40-pin GPIO connector Two mikroBUS connectors Two PIOBU/System headers	- Hundreds of possible Click™ extensions featuring Microchip functions inside -
Power management	Power supply unit Power monitoring Daughter cards power supply Backup power supply	Microchip MCP16502TAB-E/S8B Microchip PAC1934 Microchip MIC23450-AAAYML CR1220 battery holder (battery not mounted)

.....continued		
Characteristic	**Specification**	**Featured Components**
Board supply	System 5 VDC from USB Type-C System 5 VDC from DC jack	- -

Note: Raspberry Pi is a trademark of Raspberry Pi Trading.

2.3 Specifications

Table 2-2. Specifications

Characteristic	Specification
Board identification	SAMA7D65-Curiosity Kit
Board supply voltage	External or USB-powered
Temperature	Operating: 0°C to +70°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	165 mm × 120 mm x 20 mm
RoHS status	RoHS 3 compliant
China RoHS status	EFUP50
REACH status	REACH compliant

2.4 Power Sources

Two options are available to power-up the board:

- Powering through the USB Type-C connector on the USBA port (J3)
- Powering through the DC jack connector (J1)

Table 2-3. Electrical Characteristics for DC Jack Connector

Electrical Parameters	Value
Input voltage	5 VDC
Maximum input voltage (limits)	6 VDC
Current capability	6 A

⚠ CAUTION The board runs at a 3.3V voltage level logic. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g., 5V) to an I/O pin could damage the board.

2.5 Connectors on Board

The board integrates multiple peripherals and interface connectors, as shown in the following figures.

Figure 2-1. Board Connectors on Top Side

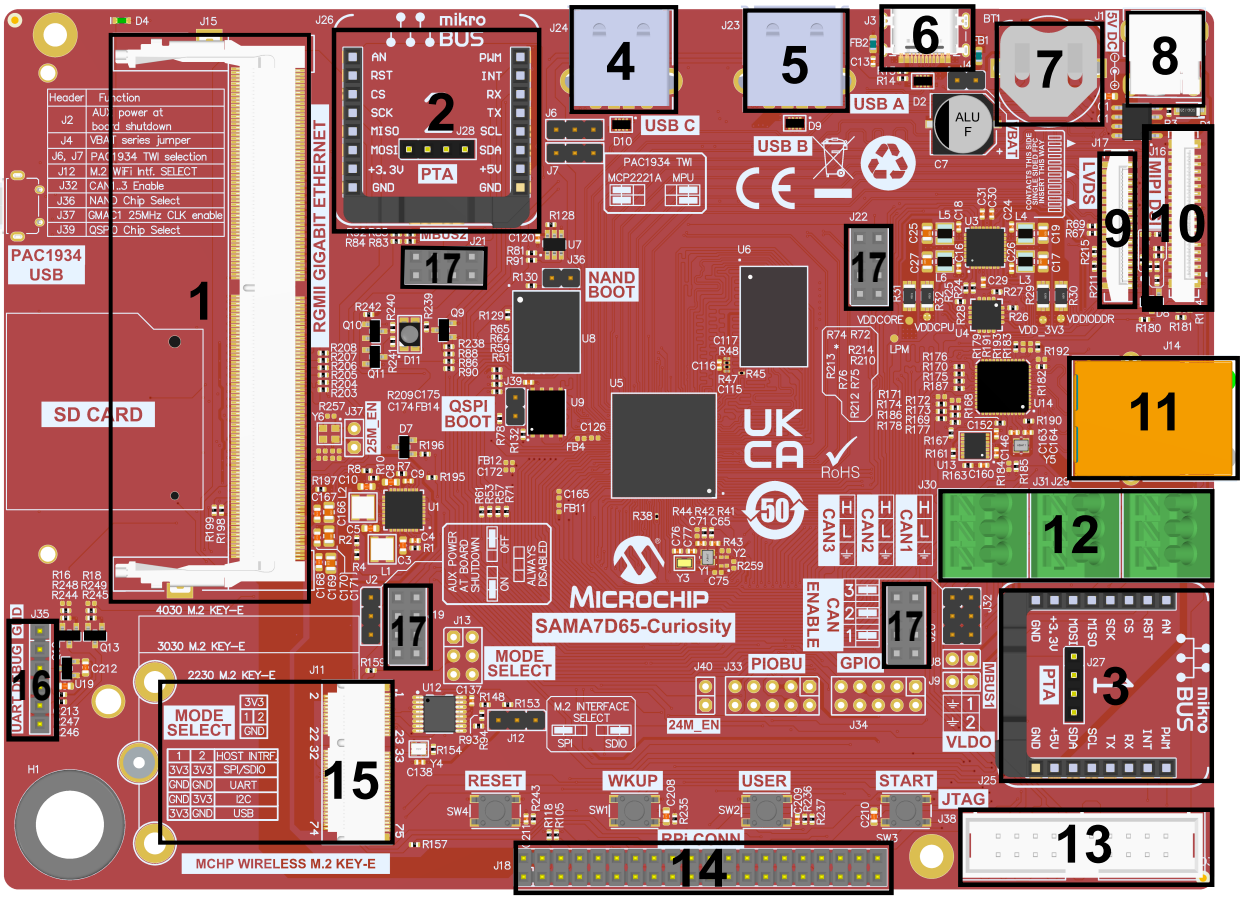


Table 2-4. Board Top Side Interface Connector Positions

Connector ID	Connector Designator	Connector Function
1	J15	10/100/1000 RGMII Ethernet and SPI SODIMM connector
2	J26	mikroBUS2 interface
3	J25	mikroBUS1 interface
4	J24	USB 2.0 Type-A (USB C)
5	J23	USB 2.0 Type-A (USB B)
6	J3	USB 2.0 Type-C (USB A)
7	BT1	CR1220 battery holder
8	J1	5V DC jack connector
9	J17	LVDS display 30-pin connector
10	J16	MIPI DSI 34-pin connector
11	J14	10/100/1000 GMAC0 Ethernet connector
12	J29, J31, J30	CAN1, CAN2 and CAN3 interfaces, respectively
13	J38	JTAG debug connector
14	J18	RPi 40-pin extension connector
15	J11	M.2 wireless interface connector
16	J35	FTDI connector (UART debugger)
17	J19, J20, J21, J22	2x4 female headers used for LCD fitting

Figure 2-2. Board Connectors on Bottom Side

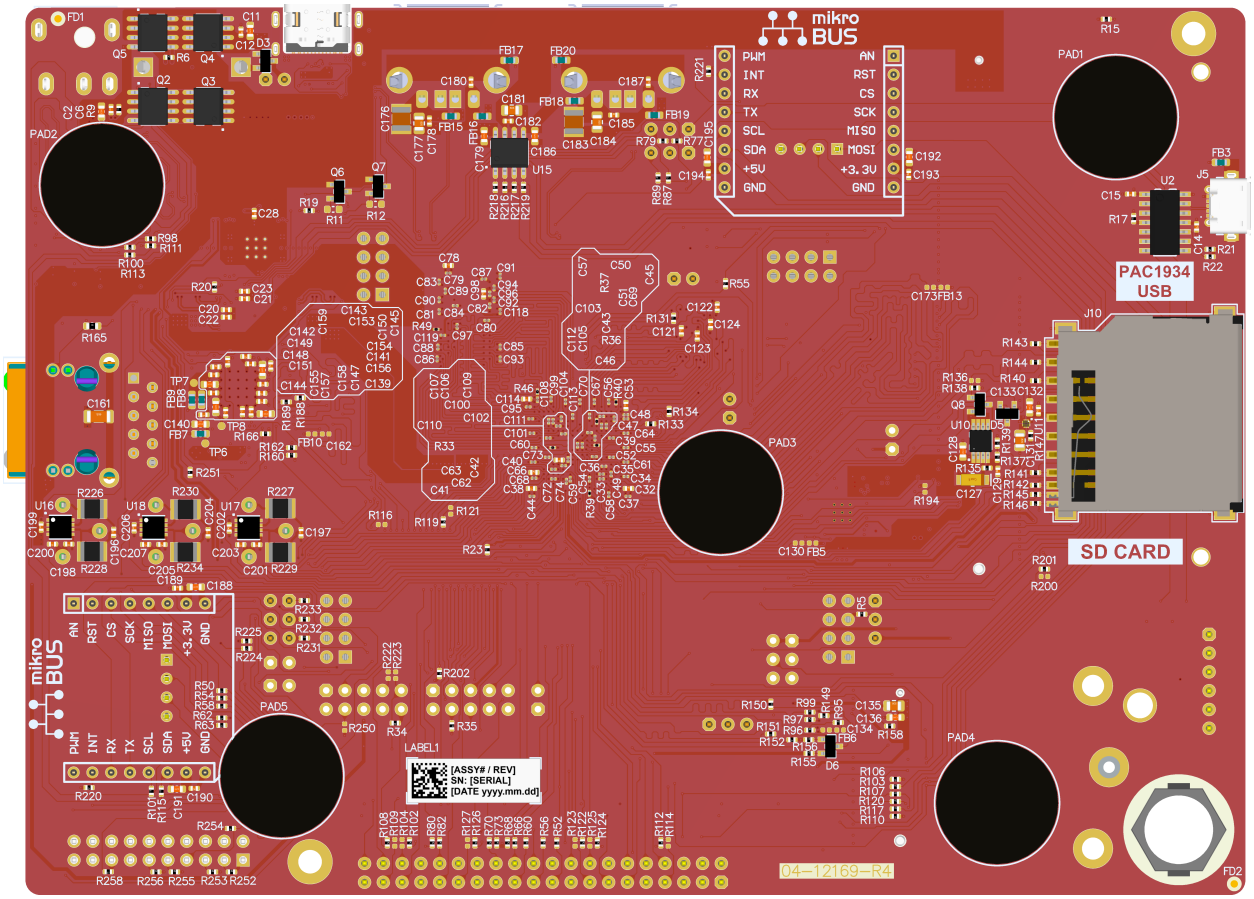


Table 2-5. Board Bottom Side Interface Connector Positions

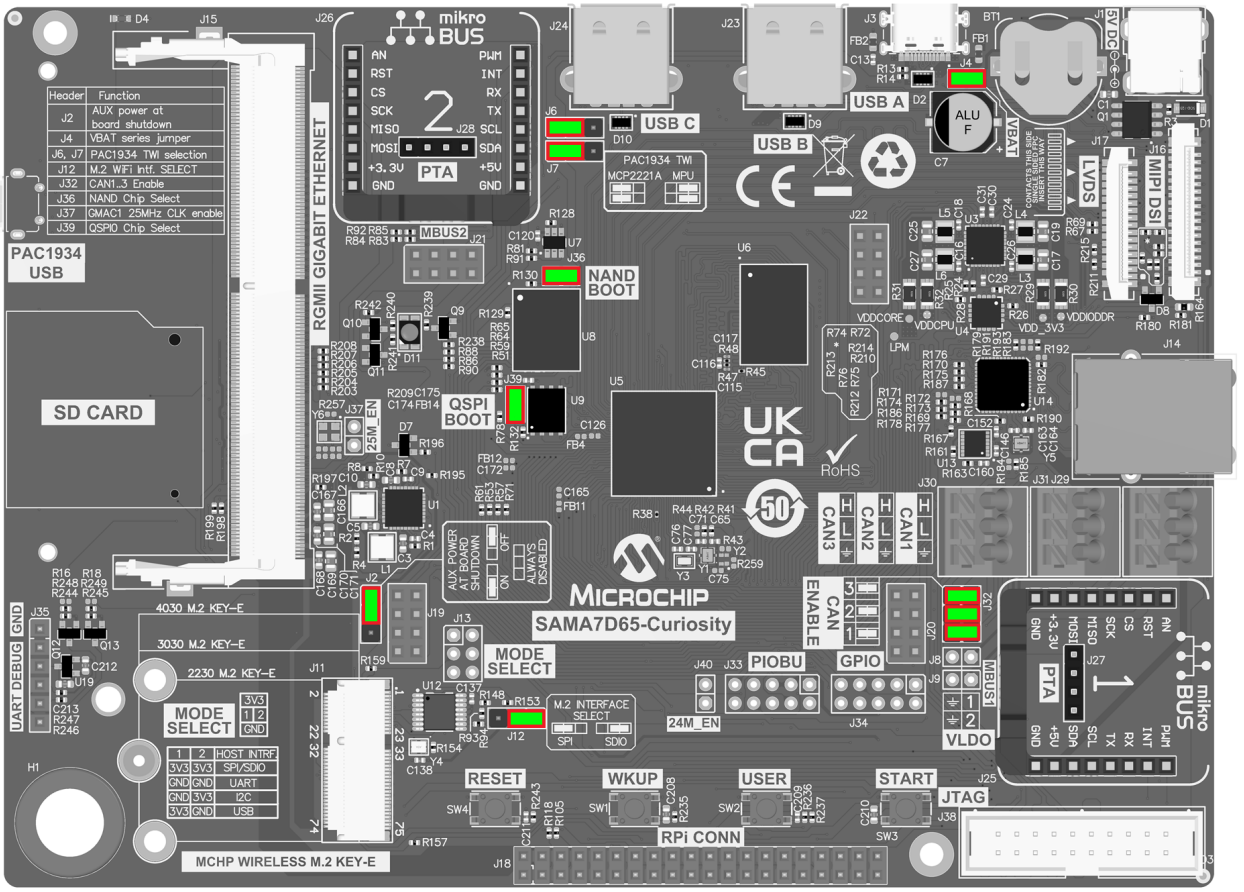
Connector ID	Connector Designator	Connector Function
1	J5	PAC1934 USB-to-I²C bridge connector
2	J10	SDMMC1 SD card interface

2.6 Default Jumper Settings

Table 2-6. Jumper Settings

Jumper	Default Setting	Function
JP1 @ J2	Closed 1-2	Extra 3.3V and 2.5V enable source select
JP2 @ J4	Closed	VDDBU current measurement
JP3 @ J6	Closed 1-2	PAC1934 TWCK selection on USB
JP4 @ J7	Closed 1-2	PAC1934 TWD selection on USB
JP5 @ J12	Closed 1-2 (default SDIO)	M.2 SDIO/SPI interface selection
JP6 @ J32	Closed 5-6	Enables CAN1 transceiver
JP7 @ J32	Closed 3-4	Enables CAN2 transceiver
JP8 @ J32	Closed 1-2	Enables CAN3 transceiver
JP9 @ J36	Closed	Enables NAND Flash boot
JP10 @ J39	Closed	Enables QSPI Flash boot

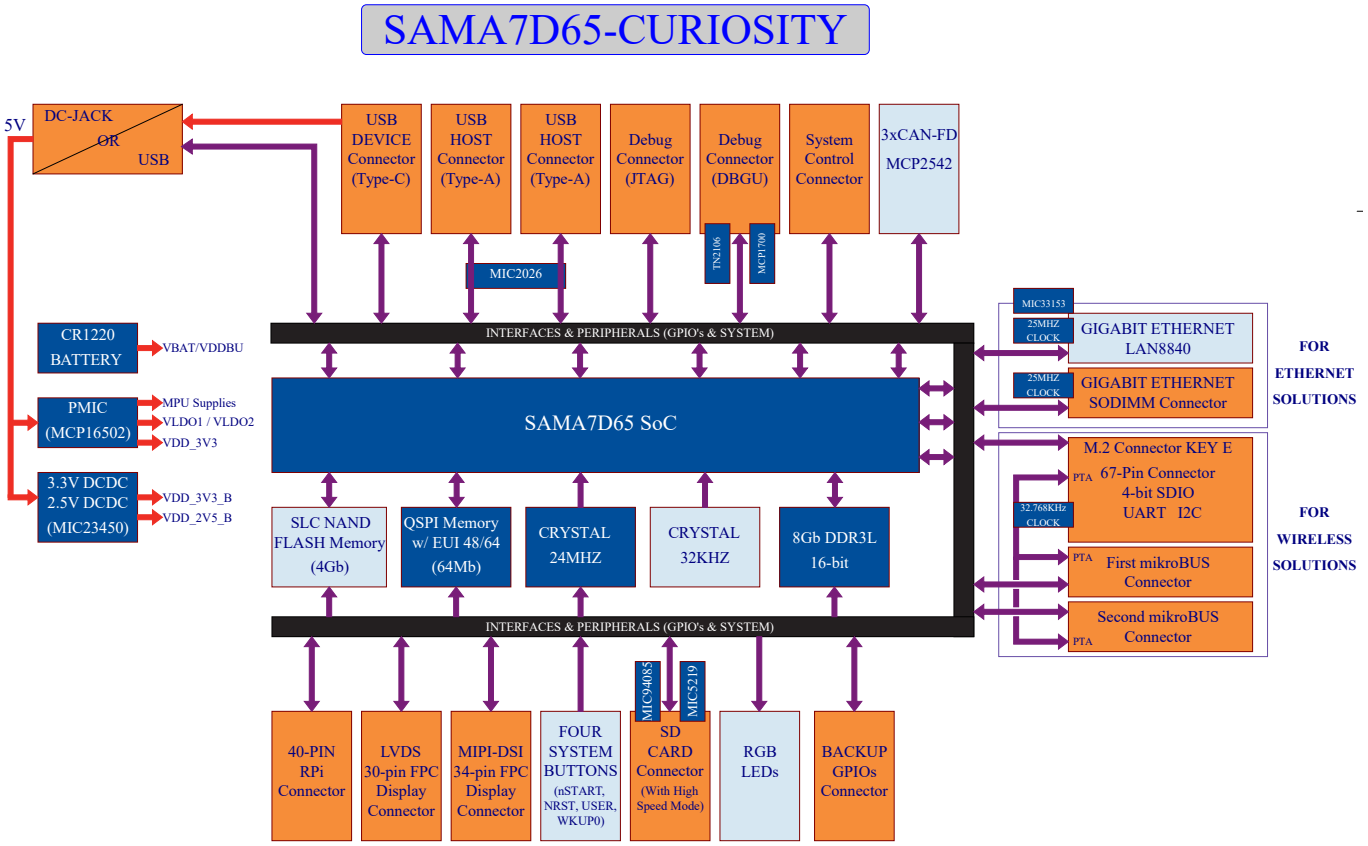
Figure 2-3. Default Jumper Settings



3. Function Blocks

This section covers the board specifications and provides a high-level description of the board's major components and interfaces. This document is not intended to provide detailed information about the processor or about any other components used on the board. Refer to the component documentation for further details.

Figure 3-1. Board Block Diagram



3.1 Power Supply Topology and Power Distribution

This section describes the implementation and circuitry that ensure adequate voltage stability for all the devices on the board and a correct power-up sequence for the MPU.

The power-up and power-down sequences indicated in the SAMA7D6 Series data sheet must be respected for a reliable operation of the device (see Recommended Reading).

3.1.1 Input Power Options

The board can be powered through:

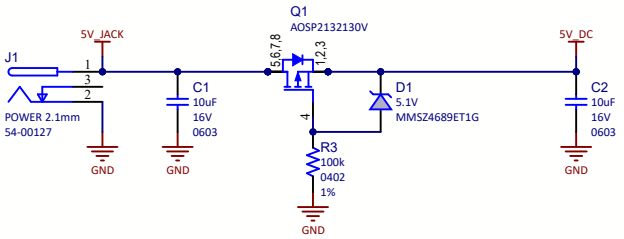
- An external AC to DC +5V wall adapter connected via a 2.1 mm center-positive plug into the power jack of the board (J1); the recommended output capability of the power adapter is 6A if the board is used with M.2 or SODIMM daughter cards.
- USB port A (J3) through a USB type-A to type-C cable.

WARNING Note that a symmetric type-C to type-C USB cable cannot be used to power the board.

3.1.1.1 Wall Adapter Input

The 5V DC Jack from the wall adapter is protected through an overvoltage and reverse voltage protection circuit implemented with Q1 and D1. The following figure shows the wall adapter input power supply topology.

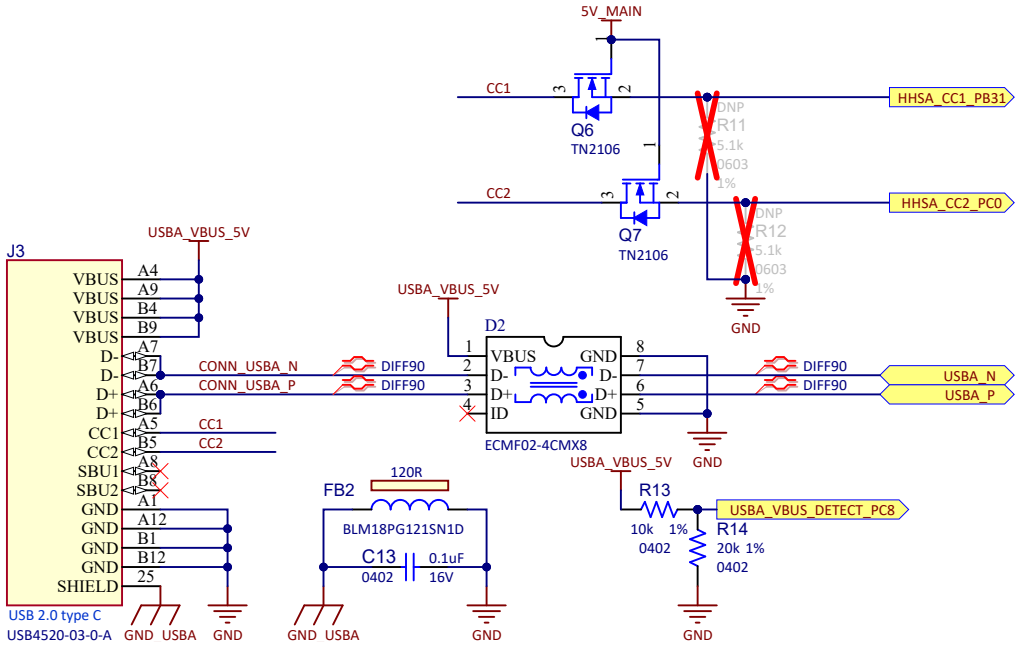
Figure 3-2. Wall Adapter Input Power Schematic



3.1.1.2 USB Supply Input

The USB-powered operation comes from the USB device port connected to a PC or a 5 VDC supply through a USB type-A to type-C cable. The USB supply is enough to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power. If a USB host port is required for the application, it is recommended to use the external DC supply or a more capable USB external power supply. The following figure shows the USB input power supply topology.

Figure 3-3. USB Input Power Schematic



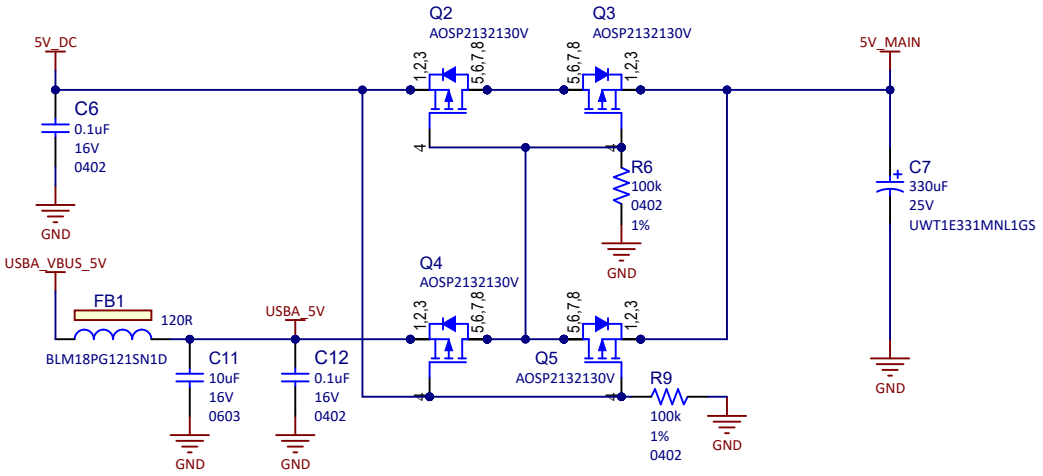
Note: USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

WARNING Note that a symmetric type-C to type-C USB cable cannot be used to power the board.

3.1.1.3 Automatic Power Switch

The switch between the two powering options is made by four transistors in an ideal diode configuration that ensures the separation between the two when both are plugged. The switch prioritizes powering from the wall adapter to maximize power transfer. The following figure shows the automatic power switch.

Figure 3-4. Automatic Power Switch Schematic



3.1.2 Power Management Integrated Circuit (PMIC)

The MCP16502 is a fully-featured PMIC optimized for Microchip MPU devices.

The MCP16502 integrates four DC-DC buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an interrupt flag and an I²C interface.

All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.

Two 300 mA LDOs are provided so that sensitive analog loads can be supported.

The default power channel sequencing is built-in, according to the requirements of the Microchip MPU device.

The MCP16502 features a low no-load operational quiescent current, and draws less than 10 µA in full shutdown.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

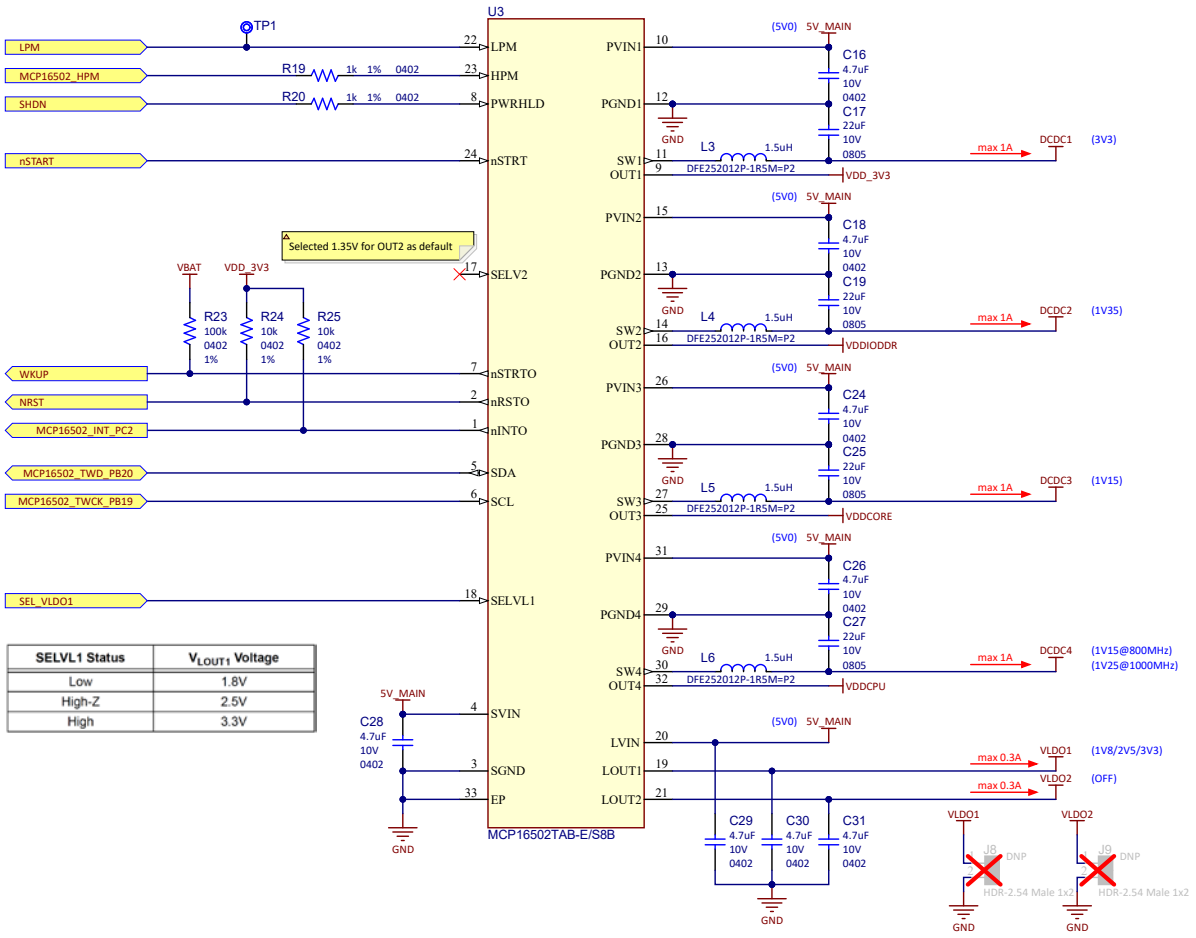
The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package. For more information on the MCP16502, refer to the product web page.

The MCP16502TAB provides all the specific voltages required for the MPU power rails:

- Buck1 supplies 3.3V to the SAMA7D6 Series I/O pads and devices (VDD_3V3).
- Buck2 supplies 1.35V to the SAMA7D6 Series DDR3 PHY pads (VDDIODDR) and external DDR3L memory device.
- Buck3 supplies 1.15V to the SAMA7D6 Series core (VDDCORE).
- Buck4 supplies 1.15V to the SAMA7D6 Series CPU (VDDCPU).

The figure below shows the power management scheme.

Figure 3-5. Power Management Unit Schematic



SELVL1 Status	V_{LOUT1} Voltage
Low	1.8V
High-Z	2.5V
High	3.3V

The two LDO outputs (VLDO1, VLDO2) are available for free use.

Table 3-1. MCP16502 TWI Address

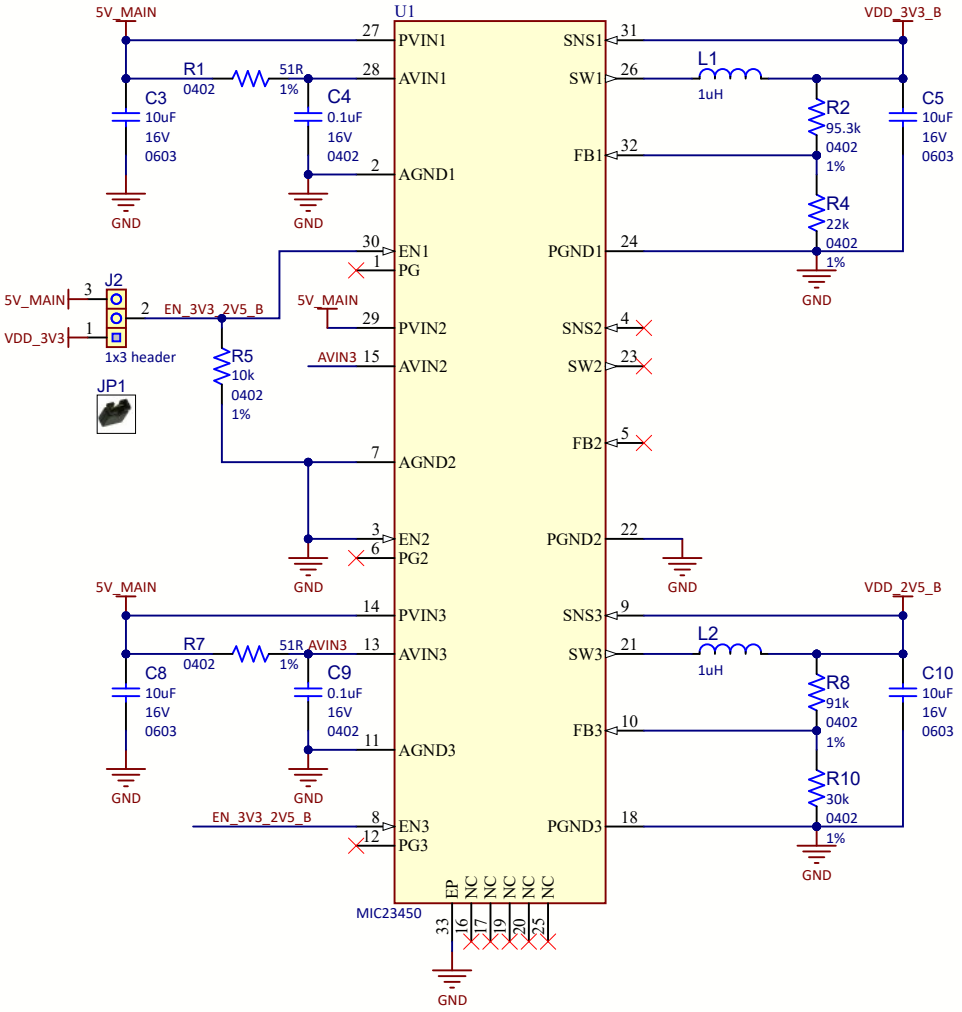
Device	7-bit Client Address
MCP16502	1011_011

3.1.3 Extra Power Supplies

The board supports many add-on boards with various power supply constraints. To satisfy all power requirements of large loads from SODIMM add-ons and M.2 daughter cards, additional power supplies are implemented on the main board, providing additional 3.3V (VDD_3V3_B) and 2.5V rails (VDD_2V5_B).

The MIC23450 is a high-efficiency, 3 MHz, triple 2A, synchronous buck regulator with HyperLight Load® mode and low-output ripple voltage over the entire load range. For more information, refer to www.microchip.com/en-us/product/mic23450.

Figure 3-6. Extra Power Supplies Schematic



If the JP1 jumper is placed on header J2 pins 2-3 (5V_MAIN connected to EN_3V3_2V5_B), it will enable the extra power simultaneously with the system power.

If a low-power consumption is required during PMIC shutdown, JP1 can be moved to 1-2 position of J2 (VDD_3V3 connected to EN_3V3_2V5_B). While the PMIC is in Shutdown mode, the enable pin of MIC23450 is kept low, disabling the 2.5V and 3.3V outputs. This is the default jumper configuration of the kit.

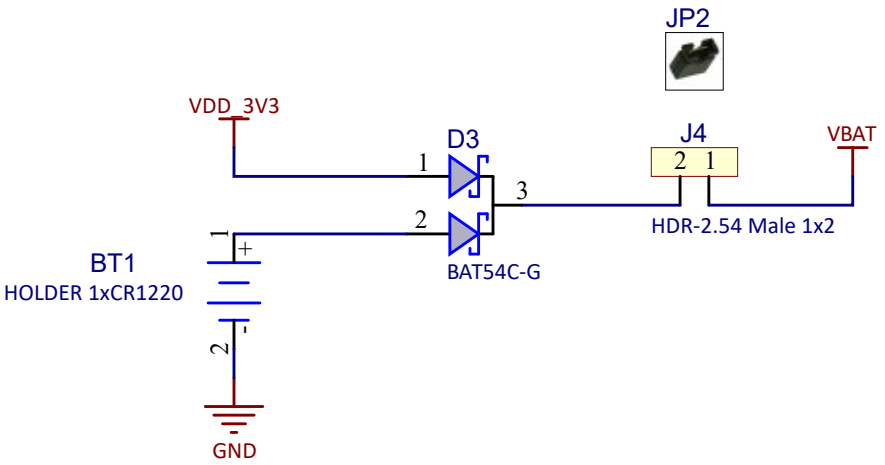
If the jumper is not placed on any position, the R5 resistor keeps the enable pin of MIC23450 low, disabling its outputs.

3.1.4 Battery Unit

A 3V CR1220 battery can be placed in the BT1 battery holder to permanently maintain the VDDBU voltage. This function allows the user to shut down the MPU and the system, thus entering a Low-Power mode, and still keep the custom configuration that was previously set in the MPU backup area.

Jumper JP2 must be in place for proper operation of the MPU and can be removed if the user wants to bring the MPU back to the initial configuration, by resetting the Backup registers (BUREG).

Figure 3-7. Backup Circuitry Schematic



Note: The board will reset if the jumper is removed during normal board operation.

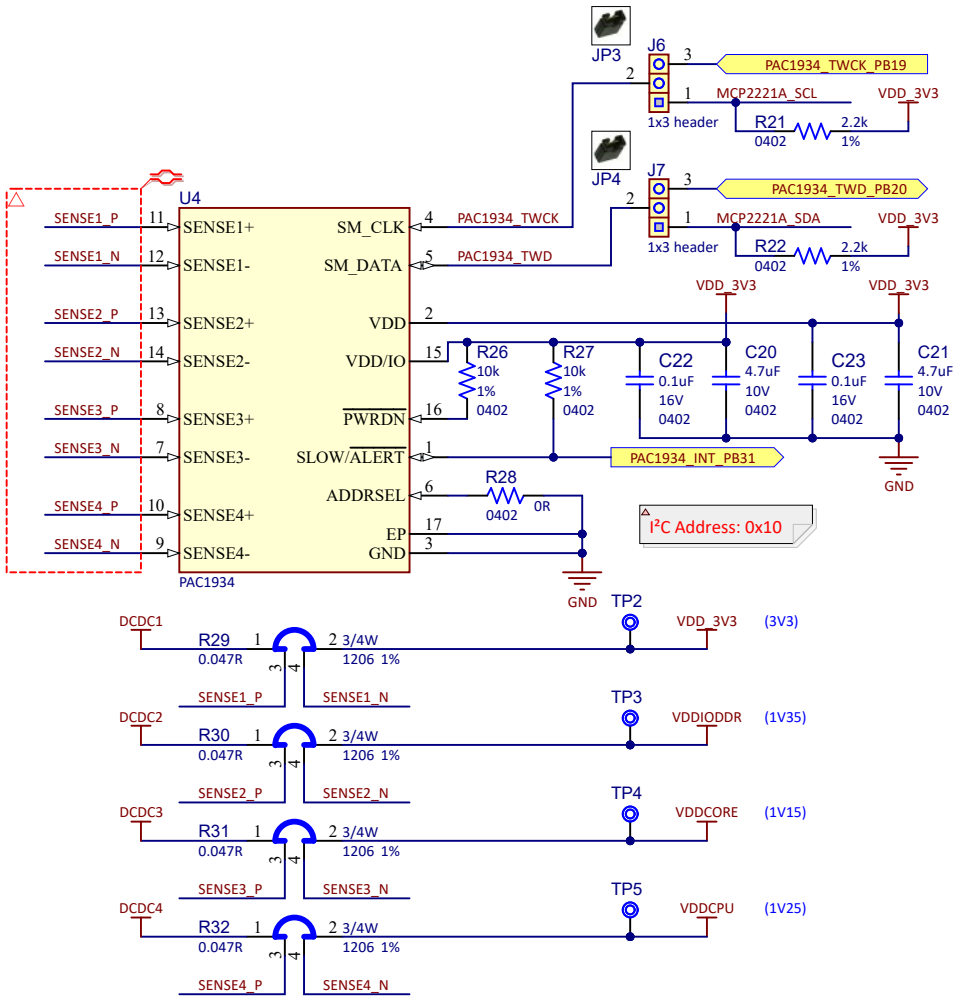
3.1.5 Power Measurement

The board features an embedded power measurement device, the PAC1934, used for measuring the power consumption of the main power rails related to the MPU and peripherals.

The PAC1934 is a four-channel power/energy monitor with a current sensor amplifier and bus voltage monitors that feed high-resolution ADCs. Digital circuitry performs power calculations and energy accumulation. The PAC1934 enables energy monitoring with integration periods from 1 millisecond up to 36 hours. Bus voltage, sense resistor voltage, and accumulated proportional power are stored in registers for retrieval by the system host or embedded controller. For more information, refer to www.microchip.com/en-us/product/pac1934.

Four power rails are monitored: VDD_3V3, VDDIODDR, VDDCORE, VDDCPU. Each rail has a 0.047-Ohm shunt resistor for current measurement.

Figure 3-8. Power Measurement Schematic



The board features two options for retrieving data:

- On-board USB-to-I²C bridge to access data with an external computer
- Host SAMA7D6 Series MPU to access the data via a local TWI bus

A set of jumpers is used to manually select between the two access modes, on headers J6 and J7.

By default, the USB-to-I²C bridge is selected.

For more details concerning the USB-to-I²C bridge, see USB-to-I²C bridge.

3.2 Processor

3.2.1 Processor Power Supplies

The SAMA7D6 Series is a high-performance Arm® Cortex®-A7 CPU-based embedded microprocessor (MPU) targeting HMI and connectivity applications in the home/building, industrial and appliance markets.

The SAMA7D6 Series is delivered with a comprehensive development suite that includes a mainline Linux® distribution and the Microchip MPLAB® X/Harmony software framework.

Running at up to 1 GHz, the device offers support for multiple memories, such as 16-bit DDR2, DDR3, DDR3L, LPDDR2, LPDDR3, octal/quad SPI and e.MMC Flash. It integrates various display

interfaces, including MIPI DSI, LVDS and 8-bit serial RGB, a dual 10/100/1000 Ethernet MAC and an I3C controller.

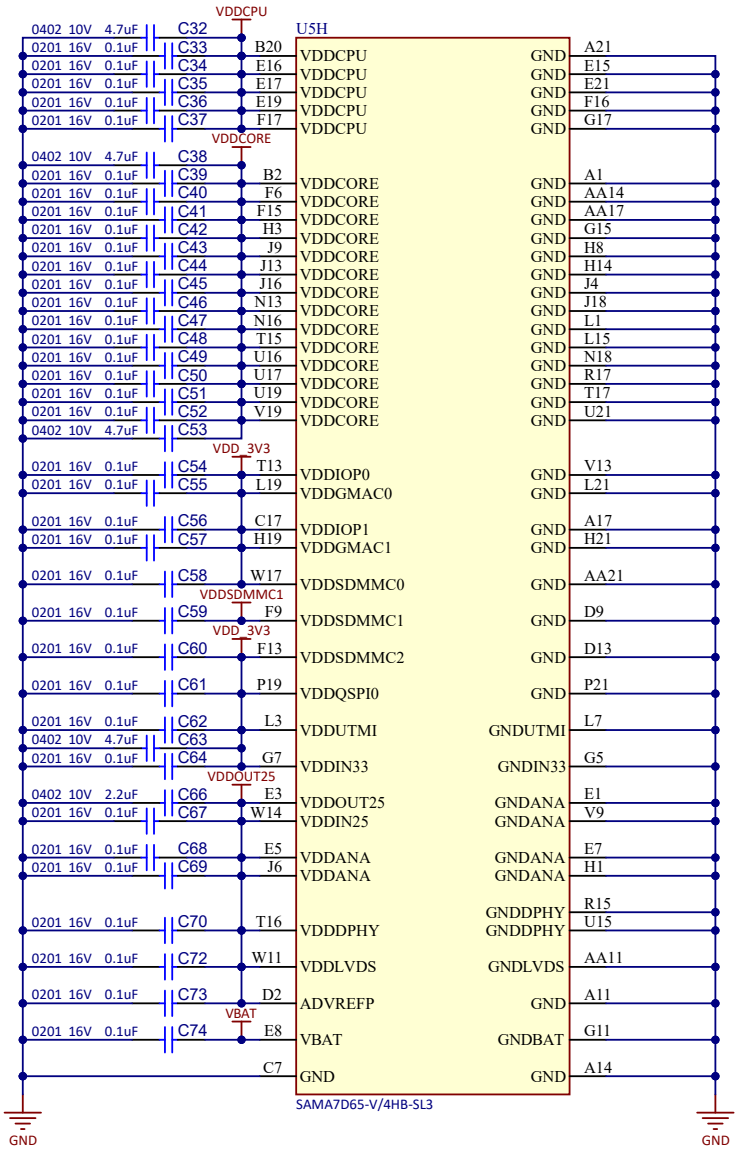
The SAMA7D6 Series features connectivity options such as five CAN-FD and three high-speed USB interfaces and embeds advanced security functions, such as PUF, secure boot, secure key storage and high-performance crypto accelerators for AES, SHA, RSA and ECC.

The power management unit IC (MCP16502) provides all power supplies required by the SAMA7D6 Series MPU:

- 1.15V ... 1.25V for the CPU power rail (VDDCPU)
- 1.15V for the core power rail (VDDCORE)
- 3.3V for I/Os, oscillators, LDO input and digital power rails (VDDUTMI, VDDIOP0, VDDIOP1, VDDQSPI0, VDDQSPI1, VDDSDMMC0, VDDSDMMC2, VDDIN33)
- 2.5V for analog rail and MIPI D-PHY (VDDANA, VDDDPHY). This rail is provided by the embedded LDO output (VDDOUT25).

Decoupling capacitors are placed close to the MPU power pins to stabilize the voltage rails.

Figure 3-9. SAMA7D6 Series MPU Power Decoupling



3.2.2 Main Configuration and Control

The following figure shows the main block for processor configuration and control.

Figure 3-10. Processor Main Configuration and Control

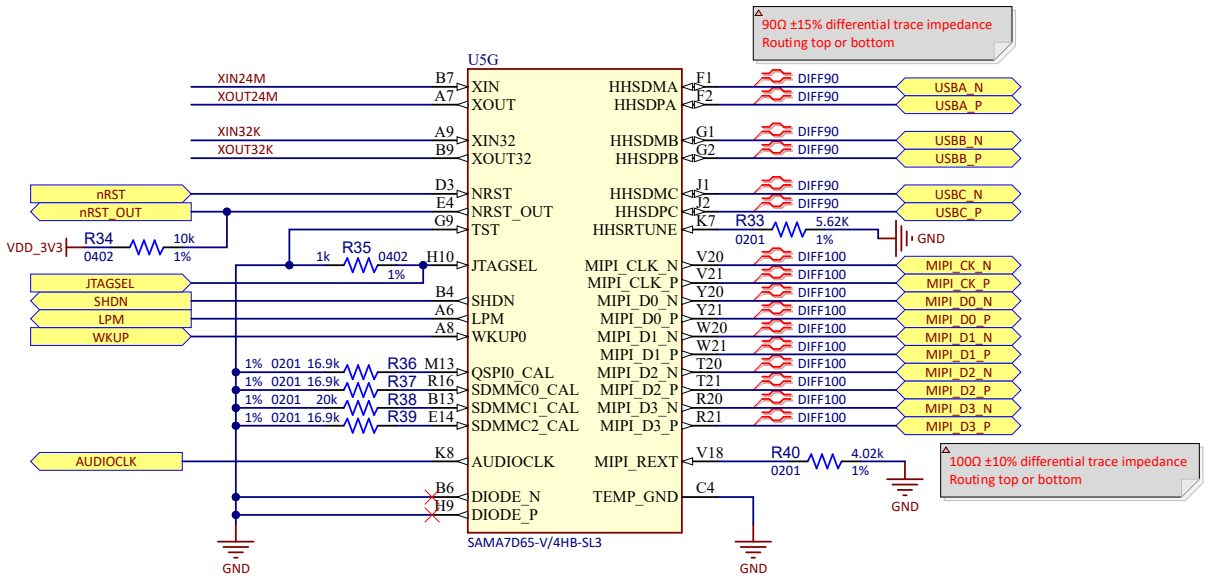


Table 3-2. Processor Main Configuration and Control

Pin Name	Type	Used for
XIN	Input	Main clock oscillator input
XOUT	Output	Main clock oscillator output
XIN32	Input	Slow clock oscillator input
XOUT32	Output	Slow clock oscillator output
SHDN	Output	Signal used to enable and disable an external power supply circuit
WKUP0	Input	Event detection input pin used to wake up the processor from Shutdown state
JTAGSEL	Input	When pulled high, enables the JTAG boundary scan
NRST	Input	Processor reset input
NRST_OUT	Output	Peripheral reset output
TST	Input	Reserved for processor manufacturing tests
LPM	Output	Low-Power mode enable output
QSPI0_CAL	Input	QSPI0 cell calibration
SDMMC0_CAL	Input	SDMMC0 cell calibration
SDMMC1_CAL	Input	SDMMC1 cell calibration
SDMMC2_CAL	Input	SDMMC2 cell calibration
AUDIOCLK	Output	Audio PLL clock output
HHSA_DM	Bidirectional	USB A negative differential signal
HHSA_DP	Bidirectional	USB A positive differential signal
HHSRTUNE	Input	USB cell calibration
HHSB_DM	Bidirectional	USB B negative differential signal
HHSB_DP	Bidirectional	USB B positive differential signal

.....continued		
Pin Name	**Type**	**Used for**
HHSC_DM	Bidirectional	USB C negative differential signal
HHSC_DP	Bidirectional	USB C positive differential signal
MIPI_CLK_N	Output	MIPI clock negative differential signal
MIPI_CLK_P	Output	MIPI clock positive differential signal
MIPI_DO_N	Output	MIPI data 0 negative differential signal
MIPI_DO_P	Output	MIPI data 0 positive differential signal
MIPI_D1_N	Output	MIPI data 1 negative differential signal
MIPI_D1_P	Output	MIPI data 1 positive differential signal
MIPI_D2_N	Output	MIPI data 2 negative differential signal
MIPI_D2_P	Output	MIPI data 2 positive differential signal
MIPI_D3_N	Output	MIPI data 3 negative differential signal
MIPI_D3_P	Output	MIPI data 3 positive differential signal
MIPI_REXT	Input	MIPI calibration cell
DIODE_N	Output	Reserved
DIODE_P	Output	Reserved
TEMP_GND	Input	GND

3.2.3 Clock Circuitry

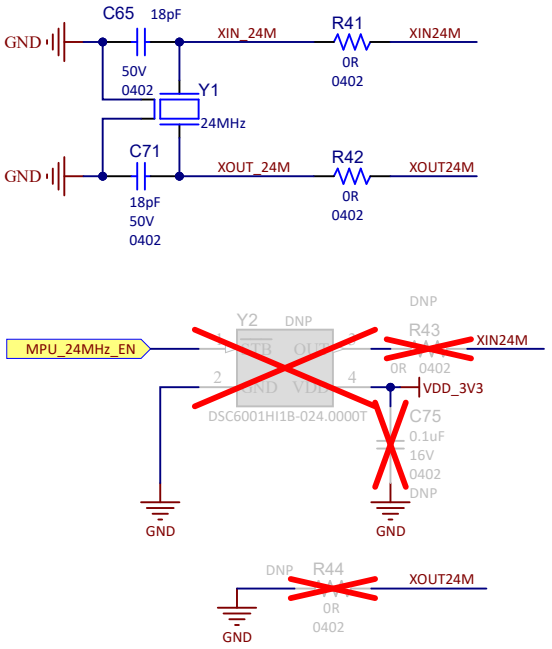
The MPU embedded clock generator generates the required clocks based on two oscillators: one slow clock (SLCK) oscillator running at 32.768 kHz and one main clock oscillator running at 24 MHz.

3.2.3.1 Main Clock Circuitry

The main clock oscillator is implemented with the crystal oscillator ECS-240-10-37B2-JTN-TR.

For evaluation purposes, the user can mount a 1.6 mm x 1.2 mm size MEMS oscillator instead of the crystal, using the PCB footprint reservation (Y2). In that case, remove resistors R41 and R42, and populate resistors R43 and R44, and capacitors C75 and Y2.

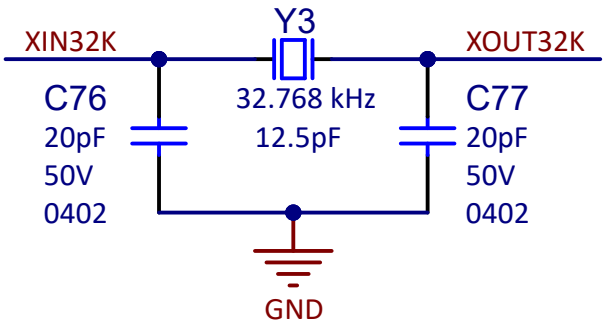
Figure 3-11. Processor Main Clock Schematic



3.2.3.2 Slow Clock Circuitry

The slow clock oscillator is implemented with an FC-12M 32.7680KA-A3 crystal device.

Figure 3-12. Processor Slow Clock Schematic

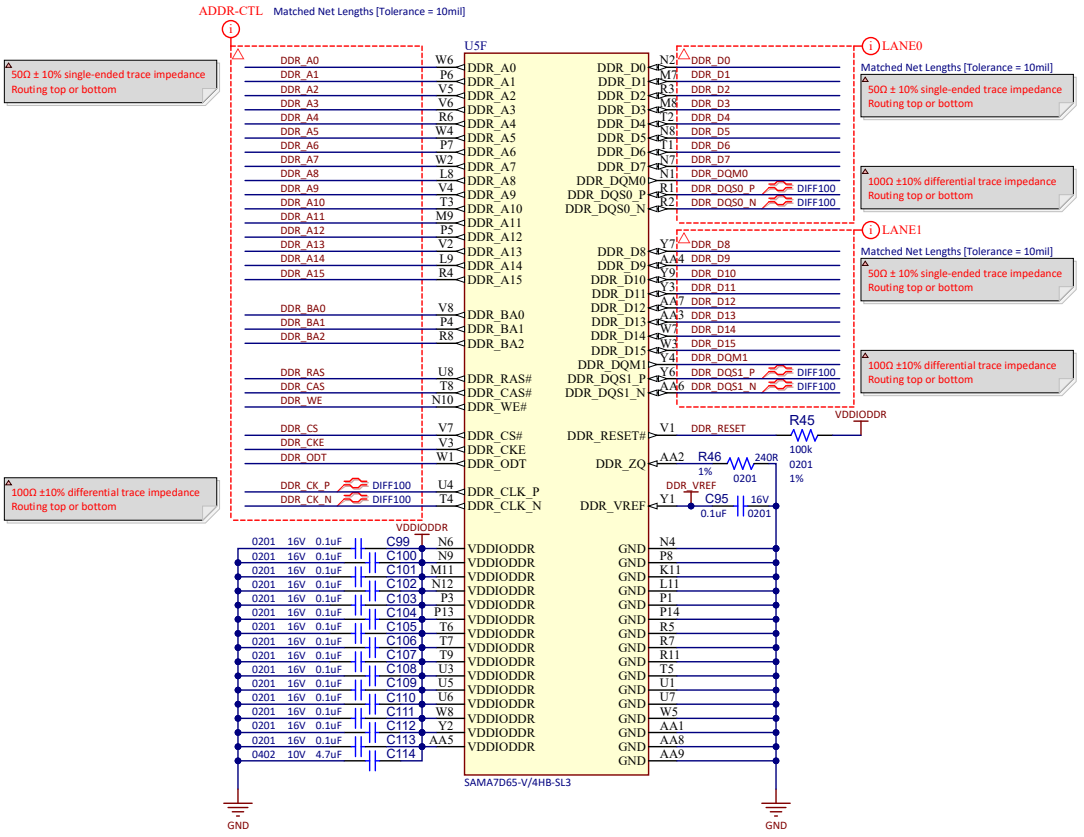


3.2.4 DDR Controller and DDR3L Memory Device

The SDRAM memory interface is made of the Universal DDR Memory Controller (UDDRC) and the physical layer interface (DDR3PHY). The UDDRC receives transactions from the internal buses. These transactions are queued internally and scheduled for access in order to the DDR-SDRAM while satisfying the DDR-SDRAM protocol timing requirements, transaction priorities, and dependencies between transactions.

One external DDR3L memory (8-Gbit Alliance Memory, Inc. AS4C512M16D3LA-10BIN) is used as system RAM, totaling 1 GByte of SDRAM on the board. The memory bus is 16 bits wide and operates with a frequency of up to 533 MHz.

Figure 3-13. Processor MPDDRC Controller



The DDR_VREF pin serves as a voltage reference input for the DDR I/Os when DDR or LPDDR external SDRAM memories are used. The DDR_VREF level is obtained from VDDIODDR using a ½ resistor voltage divider.

Figure 3-14. DDR_VREF Source

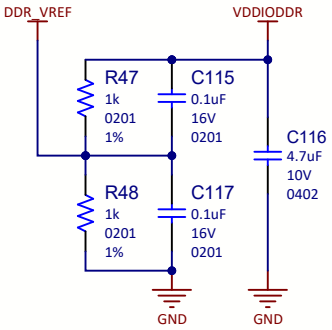
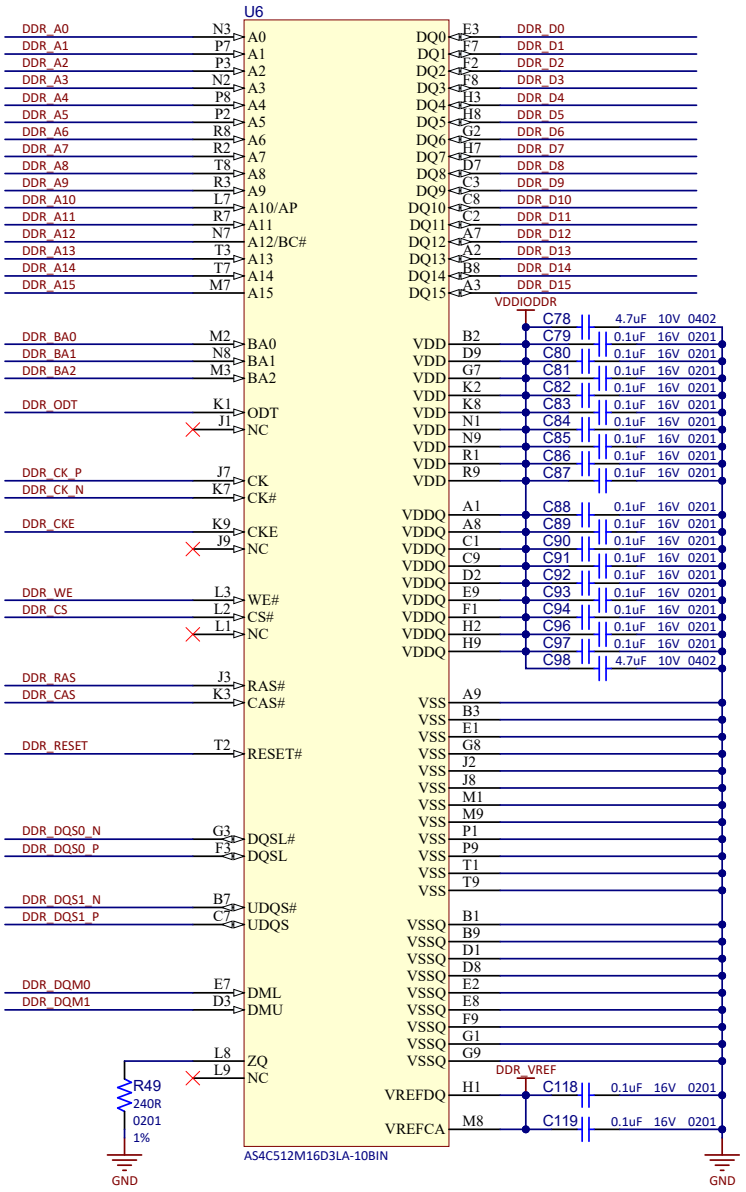


Figure 3-15. DDR3L SDRAM Device



3.2.5 Processor PIOs

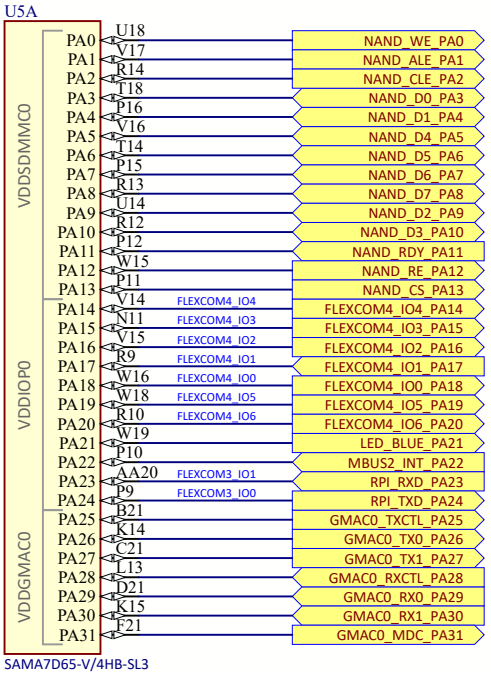
This section describes all the signals connected to the SAMA7D6 Series MPU ports. Some of the ports are multiplexed to accommodate more devices on the board and to showcase multiple functions the SAMA7D6 Series MPU can address off a single PIO. Some of the ports that share multiple functions are split through passive resistors placed on the board as close to the MPU as possible, but are configured so that only one function is available at a time, requiring manual replacement of some resistors to access the alternate function.

3.2.5.1 PIOA Bank

The PIOA bank is mainly used for the FLEXCOM4, NAND and part of GMAC0 interfaces over power rails VDDIOP0, VDDSDMMC0 and VDDGMAC0, respectively.

The following schematic shows the PIOA bank distribution.

Figure 3-16. SAMA7D6 Series PIOA Bank Distribution



The following table describes each PIOA bank function.

Table 3-3. SAMA7D6 Series MPU PIOA Bank Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PA0	VDDSDMMC0	NAND_WE	NAND Flash Write Enable signal
PA1	VDDSDMMC0	NAND_ALE	NAND Flash Address Latch Enable signal
PA2	VDDSDMMC0	NAND_CLE	NAND Flash Command Latch Enable signal
PA3	VDDSDMMC0	NAND_D0	NAND Flash data 0
PA4	VDDSDMMC0	NAND_D1	NAND Flash data 1
PA5	VDDSDMMC0	NAND_D4	NAND Flash data 4
PA6	VDDSDMMC0	NAND_D5	NAND Flash data 5
PA7	VDDSDMMC0	NAND_D6	NAND Flash data 6
PA8	VDDSDMMC0	NAND_D7	NAND Flash data 7
PA9	VDDSDMMC0	NAND_D2	NAND Flash data 2
PA10	VDDSDMMC0	NAND_D3	NAND Flash data 3
PA11	VDDSDMMC0	NAND_RDY	NAND Flash Ready signal
PA12	VDDSDMMC0	NAND_RE	NAND Flash Output Enable signal
PA13	VDDSDMMC0	NAND_CS	NAND Flash Chip Select line
PA14	VDDIOP0	FLEXCOM4_IO4	mikroBUS2 Chip Select
PA15	VDDIOP0	FLEXCOM4_IO3	mikroBUS1 Chip Select
PA16	VDDIOP0	FLEXCOM4_IO2	SPI clock (RPi, mikroBUS1, mikroBUS2)
PA17	VDDIOP0	FLEXCOM4_IO1	SPI MISO (RPi, mikroBUS1, mikroBUS2)
PA18	VDDIOP0	FLEXCOM4_IO0	SPI MOSI (RPi, mikroBUS1, mikroBUS2)
PA19	VDDIOP0	FLEXCOM4_IO5	RPi SPI Chip Select 0

.....continued

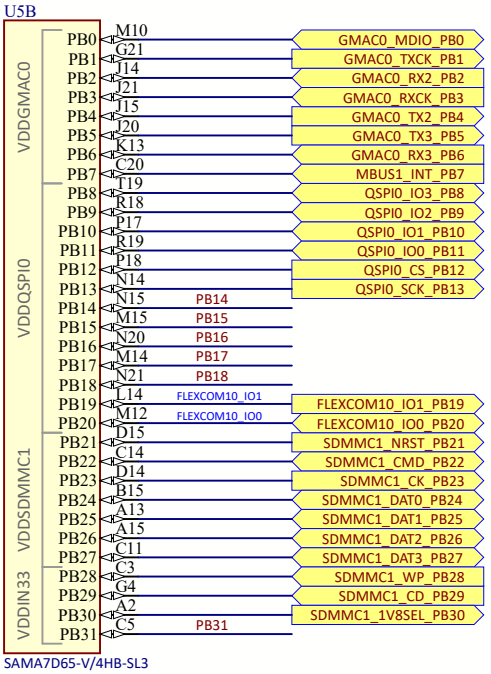
PIO	Power Rail	Function	Signal Description
PA20	VDDIOP0	FLEXCOM4_IO6	RPi SPI Chip Select 1/GMAC1 SPI Chip Select
PA21	VDDIOP0	LED_BLUE	RGB LED blue channel
PA22	VDDIOP0	MBUS2_INT	mikroBUS2 interrupt
PA23	VDDIOP0	RPi_RXD	RPi UART RX
PA24	VDDIOP0	RPi_TXD	RPi UART TX
PA25	VDDGMAC0	GMAC0_TXCTL	GMAC0 RGMII transmit enable
PA26	VDDGMAC0	GMAC0_TX0	GMAC0 RGMII transmit data 0
PA27	VDDGMAC0	GMAC0_TX1	GMAC0 RGMII transmit data 1
PA28	VDDGMAC0	GMAC0_RXCTL	GMAC0 RGMII Receive Control signal
PA29	VDDGMAC0	GMAC0_RX0	GMAC0 RGMII RX data line 0
PA30	VDDGMAC0	GMAC0_RX1	GMAC0 RGMII RX data line 1
PA31	VDDGMAC0	GMAC0_MDC	GMAC0 Management Data Clock signal

3.2.5.2 PIOB Bank

The PIOB bank is mainly used for the rest of GMAC0, QSPI0 and SD card interfaces over power rails VDDGMAC0, VDDQSPI0, VDDSDMMC1 and VDDIN33.

The following schematic shows the PIOB bank distribution.

Figure 3-17. SAMA7D6 Series PIOB Bank Distribution



The following table describes each PIOB bank function.

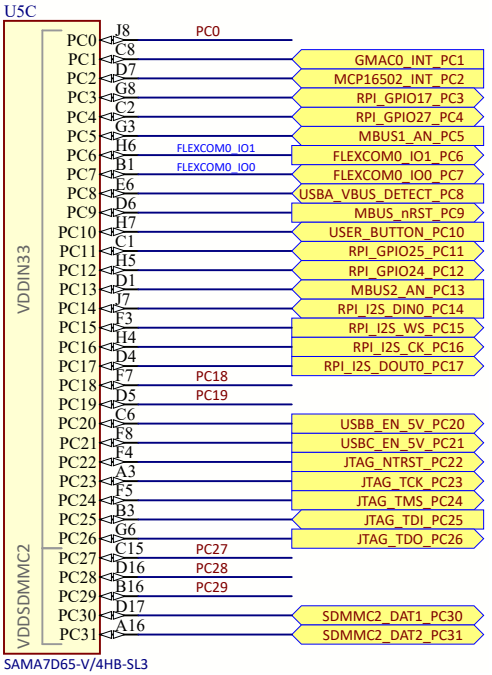
Table 3-4. SAMA7D6 Series PIOB Bank Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PB0	VDDGMAC0	GMAC0_MDIO	GMAC0 RGMII Management Data I/O signal
PB1	VDDGMAC0	GMAC0_TXCK	GMAC0 RGMII Transmit Clock signal
PB2	VDDGMAC0	GMAC0_RX2	GMAC0 RGMII TX Data Line 2
PB3	VDDGMAC0	GMAC0_RXCK	GMAC0 RGMII Receive Clock signal
PB4	VDDGMAC0	GMAC0_TX2	GMAC0 RGMII TX Data Line 2
PB5	VDDGMAC0	GMAC0_TX3	GMAC0 RGMII TX Data Line 3
PB6	VDDGMAC0	GMAC0_RX3	GMAC0 RGMII RX Data Line 3
PB7	VDDGMAC0	MBUS1_INT	mikroBUS1 interrupt line
PB8	VDDQSPI0	QSPI0_IO3	QSPI0 Data Line 3
PB9	VDDQSPI0	QSPI0_IO2	QSPI0 Data Line 2
PB10	VDDQSPI0	QSPI0_IO1	QSPI0 Data Line 1
PB11	VDDQSPI0	QSPI0_IO0	QSPI0 Data Line 0
PB12	VDDQSPI0	QSPI0_CS	QSPI0 Chip Select signal
PB13	VDDQSPI0	QSPI0_SCK	QSPI0 Clock signal
PB14	VDDQSPI0	PB14 PIO	MIPI DSI/LVDS PWM signal
PB15	VDDQSPI0	PB15 PIO	mikroBUS1 PWM/RPi PWM0/RGB LED green channel
PB16	VDDQSPI0	PB16 PIO	MIPI DSI/LVDS Interrupt signal
PB17	VDDQSPI0	PB17 PIO	mikroBUS2 PWM/RPi PWM1/RGB LED red channel
PB18	VDDQSPI0	PB18 PIO	MIPI DSI/LVDS Interrupt signal Enable signal
PB19	VDDQSPI0	FLEXCOM10_IO1	MCP16502/PAC1934/EEPROM/SODIMM TWCK
PB20	VDDQSPI0	FLEXCOM10_IO0	MCP16502/PAC1934/EEPROM/SODIMM TWD
PB21	VDDSDMMC1	SDMMC1_NRST	SDMMC1 SD Card Reset signal
PB22	VDDSDMMC1	SDMMC1_CMD	SDMMC1 SD Card Command signal
PB23	VDDSDMMC1	SDMMC1_CK	SDMMC1 SD Card Clock signal
PB24	VDDSDMMC1	SDMMC1_DAT0	SDMMC1 SD Card Data 0
PB25	VDDSDMMC1	SDMMC1_DAT1	SDMMC1 SD Card Data 1
PB26	VDDSDMMC1	SDMMC1_DAT2	SDMMC1 SD Card Data 2
PB27	VDDSDMMC1	SDMMC1_DAT3	SDMMC1 SD Card Data 3
PB28	VDDIN33	SDMMC1_WP	SDMMC1 SD Card Write-Protect
PB29	VDDIN33	SDMMC1_CD	SDMMC1 SD Card Detect signal
PB30	VDDIN33	SDMMC1_1V8SEL	SDMMC1 SD Card I/O Voltage Select
PB31	VDDIN33	PIO PB31	PAC1934 interrupt/RPi GPCLK0 signal (not connected by default, R114 DNP)/USBA CC1 (not connected by default, R116 DNP)

3.2.5.3 PIOC Bank

The PIOC bank is mainly used for RPi, and JTAG interface over power rails VDDIN33 and VDDSDMMC2. The following schematic shows the PIOC bank distribution.

Figure 3-18. SAMA7D6 Series PIOC Bank Distribution



The following table describes each PIOC bank function.

Table 3-5. SAMA7D6 Series PIOC Bank Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PC0	VDDIN33	RPI_GPCLK2	RPI GPCLK2 signal/USBA CC2 (not connected by default, R121 DNP)
PC1	VDDIN33	GMAC0_INT	SODIMM interrupt line
PC2	VDDIN33	MCP16502_INT	MCP16502 interrupt line
PC3	VDDIN33	RPI_GPIO17	RPI GPIO17 signal
PC4	VDDIN33	RPI_GPIO27	RPI GPIO27 signal
PC5	VDDIN33	MBUS1_AN	mikroBUS1 analog input
PC6	VDDIN33	FLEXCOM0_IO1	LVDS/MIPI/MBUS1/MBUS2/RPI/M.2 TWCK
PC7	VDDIN33	FLEXCOM0_IO0	LVDS/MIPI/MBUS1/MBUS2/RPI/M.2 TWD
PC8	VDDIN33	USBA_VBUS_DETECT	USBA VBUS detection
PC9	VDDIN33	MBUS_nRST	mikroBUS1 and mikroBUS2 Reset signal
PC10	VDDIN33	USER_BUTTON	Board user button
PC11	VDDIN33	RPI_GPIO25	RPI GPIO25 signal
PC12	VDDIN33	RPI_GPIO24	RPI GPIO24 signal
PC13	VDDIN33	MBUS2_AN	mikroBUS2 analog input
PC14	VDDIN33	RPI_I2S_DIN0	RPI I2S DIN0 signal
PC15	VDDIN33	RPI_I2S_WS	RPI I2S WS signal
PC16	VDDIN33	RPI_I2S_CK	RPI I2S Clock signal
PC17	VDDIN33	RPI_I2S_DOUT0	RPI I2S DOUT0 signal
PC18	VDDIN33	PC18 PIO	USBB overcurrent detection/RPI GPIO16 signal (not connected by default, R104 DNP)

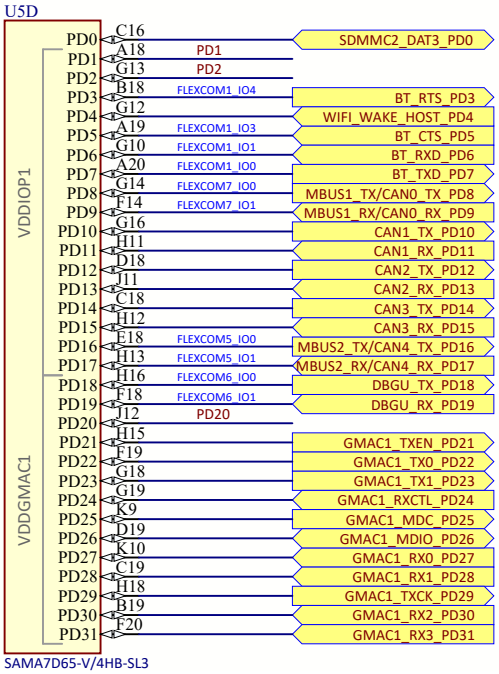
.....continued

PIO	Power Rail	Function	Signal Description
PC19	VDDIN33	PC19 PIO	USBC overcurrent detection/RPI GPIO26 signal (not connected by default, R109 DNP)
PC20	VDDIN33	USBB_EN_5V	USBB Enable signal
PC21	VDDIN33	USBC_EN_5V	USBC Enable signal
PC22	VDDIN33	JTAG_NTRST	JTAG NTRST signal
PC23	VDDIN33	JTAG_TCK	JTAG TCK signal
PC24	VDDIN33	JTAG_TMS	JTAG TMS signal
PC25	VDDIN33	JTAG_TDI	JTAG TDI signal
PC26	VDDIN33	JTAG_TDO	JTAG TDO signal
PC27	VDDSDMMC2	PC27 PIO	M.2 SDMMC CMD signal/M.2 SPI MOSI signal
PC28	VDDSDMMC2	PC28 PIO	M.2 SDMMC CMD signal/M.2 SPI MISO signal
PC29	VDDSDMMC2	PC29 PIO	M.2 SDMMC DAT0 signal/M.2 SPI clock signal
PC30	VDDSDMMC2	SDMMC2_DAT1	M.2 SDMMC2 DAT1 signal
PC31	VDDSDMMC2	SDMMC2_DAT2	M.2 SDMMC2 DAT2 signal

3.2.5.4 PIOD Bank

The PIOD bank is mainly used for CAN and GMAC1 RGMII interfaces, over power rails VDDSDMMC2, VDDIOP1 and VDDGMAC1. The following schematic shows the PIOD bank distribution.

Figure 3-19. SAMA7D6 Series PIOD Bank Distribution



The following table describes each PIOD bank function.

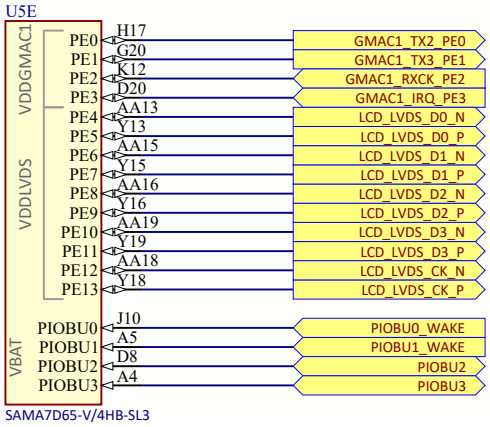
Table 3-6. SAMA7D6 Series PIOD Bank Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PD0	VDDSDMMC2	SDMMC2_DAT3	M.2 SDMMC2 DAT3 signal
PD1	VDDIOP1	PD1 PIO	M.2 interrupt line/RPI GPIO22 signal (not connected by default, R123 DNP)
PD2	VDDIOP1	PD2 PIO	M.2 TWI interrupt line/RPI GPIO23 signal (not connected by default, R125 DNP)
PD3	VDDIOP1	BT_RTS	M.2 UART RTS signal
PD4	VDDIOP1	WIFI_WAKE_HOST	M.2 WiFi interrupt line
PD5	VDDIOP1	BT_CTS	M.2 UART CTS signal
PD6	VDDIOP1	BT_RXD	M.2 UART RX signal
PD7	VDDIOP1	BT_TXD	M.2 UART TX signal
PD8	VDDIOP1	MBUS1_TX/CAN0_TX	mikroBUS1 TX signal/CAN0 TX signal
PD9	VDDIOP1	MBUS1_RX/CAN0_RX	mikroBUS1 RX signal/CAN0 RX signal
PD10	VDDIOP1	CAN1_TX	CAN1 TX signal
PD11	VDDIOP1	CAN1_RX	CAN1 RX signal
PD12	VDDIOP1	CAN2_TX	CAN2 TX signal
PD13	VDDIOP1	CAN2_RX	CAN2 RX signal
PD14	VDDIOP1	CAN3_TX	CAN3 TX signal
PD15	VDDIOP1	CAN3_RX	CAN3 RX signal
PD16	VDDIOP1	MBUS2_TX/CAN4_TX	mikroBUS2 TX signal/CAN4 TX signal
PD17	VDDIOP1	MBUS2_RX/CAN4_RX	mikroBUS2 RX signal/CAN4 RX signal
PD18	VDDGMAC1	DBGU_TX	MPU UART debug TX
PD19	VDDGMAC1	DBGU_RX	MPU UART debug RX
PD20	VDDGMAC1	PD20 PIO	M.2 reset line/RPI GPCLK1 signal (not connected by default, R127 DNP)
PD21	VDDGMAC1	GMAC1_TXEN	GMAC1 RGMII Transmit Enable signal
PD22	VDDGMAC1	GMAC1_TX0	GMAC1 RGMII TX data line 0
PD23	VDDGMAC1	GMAC1_TX1	GMAC1 RGMII TX data line 1
PD24	VDDGMAC1	GMAC1_RXCTL	GMAC1 RGMII Receive Control signal
PD25	VDDGMAC1	GMAC1_MDC	GMAC1 RGMII management data clock
PD26	VDDGMAC1	GMAC1_MDIO	GMAC1 RGMII Management Data I/O signal
PD27	VDDGMAC1	GMAC1_RX0	GMAC1 RGMII RX data line 0
PD28	VDDGMAC1	GMAC1_RX1	GMAC1 RGMII RX data line 1
PD29	VDDGMAC1	GMAC1_TXCK	GMAC1 RGMII transmit clock
PD30	VDDGMAC1	GMAC1_RX2	GMAC1 RGMII RX data line 2
PD31	VDDGMAC1	GMAC1_RX3	GMAC1 RGMII RX data line 3

3.2.5.5 PIOE Bank

The PIOE bank is mainly used for GMAC1 and LVDS interfaces, over VDDGMAC1 and VDDLVDS power rails. The following schematic shows the PIOE bank distribution.

Figure 3-20. SAMA7D6 Series PIOE Bank Distribution



The following table describes each PIOE bank function.

Table 3-7. SAMA7D6 Series PIOE Bank Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PE0	VDDGMAC1	GMAC1_TX2	GMAC1 RGMII TX data line 2
PE1	VDDGMAC1	GMAC1_TX3	GMAC1 RGMII TX data line 3
PE2	VDDGMAC1	GMAC1_RXCK	GMAC1 RGMII Receive Clock signal
PE3	VDDGMAC1	GMAC1_IRQ	GMAC1 Interrupt signal
PE4	VDDLVDS	LCD_LVDS_DO_N	LCD LVDS Data Lane 0 Negative signal
PE5	VDDLVDS	LCD_LVDS_DO_P	LCD LVDS Data Lane 0 Positive signal
PE6	VDDLVDS	LCD_LVDS_D1_N	LCD LVDS Data Lane 1 Negative signal
PE7	VDDLVDS	LCD_LVDS_D1_P	LCD LVDS Data Lane 1 Positive signal
PE8	VDDLVDS	LCD_LVDS_D2_N	LCD LVDS Data Lane 2 Negative signal
PE9	VDDLVDS	LCD_LVDS_D2_P	LCD LVDS Data Lane 2 Positive signal
PE10	VDDLVDS	LCD_LVDS_D3_N	LCD LVDS Data Lane 3 Negative signal
PE11	VDDLVDS	LCD_LVDS_D3_P	LCD LVDS Data Lane 3 Positive signal
PE12	VDDLVDS	LCD_LVDS_CK_N	LCD LVDS Clock Negative signal
PE13	VDDLVDS	LCD_LVDS_CK_P	LCD LVDS Clock Positive signal

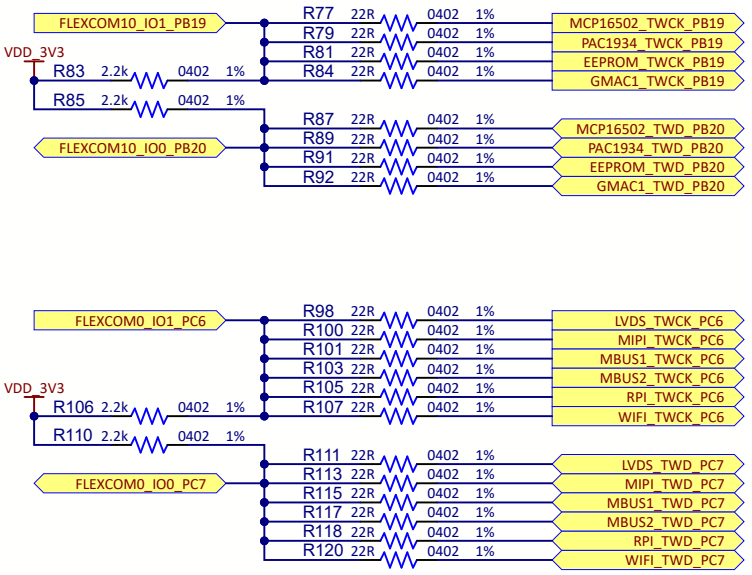
3.2.6 Processor Interface Distribution

This section details the processor PIOs distribution and explains the applicable procedure to access the multiplexed functions.

3.2.6.1 TWI Distribution

The board features two TWIs (Two Wire Interface, I²C compatible). The following schematic shows the TWI distribution, implemented with FLEXCOM0 and FLEXCOM10.

Figure 3-21. TWI Distribution Schematic



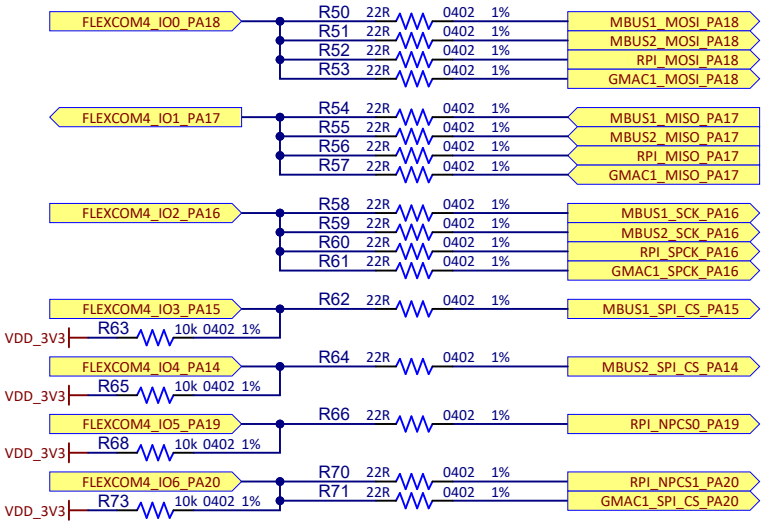
FLEXCOM10 (using pins PB19 and PB20) is attached to MCP16502, PAC1934, EEPROM and GMAC1.

FLEXCOM0 (using pins PC6 and PC7) is attached to the LVDS display connector, MIPI display connector, mikroBUS1, mikroBUS2, Raspberry Pi 40-pin connector and M.2 connector.

3.2.6.2 SPI Distribution

The board features three SPIs (Serial Peripheral Interface). The following schematic shows the SPI distribution.

Figure 3-22. SPI Distribution Schematic



The serial clock and data lines are shared by the four connected peripherals. Each peripheral has its own dedicated Chip Select line, with one exception, as shown in the table below.

Table 3-8. SPI Chip Select Peripheral Distribution

Peripheral	Interface	Chip Select Number	PIO
mikroBUS1	FLEXCOM4	NPCS0	PA15
mikroBUS2		NPCS1	PA14
40-pin RPi connector		NPCS2	PA19
40-pin RPi connector		NPCS3	PA20
SODIMM connector			

The exception is NPCS3, which is shared between the CS1 line of the RPi connector and the SPI Chip Select of the SODIMM connector, used to host EDS2 boards. Some EDS2 daughter boards have SPI communication devices on them.

WARNING If such a daughter board must be used, make sure not to have an RPi HAT with CS1 loaded on a device, otherwise a conflict will arise on the bus.

3.3 On-Board and External Memories

The SAMA7D6 Series MPU features a Universal DDR Memory Controller (UDDRC), one Quad Serial Peripheral Interface (QSPI), three Secure Digital MultiMedia Card Controllers (SDMMC), one octal SPI interface and one Static Memory Controller (SMC) to enable interfacing with a wide range of external memories. This section describes the memory devices mounted on the board:

- One 16-bit, 8-Gbit DDR3L SDRAM
- One 64-Mbit Serial quad I/O NOR Flash with preprogrammed EUI-48 MAC ID
- One 4-Gbit SLC NAND Flash memory device
- One 2-Kbit TWI EEPROM

Additional memory can be added to the board by:

- installing an SD card in the SD card slot
- using the USB ports

Support depends on the OS driver support.

3.3.1 DDR3L SDRAM

See DDR Controller and DDR3L Memory Device for details related to the on-board DDR3L memory and the connectivity with the DDR memory controller.

3.3.2 Quad SPI NOR Flash Memory

The board features one Quad Serial Peripheral Interface (QSPI) memory SST26VF064BEUI-104I/MF running up to 104 MHz.

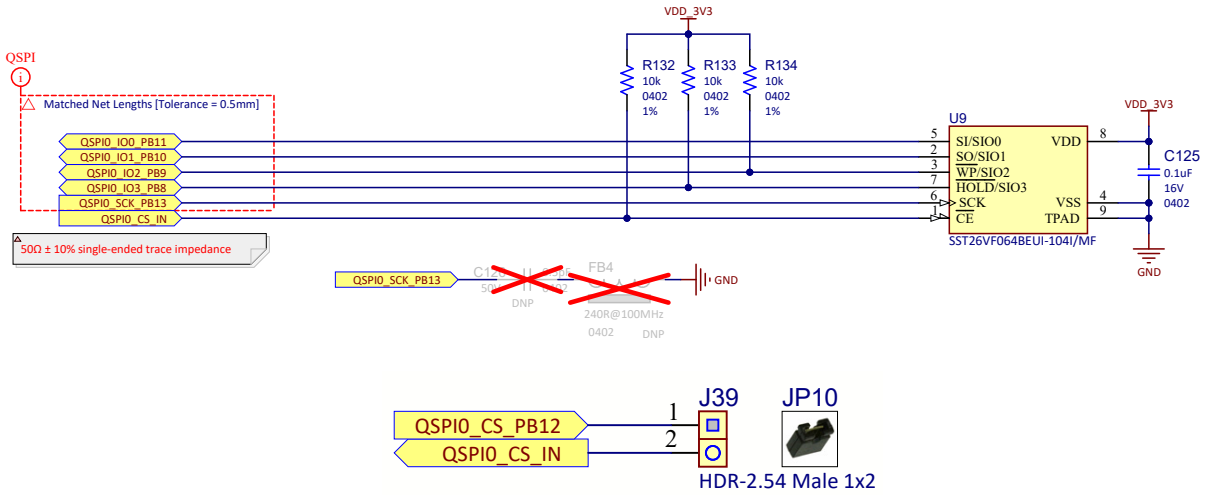
The QSPI is a synchronous serial data link that provides communication with external devices in Host mode.

Using the QSPI, the system can execute code directly from a serial Flash memory (XIP) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories such as ROM, SRAM, DRAM, embedded Flash memory, etc.

With the support of the Quad SPI protocol, the system can use high-performance serial Flash memories which are small and inexpensive compared to parallel Flash memories.

The QSPI memory device embeds one EUI-48 address which can be used to assign a MAC address to one of the GMAC interfaces.

Figure 3-23. Quad SPI Serial Flash Memory Schematic



Keep the JP10 jumper placed on the J39 header to be able to boot from (or use) the QSPI Flash memory.

Remove the JP10 jumper to prevent the system from booting from the QSPI Flash memory.

Table 3-9. QSPI Flash Memory Signal Description

PIO	Signal Name	Signal Description
PB8	QSPI0_IO3	QSPI0 data line 3
PB9	QSPI0_IO2	QSPI0 data line 2
PB10	QSPI0_IO1	QSPI0 data line 1
PB11	QSPI0_IO0	QSPI0 data line 0
PB12	QSPI0_CS	QSPI0 Chip Select signal
PB13	QSPI0_SCK	QSPI0 Clock signal

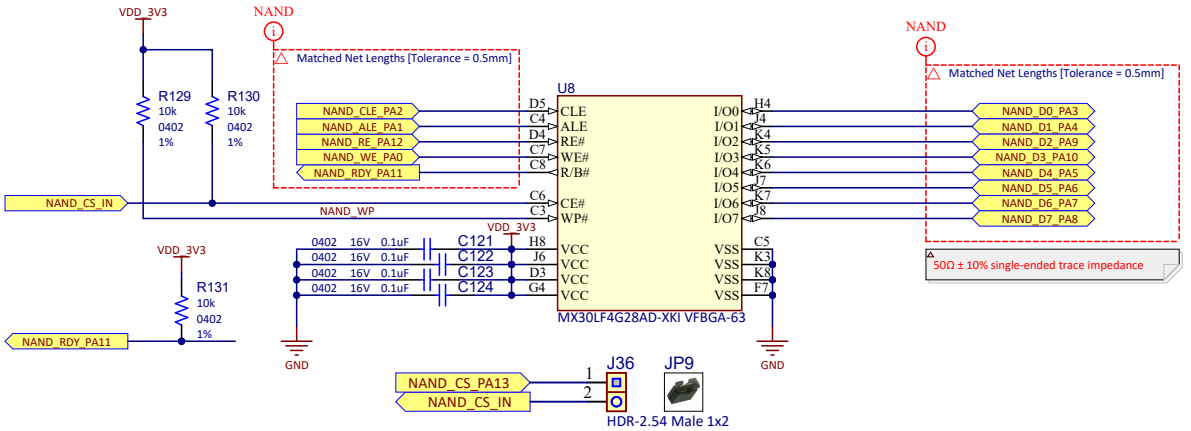
3.3.3 NAND Flash Memory

The board features one SLC 4-Gbit NAND Flash memory, MX30LF4G28AD-XKI.

The high capacity of this memory device allows for large programs and operating systems to be stored.

The SAMA7D6 Series MPU features one Programmable Multibit Error Correcting Code (PMECC) controller, which can be used to generate redundancy information for both SLC and MLC NAND devices. It supports redundancy for correction of 2, 4, 8, 12, 24 or 32 errors per sector of data.

Figure 3-24. NAND Flash Memory Schematic



Keep the JP9 jumper placed on the J36 header to be able to boot from (or use) the NAND Flash memory.

Remove the JP9 jumper to prevent the system from booting from the NAND Flash memory.

Table 3-10. NAND Flash Memory Signal Description

PIO	Signal Name	Signal Description
PA0	NAND_WE	NAND Flash Write Enable signal
PA1	NAND_ALE	NAND Flash Address Latch Enable signal
PA2	NAND_CLE	NAND Flash Command Latch Enable signal
PA3	NAND_D0	NAND Flash data 0
PA4	NAND_D1	NAND Flash data 1
PA5	NAND_D4	NAND Flash data 4
PA6	NAND_D5	NAND Flash data 5
PA7	NAND_D6	NAND Flash data 6
PA8	NAND_D7	NAND Flash data 7
PA9	NAND_D2	NAND Flash data 2
PA10	NAND_D3	NAND Flash data 3
PA11	NAND_RDY	NAND Flash Ready signal
PA12	NAND_RE	NAND Flash Output Enable signal
PA13	NAND_CS	NAND Flash Chip Select line

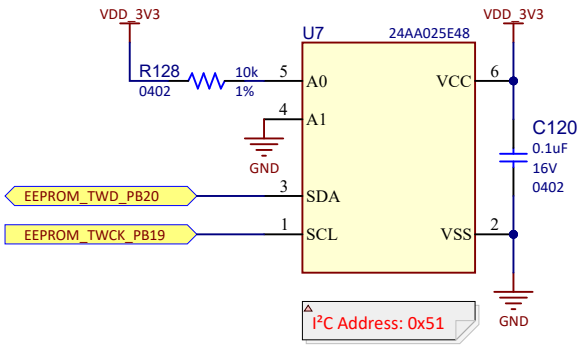
3.3.4 EEPROM

The board features one 2-Kbit EEPROM, 24AA025E48.

The EEPROM is connected to the TWI bus corresponding to FLEXCOM10 (PB20 and PB19).

The EEPROM embeds one EUI-48 address which can be used to assign a MAC address to one of the GMAC interfaces.

Figure 3-25. EEPROM Schematic



The device address is fixed at 0x51.

Table 3-11. EEPROM Signal Description

PIO	Signal Name	Signal Description
PB19	EEPROM_TWCK_PB19	EEPROM TWI Clock signal
PB20	EEPROM_TWD_PB20	EEPROM TWI Data signal

3.4 Peripheral Interfaces

Several interfaces and connectors are implemented in the board to enable the user to test all the features offered by the MPU and to facilitate a reference design for future customer applications.

This section describes the following peripherals mounted on the board:

- 10/100/1000 RGMII SODIMM Ethernet interface
- 10/100/1000 on-board RGMII Ethernet interface
- USB host/device interface
- MIPI DSI display interface
- LVDS display interface
- Secure Digital Multimedia Card (SDMMC)
- M.2 wireless interface
- 3x CAN interfaces with PHYs and connectors + 2 more available on mikroBUS headers
- 2x mikroBUS Click interfaces
- RPi 40-pin GPIO interface
- Debug interface
- User interface
- Extra pin connectors

3.4.1 10/100/1000 RGMII SODIMM Ethernet Interface

The board exposes all the necessary RGMII signals provided by the embedded Ethernet GMAC1 controller. The RGMII slot is a one-piece (J15) 260-pin SODIMM connector. This allows connectivity to multiple inexpensive add-on boards equipped with RGMII compatible PHYs and switches.

The list of Ethernet device daughter boards can be seen below and is subject to future additions.

- EV12N54A - LAN8840 Gigabit Ethernet PHY

The board supplies 5V power to the daughter board and provides additional 3.3V and 2.5V power from the dedicated auxiliary power supply.

An optional on-board 25-MHz oscillator provides the 25-MHz input clock for the PHY or switch embedded in the daughter board. If not needed, it can be manually disabled by removing the jumper placed on header J37.

Separate MDIO interfaces at the connector allow the MPU to manage the daughter board device.

An individual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in the Microchip SST26VF064BEUI-104I/SM QSPI Flash memory and in the Microchip 24AA025E48 TWI EEPROM.

This interface also features SPI connectivity which will serve to connect to Ethernet switches that require SPI communication.

Figure 3-26. 10/100/1000 RGMII SODIMM Ethernet Interface Schematic

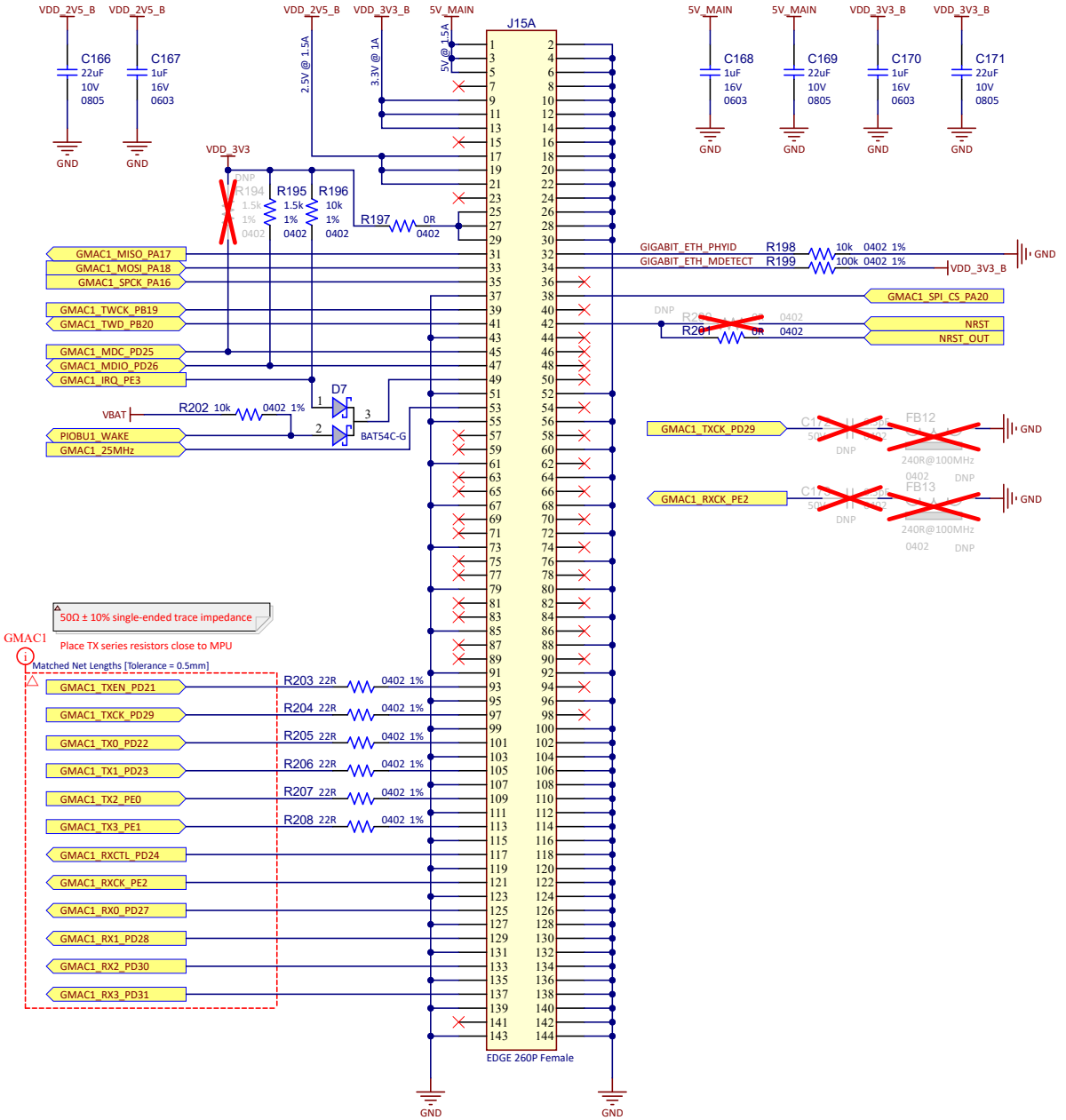


Table 3-12. 10/100/1000 RGMII SODIMM Ethernet Interface Signal Description

PIO	Signal Name	Signal Description
PD21	GMAC1_TXEN_PD21	RGMII Transmit Enable signal
PD22	GMAC1_TX0_PD22	RGMII TX data line 0
PD23	GMAC1_TX1_PD23	RGMII TX data line 1
PD24	GMAC1_RXCTL_PD24	RGMII Receive Control signal
PD27	GMAC1_RX0_PD27	RGMII RX data line 0
PD28	GMAC1_RX1_PD28	RGMII RX data line 1
PD25	GMAC1_MDC_PD25	RGMII Management Data Clock signal
PD26	GMAC1_MDIO_PD26	RGMII Management Data I/O signal
PD29	GMAC1_TXCK_PD29	RGMII Transmit Clock signal
PE0	GMAC1_TX2_PE0	RGMII TX data line 2
PE1	GMAC1_TX3_PE1	RGMII TX data line 3
PD30	GMAC1_RX2_PD30	RGMII RX data line 2
PD31	GMAC1_RX3_PD31	RGMII RX data line 3
PE2	GMAC1_RXCK_PE2	RGMII Receive Clock signal
PE3	GMAC1_IRQ_PE3	Ethernet Device Interrupt signal
PB20	GMAC1_TWD_PB20	Daughter Board TWI Data signal
PB19	GMAC1_TWCK_PB19	Daughter Board TWI Clock signal
PA16	GMAC1_SPCK_PA16	Daughter Board SPI Clock signal
PA17	GMAC1_MISO_PA17	Daughter Board SPI MISO signal
PA18	GMAC1_MOSI_PA18	Daughter Board SPI MOSI signal
PA20	GMAC1_SPI_CS_PA20	Daughter Board SPI Chip Select

3.4.2 10/100/1000 On-Board RGMII Ethernet Interface

The board features a complete on-board RGMII Ethernet interface, implemented with the LAN8840 PHY.

The LAN8840 is a low-power, single-port, triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver (PHY) that is optimized for precision process timing. The device enables highly accurate synchronization of motors, valves, actuators and sensors over standard CAT-5, CAT-5e and CAT-6 unshielded twisted pair (UTP) cables. For more information on the LAN8840, refer to www.microchip.com/en-us/product/LAN8840.

The LAN8840 1.1V core power is supplied by an external MIC33153 DC-DC converter. For more information on the MIC33153, refer to www.microchip.com/en-us/product/MIC33153.

The LAN8840 supports industry-standard RGMII (Reduced Gigabit Media Independent Interface) providing chip-to-chip connection to a host device with an integrated Gigabit Ethernet MAC.

An individual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in the Microchip SST26VF064BEUI-104I/SM QSPI Flash memory and in the Microchip 24AA025E48 TWI EEPROM. For more information on SST26VF064BEUI, refer to www.microchip.com/en-us/product/SST26VF064BEUI.

Additionally, for monitoring and control purposes, the RJ45 connectors feature LED functionality to indicate activity, link, and speed status.

Figure 3-27. 10/100/1000 On-Board RGMII Ethernet Interface Schematic

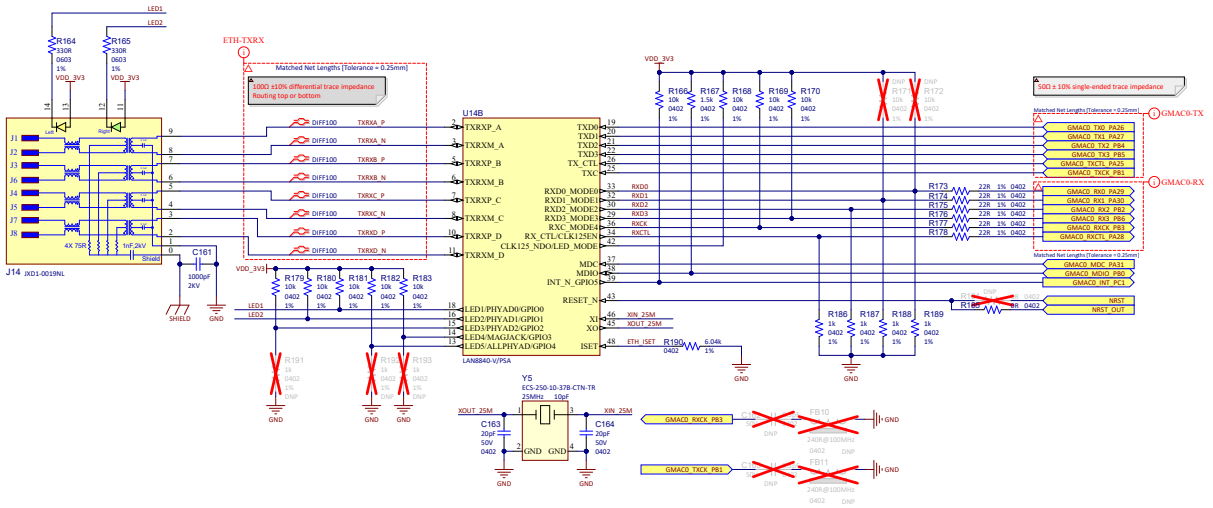


Figure 3-28. MIC33153 Ethernet Power Supply Schematic

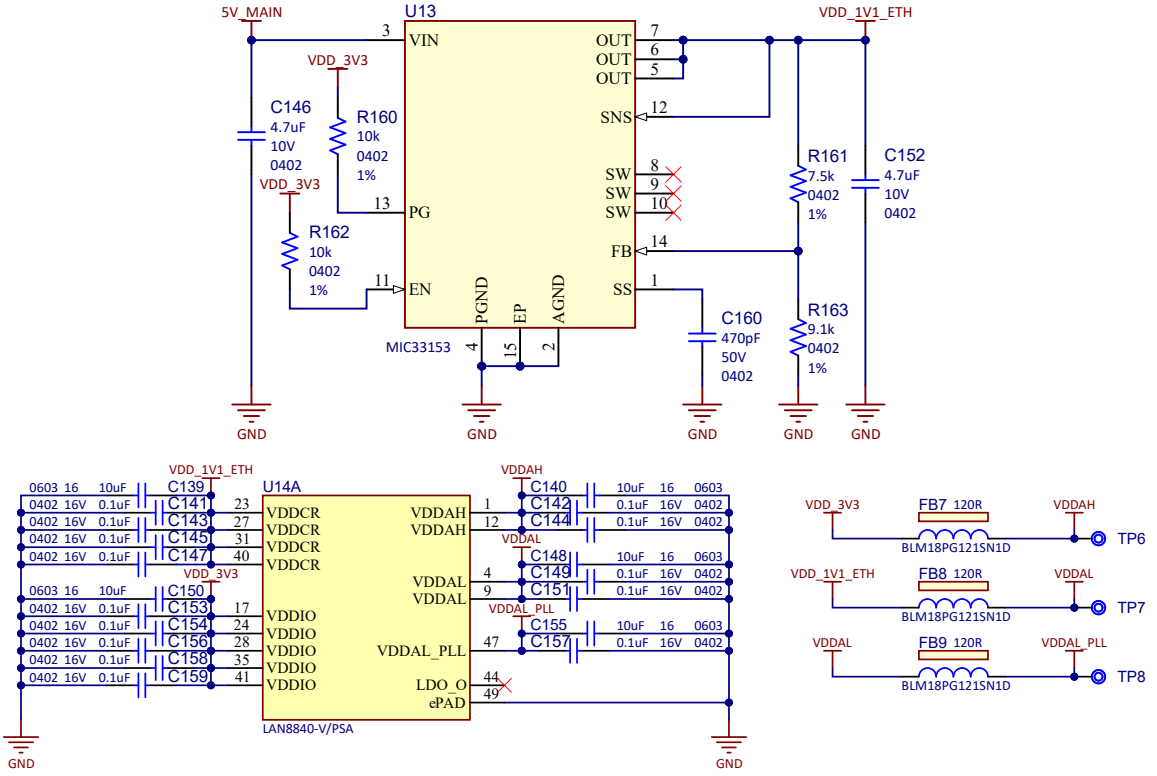


Table 3-13. 10/100/1000 On-Board RGMII Ethernet Interface Signal Description

PIO	Signal Name	Signal Description
PA25	GMAC0_TXCTL_PA25	RGMII Transmit Enable signal
PA26	GMAC0_TX0_PA26	RGMII TX data line 0
PA27	GMAC0_TX1_PA27	RGMII TX data line 1
PA28	GMAC0_RXCTL_PA28	RGMII Receive Control signal
PA29	GMAC0_RX0_PA29	RGMII RX data line 0

.....continued		
PIO	**Signal Name**	**Signal Description**
PA30	GMAC0_RX1_PA30	RGMII RX data line 1
PA31	GMAC0_MDC_PA31	RGMII Management Data Clock signal
PB0	GMAC0_MDIO_PB0	RGMII Management Data I/O signal
PB1	GMAC0_TXCK_PB1	RGMII Transmit Clock signal
PB4	GMAC0_TX2_PB4	RGMII TX data line 2
PB5	GMAC0_TX3_PB5	RGMII TX data line 3
PB2	GMAC0_RX2_PB2	RGMII RX data line 2
PB6	GMAC0_RX3_PB6	RGMII RX data line 3
PB3	GMAC0_RXCK_PB3	RGMII Receive Clock signal
PC1	GMAC0_INT_PC1	Ethernet Device Interrupt signal

3.4.3 USB Host/Device Interface

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High-Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The board features three USB communication ports named USB-A, USB-B and USB-C.

On this board, the USB-A port can act only as a USB device interface and can be accessed via the USB Type-C connector (J3).

Two resistors are placed on its power rail to form a voltage divider, converting 5V into 3.3V that is then used to signal the presence of a USB host to the MPU.

The USB-A port is used as a power source, as mentioned in USB Supply Input. In most cases, this port is limited to 500 mA.

Figure 3-29. USB-A Port

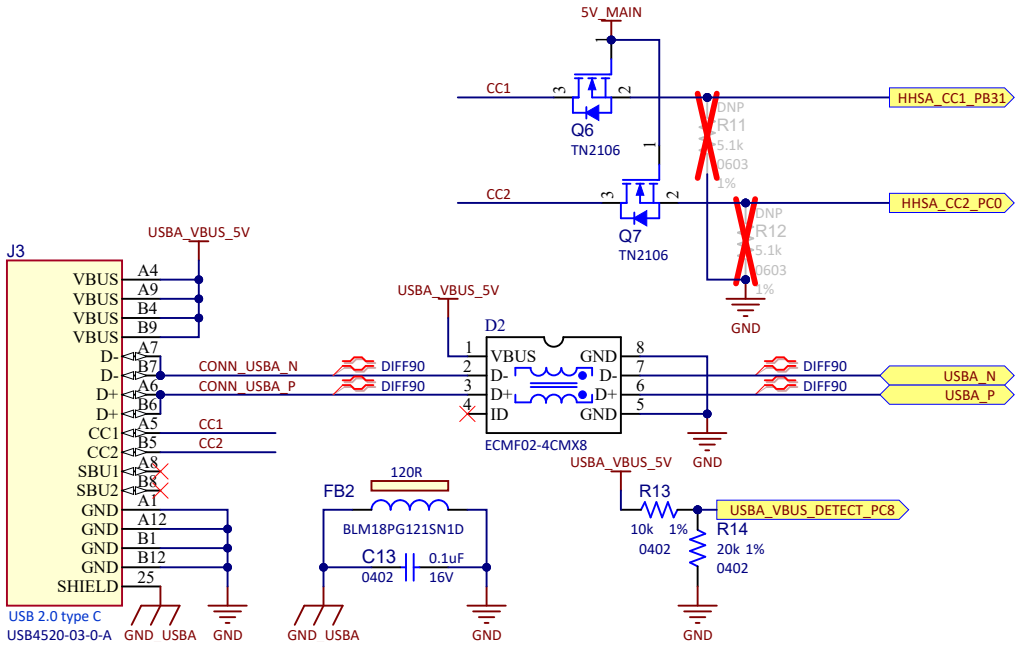


Table 3-14. USB-A Connector Signal Description

Pin No.	Signal Name	Signal Description
A4, A9, B4, B9	USBA_VBUS_5V	USB 5V power input
A7, B7	USBA_CONN_N	USB port data minus
A6, B6	USBA_CONN_P	USB port data plus
A1, A12, B1, B12	GND	Ground
A5, B5	CC1, CC2	Configuration channel

Table 3-15. USB-A PIO Signal Description

PIO	Signal Name	Signal Description
PC8	USBA_VBUS_DETECT_PC8	VBUS detection

The USB-B port is exposed on a USB Type-A connector and acts as host.

Figure 3-30. USB-B Port Schematic

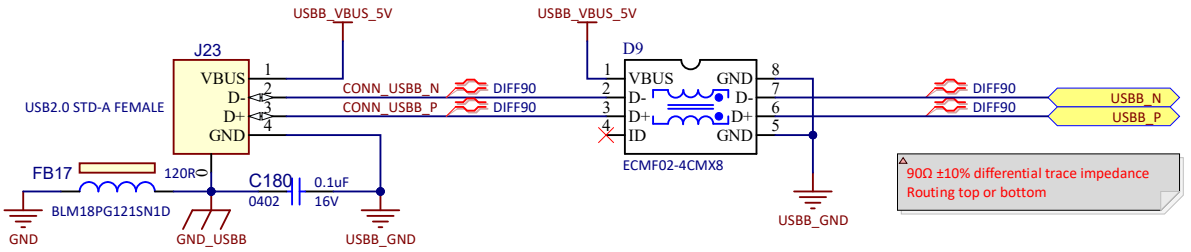


Table 3-16. USB-B Connector Signal Description

Pin No.	Signal Name	Signal Description
1	USBB_VBUS_5V	USB 5V power output
2	USBB_CONN_N	USB port data minus
3	USBB_CONN_P	USB port data plus
4	USBB_GND	Ground

The USB-C port is exposed on another USB Type-A connector and acts as host.

Figure 3-31. USB-C Port Schematic

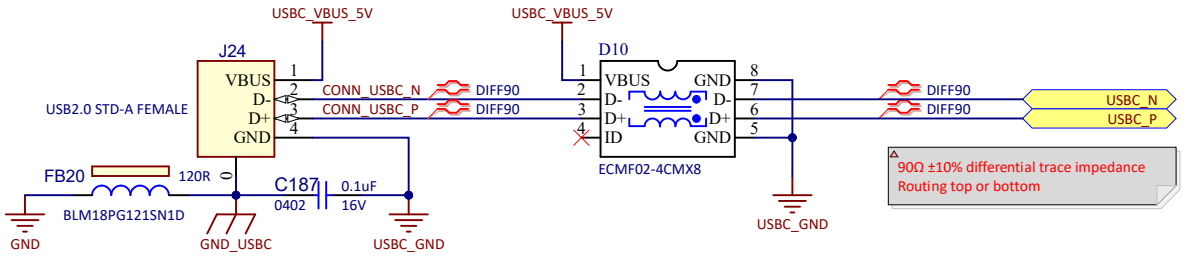


Table 3-17. USB-C Connector Signal Description

Pin No.	Signal Name	Signal Description
1	USBC_VBUS_5V	USB 5V power output
2	USBC_CONN_N	USB port data minus
3	USBC_CONN_P	USB port data plus
4	USBC_GND	Ground

In Host mode, the USB host ports B and C are both equipped with a 500-mA high-side power switch output from one MIC2026 device to enable self-powered and bus-powered applications. USBB_EN_5V_PC20 and USBC_EN_5V_PC21 signals control the current limiting power switch MIC2026, which in turn supplies power to a client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2026 limits the current and indicates an overcurrent with the USBB_OVCUR_PC18 and USBC_OVCUR_PC19 signals. For more information about the MIC2026, refer to the product web page.

Figure 3-32. USB-B and USB-C Hosts Power Schematic

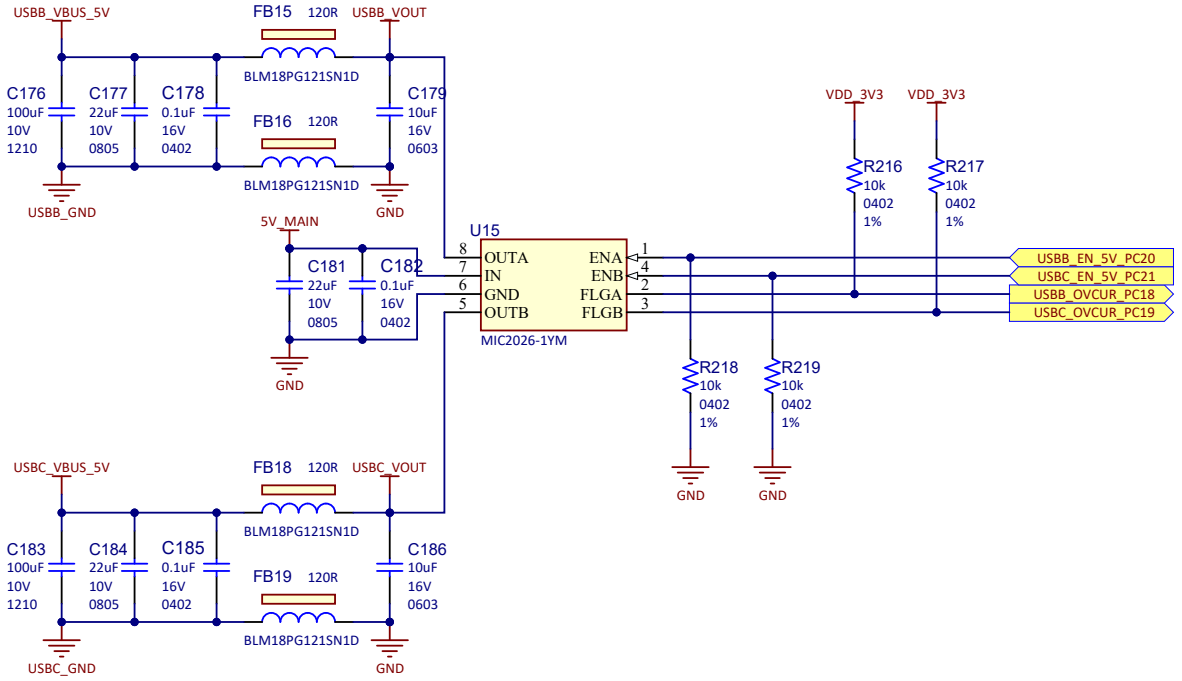


Table 3-18. USB-B PIO Signal Description

PIO	Signal Name	Signal Description
PC20	USBB_EN_5V_PC20	USB-B host power enable signal
PC18	USBB_OVCUR_PC18	USB-B power overcurrent interrupt line
PC21	USBC_EN_5V_PC21	USB-C host power enable signal
PC19	USBC_OVCUR_PC19	USB-C power overcurrent interrupt line

3.4.4 MIPI DSI Display Interface

The MIPI Display Serial Interface (DSI) Host Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The DSI host provides an interface between the LCD Controller (LCDC) and the MIPI D-PHY, allowing communication with a DSI-compliant display.

The DSI sends data to a DSI-compliant display. A D-PHY configured as a host (TX) acts as the physical layer.

On the board, an external MIPI display can be connected to the J16 34-pin FPC connector.

Figure 3-33. MIPI DSI Display Connector Schematic

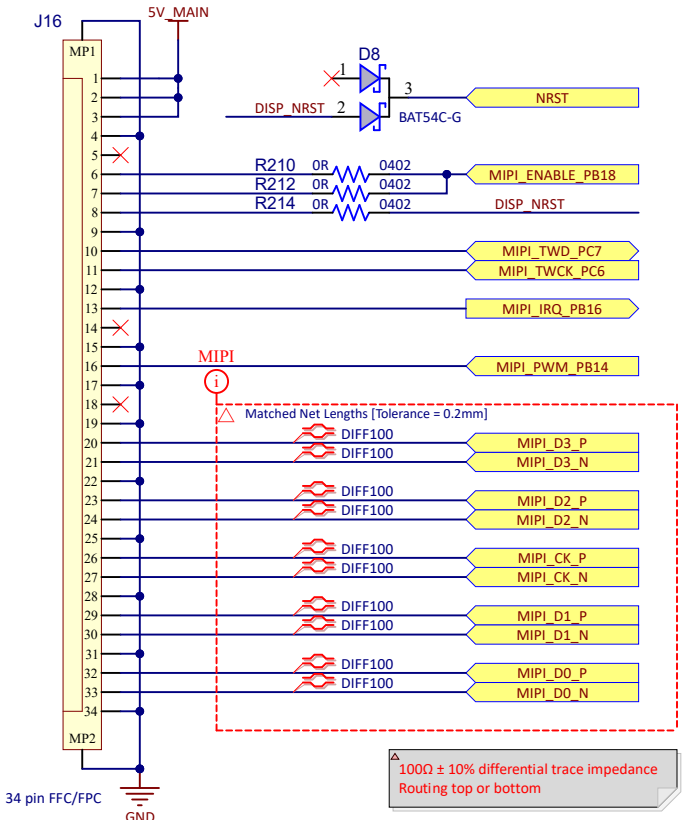


Table 3-19. MIPI DSI Display Connector Signal Description

PIO	Signal Name	Signal Description
PB18	MIPI_ENABLE_PB18	Display enable signal
PB16	MIPI_IRQ_PB16	Display touchscreen interrupt line
PB14	MIPI_PWM_PB14	Display PWM signal
PC6	MIPI_TWCK_PC6	Display TWI clock signal
PC7	MIPI_TWD_PC7	Display TWI data signal

3.4.5 LVDS Display Interface

The Low Voltage Differential Signaling Controller (LVDSC) manages data format conversion from the LCD Controller internal DPI bus to OpenLDI LVDS output signals.

LVDSC functions include bit mapping, balanced mode management and serializer.

On the board, an external LVDS display can be connected to the J17 30-pin FPC connector.

Figure 3-34. LVDS Display Connector Schematic

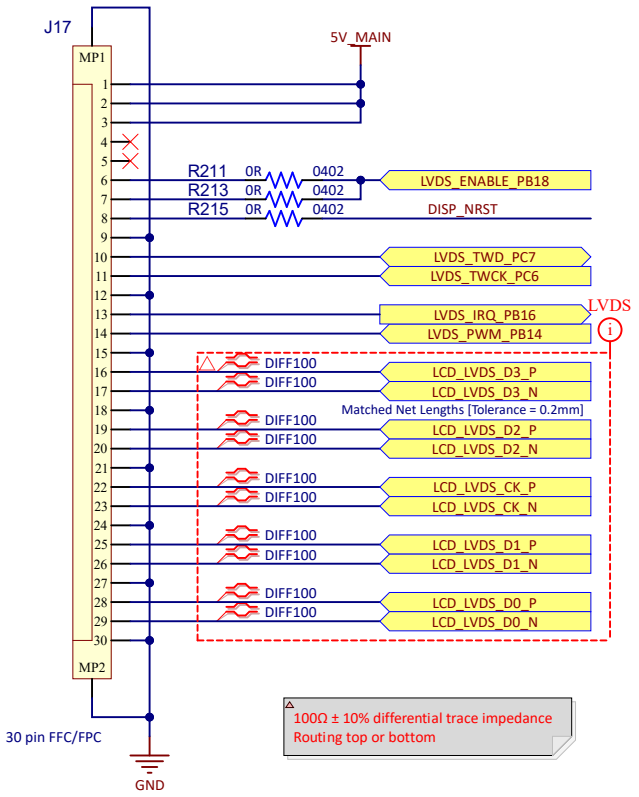


Table 3-20. LVDS Display Connector Signal Description

PIO	Signal Name	Signal Description
PB18	LVDS_ENABLE_PB18	Display enable signal
PB16	LVDS_IRQ_PB16	Display touchscreen interrupt line
PB14	LVDS_PWM_PB14	Display PWM signal
PC6	LVDS_TWCK_PC6	Display TWI clock signal
PC7	LVDS_TWD_PC7	Display TWI data signal

3.4.6 Secure Digital Multimedia Cards (SDMMC)

The SD (Secure Digital) cards are a non-volatile memory card format used as a mass storage memory in mobile devices.

The board has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) Specification V5.1, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 Specification.

3.4.6.1 SDMMC1 Connector

A 4-bit full-size SD card connector, J10, connected to the SDMMC1 interface, is mounted on the bottom side of the board. The SDMMC1 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection and write protect switch.

This connector gives access to the boot environment.

The user can perform a hard reset of the SD card by toggling the PB21 PIO of the MPU, which corresponds to the reset line of the SDMMC1 interface. The same hard reset will be performed automatically at each system reset, when NRST is asserted low.

The hard reset is performed by power cycling the SD card power using the MIC94085YFT high-side load switch. For more details about the MIC94085YFT device, refer to the product web page.

Figure 3-35. SDMMC1 Connector Schematic

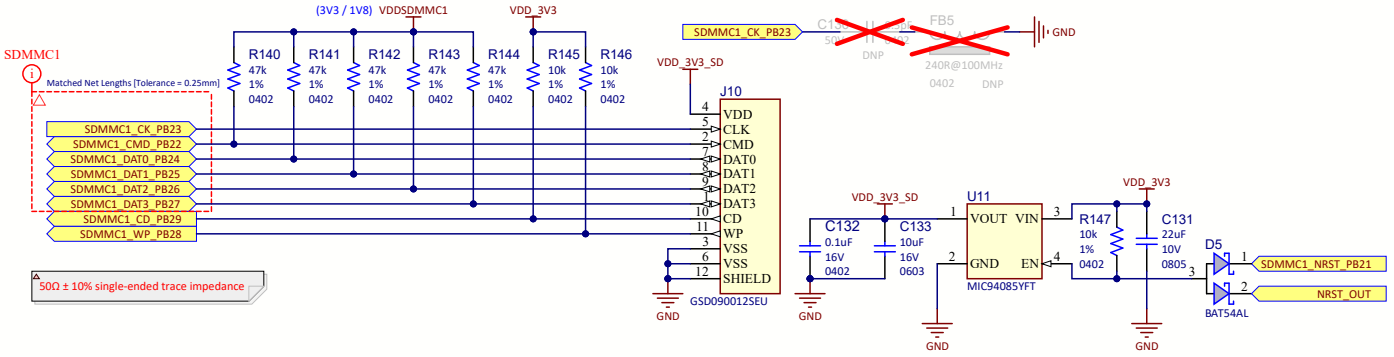


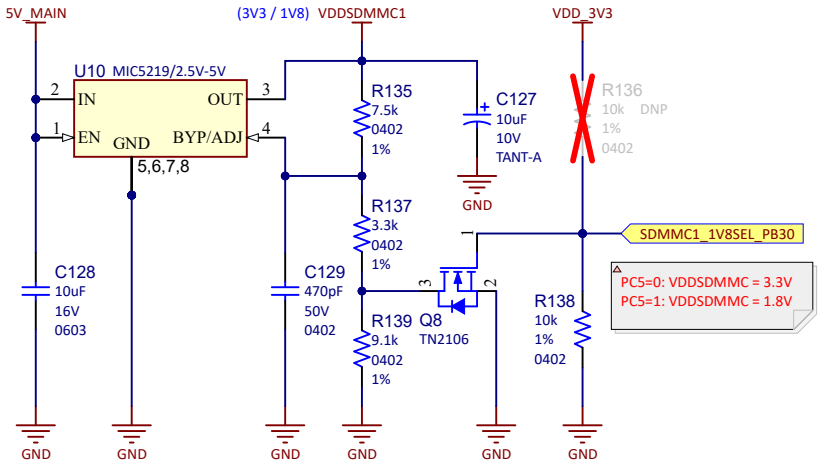
Table 3-21. SDMMC1 Connector Signal Description

PIO	Signal Name	Signal Description
PB24	SDMMC1_DAT0_PB24	SDMMC1 data line 0
PB25	SDMMC1_DAT1_PB25	SDMMC1 data line 1
PB26	SDMMC1_DAT2_PB26	SDMMC1 data line 2
PB27	SDMMC1_DAT3_PB27	SDMMC1 data line 3
PB23	SDMMC1_CK_PB23	SDMMC1 Clock signal
PB22	SDMMC1_CMD_PB22	SDMMC1 command line
PB29	SDMMC1_CD_PB29	SDMMC1 Card Detect signal
PB28	SDMMC1_WP_PB28	SDMMC1 write-protect line
PB21	SDMMC1_NRST_PB21	Device reset line

The SDMMC1 interface supports switching the I/O voltage level from 3.3 V to 1.8 V to enable ultra-high speed modes (such as DDR50 and SDR104) for the SD card. The SAMA7D6 Series MPU will perform the switch by asserting the PB30 PIO on high when a card supporting high-speed modes is detected (depending on software support). The schematic below describes the circuit which generates the required 3.3/1.8V voltages using the adjustable LDO MIC5219.

For more details about the MIC5219 device, refer to the product web page.

Figure 3-36. SDMMC1 I/O Voltage Switch Schematic



3.4.6.2 M.2 Wireless Interface

The board features one M.2 interface for connecting compatible wireless add-on cards.

Only wireless cards compatible with the PCIe M.2 Key E slot (J11) are supported.

The main interface integrated in the M.2 slot is SDMMC2, for the WiFi component of the add-on card. An optional SPI interface is also multiplexed with the SDMMC2 pins and is available by changing the JP5 jumper position on the J12 header.

The M.2 slot also features a UART interface with hardware flow control for the Bluetooth component of the add-on card.

An external 32.768-kHz oscillator provides the 32.768-kHz clock.

Other miscellaneous signals are present for reset, host interrupts and wake-up, device wake-up, TWI and PTA.

Power is ensured by the auxiliary 3.3V supply (U1).

The MODE select header J13, near the J11 slot, is reserved for future use.

Figure 3-37. M.2 Wireless Interface Connector Schematic

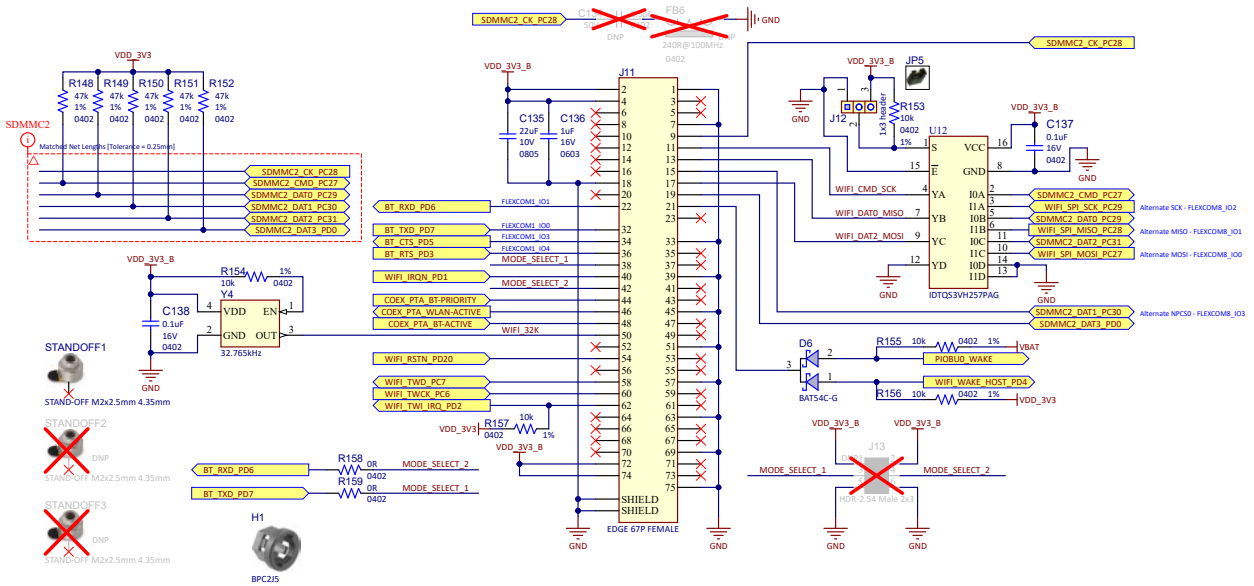


Table 3-22. M.2 Wireless Interface Connector Signal Description

PIO	Signal Name	Signal Description
PC28	SDMMC2_CK_PC28	SDMMC2 Clock signal
PC27	SDMMC2_CMD_PC27	SDMMC2 command line
PD20	WIFI_RSTN_PD20	M.2 device reset line
PC29	SDMMC2_DAT0_PC29	SDMMC2 data line 0
PC30	SDMMC2_DAT1_PC30	SDMMC2 data line 1
PC31	SDMMC2_DAT2_PC31	SDMMC2 data line 2
PD0	SDMMC2_DAT3_PD0	SDMMC2 data line 3
PC7	WIFI_TWD_PC7	M.2 device TWI Data signal
PC6	WIFI_TWCK_PC6	M.2 device TWI Clock signal
PD4	WIFI_WAKE_HOST_PD4	M.2 host Wake-up signal
PD1	WIFI_IRQN_PD1	M.2 device interrupt line
PD2	WIFI_TWI_IRQ_PD2	M.2 TWI host interrupt line
PD7	BT_TXD_PD7	Bluetooth UART Transmit Data signal
PD6	BT_RXD_PD6	Bluetooth UART Receive Data signal
PD5	BT_CTS_PD5	Bluetooth UART Clear to Send signal
PD3	BT_RTS_PD3	Bluetooth UART Ready to Send signal
PC27	WIFI_SPI_MOSI_PC27	M.2 device serial data input
PC28	WIFI_SPI_MISO_PC28	M.2 device serial data output
PC29	WIFI_SPI_SCK_PC29	M.2 device serial Clock signal
PIOBU0	PIOBU0_WAKE	M.2 host back-up Wake-up signal

3.4.7 3x CAN Interfaces

The Controller Area Network (MCAN) performs communication according to ISO 11898-1:2015 and to the Bosch CAN FD specification. Additional transceiver hardware is required for connection to the physical layer.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN core to the Message RAM, as well as providing receive message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN core, as well as providing transmit status information.

Acceptance filtering is implemented by a combination of up to 128 filter elements, where each element can be configured as a range, as a bit mask, or as a dedicated ID filter.

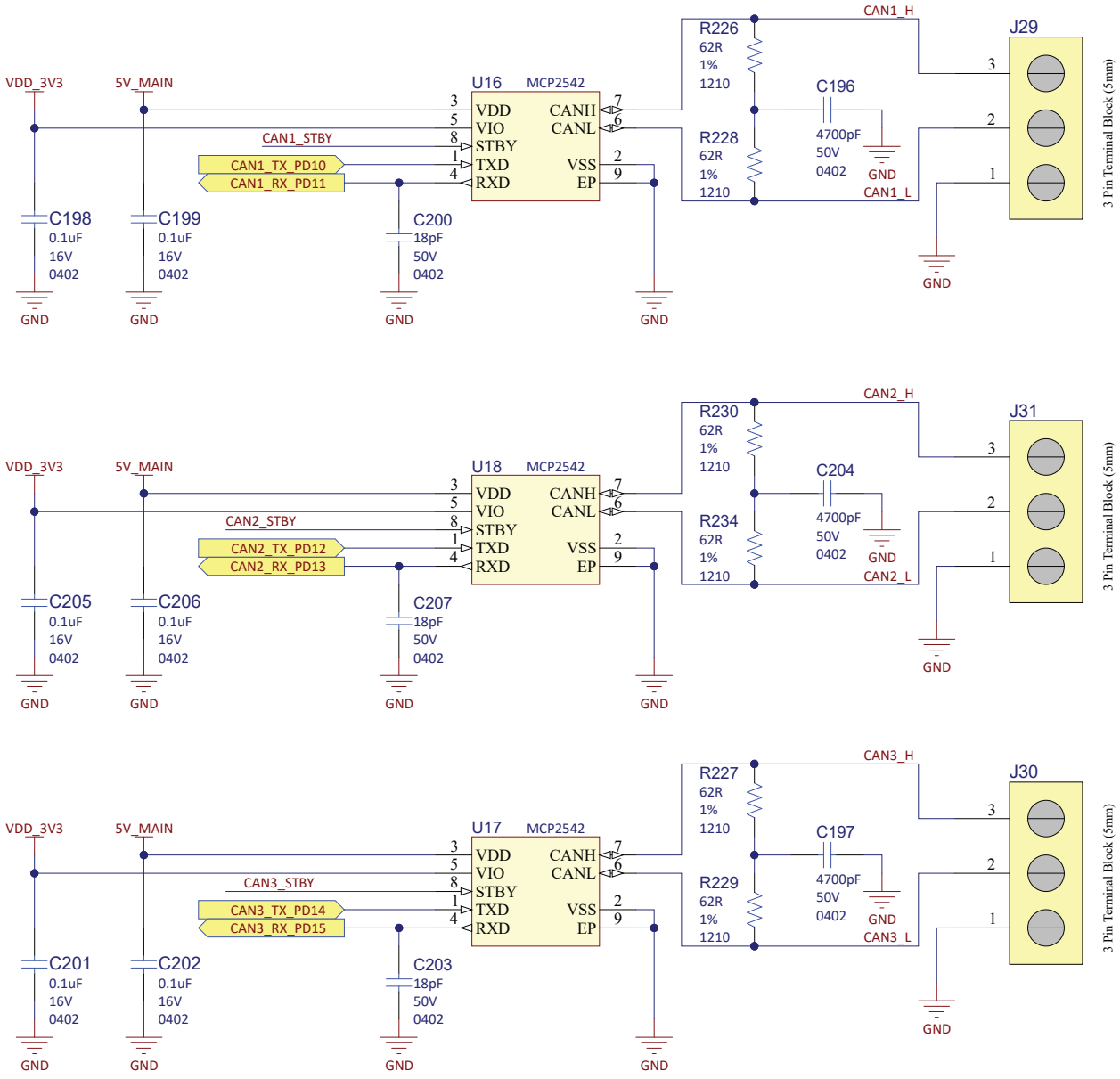
The board features three dedicated MCAN interfaces, each equipped with a MCP2542FD CAN transceiver. The MCP2542FD CAN transceiver is designed for high-speed CAN FD applications up to an 8-Mbps communication speed. The maximum propagation delay was improved to support longer bus length. The device meets the automotive requirements for CAN FD bit rates exceeding 2 Mbps, low quiescent current, electromagnetic compatibility (EMC) and electrostatic discharge (ESD).

For more details about the MCP2542FD device, refer to the product web page.

By default, all MCP2542FD CAN transceivers are enabled and can be manually put in Stand-By mode by placing the appropriate jumper on header J32.

Each CAN port features a 3-pin terminal block. Wires can be plugged in the terminal blocks without the use of a screwdriver.

Figure 3-38. CAN Interface Schematics



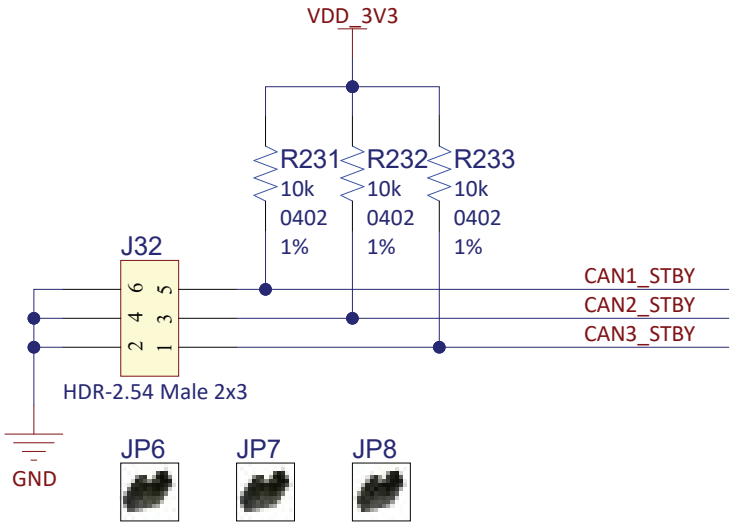


Table 3-23. CAN Connector Pin Assignment

PIO	Signal Name	Signal Description
PD10	CAN1_TX_PD10	CAN1 Transmit signal
PD11	CAN1_RX_PD11	CAN1 Receive signal
PD12	CAN2_TX_PD12	CAN2 Transmit signal
PD13	CAN2_RX_PD13	CAN2 Receive signal
PD14	CAN3_TX_PD14	CAN3 Transmit signal
PD15	CAN3_RX_PD15	CAN3 Receive signal

3.4.8 Dual mikroBUS Click Interfaces

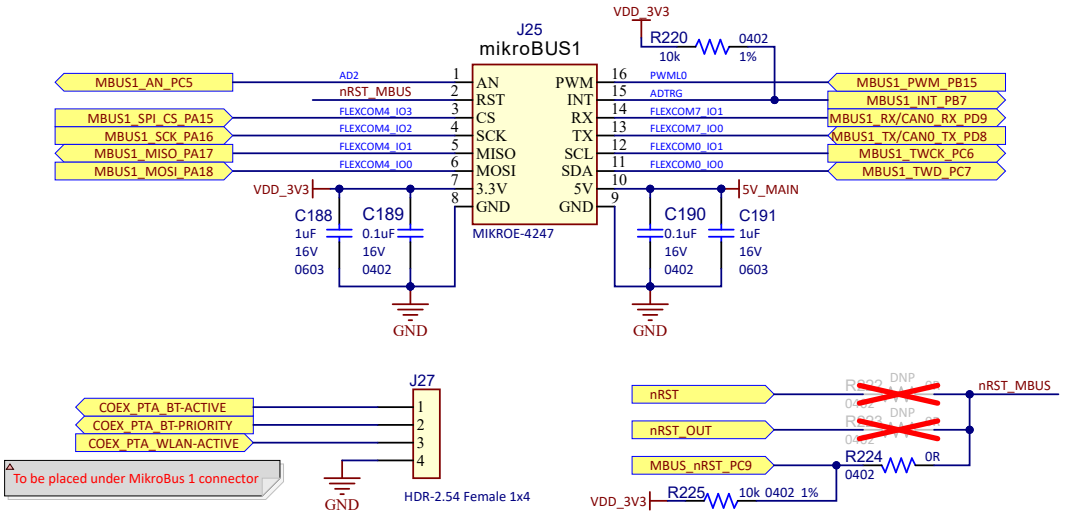
The board hosts two (J25 and J26) official mikroBUS sockets, implementing the mikroBUS standard. For details, refer to the mikroBUS documentation on www.mikroe.com/mikrobus.

In addition to the standard mikroBUS format, each socket features one 4-pin female header to implement the PTA feature for selected mikroBUS radio click boards.

3.4.8.1 mikroBUS 1 Connector

The first mikroBUS socket (J25) implements all mikroBUS features, as shown in the schematic below. The reset feature is ensured (by default) by the PIO port PC9 and can be swapped to the system reset line or peripheral reset line by moving resistor R224 to R222 or R223, respectively.

Figure 3-39. mikroBUS 1 Interface Schematic



The first mikroBUS interface features an SPI bus shared with the second mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PA15 for the mikroBUS1 interface).

The first mikroBUS interface features a two-wire interface (PC6 and PC7) shared with the second mikroBUS interface and with the 40-pin RPi connector. The end user must pay attention to the I²C addresses used on these nodes.

The PWM feature of the first mikroBUS interface (PB15) is shared with the green junction of the D11 RGB LED.

To evaluate the CAN-FD interface, use selected mikroBUS click boards having the CAN-FD transceivers implemented in place of the standard UART RX/TX signals.

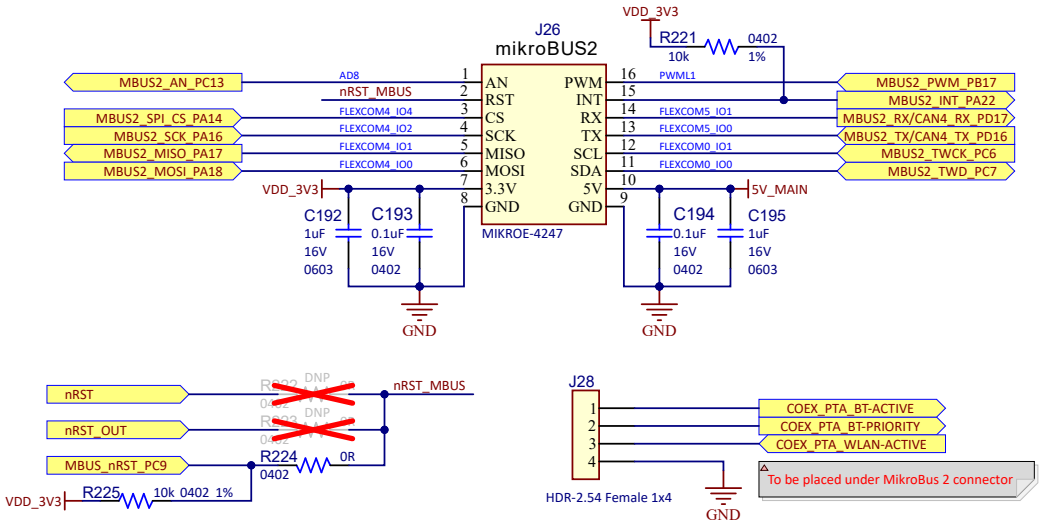
Table 3-24. mikroBUS 1 Connector Pin Assignment

Function	PIO	mBUS Signal	Pin No.	Pin No.	mBUS Signal	PIO	Function
Analog input	PC5	AN	1	16	PWM	PB15	PWM
Reset	PC9	nRST_MBUS	2	15	INT	PB7	Interrupt
SPI Chip Select	PA15	SPI_CS	3	14	RX-CAN0	PD9	UART receive (mBUS output to SAM)
SPI Clock	PA16	SCK	4	13	TX-CAN0	PD8	UART transmit (mBUS input from SAM)
SPI MISO	PA17	MISO	5	12	TWCK	PC6	TWI clock
SPI MOSI	PA18	MOSI	6	11	TWD	PC7	TWI data
VCC	-	3.3V supply	7	10	5V supply	-	VDD
Ground	-	GND	8	9	GND	-	Ground

3.4.8.2 mikroBUS 2 Connector

The second mikroBUS socket (J26) implements all mikroBUS features, as shown in the schematic below. The reset feature is ensured (by default) by the PIO port PC9 and can be swapped to the system reset line or peripheral reset line by moving resistor R224 to R222 or R223, respectively.

Figure 3-40. mikroBUS 2 Interface



The second mikroBUS interface features an SPI bus shared with the first mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PA14 for the mikroBUS2 interface). I/Os in common are PA16, PA17 and PA18. That means that the SPI interface cannot be used at the same time on the two mikroBUS interfaces.

The second mikroBUS interface features a two-wire interface (PC6 and PC7) shared with the second mikroBUS interface and with the 40-pin RPi connector. The end user must pay attention to the I²C addresses used on these nodes.

The PWM feature of the second mikroBUS interface (PB17) is shared with the red junction of the D11 RGB LED.

To evaluate the CAN-FD interface, use selected mikroBUS click boards having the CAN-FD transceivers implemented in place of the standard UART RX/TX signals.

Table 3-25. mikroBUS 2 Connector Pin Assignment

Function	PIO	mBUS Signal	Pin No.	Pin No.	mBUS Signal	PIO	Function
Analog input	PC13	AN	1	16	PWM	PB17	PWM
Reset	PC9	nRST_MBUS	2	15	INT	PA22	Interrupt
SPI Chip Select	PA14	SPI_CS	3	14	RX-CAN4	PD17	UART receive (mBUS output to SAM)
SPI Clock	PA16	SCK	4	13	TX-CAN4	PD16	UART transmit (mBUS input from SAM)
SPI MISO	PA17	MISO	5	12	TWCK	PC6	TWI clock
SPI MOSI	PA18	MOSI	6	11	TWD	PC7	TWI data
VCC	-	3.3V supply	7	10	5V supply	-	VDD
Ground	-	GND	8	9	GND	-	Ground

3.4.9 RPi 40-Pin GPIO Interface

The board features a 40-pin connector (RPi compatible) for free use.

Figure 3-41. 40-Pin GPIO Connector Schematic

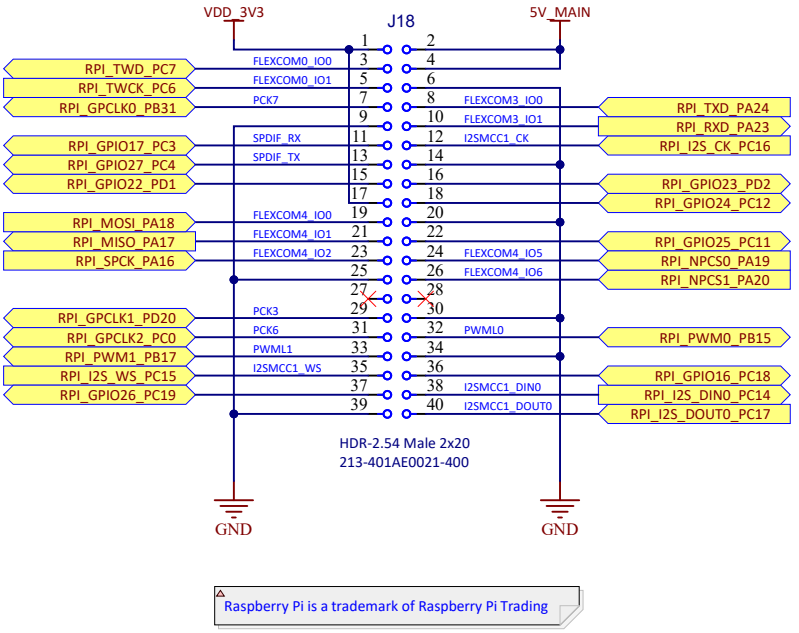


Table 3-26. 40-Pin GPIO Pin Assignment

Signal	Pin No.	Pin No.	Signal
VDD_3V3	1	2	5V_MAIN
RPI_TWD_PC7	3	4	5V_MAIN
RPI_TWCK_PC6	5	6	GND
RPI_GPCLK0_PB31	7	8	RPI _TXD_PA24
GND	9	10	RPI _RXD_PA23
RPI_GPIO17_PC3	11	12	RPI_I2S_CK_PC16
RPI_GPIO27_PC4	13	14	GND
RPI_GPIO22_PD1	15	16	RPI_GPIO23_PD2
VDD_3V3	17	18	RPI_GPIO24_PC12
RPI_MOSI_PA18	19	20	GND
RPI_MISO_PA17	21	22	RPI_GPIO25_PC11
RPI_SCK_PA16	23	24	RPI_NPCS0_PA19
GND	25	26	RPI_NPCS1_PA20
–	27	28	–
RPI_GPCLK1_PD20	29	30	GND
RPI_GPCLK2_PC0	31	32	RPI_PWM0_PB15
RPI_PWM1_PB17	33	34	GND
RPI_I2S_WS_PC15	35	36	RPI_GPIO16_PC18
RPI_GPIO26_PC19	37	38	RPI_I2S_DIN0_PC14
GND	39	40	RPI_I2S_DOUT0_PC17

In addition to the standard interfaces assigned on the 40-pin connector, alternate functions are available on certain pins. See the table below.

Table 3-27. 40-Pin GPIO Alternate Functions

Signal	PIO	Pin No.	Alternate Function	IOset
RPI_GPIO24_PC12	PC12	18	PDMC1_CLK	1
RPI_GPIO25_PC11	PC11	22	PDMC1_DS0	1
RPI_RXD_PA23	PA23	10	PDMC0_CLK	1
RPI_TXD_PA24	PA24	8	PDMC0_DS0	1
RPI_GPIO17_PC3	PC3	11	SPDIF_RX	2
RPI_GPIO27_PC4	PC4	13	SPDIF_TX	2

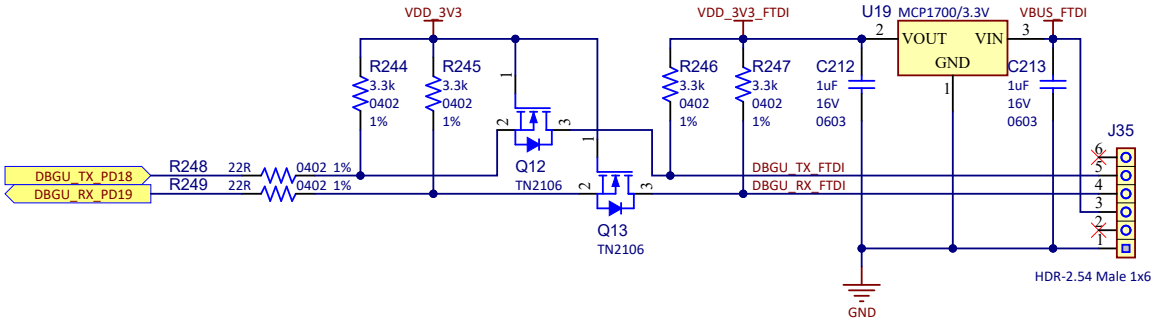
3.4.10 Debug Interface

The board includes three interfaces for debugging purposes.

3.4.10.1 Serial Debug Com Port (FTDI)

The board features a dedicated serial port for debugging, accessible through header J35. Various interfaces can be used as a USB/Serial DBGU port bridge, such as the FTDI TTL-232R USB-to-TTL serial cable.

Figure 3-42. Serial Debug Port Schematic



The DBGU serial port uses the MCP1700/3.3V LDO to prevent any voltage higher than 3.3V to be applied on any 3.3V-only tolerant external USB-to-UART converter. For more details about the MCP1700/3.3V device, refer to the product web page.

An inexpensive level shifter solution is also implemented using two TN2106 N-channel MOSFETs.

For more details about the TN2106 device, refer to the product web page.

Table 3-28. Serial Debug Port Signal Description

PIO	Signal Name	Signal Description
PD19	DBGU_RX_PD19	UART receive data line
PD18	DBGU_TX_PD18	UART transmit data line

3.4.10.2 Debug JTAG

A 20-pin JTAG header (J38) is provided on the board to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-43. JTAG Connector Schematic

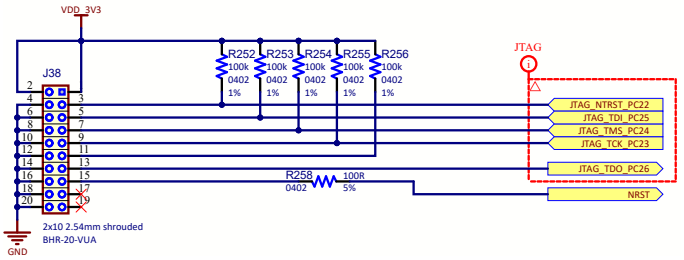


Table 3-29. JTAG Connector Pin Assignment

Signal	Pin No.	Pin No.	Signal
VDD_3V3	2	1	VDD_3V3
GND	4	3	NTRST
GND	6	5	TDI
GND	8	7	TMS
GND	10	9	TCK
GND	12	11	VDD_3V3
GND	14	13	TDO
GND	16	15	NRST
GND	18	17	NC
GND	20	19	NC

3.4.10.3 USB-to-I²C bridge

One of the options to access the power measurement data from the PAC1934 device is via the USB-to-I²C bridge MCP2221A.

When using this device to access the PAC1934, make sure that the J6 and J7 headers have jumpers placed in the corresponding position. By default, the USB-to-I²C device is selected.

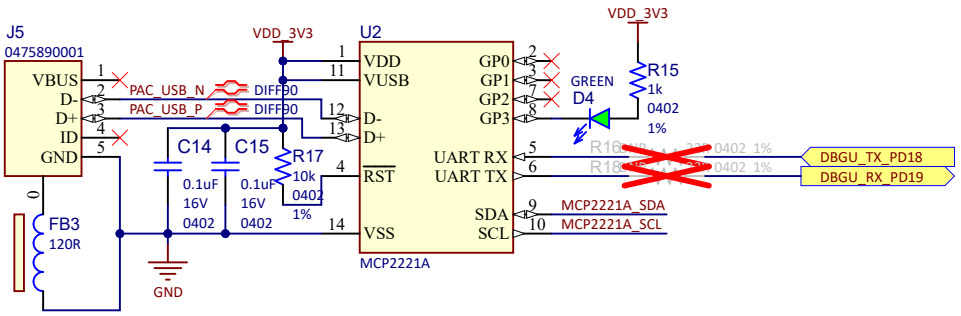
Connect the device to a computer using a USB-microAB cable plugged in the J5 connector.

Beforehand, the required MCP2221A device drivers and PAC1934 demo application should be installed.

Additionally, the MCP2221A can be used as a serial debug port instead of the dedicated FTDI header J35. To enable this feature, populate the R16 and R18 resistors.

For more details about the MCP2221A device, refer to the product web page.

Figure 3-44. MCP2221A Schematic



3.4.11 User Interface

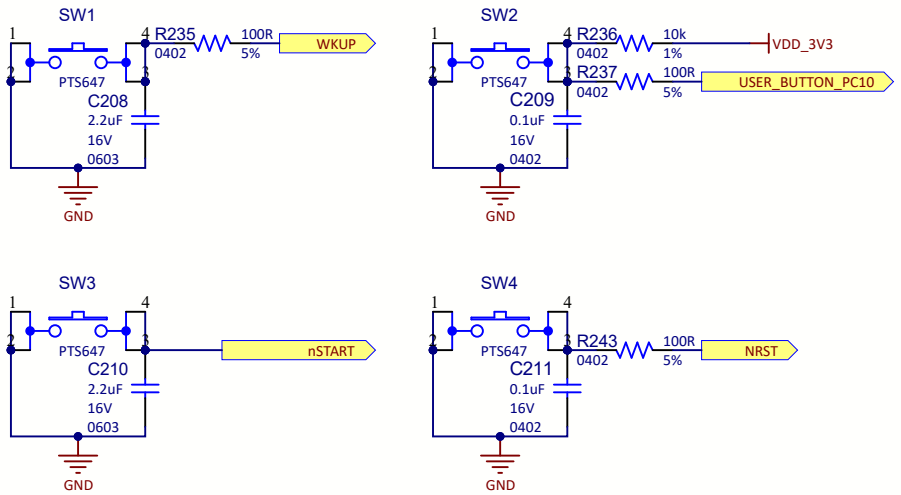
Board includes several user interaction features, like buttons and LEDs.

3.4.11.1 Push Button Switches

The board features four push buttons:

- One Board Wake-up push button (SW1) connected to the WKUP signal. It is used to wake up the MPU from a Low-Power state.
- One User push button (SW2) connected to PIO PC10. This is for user usage.
- One Start push button (SW3) connected to the MCP16502 pin. When pressed, the PMIC start-up sequence is initiated if the buck converters are off. Pressing the Start button will also assert the WKUP signal to wake up the MPU from a Low-Power state.
- One Board Reset push button (SW4). When pressed, the processor is reset.

Figure 3-45. Push Button Schematics



3.4.11.2 RGB LED

The board features one common anode RGB LED, D11. The three LED cathodes are controlled via GPIO pins. The red LED junction always turns on at board reset.

Figure 3-46. RGB LED

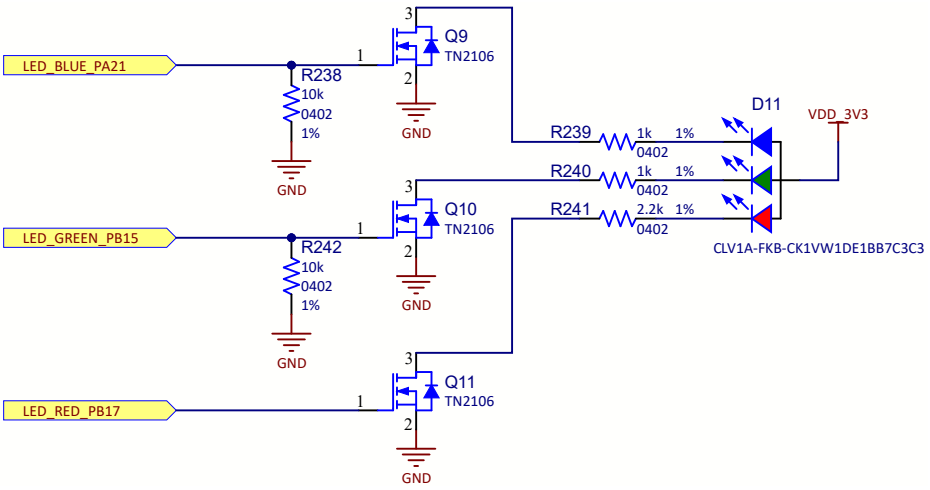


Table 3-30. RGB LED Signal Description

PIO	Signal Name	Signal Description
PB17	LED_RED_PB17	Red LED
PB15	LED_GREEN_PB15	Green LED
PA21	LED_BLUE_PA21	Blue LED

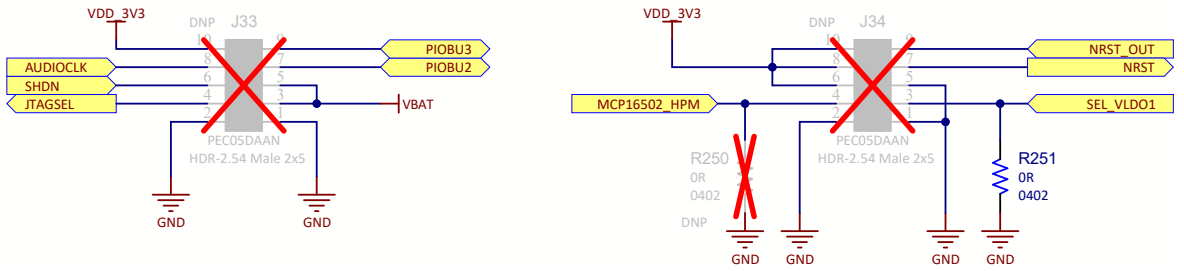
3.4.12 Tamper and System Signal Connectors

Unused signals and PIOs provided by the MPU are routed on separate connectors, J33 and J34 (not mounted). System signals are also accessible externally on these connectors.

The board provides two tamper pins for static or dynamic intrusion detections on header J33. Audio clock signal, shutdown and JTAGSEL are also present on the same connector.

Unused and available system signals are available on header J34.

Figure 3-47. Tamper and System Signals Connectors Schematic



The tables below provide a signal description of headers J33 and J34.

Table 3-31. J33 Signal Description

Signal Name	Signal Description
PIOBU2	Tamper I/O 2
PIOBU3	Tamper I/O 3
AUDIOCLK	Dedicated audio clock signal
SHDN	Signal used to enable and disable an external power supply circuit
JTAGSEL	When pulled high, enables the JTAG boundary scan

Table 3-32. J34 Signal Description

Signal Name	Signal Description
MCP16502_HPM	PMIC High-Power mode enable
NRST_OUT	Peripheral reset output
NRST	Processor reset input
SEL_VLDO1	Selects the output voltage of LDO1 of the MCP16502 PMIC

4. Installation and Operation

4.1 System and Configuration Requirements

The board requires the following:

- A personal computer
- USB cable (provided in the kit box)
- One USB-UART converter (ex: FTDI TTL-232R-3V3 or compatible)

4.2 Board Setup

Follow these steps before using the board:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the default jumper settings (see Default Jumper Settings).
3. Connect the USB Type-C cable to connector J3 (USB-A on silkscreen port).
4. Connect the other end of the cable to a free port on the PC.
5. Connect a USB-UART converter to J35, making sure to also connect the VBUS_FTDI power source.
6. Open a terminal (console 115200, N, 8, 1) on the PC for the USB-UART converter.
7. Reset the board. The start-up message “RomBOOT” should appear on the console.

4.3 Board Operation Hints and Tips

- Only use the USB cable included in the kit box or an equivalent one for powering the board.
- When powering the board, it will start automatically without the need to press the START button.
- Make sure the board is not powered when plugging and unplugging daughter boards (on mikroBUS, M.2, 10/100/1000 SODIMM slot, RPi connector) and displays. Exceptions to this rule can be made for USB connectors.

5. Errata

5.1 VBAT Battery Power Leakage

In some scenarios, the M.2 and SODIMM interrupt sources can cause a VBAT battery power leakage. This can occur through the interrupt pins when a daughter card is attached. The purpose of these interrupt sources is to wake up the MPU from Low-Power modes.

To determine if there is a power leakage:

1. Unpower the board, insert a coin battery in the BT1 connector and make sure no daughter card is attached.
2. Remove jumper JP2 from header J4.
3. Measure the current through the battery.
4. Connect the daughter card.
5. Measure the current again.

If the current is higher than the current previously measured and the wake-up functionality is not required, remove the corresponding diode:

- D6 for the M.2 interface
- D7 for the SODIMM interface

If the wake-up functionality of the daughter card is required, make sure to remove the daughter card connected to SAMA7D65-Curiosity while not using the board, to save battery life.

6. Appendix: Schematics

This section contains the following schematics:

- Block Diagram
- PIO Muxing and Jumper Settings
- Power Inputs
- Power Management
- MPU Clocks Power System Ports
- MPU External Memory Controller and Device
- PIO Assignment and FLEXCOM Distribution
- SD Card, NAND Flash, QSPI, EEPROM Memory
- M.2 Interface
- On-Board 10/100/1000 Ethernet Interface
- 10/100/1000 SODIMM Ethernet Interface
- MIPI DSI, LVDS Interfaces, RPi 40-Pin Connector
- USB Interface
- mikroBUS 1, mikroBUS 2, CAN Interface
- User, Debug Interface, Tamper, System Connectors
- Top Assembly
- Bottom Assembly

Figure 6-1. Block Diagram

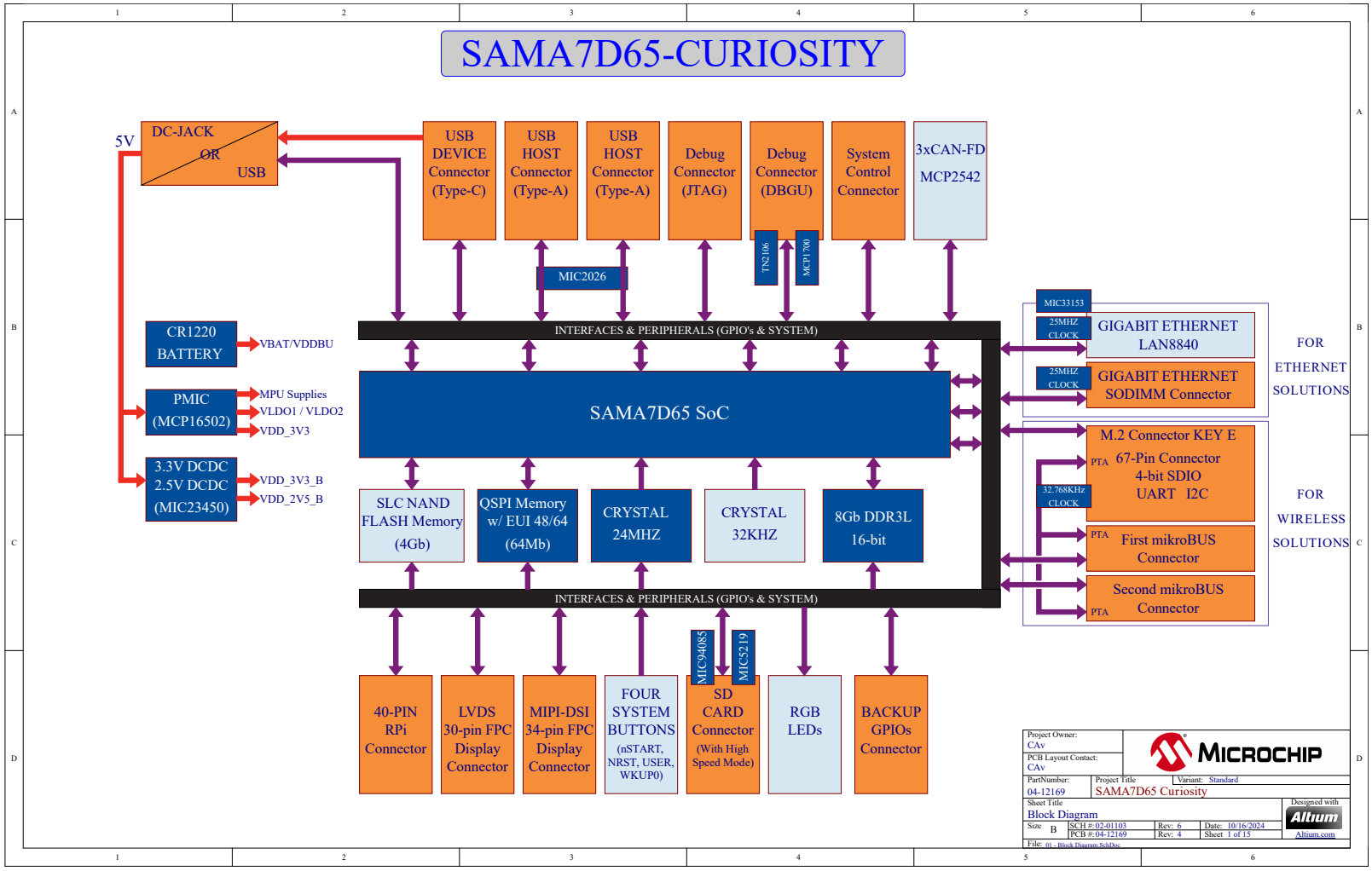
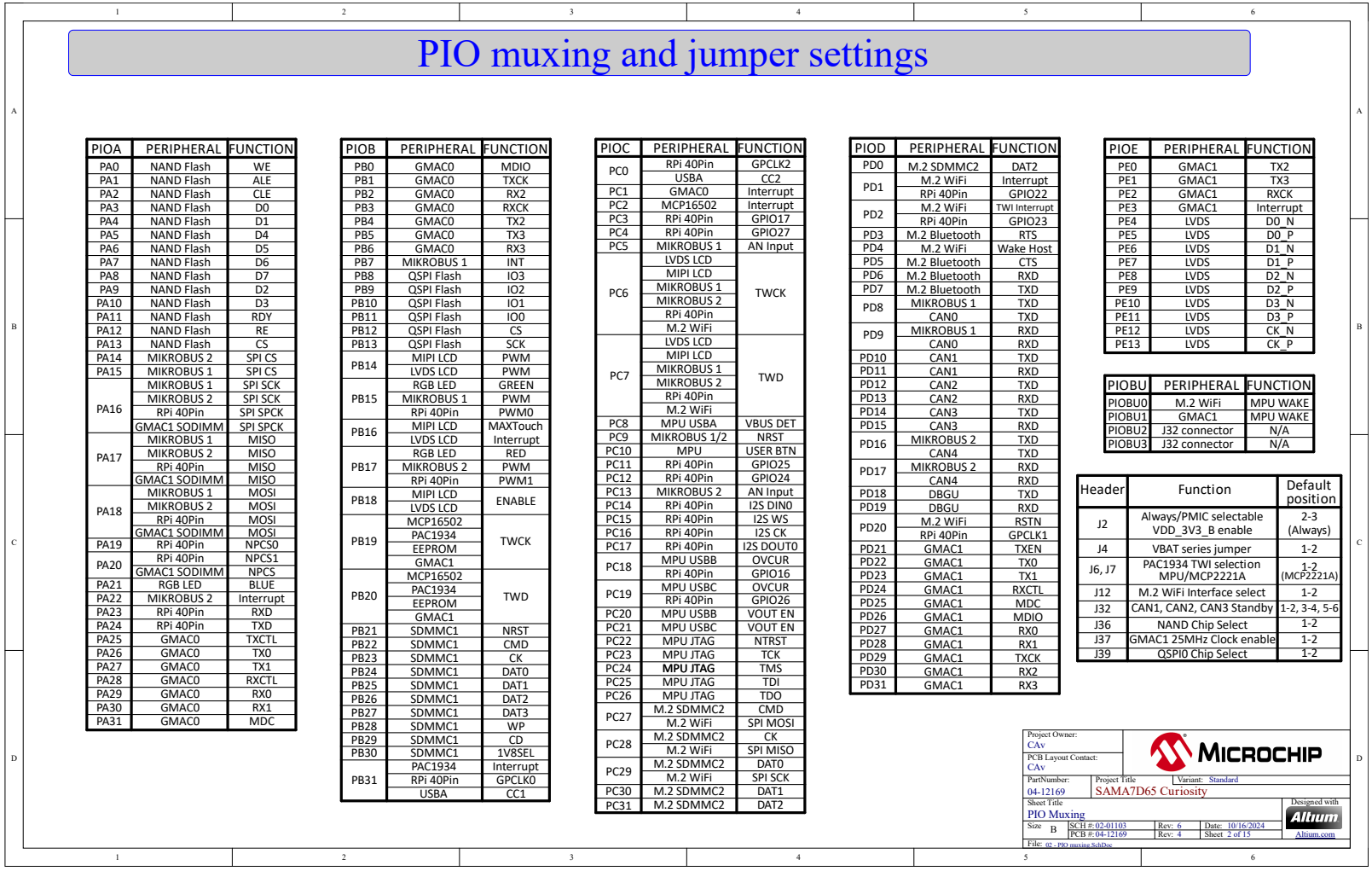


Figure 6-2. PIO Muxing and Jumper Settings Schematic



PIOA	PERIPHERAL	FUNCTION
PA0	NAND Flash	WE
PA1	NAND Flash	ALE
PA2	NAND Flash	CLE
PA3	NAND Flash	D0
PA4	NAND Flash	D1
PA5	NAND Flash	D4
PA6	NAND Flash	D5
PA7	NAND Flash	D6
PA8	NAND Flash	D7
PA9	NAND Flash	D2
PA10	NAND Flash	D3
PA11	NAND Flash	RDY
PA12	NAND Flash	RE
PA13	NAND Flash	CS
PA14	MIKROBUS 2	SPI CS
PA15	MIKROBUS 1	SPI CS
PA16	MIKROBUS 1	SPI SCK
	MIKROBUS 2	SPI SCK
	RPi 40Pin	SPI SPCK
	GMAC1 SODIMM	SPI SPCK
PA17	MIKROBUS 1	MISO
	MIKROBUS 2	MISO
	RPi 40Pin	MISO
	GMAC1 SODIMM	MISO
PA18	MIKROBUS 1	MOSI
	MIKROBUS 2	MOSI
	RPi 40Pin	MOSI
	GMAC1 SODIMM	MOSI
PA19	RPi 40Pin	NPCS0
PA20	RPi 40Pin	NPCS1
	GMAC1 SODIMM	NPCS
PA21	RGB LED	BLUE
PA22	MIKROBUS 2	Interrupt
PA23	RPi 40Pin	RXD
PA24	RPi 40Pin	TXD
PA25	GMAC0	TXCTL
PA26	GMAC0	TX0
PA27	GMAC0	TX1
PA28	GMAC0	RXCTL
PA29	GMAC0	RX0
PA30	GMAC0	RX1
PA31	GMAC0	MDC

PIOB	PERIPHERAL	FUNCTION
PB0	GMAC0	MDIO
PB1	GMAC0	TXCK
PB2	GMAC0	RX2
PB3	GMAC0	RXCK
PB4	GMAC0	TX2
PB5	GMAC0	TX3
PB6	GMAC0	RX3
PB7	MIKROBUS 1	INT
PB8	QSPI Flash	IO3
PB9	QSPI Flash	IO2
PB10	QSPI Flash	IO1
PB11	QSPI Flash	IO0
PB12	QSPI Flash	CS
PB13	QSPI Flash	SCK
PB14	MIPI LCD	PWM
	LVDS LCD	PWM
PB15	RGB LED	GREEN
	MIKROBUS 1	PWM
	RPi 40Pin	PWM0
PB16	MIPI LCD	MAXTouch Interrupt
	LVDS LCD	
PB17	RGB LED	RED
	MIKROBUS 2	PWM
	RPi 40Pin	PWM1
PB18	MIPI LCD	ENABLE
	LVDS LCD	
PB19	MCP16502	TWCK
	PAC1934	
	EEPROM	
	GMAC1	
PB20	MCP16502	TWD
	PAC1934	
	EEPROM	
	GMAC1	
PB21	SDMMC1	NRST
PB22	SDMMC1	CMD
PB23	SDMMC1	CK
PB24	SDMMC1	DAT0
PB25	SDMMC1	DAT1
PB26	SDMMC1	DAT2
PB27	SDMMC1	DAT3
PB28	SDMMC1	WP
PB29	SDMMC1	CD
PB30	SDMMC1	1V8SEL
PB31	PAC1934	Interrupt
	RPi 40Pin	GPCLK0
	USBA	CC1

PIOC	PERIPHERAL	FUNCTION
PC0	RPi 40Pin	GPCLK2
	USBA	CC2
PC1	GMAC0	Interrupt
PC2	MCP16502	Interrupt
PC3	RPi 40Pin	GPIO17
PC4	RPi 40Pin	GPIO27
PC5	MIKROBUS 1	AN Input
PC6	LVDS LCD	TWCK
	MIPI LCD	
	MIKROBUS 1	
	MIKROBUS 2	
	RPi 40Pin	
	M.2 WiFi	
PC7	LVDS LCD	TWD
	MIPI LCD	
	MIKROBUS 1	
	MIKROBUS 2	
	RPi 40Pin	
	M.2 WiFi	
PC8	MPU USBA	VBUS DET
PC9	MIKROBUS 1/2	NRST
PC10	MPU	USER BTN
PC11	RPi 40Pin	GPIO25
PC12	RPi 40Pin	GPIO24
PC13	MIKROBUS 2	AN Input
PC14	RPi 40Pin	I2S DIN0
PC15	RPi 40Pin	I2S WS
PC16	RPi 40Pin	I2S CK
PC17	RPi 40Pin	I2S DOUT0
PC18	MPU USBB	OVCUR
	RPi 40Pin	GPIO16
PC19	MPU USBC	OVCUR
	RPi 40Pin	GPIO26
PC20	MPU USBB	VOUT EN
PC21	MPU USBC	VOUT EN
PC22	MPU JTAG	NTRST
PC23	MPU JTAG	TCK
PC24	**MPU JTAG**	TMS
PC25	MPU JTAG	TDI
PC26	MPU JTAG	TDO
PC27	M.2 SDMMC2	CMD
	M.2 WiFi	SPI MOSI
PC28	M.2 SDMMC2	CK
	M.2 WiFi	SPI MISO
PC29	M.2 SDMMC2	DAT0
	M.2 WiFi	SPI SCK
PC30	M.2 SDMMC2	DAT1
PC31	M.2 SDMMC2	DAT2

PIOD	PERIPHERAL	FUNCTION
PD0	M.2 SDMMC2	DAT2
PD1	M.2 WiFi	Interrupt
	RPi 40Pin	GPIO22
PD2	M.2 WiFi	TWI Interrupt
	RPi 40Pin	GPIO23
PD3	M.2 Bluetooth	RTS
PD4	M.2 WiFi	Wake Host
PD5	M.2 Bluetooth	CTS
PD6	M.2 Bluetooth	RXD
PD7	M.2 Bluetooth	TXD
PD8	MIKROBUS 1	TXD
	CAN0	TXD
PD9	MIKROBUS 1	RXD
	CAN0	RXD
PD10	CAN1	TXD
PD11	CAN1	RXD
PD12	CAN2	TXD
PD13	CAN2	RXD
PD14	CAN3	TXD
PD15	CAN3	RXD
PD16	MIKROBUS 2	TXD
	CAN4	TXD
PD17	MIKROBUS 2	RXD
	CAN4	RXD
PD18	DBGU	TXD
PD19	DBGU	RXD
PD20	M.2 WiFi	RSTN
	RPi 40Pin	GPCLK1
PD21	GMAC1	TXEN
PD22	GMAC1	TX0
PD23	GMAC1	TX1
PD24	GMAC1	RXCTL
PD25	GMAC1	MDC
PD26	GMAC1	MDIO
PD27	GMAC1	RX0
PD28	GMAC1	RX1
PD29	GMAC1	TXCK
PD30	GMAC1	RX2
PD31	GMAC1	RX3

PIOE	PERIPHERAL	FUNCTION
PE0	GMAC1	TX2
PE1	GMAC1	TX3
PE2	GMAC1	RXCK
PE3	GMAC1	Interrupt
PE4	LVDS	D0_N
PE5	LVDS	D0_P
PE6	LVDS	D1_N
PE7	LVDS	D1_P
PE8	LVDS	D2_N
PE9	LVDS	D2_P
PE10	LVDS	D3_N
PE11	LVDS	D3_P
PE12	LVDS	CK_N
PE13	LVDS	CK_P

PIOBU	PERIPHERAL	FUNCTION
PIOBU0	M.2 WiFi	MPU WAKE
PIOBU1	GMAC1	MPU WAKE
PIOBU2	J32 connector	N/A
PIOBU3	J32 connector	N/A

Header	Function	Default position
J2	Always/PMIC selectable VDD_3V3_B enable	2-3 (Always)
J4	VBAT series jumper	1-2
J6, J7	PAC1934 TWI selection MPU/MCP2221A	1-2 (MCP2221A)
J12	M.2 WiFi Interface select	1-2
J32	CAN1, CAN2, CAN3 Standby	1-2, 3-4, 5-6
J36	NAND Chip Select	1-2
J37	GMAC1 25MHz Clock enable	1-2
J39	QSPI0 Chip Select	1-2

Project Owner: CAv
PCB Layout Contact: CAv
PartNumber: 04-12169
Project Title: SAMA7D65 Curiosity
Variant: Standard
Sheet Title: PIO Muxing
Size: B
SCH #: 02-01103 Rev: 6 Date: 10/16/2024
PCB #: 04-12169 Rev: 4 Sheet 2 of 15
File: 02 - PIO muxing.SchDoc
Designed with Altium
Altium.com

Figure 6-3. Power Inputs Schematic

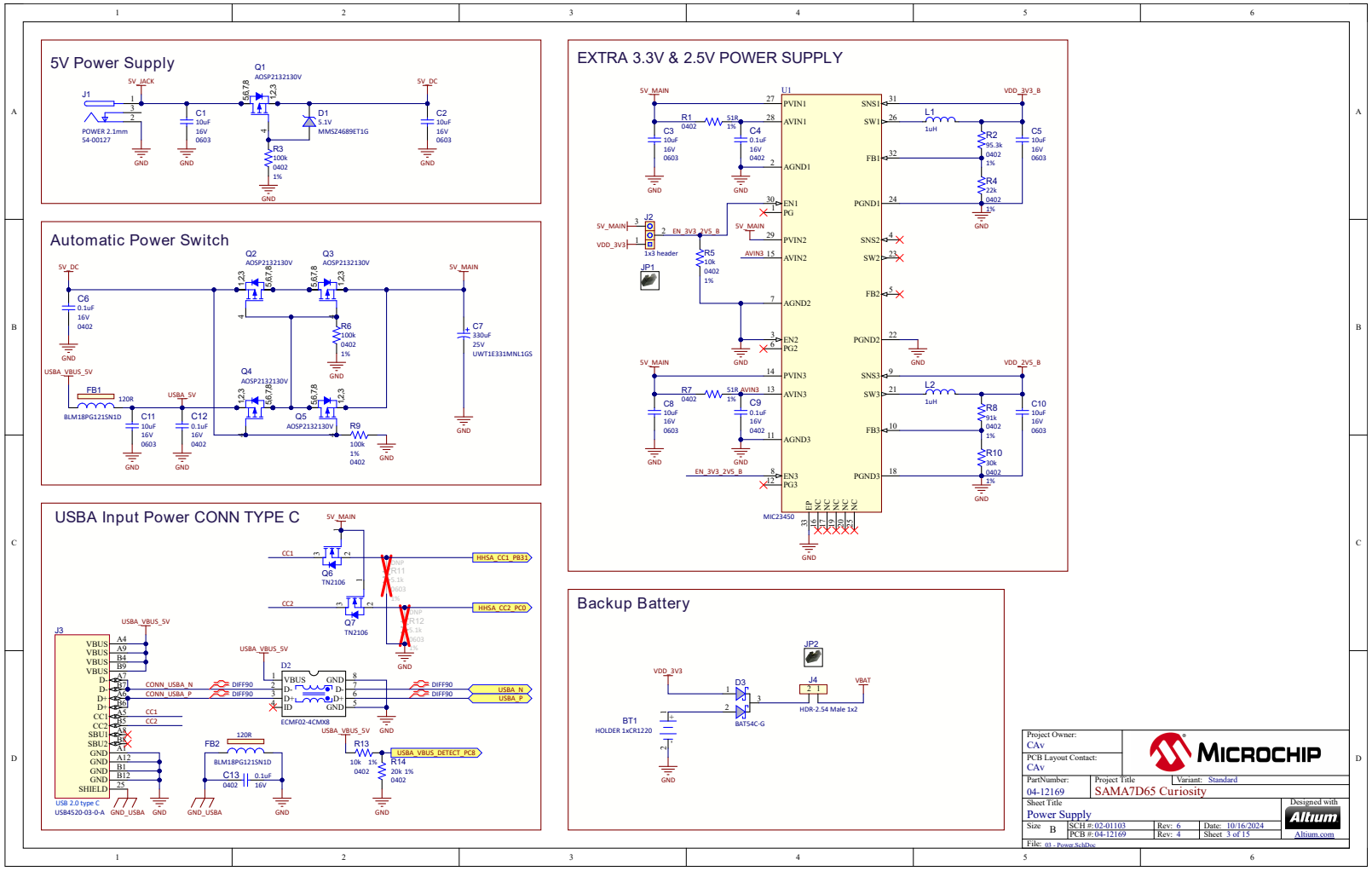


Figure 6-4. Power Management Schematic

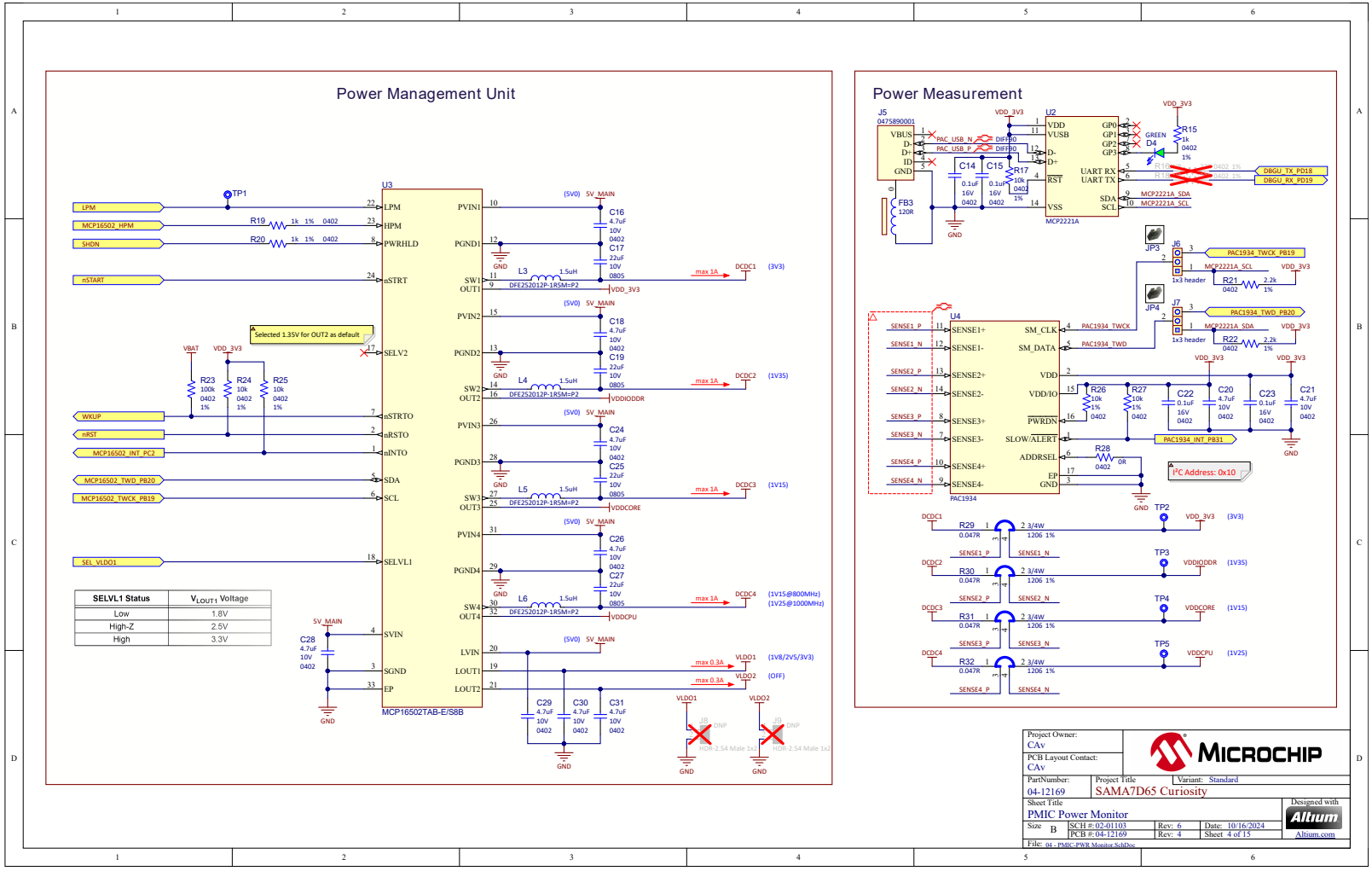


Figure 6-5. MPU Clocks Power System Ports Schematic

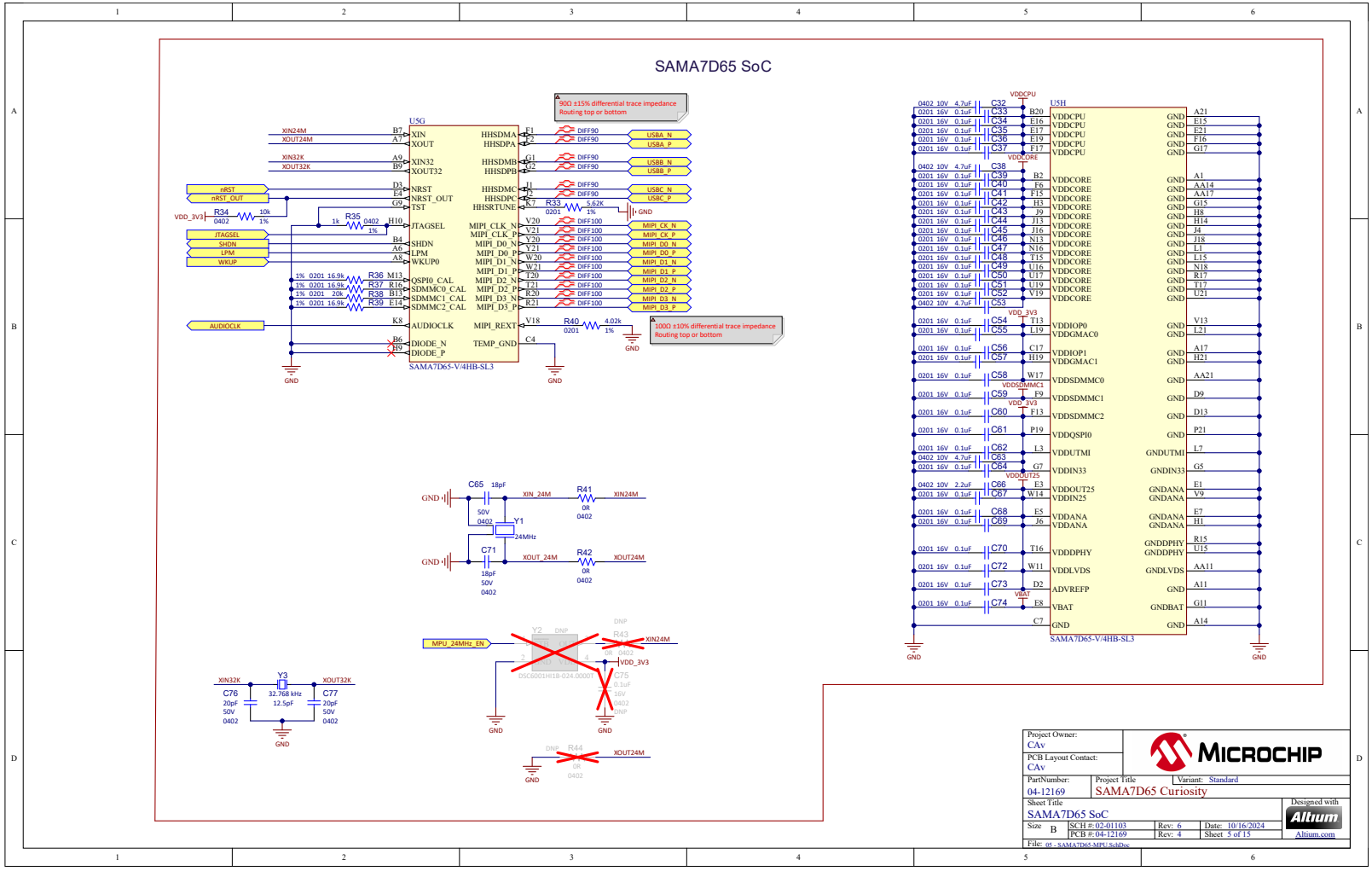


Figure 6-6. MPU External Memory Controller and Device Schematic

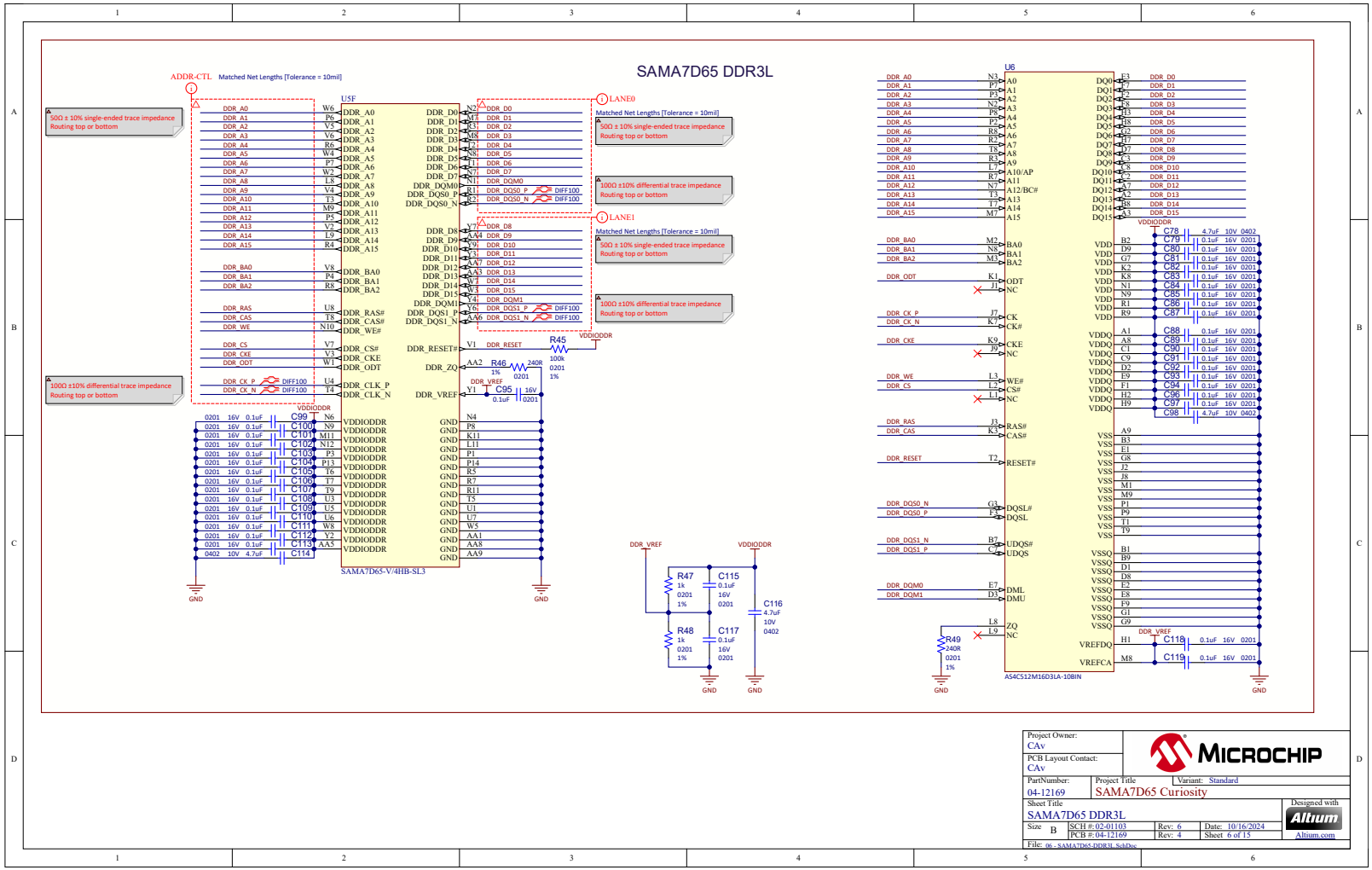


Figure 6-7. PIO Assignment and FLEXCOM Distribution Schematic

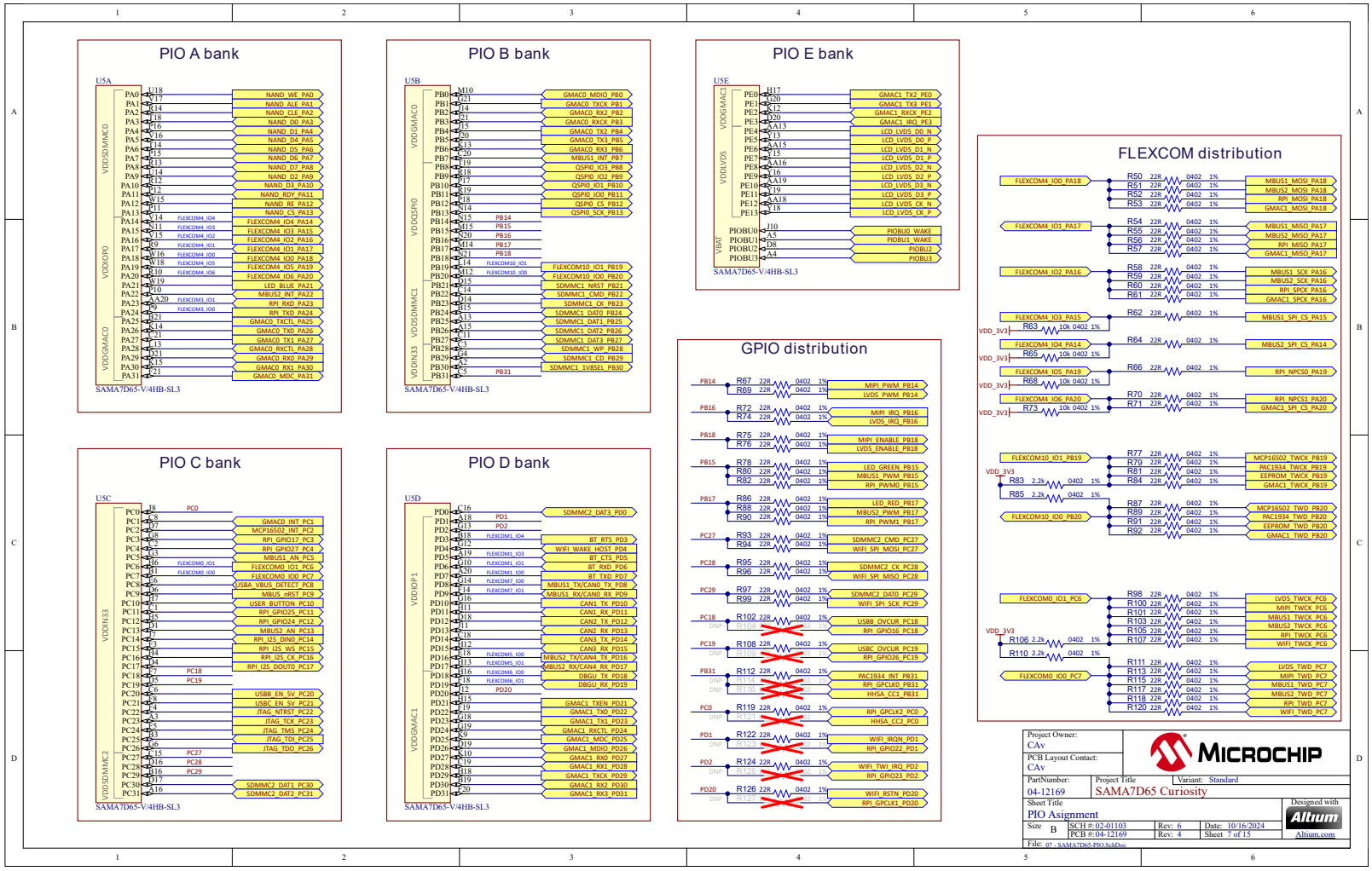


Figure 6-8. SD Card, NAND Flash, QSPI, EEPROM Memory Schematic

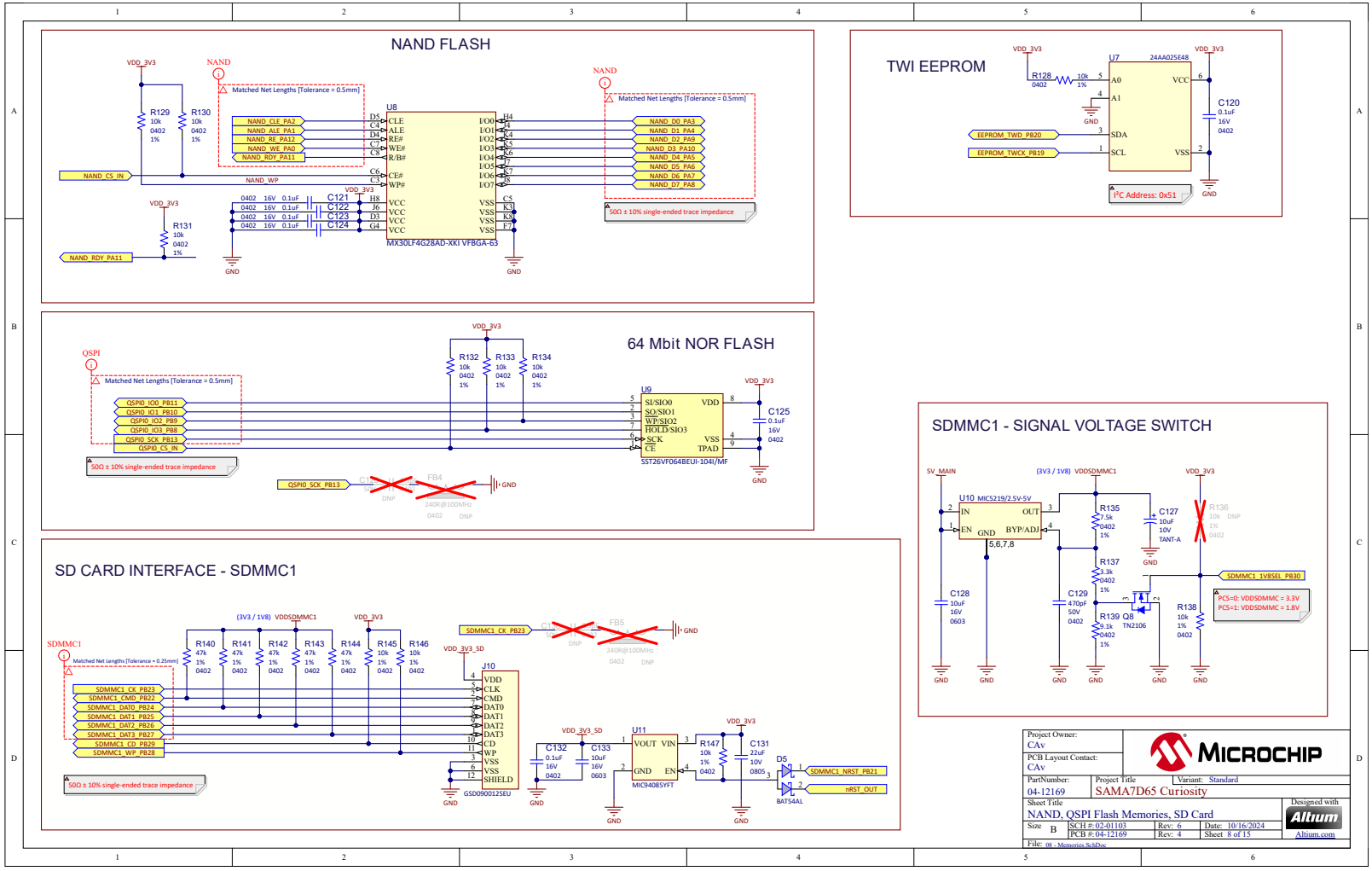


Figure 6-9. M.2 Interface Schematic

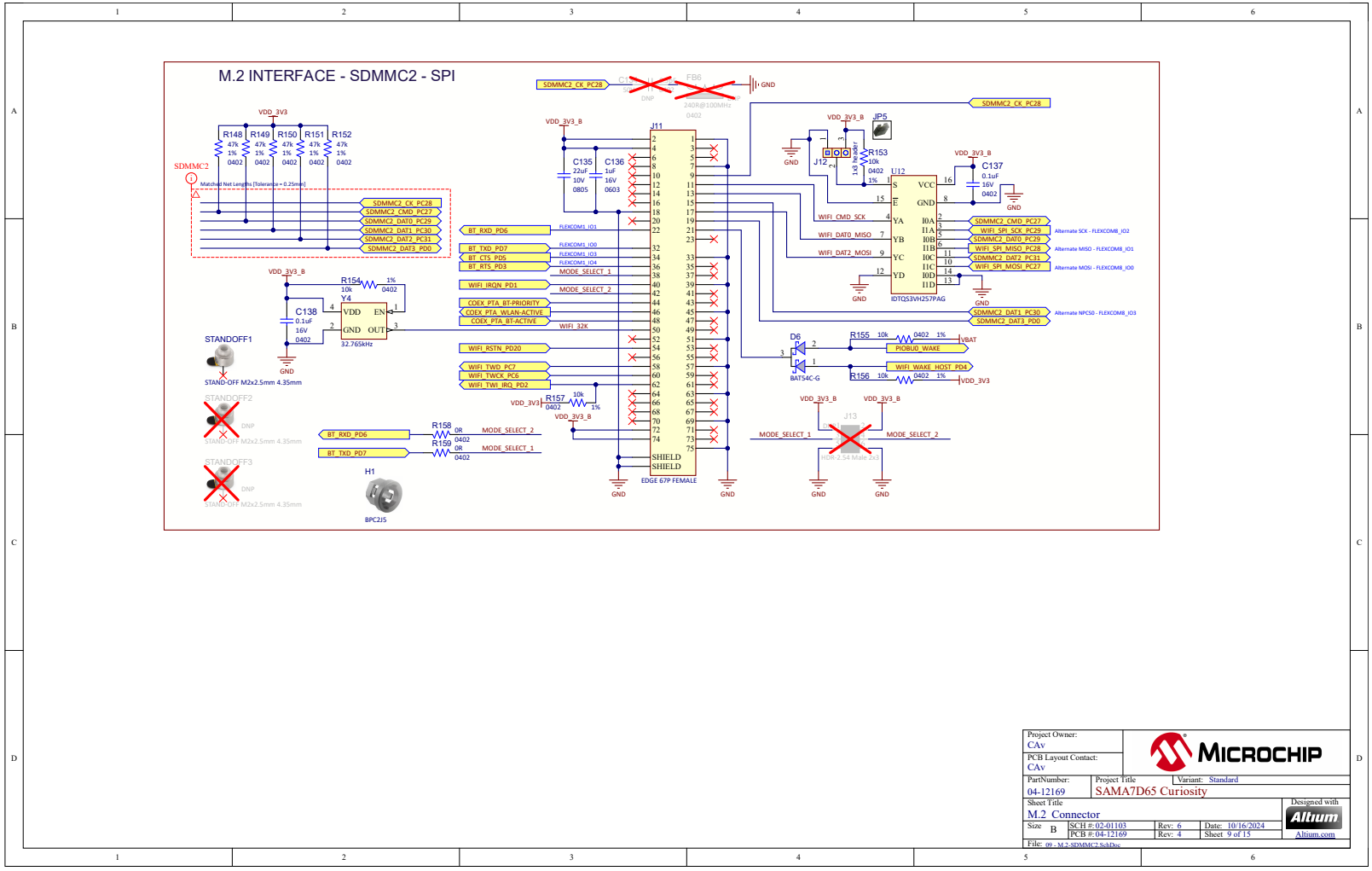


Figure 6-10. On-Board 10/100/1000 Ethernet Interface Schematic

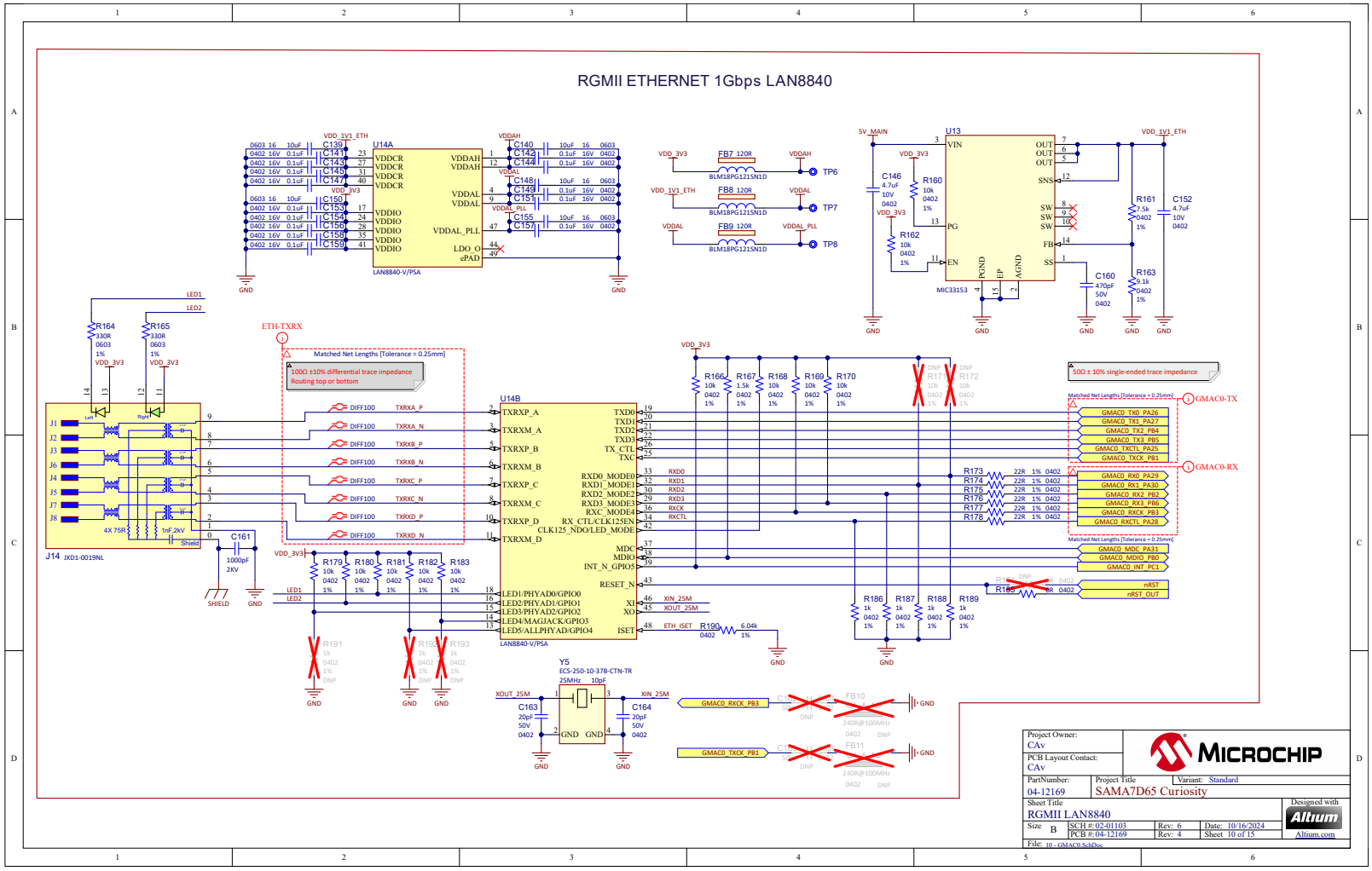


Figure 6-11. 10/100/1000 SODIMM Ethernet Interface Schematic

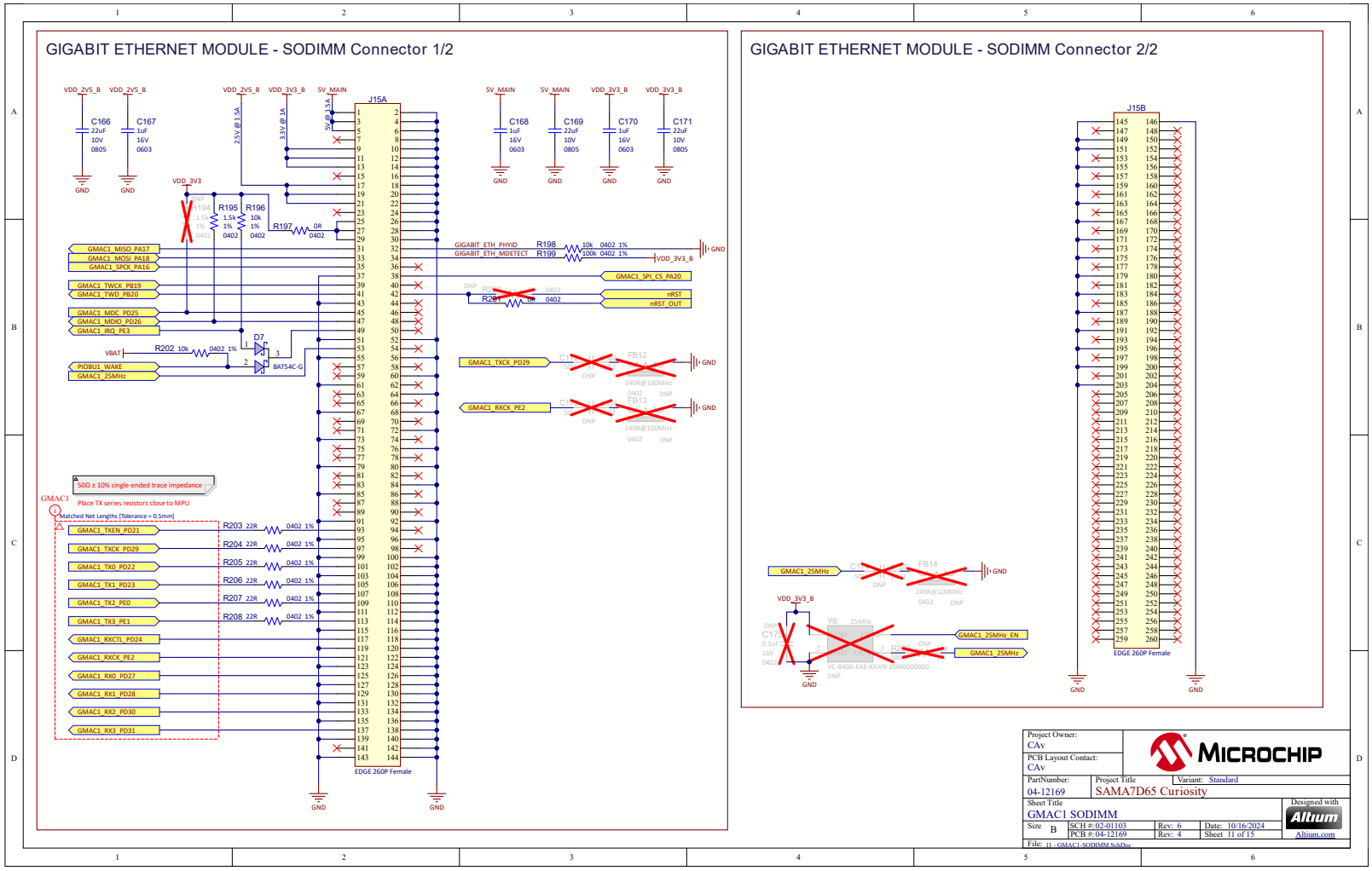


Figure 6-12. MIPI DSI, LVDS Interfaces, RPi 40-Pin Connector Schematic

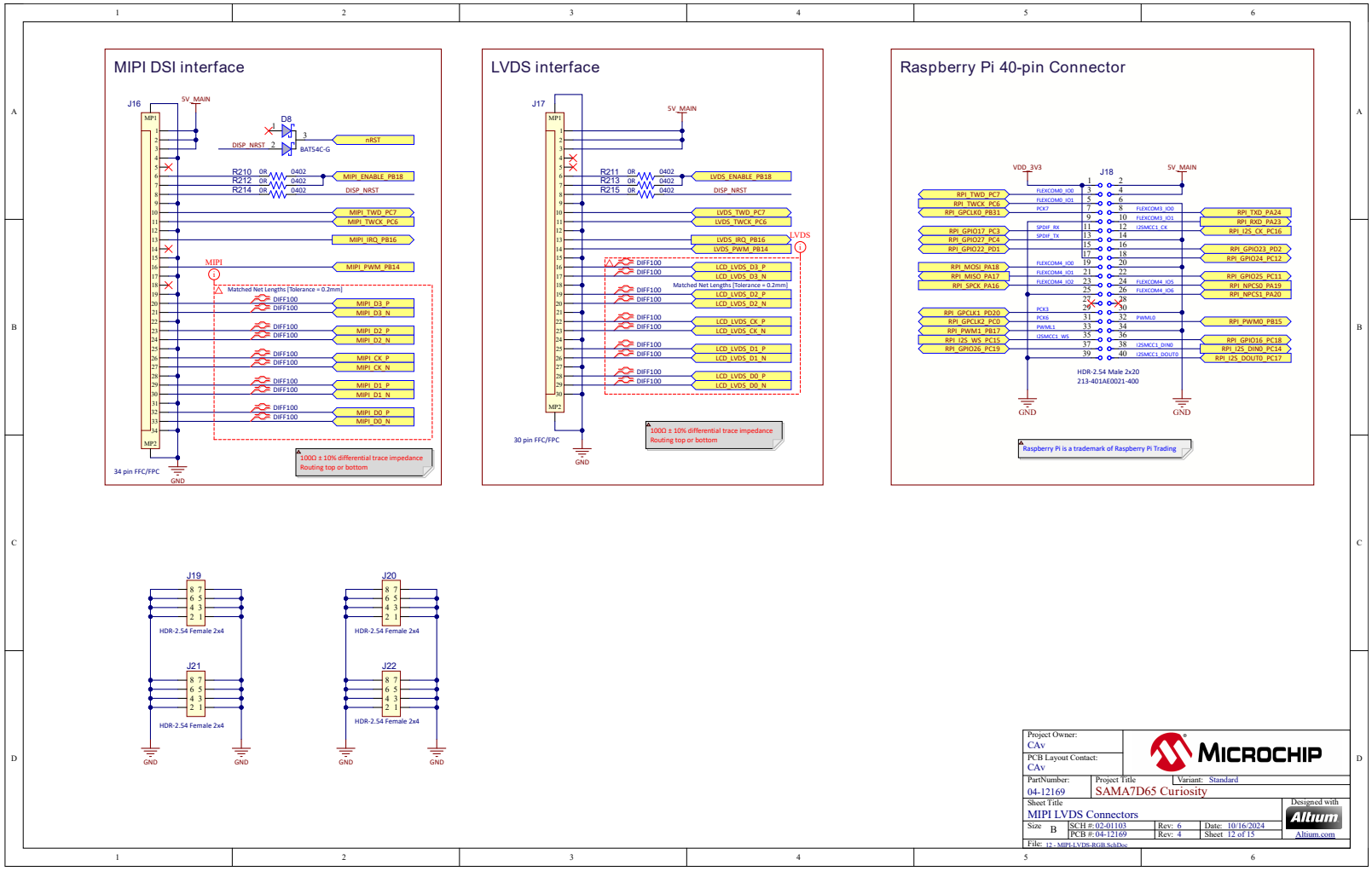


Figure 6-13. USB Interface Schematic

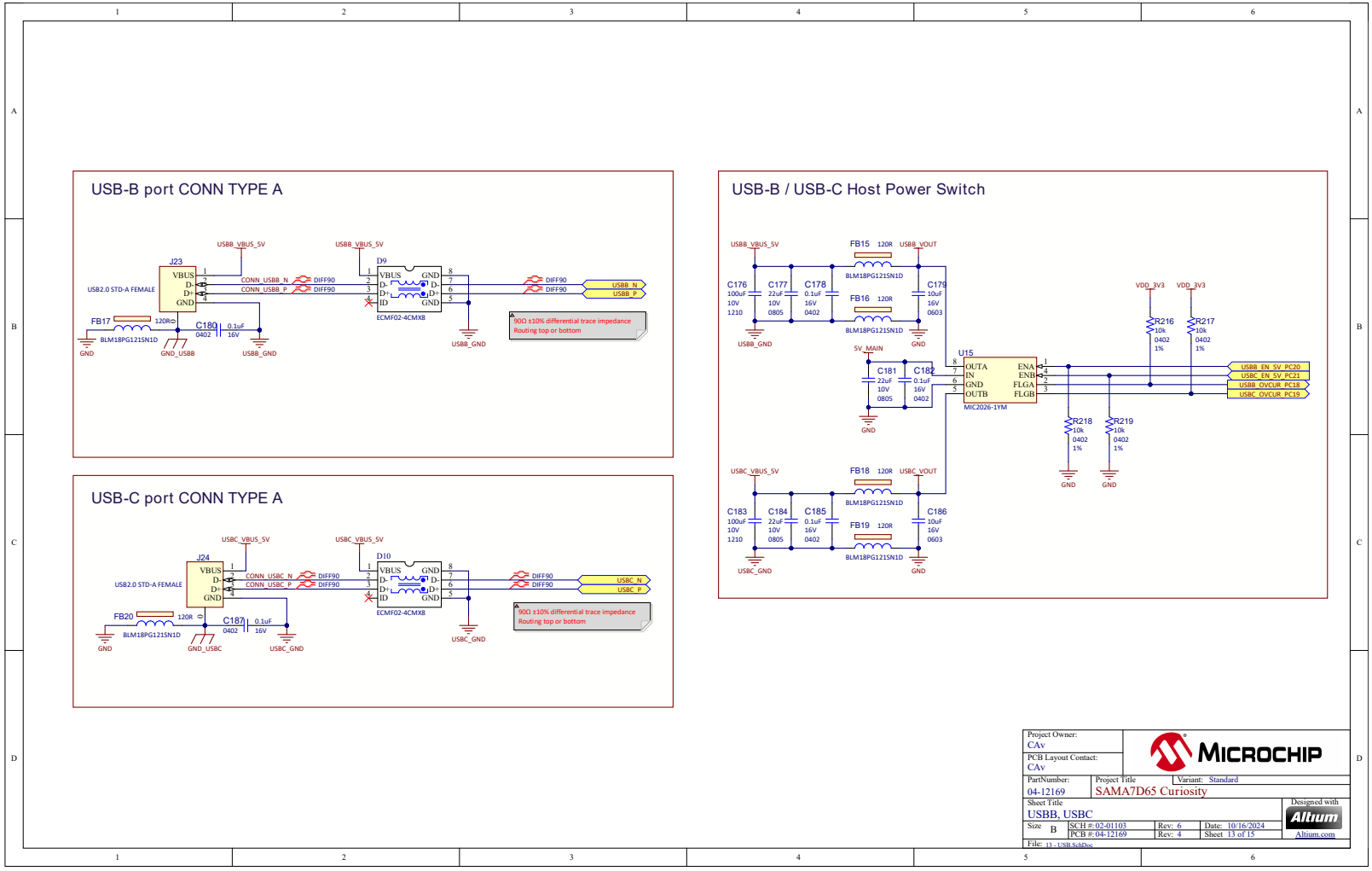


Figure 6-14. mikroBUS 1, mikroBUS 2, CAN Interface Schematic

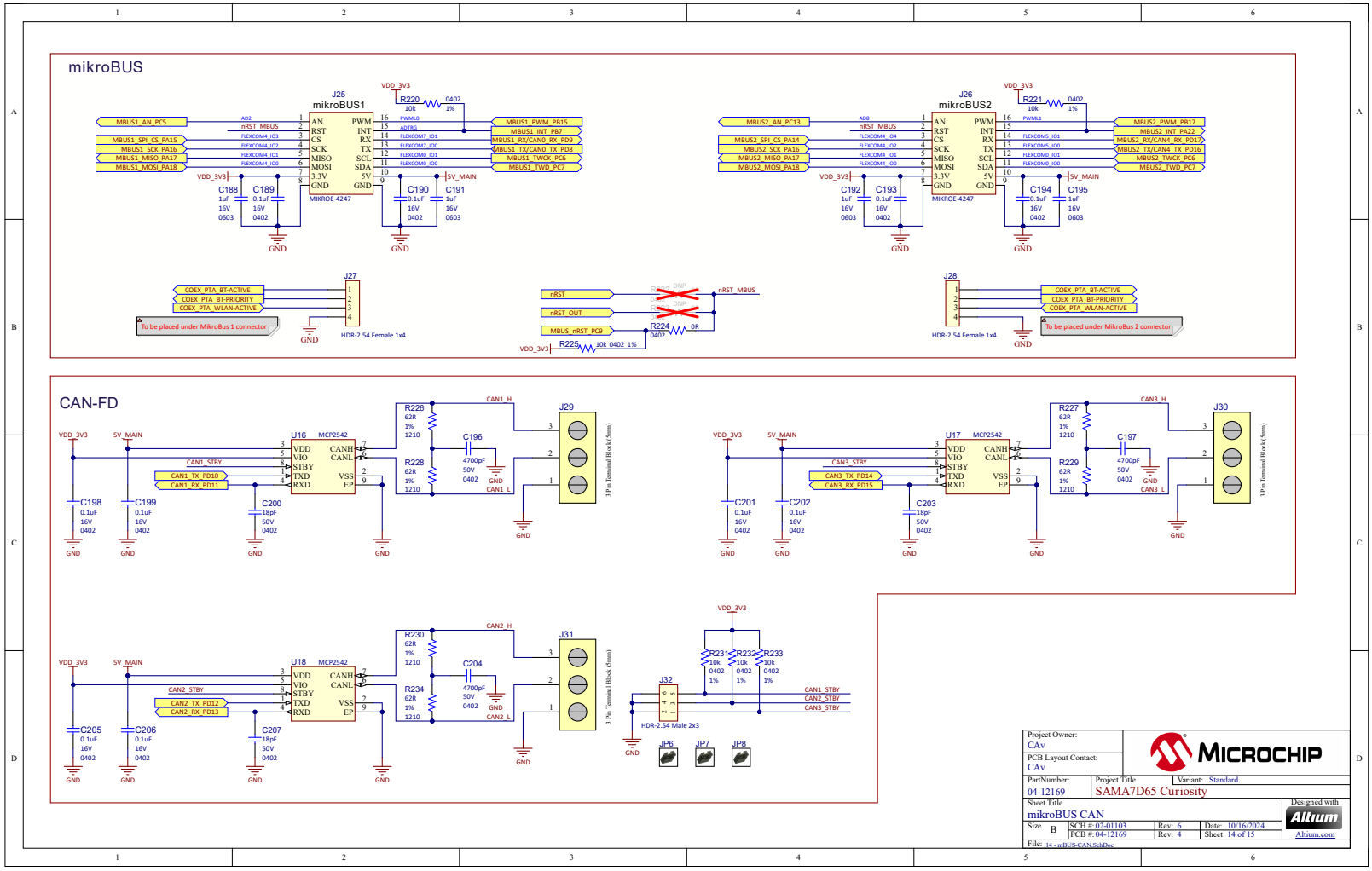


Figure 6-15. User, Debug Interface, Tamper, System Connectors Schematic

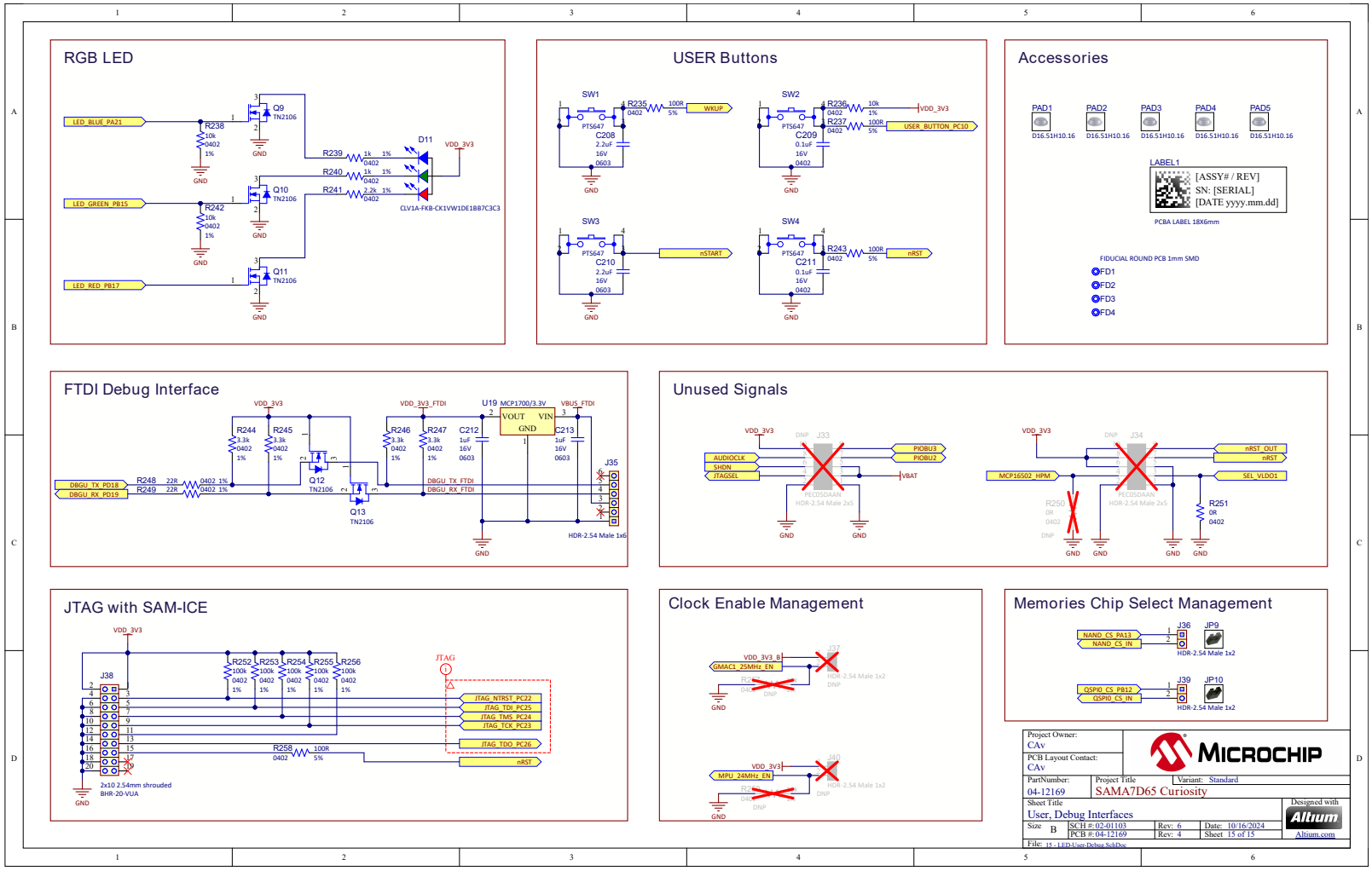


Figure 6-16. Top Assembly Drawing

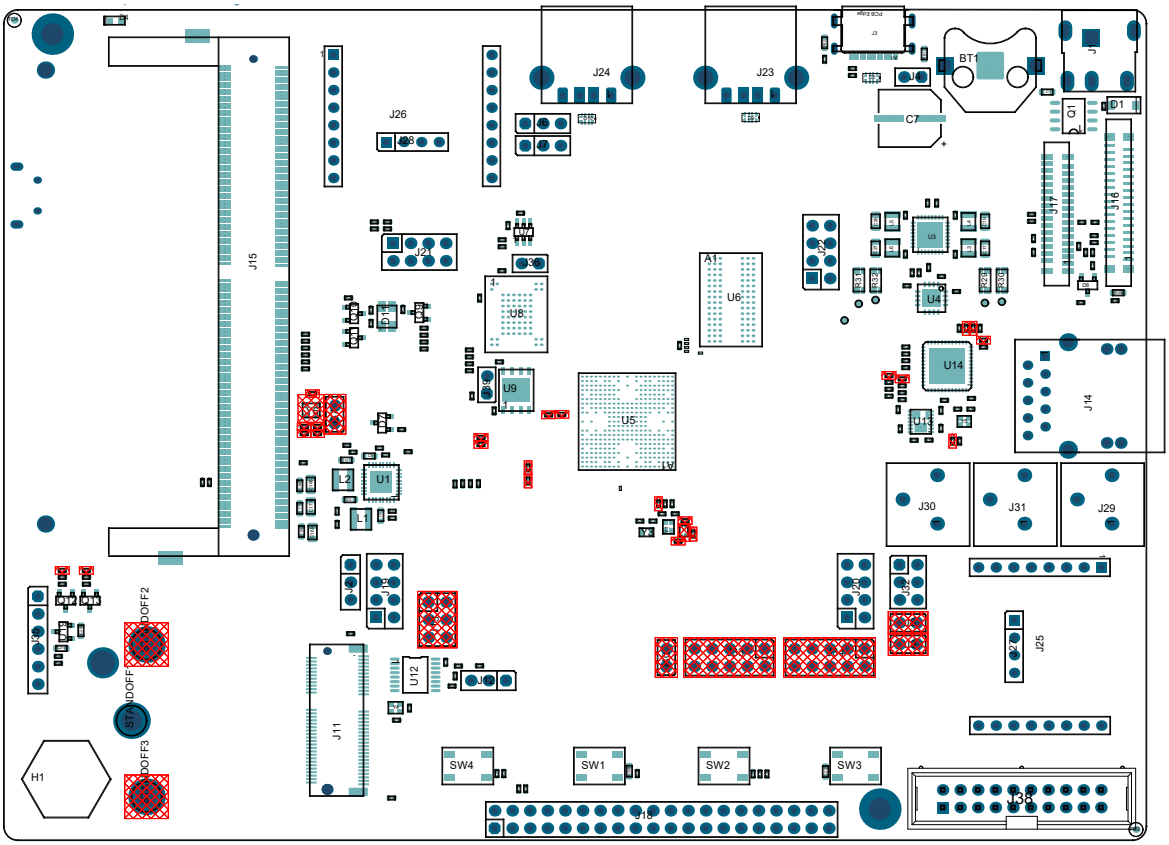
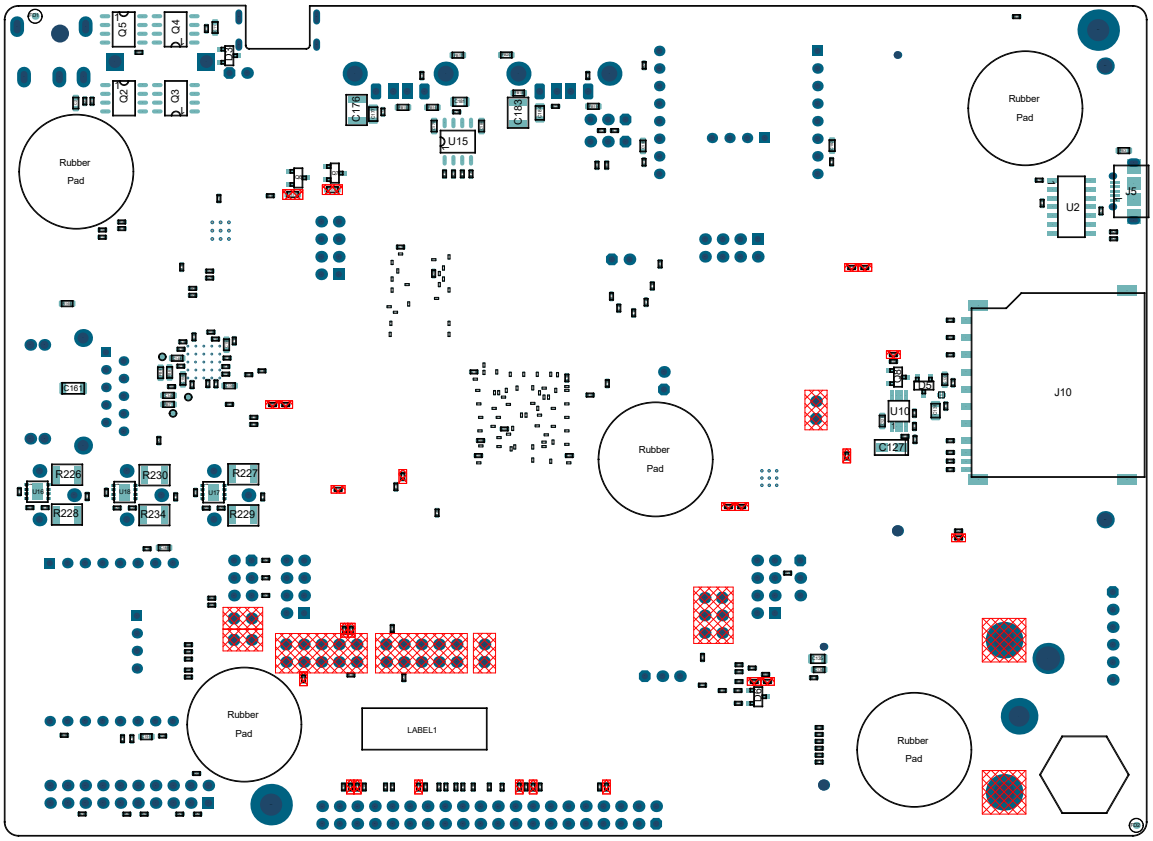


Figure 6-17. Bottom Assembly Drawing



7. Revision History

7.1 Rev. A - 12/2024

First issue.

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