

Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor Core
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - Embedded ICE (In-Circuit Emulation)
- 8K Bytes On-chip SRAM
 - 32-bit Data Bus
 - Single-clock Cycle Access
- Fully-programmable External Bus Interface (EBI)
 - Maximum External Address Space of 64M Bytes
 - Up to 8 Chip Selects
 - Software Programmable 8-/16-bit External Data Bus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
 - 4 External Interrupts, Including a High-priority Low-latency Interrupt Request
- 32 Programmable I/O Lines
- 3-channel 16-bit Timer/Counter
 - 3 External Clock Inputs
 - 2 Multi-purpose I/O Pins per Channel
- 2 USARTs
 - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Advanced Power-saving Features
 - CPU and Peripheral Can be Deactivated Individually
- Fully Static Operation: 0 Hz to 40 MHz Internal Frequency Range at 3.0 V, 85°C
- 1.8V to 3.6V Operating Range
- Available in a 100-lead TQFP Package

Description

The AT91M40800 microcontroller is a member of the Atmel AT91 16-/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The AT91M40800 microcontroller features a direct connection to off-chip memory, including Flash, through the fully-programmable External Bus Interface (EBI). An eight-level priority vectored interrupt controller, in conjunction with the Peripheral Data Controller, significantly improves the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with on-chip high-speed memory and a wide range of peripheral functions on a monolithic chip, the AT91M40800 is a powerful microcontroller that offers a flexible, cost-effective solution to many compute-intensive embedded control applications.



AT91 ARM® Thumb® Microcontrollers

AT91M40800 Electrical Characterisitics



Absolute Maximum Ratings*

Operating Temperature (Industrial) ..	-40° C to + 85° C
Storage Temperature	-60° C to + 150° C
Voltage on Any Input Pin with Respect to Ground	-0.5V to + 5.5V
Maximum Operating Voltage	4.6V
DC Output Current	6 mA

***NOTICE:**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The following characteristics are applicable to the Operating Temperature range: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise specified and are certified for a Junction Temperature up to $T_J = 100^{\circ}\text{C}$.

Table 1. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	DC Supply		1.8		3.6	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3\text{V}$			0.8	V
V_{IH}	Input High Voltage	$V_{DD} = 3.3\text{V}$	2.0			V
V_{OL}	Output Low Voltage	$I_{OL} = 2.0\text{ mA}$, $V_{DD} = 3.3\text{V}$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = 2.0\text{ mA}$, $V_{DD} = 3.3\text{V}$	2.4			V
I_{LEAK}	Input Leakage Current				4	μA
I_{PULL}	Input Pull-up Current	$V_{DD} = 3.6\text{V}$, $V_{IN} = 0\text{V}$			350	μA
C_{IN}	Input Capacitance				6.6	pF
I_{SC}	Static Current	$V_{DD} = 3.6\text{V}$; MCKI = 0 Hz All inputs driven TMS, TDI, TCK, NRST = 1	$T_A = 25^{\circ}\text{C}$		12.5	μA
			$T_A = 85^{\circ}\text{C}$		250	

Power Consumption

The values in the following tables are measured values in the operating conditions indicated (i.e., $V_{DD} = 3.3V$ or $2.0V$, $T_A = 25^\circ C$) on the AT91EB40 Evaluation Board.

Table 2. Power Consumption

Mode	Conditions	V_{DD}		Unit
		2.0V	3.3V	
Reset		0.06	0.10	mW/MHz
Normal	Fetch in ARM mode out of internal SRAM All peripheral clocks activated	1.38	4.63	
	Fetch in ARM mode out of internal SRAM All peripheral clocks deactivated	1.04	3.44	
Idle	All peripheral clocks activated	0.61	2.06	
	All peripheral clocks deactivated	0.19	0.79	

Table 3. Power Consumption per Peripheral

Peripheral	V_{DD}		Unit
	2.0V	3.3V	
PIO Controller	0.01	0.16	mW/MHz
Timer/Counter Channel	0.01	0.15	
Timer/Counter Block (3 Channels)	0.02	0.35	
USART	0.03	0.40	

Thermal and Reliability Considerations

Thermal Data

In Table 4, the device lifetime is estimated with the MIL-217 standard in the “moderately controlled” environmental model (this model is described as corresponding to an installation in a permanent rack with adequate cooling air), depending on the device Junction Temperature. (For details see the section “Junction Temperature” on page 5.)

Note that the user must be extremely cautious with this MTBF calculation: as the MIL-217 model is pessimistic with respect to observed values due to the way the data/models are obtained (test under severe conditions). The life test results that have been measured are always better than the predicted ones.

Table 4. MTBF Versus Junction Temperature

Junction Temperature (T_J) (°C)	Estimated Lifetime (MTBF) (Year)
100	40
125	22
150	12
175	7

Table 5 summarizes the thermal resistance data related to the package of interest.

Table 5. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	40	°C/ W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	6.4	

Reliability Data

The number of gates and the device die size are provided for the user to calculate reliability data with another standard and/or in another environmental model.

Table 6. Reliability Data

Parameter	Data	Unit
Number of Logic Gates	272	K gates
Number of Memory Gates	400	K gates
Device Die Size	17.6	mm ²

Junction Temperature

The average chip-junction temperature T_J in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

Where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 5 on page 4.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 5 on page 4.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section “Power Consumption” on page 3.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and thereby decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Conditions

Timing Results

The delays are given as typical values in the following conditions:

- $V_{DD} = 3.3V$
- Ambient Temperature = $25^{\circ}C$
- Load Capacitance = 0 pF
- The output level change detection is $0.5 \times V_{DD}$
- The input level is $0.3 \times V_{DD}$ for a low-level detection and is $0.7 \times V_{DD}$ for a high level detection.

The minimum and maximum values given in the AC characteristics tables of this datasheet take into account the process variation and the design.

In order to obtain the timing for other conditions, the following equation should be used:

$$t = \delta_{T^{\circ}} \times \delta_{VDD} \times (t_{DATASHEET} + \sum C_{SIGNAL} \times \delta_{CSIGNAL})$$

Where:

- $\delta_{T^{\circ}}$ is the derating factor in temperature given in Figure 1.
- δ_{VDD} is the derating factor for the Power Supply given in Figure 2.
- $t_{DATASHEET}$ is the minimum or maximum timing value given in this datasheet for a load capacitance of 0 pF.
- C_{SIGNAL} is the capacitance load on the considered output pin.⁽¹⁾
- $\delta_{CSIGNAL}$ is the load derating factor depending on the capacitance load on the related output pins given in Min and Max values in this datasheet.

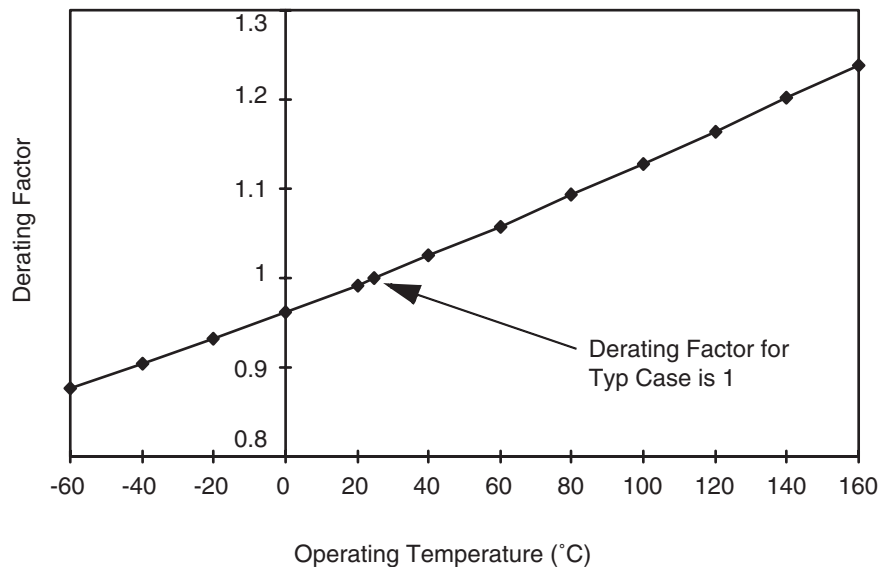
The input delays are given as typical values.

The input delays are given as typical value.

Note: 1. The user must take into account the package capacitance load contribution (C_{IN}) described in Table 1 on page 2.

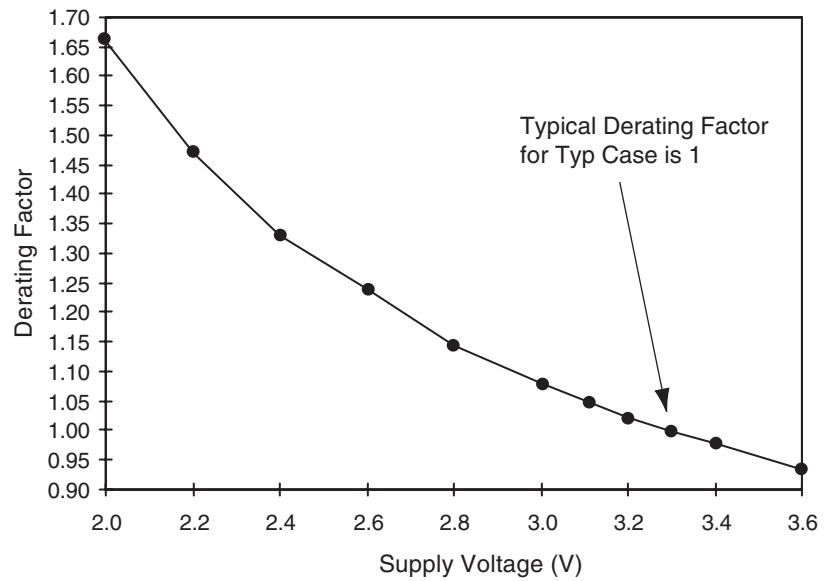
Temperature Derating Factor

Figure 1. Derating Curve for Different Operating Temperatures



Supply Voltage Derating Factor

Figure 2. Derating Curve for Different Supply Voltages



Note: This derating factor is applicable only to timings related to output pins.

Clock Waveforms

Table 7. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CP})$	Oscillator Frequency			47.7	MHz
t_{CP}	Oscillator Period		21.0		ns
t_{CH}	High Half-period		9.1		ns
t_{CL}	Low Half-period		9.4		ns

Table 8. Clock Propagation Times

Symbol	Parameter	Conditions	Min	Max	Units
t_{CDLH}	Rising Edge Propagation Time	$C_{MCKO} = 0 \text{ pF}$	4.2	6.6	ns
		C_{MCKO} derating	0.034	0.053	ns/pF
t_{CDHL}	Falling Edge Propagation Time	$C_{MCKO} = 0 \text{ pF}$	4.5	7.1	ns
		C_{MCKO} derating	0.042	0.066	ns/pF

Figure 3. Clock Waveform

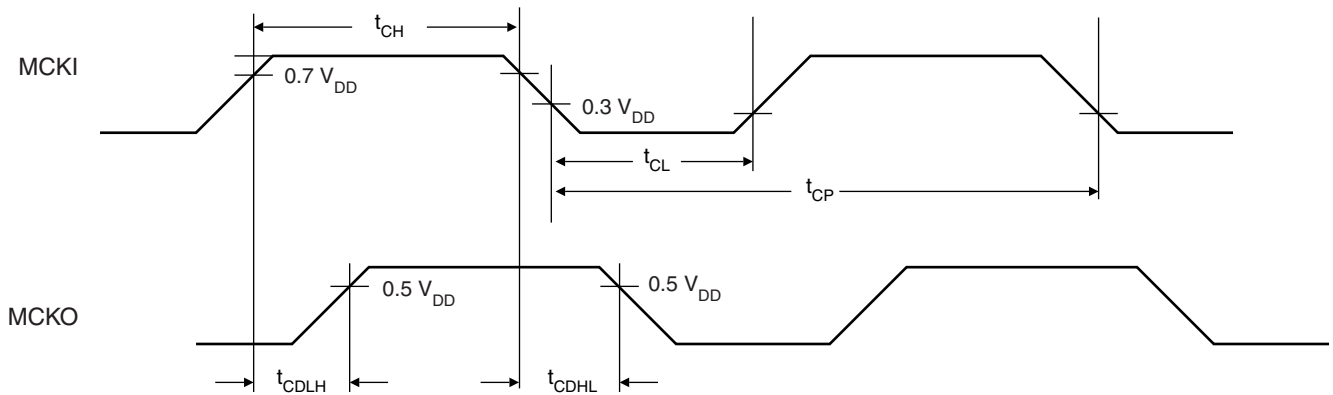
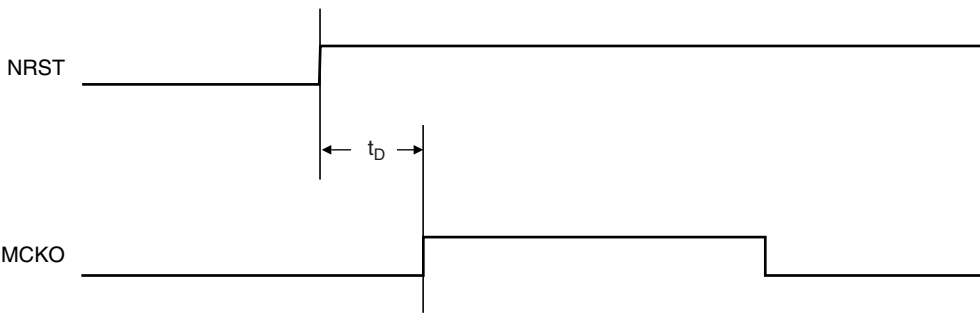


Table 9. NRST to MCKO

Symbol	Parameter	Min	Max	Units
t_D	NRST Rising Edge to MCKO Valid Time	$3(t_{CP}/2)$	$7(t_{CP}/2)$	ns

Figure 4. MCKO Relative to NRST



AC Characteristics

EBI Signals Relative to MCKI

The following tables show timings relative to operating condition limits defined in the section “Timing Results” on page 6. See Figure 5 on page 14.

Table 10. General-purpose EBI Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI ₁	MCKI Falling to NUB Valid	C _{NUB} = 0 pF	5.4	11.7	ns
		C _{NUB} derating	0.034	0.066	ns/pF
EBI ₂	MCKI Falling to NLB/A0 Valid	C _{NLB} = 0 pF	4.3	8.7	ns
		C _{NLB} derating	0.038	0.062	ns/pF
EBI ₃	MCKI Falling to A1 - A23 Valid	C _{ADD} = 0 pF	4.2	10.0	ns
		C _{ADD} = derating	0.038	0.066	ns/pF
EBI ₄	MCKI Falling to Chip Select Change	C _{NCS} = 0 pF	4.6	10.4	ns
		C _{NCS} derating	0.038	0.057	ns/pF
EBI ₅	NWAIT Setup before MCKI Rising		0.6		ns
EBI ₆	NWAIT Hold after MCKI Rising		3.2		ns

Table 11. EBI Write Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI ₇	MCKI Rising to NWR Active (No Wait States)	C _{NWR} = 0 pF	4.3	7.1	ns
		C _{NWR} derating	0.042	0.066	ns/pF
EBI ₈	MCKI Rising to NWR Active (Wait States)	C _{NWR} = 0 pF	5.0	8.2	ns
		C _{NWR} derating	0.042	0.066	ns/pF
EBI ₉	MCKI Falling to NWR Inactive (No Wait States)	C _{NWR} = 0 pF	4.9	8.0	ns
		C _{NWR} derating	0.034	0.053	ns/pF
EBI ₁₀	MCKI Rising to NWR Inactive (Wait States)	C _{NWR} = 0 pF	5.0	8.2	ns
		C _{NWR} derating	0.034	0.053	ns/pF
EBI ₁₁	MCKI Rising to D0 - D15 Out Valid	C _{DATA} = 0 pF	4.1	8.6	ns
		C _{DATA} derating	0	0.066	ns/pF
EBI ₁₂	NWR High to NUB Change	C _{NUB} = 0 pF	3.3	7.6	ns
		C _{NUB} derating	0.034	0.066	ns/pF
EBI ₁₃	NWR High to NLB/A0 Change	C _{NLB} = 0 pF	2.8	4.6	ns
		C _{NLB} derating	0.042	0.066	ns/pF
EBI ₁₄	NWR High to A1 - A23 Change	C _{ADD} = 0 pF	2.7	6.5	ns
		C _{ADD} derating	0.042	0.066	ns/pF
EBI ₁₅	NWR High to Chip Select Inactive	C _{NCS} = 0 pF	3.2	6.4	ns
		C _{NCS} derating	0.034	0.066	ns/pF
EBI ₁₆	Data Out Valid before NWR High (No Wait States) ⁽¹⁾	C = 0 pF	t _{CH} - 0.9		ns
		C _{DATA} derating	-0.066		ns/pF
		C _{NWR} derating	0.053		ns/pF
EBI ₁₇	Data Out Valid before NWR High (Wait States) ⁽¹⁾	C = 0 pF	n x t _{CP} - 0.8 ⁽²⁾		ns
		C _{DATA} derating	-0.066		ns/pF
		C _{NWR} derating	0.053		ns/pF
EBI ₁₈	Data Out Valid after NWR High		2.1		ns
EBI ₁₉	NWR Minimum Pulse Width (No Wait States) ⁽¹⁾	C _{NWR} = 0 pF	t _{CH} + 0.4		ns
		C _{NWR} derating	-0.013		ns/pF
EBI ₂₀	NWR Minimum Pulse Width (Wait States) ⁽¹⁾	C _{NWR} = 0 pF	n x t _{CP} - 0.4 ⁽²⁾		ns
		C _{NWR} derating	-0.013		ns/pF

Notes: 1. The derating factor should not be applied to t_{CH} or t_{CP}
2. n = number of standard wait states inserted.

Table 12. EBI Read Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI ₂₁	MCKI Falling to NRD Active ⁽¹⁾	C _{NRD} = 0 pF	5.0	9.0	ns
		C _{NRD} derating	0.042	0.066	ns/pF
EBI ₂₂	MCKI Rising to NRD Active ⁽²⁾	C _{NRD} = 0 pF	4.1	8.6	ns
		C _{NRD} derating	0.042	0.066	ns/pF
EBI ₂₃	MCKI Falling to NRD Inactive ⁽¹⁾	C _{NRD} = 0 pF	5.2	9.4	ns
		C _{NRD} derating	0.034	0.053	ns/pF
EBI ₂₄	MCKI Falling to NRD Inactive ⁽²⁾	C _{NRD} = 0 pF	4.9	7.7	ns
		C _{NRD} derating	0.034	0.053	ns/pF
EBI ₂₅	D0 - D15 In Setup before MCKI Falling Edge ⁽⁵⁾		-0.3		ns
EBI ₂₆	D0 - D15 In Hold after MCKI Falling Edge ⁽⁵⁾		4.0		ns
EBI ₂₇	NRD High to NUB Change	C _{NUB} = 0 pF	4.1	8.4	ns
		C _{NUB} derating	0.034	0.066	ns/pF
EBI ₂₈	NRD High to NLB/A0 Change	C _{NLB} = 0 pF	3.3	5.2	ns
		C _{NLB} derating	0.042	0.066	ns/pF
EBI ₂₉	NRD High to A1 - A23 Change	C _{ADD} = 0 pF	3.2	7.1	ns
		C _{ADD} derating	0.042	0.066	ns/pF
EBI ₃₀	NRD High to Chip Select Inactive	C _{NCS} = 0 pF	3.6	6.9	ns
		C _{NCS} derating	0.034	0.066	ns/pF
EBI ₃₁	Data Setup before NRD High ⁽⁵⁾	C _{NRD} = 0 pF	9.0		ns
		C _{NRD} derating	0.053		ns/pF
EBI ₃₂	Data Hold after NRD High ⁽⁵⁾	C _{NRD} = 0 pF	-2.4		ns
		C _{NRD} derating	-0.034		ns/pF
EBI ₃₃	NRD Minimum Pulse Width ⁽¹⁾⁽³⁾	C _{NRD} = 0 pF	(n + 1) t _{CP} - 0.7 ⁽⁴⁾		ns
		C _{NRD} derating	-0.013		ns/pF
EBI ₃₄	NRD Minimum Pulse Width ⁽²⁾⁽³⁾	C _{NRD} = 0 pF	n x t _{CP} + (t _{CH} - 0.9) ⁽⁴⁾		ns
		C _{NRD} derating	-0.013		ns/pF

- Notes:
1. Early Read Protocol.
 2. Standard Read Protocol.
 3. The derating factor should not be applied to t_{CH} or t_{CP}.
 4. n = number of standard wait states inserted.
 5. Only one of these two timings needs to be met.

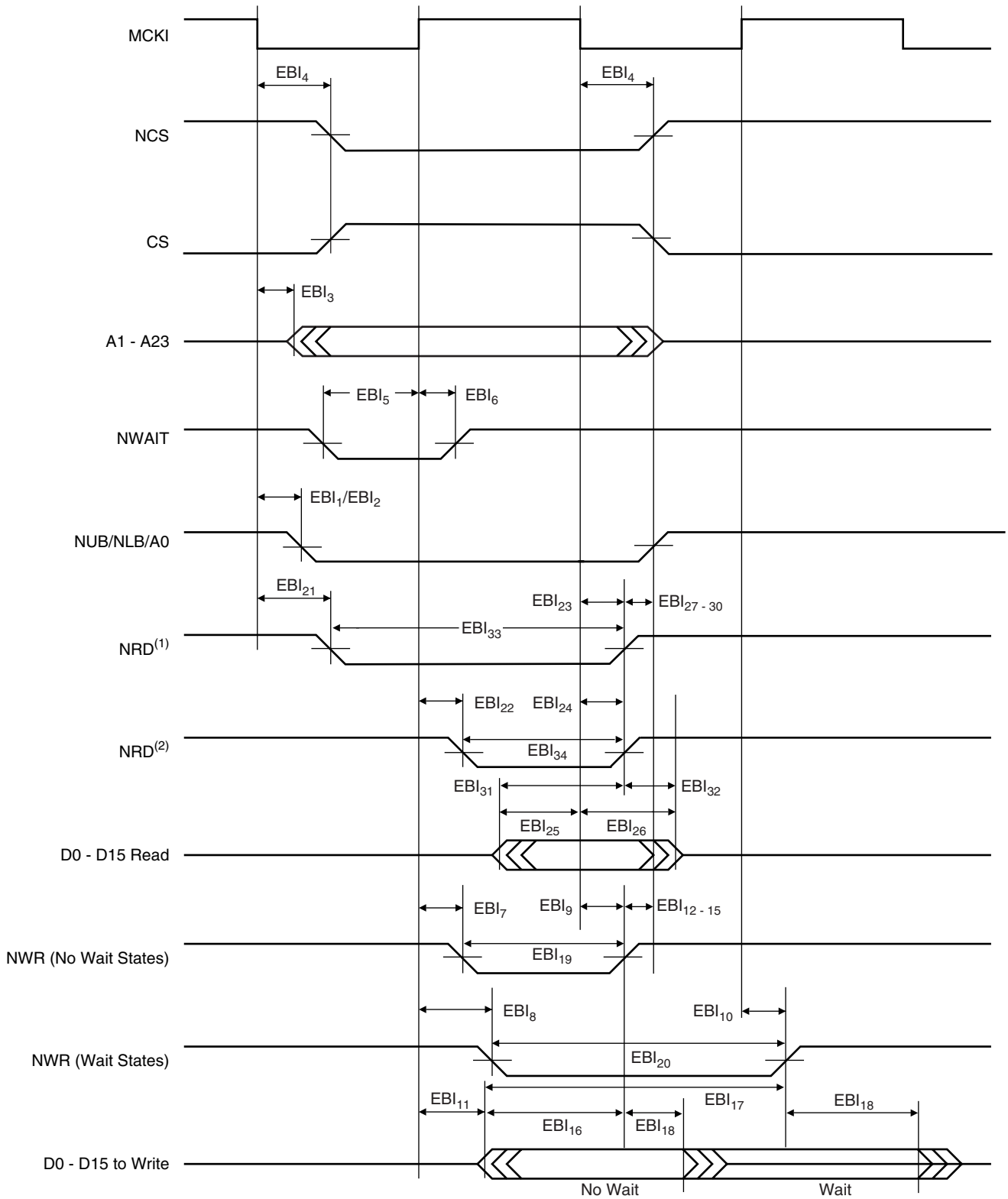
Table 13. EBI Read and Write Control Signals. Capacitance Limitation

Symbol	Parameter	Conditions	Min	Max	Units
$T_{CPLNRD}^{(1)}$	Master Clock Low Due to NRD Capacitance	$C_{NRD} = 0 \text{ pF}$	10.8		ns
		C_{NRD} derating	0.053		ns/pF
$T_{CPLNWR}^{(2)}$	Master CLock Low Due to NWR Capacitance	$C_{NWR} = 0 \text{ pF}$	8.6		ns
		C_{NWR} derating	0.053		ns/pF

Notes:

1. If this condition is not met, the action depends on the read protocol intended for use.
 - Early Read Protocol: Programing an additional t_{DF} (Data Float Output Time) cycle.
 - Standard Read Protocol: Programming an additional t_{DF} Cycle and an additional wait state.
2. Applicable only for chip select programmed with 0 wait state. If this condition is not met, at least one wait state must be programmed.

Figure 5. EBI Signals Relative to MCKI



- Notes:
1. Early Read Protocol.
 2. Standard Read Protocol.

Peripheral Signals

USART Signals

The inputs have to meet the minimum pulse width and period constraints shown in Table 14 and Table 15, and represented in Figure 6.

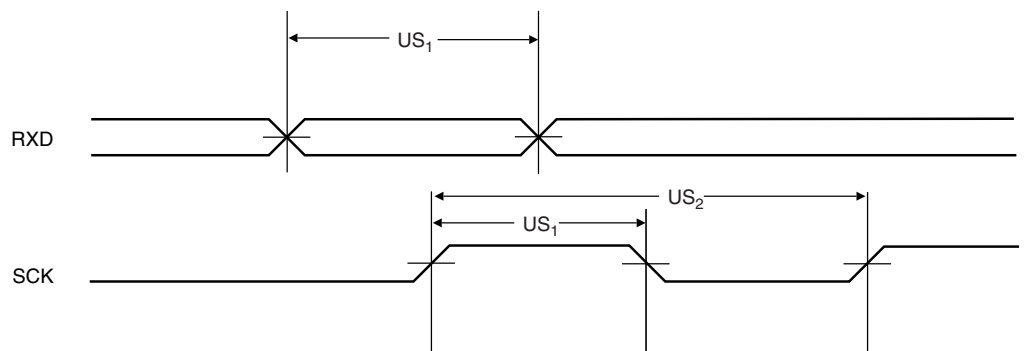
Table 14. USART Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
US ₁	SCK/RXD Minimum Pulse Width	$5(t_{CP}/2)$	ns

Table 15. USART Minimum Input Period

Symbol	Parameter	Min Input Period	Units
US ₂	SCK Minimum Input Period	$9(t_{CP}/2)$	ns

Figure 6. USART Signals



Timer/Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CP})$ in Waveform Event Detection mode and $4(t_{CP})$ in Waveform Total-count Detection mode. The inputs have to meet the minimum pulse width and minimum input period shown in Table 16 and Table 17, and as represented in Figure 7.

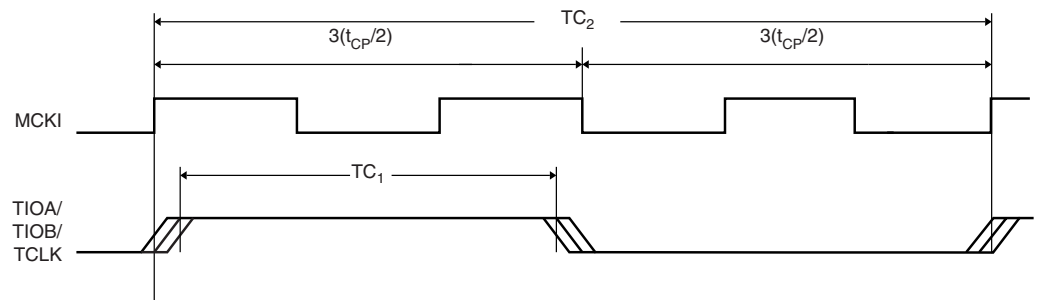
Table 16. Timer Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
TC ₁	TCLK/TIOA/TIOB Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 17. Timer Input Minimum Period

Symbol	Parameter	Min Input Period	Units
TC ₂	TCLK/TIOA/TIOB Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 7. Timer Input



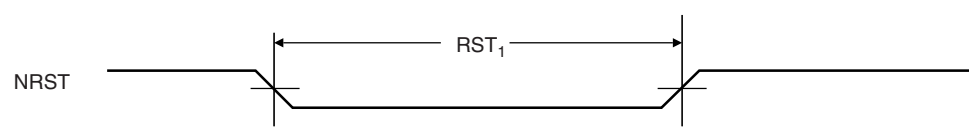
Reset Signals

A minimum pulse width is necessary, as shown in Table 18 and as represented in Figure 8.

Table 18. Reset Minimum Pulse Width

Symbol	Parameter	Min Pulse-width	Units
RST ₁	NRST Minimum Pulse Width	10(t _{CP})	ns

Figure 8. Reset Signal



Only the NRST rising edge is synchronized with MCKI. The falling edge is asynchronous.

Advanced Interrupt Controller Signals

Inputs have to meet the minimum pulse width and minimum input period shown in Table 19 and Table 20 and represented in Figure 9.

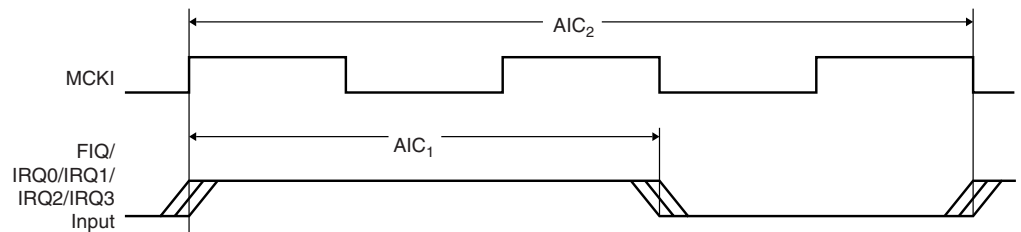
Table 19. AIC Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
AIC ₁	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 20. AIC Input Minimum Period

Symbol	Parameter	Min Input Period	Units
AIC ₂	AIC Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 9. AIC Signals



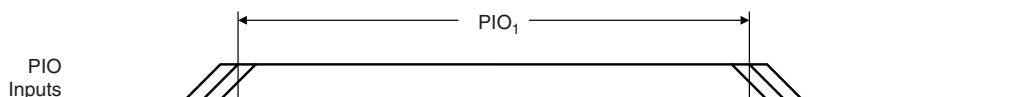
Parallel I/O Signals

The inputs have to meet the minimum pulse width shown in Table 21 and represented in Figure 10.

Table 21. PIO Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
PIO ₁	PIO Input Minimum Pulse Width	$3(t_{CP}/2)$	ns

Figure 10. PIO Signal

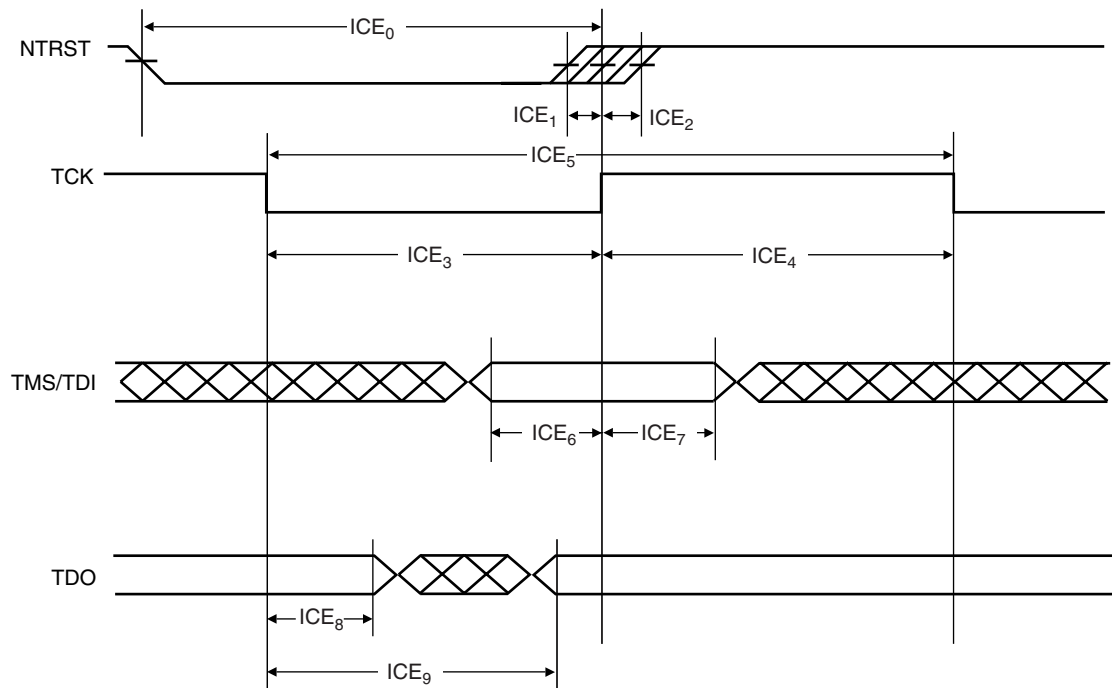


ICE Interface Signals

Table 22. ICE Interface Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
ICE ₀	NTRST Minimum Pulse Width		18.8		ns
ICE ₁	NTRST High Recovery to TCK High		1.2		ns
ICE ₂	NTRST High Removal from TCK High		-0.2		ns
ICE ₃	TCK Low Half-period		41.7		ns
ICE ₄	TCK High Half-period		40.9		ns
ICE ₅	TCK Period		82.5		ns
ICE ₆	TDI, TMS Setup before TCK High		0.5		ns
ICE ₇	TDI, TMS Hold after TCK High		0.6		ns
ICE ₈	TDO Hold Time	C _{TDO} = 0 pF	5.2		ns
		C _{TDO} derating	0		ns/pF
ICE ₉	TCK Low to TDO Valid	C _{TDO} = 0 pF		10.2	ns
		C _{TDO} derating		0.063	ns/pF

Figure 11. ICE Interface Signal





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Page: 1 “Features” “Fully Static Operation: 0 Hz to 40 MHz Internal Frequency Range at 3.0 V, 85°C” frequency and range modified

Page: 4 “Reliability Data” paragraph modified and new table inserted. “Table 6 Reliability Data”

Page: 6 “Timing Results” Cross reference added to C_{SIGNAL} part of equation.

Page: 8 Table 7. Master Clock Waveform Parameters. Values have been changed for Oscillator Frequency and Oscillator Period. Some master clock parameters deleted.

Page: 10 Table 10. General-purpose EBI Signals. EBI₄, Conditions are changed.

Page: 13 New table inserted. Table 13. Read and Write Control Signals. Capacitance Limitation. This table adds understanding to EBI Signals Relative to MCK.

Version C **Publication Date:** 19-Nov-2004

Page 8 Changes in Table 7: new figures for t_{CH} and t_{CL} , removed references to t_r and t_f . Updated Figure 3 on page 8.



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