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MxL83233

EVK User Manual

Revision History

Document No.	Release Date	Change Description
040UMR00	December 10, 2025	Initial release.

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Introduction

This document is used for the evaluation kit (EVK) of the MxL83233 device. This EVK provides a platform to evaluate the features and performance of the MxL83233.

MxL83233 EVK Setup and Pre-Configuration

- The MxL83233 EVK is pre-configured for driver enable with $DE/REb = V_L$.
- Apply $V_{CC} = 3.3V$ to $5.0V$ bench power supply to header J1 at pin 3 (J1.3) or pin 4 (J1.4).
- Apply $V_L = 1.8V$ to V_{CC} (V_L input voltage must be less than or equal to V_{CC}), and connect J6.1 and J6.2 to $V_L = V_{CC}$ or connect the bench power supply to header J22 at pin 3 (J22.3).
- Apply GND from the V_{CC} connection to J1 at pin 1 (J1.1) and GND from the V_L connection to J22 at pin 1 (J22.1).
- J21 and J23 are GND probe points on the EVK.
- When the power V_{CC} is applied at header J1, the LED at location D1 is ON.
- Apply differential signals at J27. Monitor the receiver outputs at J8.
- Apply input signals at J16. Monitor the differential signal output at J27.
- [Figure 3](#) on page 3 shows the schematic of the EVK.

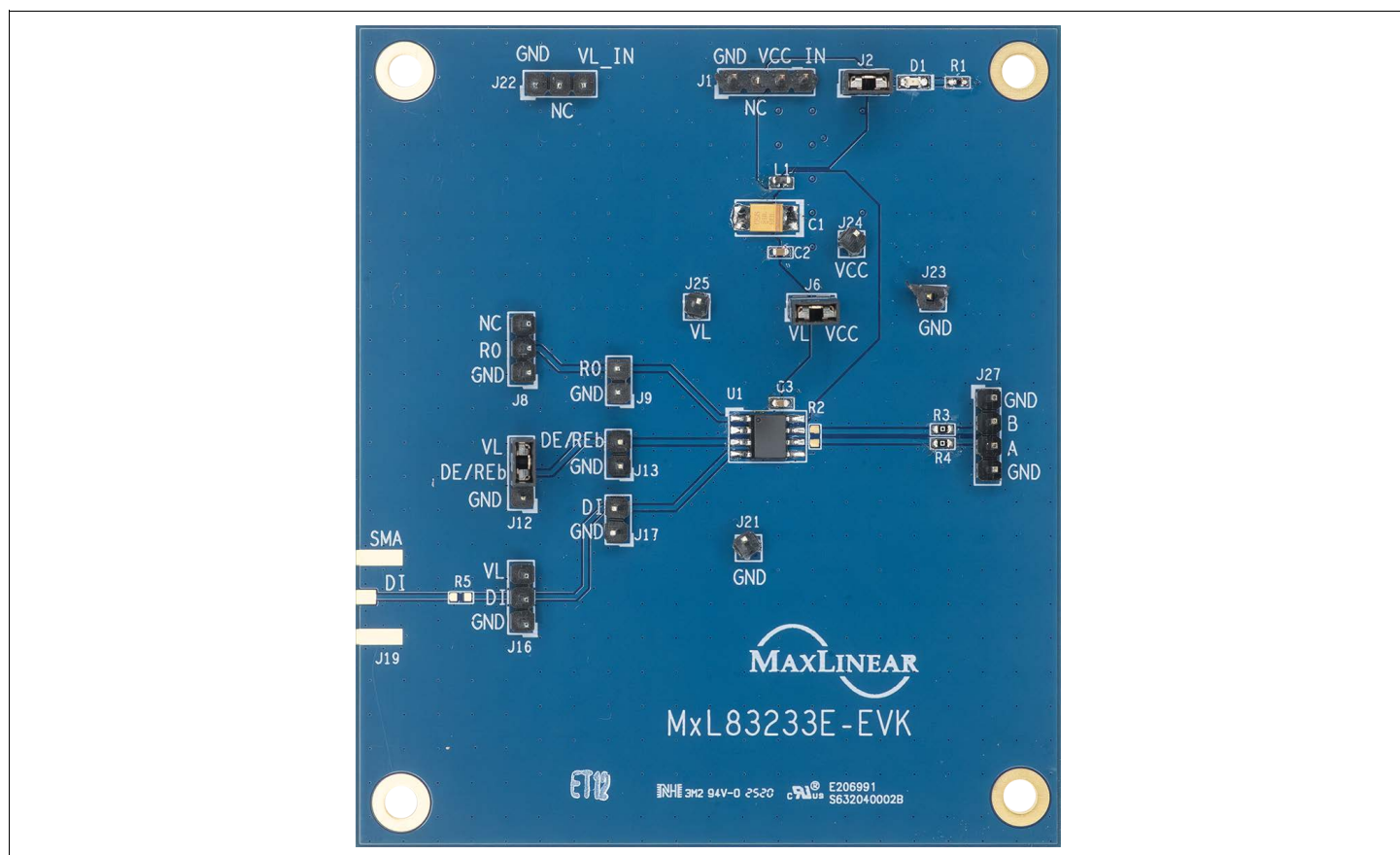


Figure 1: Top View of the MxL83233 EVK

Ordering Information

The following table lists the ordering part number for the evaluation kit.

Table 1: EVK Ordering Part Number

EVK Part Number	Description
MXL83233E-ADA-EVK-1	MxL83233 Evaluation Kit

Evaluation Kit Overview

The following figure shows the pin configuration and logic diagram of the MxL83233 device.

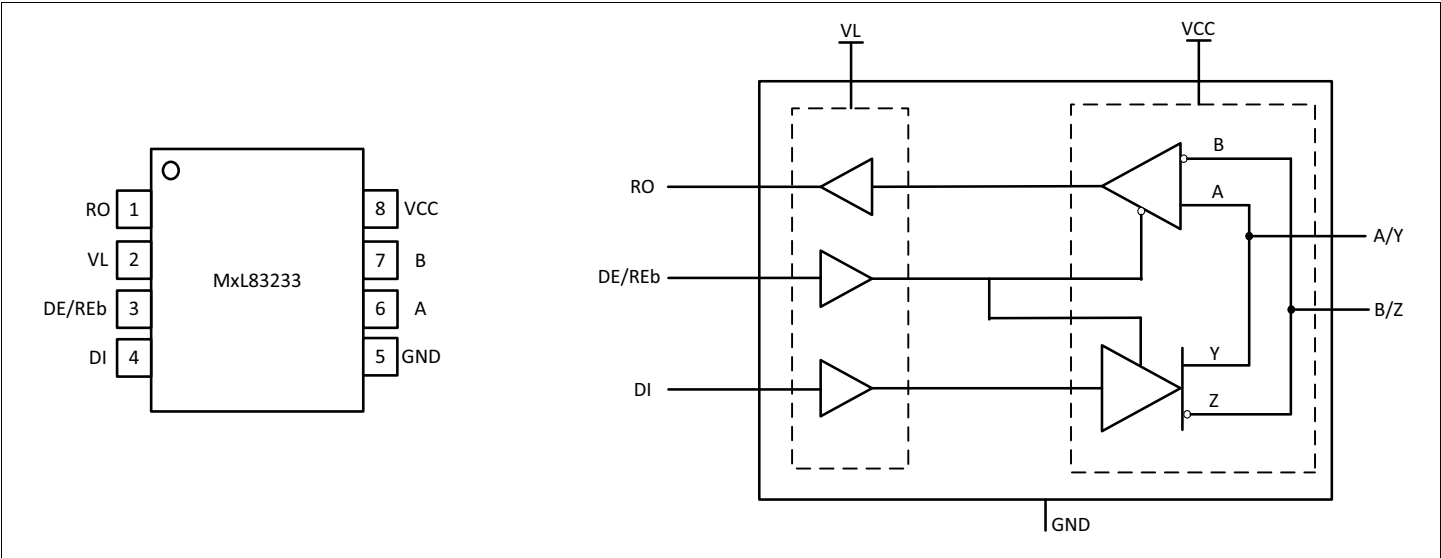


Figure 2: MxL83233 Half-Duplex Transceiver

EVK Schematic

The following figure shows the EVK schematic design of the MxL83233 device.

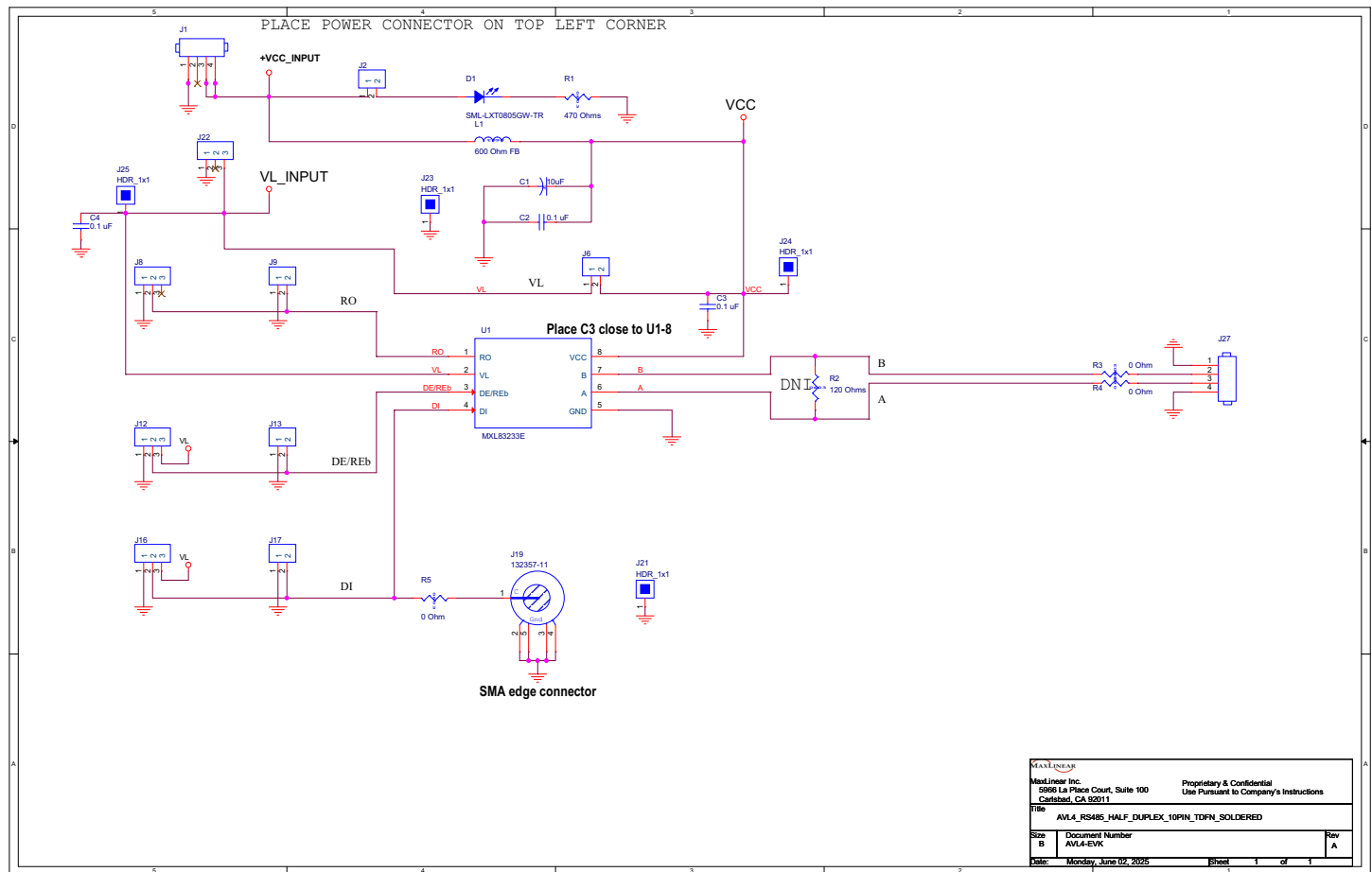


Figure 3: MxL83233 EVK Schematic

EVK PCB Layers (NSOIC8 Package)

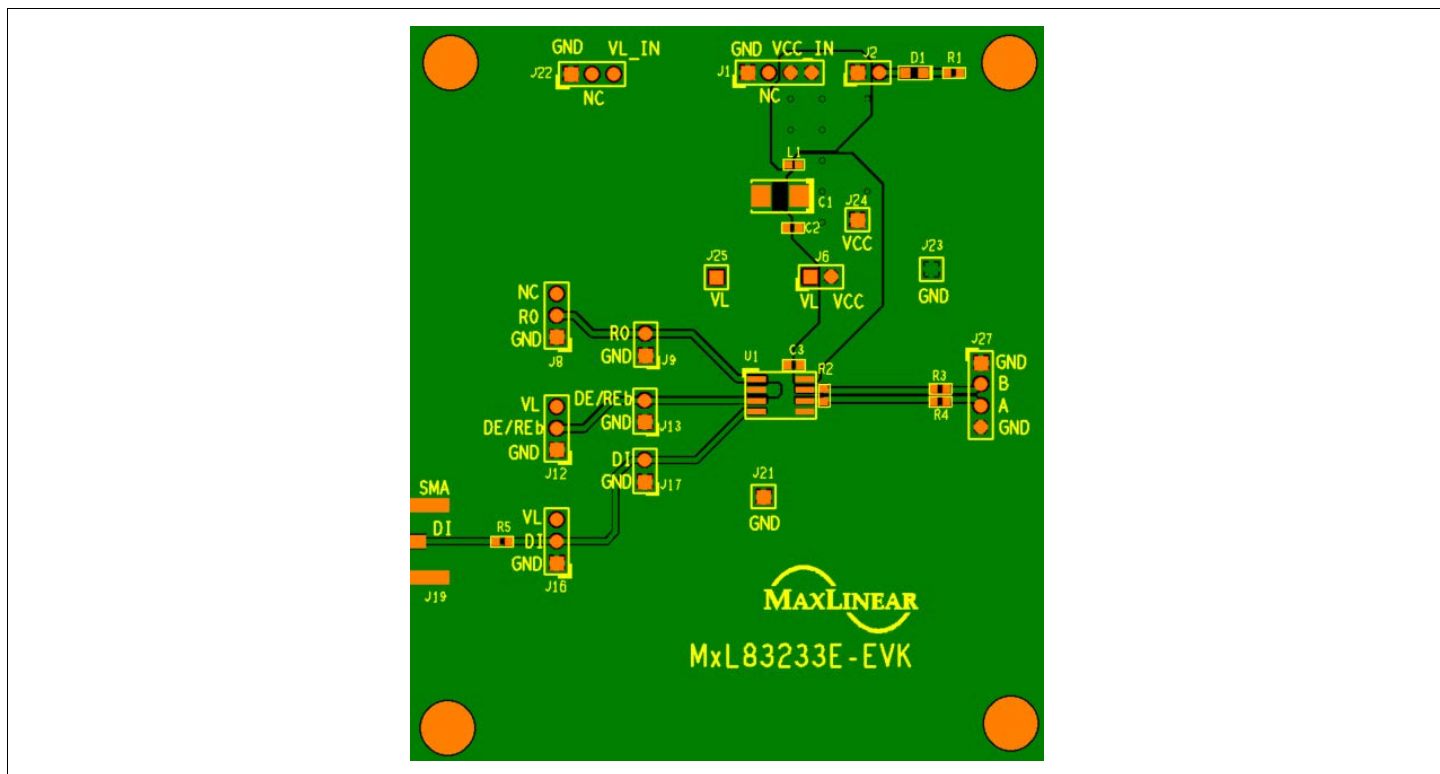


Figure 4: EVK PCB Layer 1—Top View

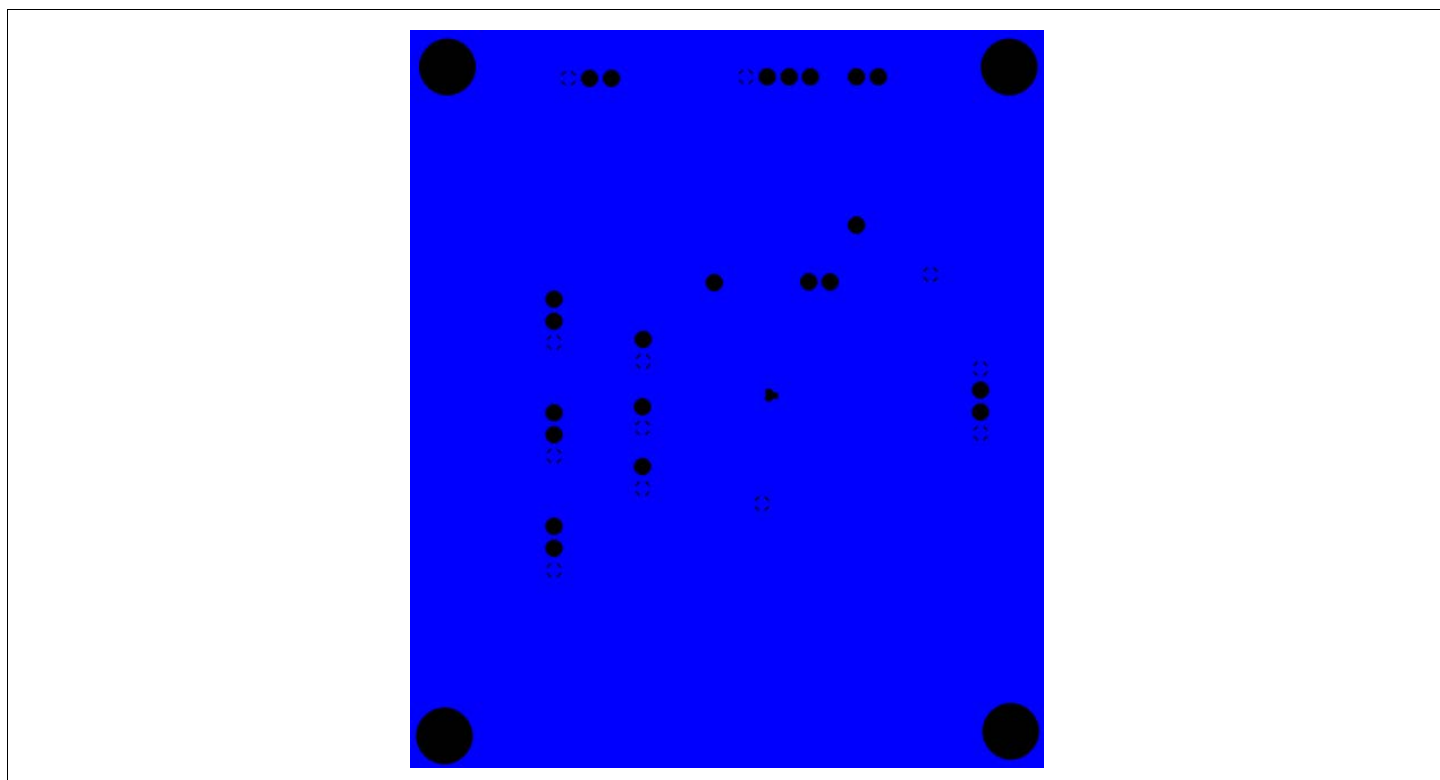


Figure 5: EVK PCB Layer 2—GND Plane

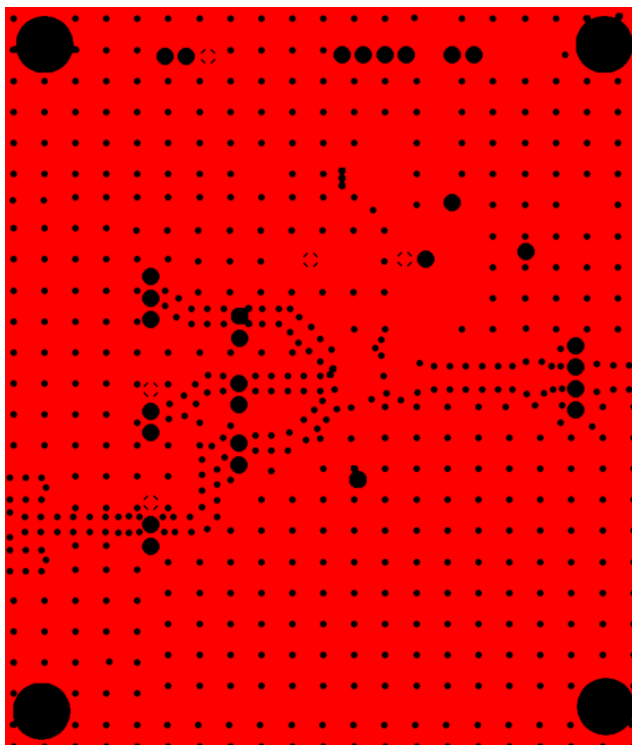


Figure 6: EVK PCB Layer 3—Power Plane

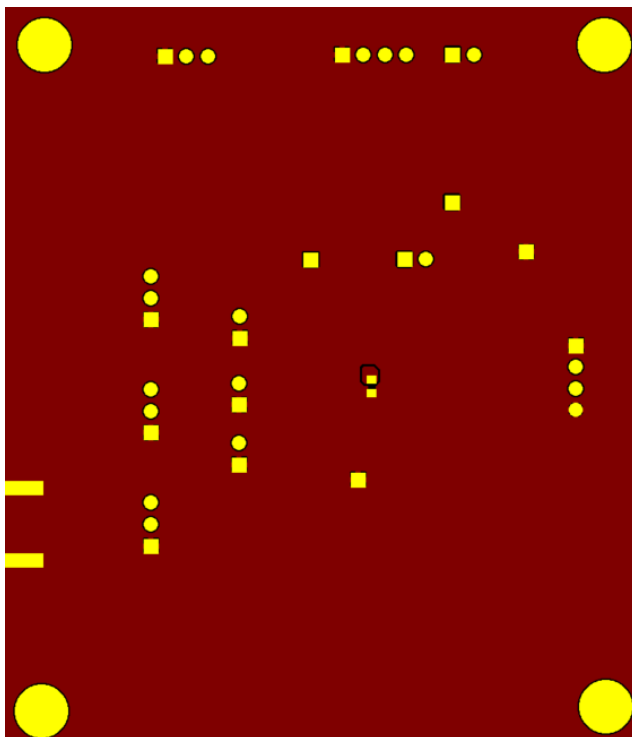


Figure 7: EVK PCB Layer 4—Bottom View

EVK Bill of Materials

Table 2: EVK Bill of Materials

Item	Quantity	Reference	Manufacturer	Part
1	1	C1	AVX	478-5235-1-ND, TANTALUM, 10 μ F, 16V, 500m Ω , 2312
2	3	C2, C3, C4	KEMET	C0603C104K5RAC7081, 0.1UF 50V, 0603 X7R
3	1	D1	Lumex	67-1553-1-ND LED GREEN DEFUSED SMD, 0805
4	2	J1, J27	Würth Electronics	613 004 111 21 CONN. HEADER 1X4, 2.54mm, 4PIN
5	5	J2, J6, J9, J13, J17	Würth Electronics	620 002 111 21 CONN. HEADER, 1X2, 2mm, 2PIN
6	4	J8, J12, J16, J22	Würth Electronics	613 003 111 21 CONN. HEADER 1X3, 2.54mm, 3PIN
7	4	J21, J23, J24, J25	Würth Electronics	620 001 111 21 CONN. HEADER, 1X1, 2mm, 1PIN
8	1	J19	Amphenol Connex	132357-11 CONN. SMA RCPT, 50 Ω
9	1	L1	Murata	490-1023-2-ND FB, Chip 600 Ω 25% 100MHz Ferrite 200mA 0603
10	1	R1	Panasonic Electronic Components	ERJ-3EKF4700V RES SMD, 470 Ω , 1%, 1/10W, 0603
11	1	R2	Panasonic Electronic Components	ERJ-H3EF1200V RES SMD, 120 Ω , 1%, 1/8W, 0603
12	3	R3, R4, R5	Panasonic Electronic Components	ERJ-3GEY0R00V RERS JUMPER, 0 Ω , SMD, 1/10W, 0603
13	1	U1	MaxLinear	MXL83233 NSOIC8

EVK Setup and Configurations

The following table lists the power header pin descriptions of the MxL83233.

Table 3: EVK Power Header Pin Description

Header	J1-Pin 1	J1-Pin 2	J1-Pin 3	J1-Pin 4
J1 	GND	NC	V_{CC}^1	V_{CC}^1
J22 	GND	NC	V_L^2	-

1. V_{CC} = 3.0V to 5.5V.

2. The V_L input ranges from 1.8V to V_{CC} supply for logic signal interface. The V_L input voltage must be less than or equal to V_{CC} .

The following table lists the header pin factory settings and descriptions of the MxL83233. For a complete view of the MxL83233 EVK, see [Figure 1](#) on page 1.

Table 4: EVK Header Pin Description and Default Settings

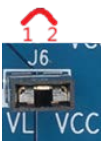
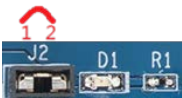
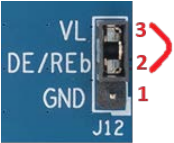
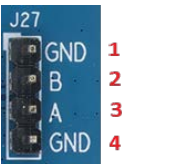
Header	Factory Setting	Description
J6 	Jumper 1-2	Power supply $V_L = V_{CC}$.
R2	Not stuff	Receiver termination resistor. Optional, not stuff by default.
J2 	Jumper 1-2	Enables power LED.
J8 	Header 3 pins	■ J8.1: GND. ■ J8.2: Receiver output (RO). ■ J8.3: NC.
J9 	Header 2 pins	■ J9.1: GND. ■ J9.2: RO (test point).

Table 4: EVK Header Pin Description and Default Settings (Continued)

Header	Factory Setting	Description
J12 	Jumper 2-3	Enables driver, DE/REb = V_L .
J13 	Header 2 pins	■ J13.1: GND. ■ J13.2: DE/REb (test point).
J16 	Header 3 pins	■ J16.1: GND. ■ J16.2: Driver input (DI). ■ J16.3: V_L.
J17 	Header 2 pins	■ J17.1: GND ■ J17.2: DI (test point).
J27 	Header 4 pins	■ J27.1: GND. ■ J27.2: B inverting input. ■ J27.3: A non-inverting input. ■ J27.4: GND.
J21 	Header 1 pin	■ J21.1: GND.
J23 	Header 1 pin	■ J23.1: GND.
J24 	Header 1 pin	■ J24.1: V_{CC} (test point).
J25 	Header 1 pin	■ J25.1: V_L (test point).

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