19-3017; Rev 1; 5/05

MAXIM

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

General Description

The MAX8553 is a 4.5V to 28V input-voltage, synchronous step-down controller that provides a complete power-management solution for DDR memory. The MAX8553 generates 1/2 V_{REFIN} voltage for VTT and VTTR. The VTT and VTTR tracking voltages are maintained within 1% of 1/2 V_{REFIN}. The MAX8554 is a 4.5V to 28V input voltage, nontracking step-down controller with a low 0.6V feedback threshold voltage. The MAX8553/MAX8554 use Maxim's proprietary Quick-PWM™ architecture for fast transient response and operate with selectable pseudo-fixed frequencies. Both controllers can operate without an external bias supply.

The controllers operate in synchronous-rectification mode to ensure balanced current sourcing and sinking capability of up to 25A. The MAX8553/MAX8554 also provide up to 95% efficiency, making them ideal for server and point-of-load applications. Additionally, a low 5µA shutdown current allows for longer battery life in notebook applications. Lossless current monitoring is achieved by monitoring the low-side MOSFET's drain-to-source voltage. The MAX8553/MAX8554 have an adjustable foldback current limit to withstand a continuous output overload and short circuit. Digital soft-start provides control of inrush current during power-up. Overvoltage protection shuts the converter down and discharges the output capacitor. The MAX8553/MAX8554 come in space-saving 16-pin QSOP packages.

Applications

Wide-Input Power Supplies

Servers and Storage Applications

ASIC and CPU Core Voltages

Notebook and LCD-PC Power Supplies

DDR I and DDR II Memory Power Supplies

AGTL Bus Termination Supplies

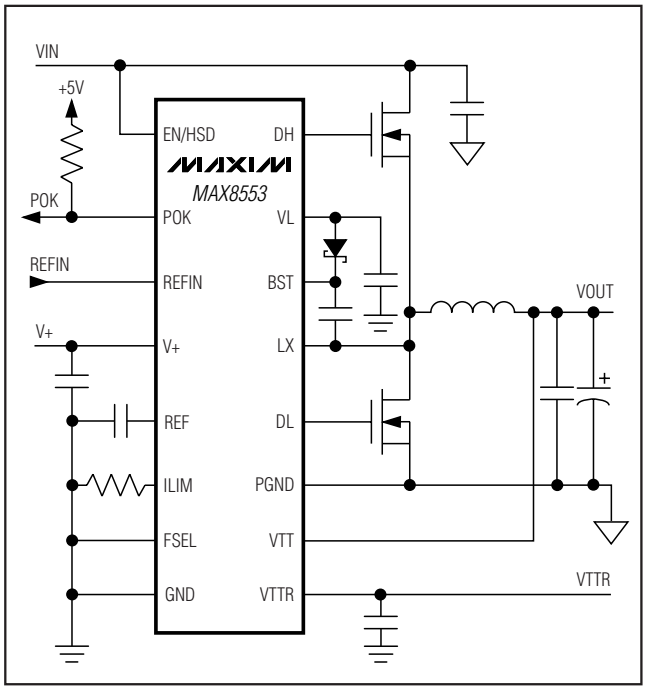
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8553EEE	-40°C to +85°C	16 QSOP
MAX8554EEE	-40°C to +85°C	16 QSOP

Features

- ♦ **Up to 25A Output-Current Capability**
- ♦ **Quick-PWM Control for Fast Loop Response**
- ♦ **Up to 95% Efficiency**
- ♦ **4.5V to 28V Input Voltage Range**
- ♦ **No External Bias Supply Required**
- ♦ **0 to 3.6V Input REFIN Range (MAX8553)**
- ♦ **Automatically Sets VTT and VTTR to within ±1% of 1/2 V_{REFIN}- (MAX8553)**
- ♦ **Low 0.6V Feedback Threshold (MAX8554)**
- ♦ **200kHz/300kHz/400kHz/550kHz Selectable Switching Frequencies**
- ♦ **Adjustable Foldback Current Limit**
- ♦ **Overvoltage Protection**
- ♦ **Digital Soft-Start**

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

ABSOLUTE MAXIMUM RATINGS

V+, EN/HSD, EN, HSD to GND .....-0.3V to +30V
PGND to GND .....-0.3V to +0.3V
VTT, REFIN, POK, OUT, FB, VL to GND .....-0.3V to +6V
REF, VTTR, DL, ILIM, FSEL to GND .....-0.3V to (V_{VL} + 0.3V)
LX to PGND .....-2V to +30V
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to +6V
LX to BST .....-6V to +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derated 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0V, ILIM = VL, PGND = LX = GND, BST = VL, **T_A = 0°C to +85°C.** Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	VL not connected to V+	6		28	V
V+ Input Voltage Range	VL connected to V+	4.5		5.5	V
EN/HSD Input Voltage Range	MAX8553 enabled	1.5		28.0	V
EN Input Voltage Range	MAX8554 enabled	1.5		28.0	V
EN Input Current			2	3	µA
HSD Input Voltage Range	MAX8554 enabled	1.5		28.0	V
HSD Input Current			20	40	µA
REFIN Input Voltage Range		0		3.6	V
V+ Supply Current (MAX8553)	V_{VTT} = +1.35V		0.8	1.2	mA
V+ Supply Current (MAX8554)	V_{FB} = 630mV		0.62	0.90	mA
REFIN Supply Current			125	250	µA
EN/HSD Supply Current			5	10	µA
VL Supply Current	V_{VL} = V_{V+} = 5.5V, V_{VTT} = +1.35V		0.8	1.2	mA
V+ Shutdown Supply Current	EN/HSD = GND		3	5	µA
REFIN Shutdown Supply Current	EN/HSD = GND			1	µA
VL Shutdown Supply Current	V_{VL} = V_{V+} = +5.5V, $V_{EN/HSD}$ = 0V		5	12	µA
VL Undervoltage-Lockout Threshold	Rising edge, typical hysteresis = 40mV	4.05	4.25	4.40	V
VTT					
VTT Input Bias Current	V_{VTT} = +1.25V	-0.15		0	µA
VTT Feedback Voltage Range		0		1.8	V
VTT Feedback Voltage Accuracy	V_{REFIN} = $V_{EN/HSD}$ = +1.8V	49.5	50	50.5	% V_{REFIN}
	V_{REFIN} = $V_{EN/HSD}$ = +3.6V	49.5	50	50.5	
FB Input Bias Current	MAX8554, V_{FB} = +600mV	-0.15		0	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0V, ILIM = VL, PGND = LX = GND, BST = VL, **T_A = 0°C to +85°C.** Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB Regulation Voltage	MAX8554, V_{OUT} = +2.5V, FSEL unconnected		0.598	0.607	0.616	V
Output Adjust Range	MAX8554 (Note 1)		0.6		3.5	V
VTT Line Regulation	$V_{EN/HSD}$ ±10%, V_{VTT} = +1.25V, I_{OUT} = 0A			±0.325		%
FB Line Regulation	MAX8554, V_{HSD} ±10%, V_{OUT} = +2.5V, I_{OUT} = 0A, FSEL unconnected			±0.325		%
VTT Load Regulation	0 < I_{OUT} < +7A, V_{VTT} = +1.25V			0.2		%
FB Load Regulation	MAX8554, 0 < I_{OUT} < +7A, V_{OUT} = +2.5V, FSEL unconnected			0.2		%
REFERENCE						
Reference Output Voltage	V_{V+} = V_{VL} = +4.5 to +5.5V, I_{REF} = 0		1.97	2.00	2.03	V
Reference Load Regulation	V_{V+} = V_{VL} = +5V, I_{REF} = 0 to 50µA				10	mV
Reference UVLO	V_{V+} = V_{VL} = +5V, reference rising, hysteresis = 27mV		1.5	1.6	1.7	V
VTTR						
VTTR Output Voltage Range			0		1.8	V
VTTR Output Accuracy	I_{VTTR} = -5mA to +5mA		49.5	50	50.5	% V_{REFIN}
	I_{VTTR} = -25mA to +25mA, V_{REFIN} = +1.8V		49	50	51	
	I_{VTTR} = -25mA to +25mA, V_{REFIN} = +3.6V		49.5	50	50.5	
Thermal Shutdown	Rising temperature, typical hysteresis = 15°C			+160		°C
SOFT-START						
ILIM Ramp Period	Ramps the ILIM trip threshold from 20% to 100% in 20% increments		0.8	1.7	3.0	ms
Output Predischarge Period	Rising edge of EN/HSD to the start of internal digital soft-start		0.8	1.7	3.0	ms
OSCILLATOR						
Oscillator Frequency	FSEL = VL			200		kHz
	FSEL = unconnected			300		
	FSEL = REF			400		
	FSEL = GND			550		
On-Time	MAX8553, V_{VTT} = +1.25V (Note 2)	FSEL = VL	2.18	2.5	2.83	µs
		FSEL unconnected	1.45	1.67	1.89	
		FSEL = REF	1.09	1.25	1.41	
		FSEL = GND	0.82	0.91	1.00	
On-Time	MAX8554, V_{OUT} = +2.5V (Note 2)	FSEL = VL	0.89	1.02	1.16	µs
		FSEL unconnected	0.61	0.71	0.80	
		FSEL = REF	0.43	0.49	0.56	
		FSEL = GND	0.33	0.37	0.41	
Off-Time	(Note 2)			350	400	ns

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0V, ILIM = VL, PGND = LX = GND, BST = VL, **T_A = 0°C to +85°C.** Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT					
Current-Limit Threshold (Positive Direction)	LX to PGND, ILIM = VL	80	100	115	mV
	LX to PGND, R_{ILIM} = 100kΩ	35	50	65	
	LX to PGND, R_{ILIM} = 400kΩ	160	200	230	
Current-Limit Threshold (Negative Direction)	LX to PGND, ILIM = VL, with respect to positive current-limit threshold	-130	-110	-90	%
ILIM Input Current			5		µA
FAULT DETECTION					
Overvoltage Threshold	MAX8553 (V_{REFIN} > +1V)	57	60	63	% V_{REFIN}
	MAX8553 (V_{REFIN} ≤ +1V)	0.576	0.600	0.624	V
	MAX8554	0.696	0.720	0.744	
VL REGULATOR					
Output Voltage	+6V < V_{V+} <+28V, 1mA < I_{VL} < 35mA	4.80	5.0	5.33	V
Line Regulation	+6V < V_{V+} < +28V, I_{VL} = 10mA		0.2		%
RMS Output Current				35	mA
Bypass Capacitor	ESR < 100mΩ	2.2			µF
DRIVER					
DH Gate-Driver On-Resistance	V_{BST} - V_{LX} = +5V		1.4	2.5	Ω
DL Gate-Driver On-Resistance (Source)	DL high state		1.6	3.0	Ω
DL Gate-Driver On-Resistance (Sink)	DL low state		0.75	1.25	Ω
Dead Time	DL rising		32		ns
	DL falling		30		
FSEL LOGIC					
Logic Input Current		-3		+3	µA
Logic Low (GND)				0.5	V
Logic REF Level	FSEL = REF	1.65		2.35	V
Logic Float Level	FSEL unconnected	3.15		3.85	V
Logic VL Level	FSEL = VL	V_{VL} - 0.4			V
EN/HSD OR EN LOGIC					
EN/HSD or EN Shutdown Current	Max $I_{EN/HSD}$ for $V_{EN/HSD}$ < +0.8V or V_{EN} < +0.8V	0.5		3.0	µA
Logic High	V_{VL} = V_{V+} = +4.5 to +5.5V, 100mV hysteresis	1.5			V
Logic Low	V_{VL} = V_{V+} = +4.5 to +5.5V			0.8	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0V, ILIM = VL, PGND = LX = GND, BST = VL, **T_A = 0°C to +85°C.** Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-OK OUTPUT					
Upper VTT and VTTR Threshold	MAX8553	55	56	57	% V_{REFIN}
Lower VTT and VTTR Threshold	MAX8553	43	44	45	% V_{REFIN}
Upper Threshold	MAX8554	0.646	0.672	0.698	V
Lower Threshold	MAX8554	0.504	0.528	0.552	V
POK Output Low Level	I_{SINK} = 2mA			0.4	V
POK Output High Leakage	V_{POK} = +5V			5	µA

ELECTRICAL CHARACTERISTICS

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL, **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
V+ Input Voltage Range	VL not connected to V+	6	28	V
V+ Input Voltage Range	VL connected to V+	4.5	5.5	V
EN/HSD Input Voltage Range	MAX8553 enabled	1.5	28.0	V
EN Input Voltage Range	MAX8554 enabled	1.5	28.0	V
EN Input Current			3	µA
HSD Input Voltage Range	MAX8554 enabled	1.5	28.0	V
HSD Input Current			40	µA
REFIN Input Voltage Range		0	3.6	V
V+ Supply Current (MAX8553)	V_{VTT} = +1.35V		1.2	mA
V+ Supply Current (MAX8554)	V_{FB} = 630mV		0.90	mA
REFIN Supply Current			250	µA
EN/HSD Supply Current			10	µA
VL Supply Current	V_{VL} = V_{V+} = 5.5V, V_{VTT} = +1.35V		1.2	mA
V+ Shutdown Supply Current	EN/HSD = GND		5	µA
REFIN Shutdown Supply Current	EN/HSD = GND		1	µA
VL Shutdown Supply Current	V_{VL} = V_{V+} = +5.5V, $V_{EN/HSD}$ = 0V		12	µA
VL Undervoltage-Lockout Threshold	Rising edge, typical hysteresis = 40mV	4.05	4.40	V
VTT				
VTT Input Bias Current	V_{VTT} = +1.25V	-0.2	0	µA
VTT Feedback Voltage Range		0	1.8	V
VTT Feedback Voltage Accuracy	V_{REFIN} = $V_{EN/HSD}$ = +1.8V	49.5	50.5	% V_{REFIN}
	V_{REFIN} = $V_{EN/HSD}$ = +3.6V	49.5	50.5	
FB Input Bias Current	MAX8554, V_{FB} = +600mV	-0.2	0	µA
FB Regulation Voltage	MAX8554, V_{OUT} = +2.5V, FSEL unconnected	0.598	0.616	V
Output Adjust Range	MAX8554 (Note 1)	0.6	3.5	V

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL, **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
REFERENCE					
Reference Output Voltage	V_{V+} = V_{VL} = +4.5 to +5.5V, I_{REF} = 0		1.97	2.03	V
Reference Load Regulation	V_{V+} = V_{VL} = +5V, I_{REF} = 0 to 50µA			10	mV
Reference UVLO	V_{V+} = V_{VL} = +5V, reference rising, hysteresis = 27mV		1.5	1.7	V
VTTR					
VTTR Output Voltage Range			0	1.8	V
VTTR Output Accuracy	I_{VTTR} = -5mA to +5mA		49.5	50.5	% V_{REFIN}
	I_{VTTR} = -25mA to +25mA, V_{REFIN} = +1.8V		49	51	
	I_{VTTR} = -25mA to +25mA, V_{REFIN} = +3.6V		49.5	50.5	
SOFT-START					
ILIM Ramp Period	Ramps the ILIM trip threshold from 20% to 100% in 20% increments		0.8	3.0	ms
Output Predischarge Period	Rising edge of EN/HSD to the start of internal digital soft-start		0.8	3.0	ms
OSCILLATOR					
On-Time	MAX8553, V_{VTT} = +1.25V (Note 2)	FSEL = VL	2.18	2.83	µs
		FSEL unconnected	1.45	1.89	
		FSEL = REF	1.09	1.41	
		FSEL = GND	0.82	1.00	
On-Time	MAX8554, V_{OUT} = +2.5V (Note 2)	FSEL = VL	0.89	1.16	µs
		FSEL unconnected	0.61	0.80	
		FSEL = REF	0.43	0.56	
		FSEL = GND	0.33	0.41	
Off-Time	(Note 2)			420	ns
CURRENT LIMIT					
Current-Limit Threshold (Positive Direction)	LX to PGND, ILIM = VL		80	115	mV
	LX to PGND, R_{ILIM} = 100kΩ		30	65	
	LX to PGND, R_{ILIM} = 400kΩ		150	230	
Current-Limit Threshold (Negative Direction)	LX to PGND, ILIM = VL, with respect to positive current-limit threshold		-130	-90	%
ILIM Input Current					µA
FAULT DETECTION					
Overvoltage Threshold	MAX8553 (V_{REFIN} > +1V)		57	63	%
	MAX8553 (V_{REFIN} ≤ +1V)		0.576	0.624	V
	MAX8554		0.696	0.744	
VL REGULATOR					
Output Voltage	+6V < V_{V+} < +28V, 1mA < I_{VL} < 35mA		4.80	5.33	V
RMS Output Current				35	mA
Bypass Capacitor	ESR < 100mΩ		2.2		µF

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{HSD} = +12V, $V_{EN/HSD}$ = V_{REFIN} = +2.5V, V_{EN} = +5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL, **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 3)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
DRIVER				
DH Gate-Driver On-Resistance	V_{BST} - V_{LX} = +5V		2.5	Ω
DL Gate-Driver On-Resistance (Source)	DL high state		3.0	Ω
DL Gate-Driver On-Resistance (Sink)	DL low state		1.25	Ω
FSEL LOGIC				
Logic Input Current		-3	+3	µA
Logic Low (GND)			0.5	V
Logic REF Level	FSEL = REF	1.65	2.35	V
Logic Float Level	FSEL unconnected	3.15	3.85	V
Logic VL Level	FSEL = VL	V_{VL} - 0.4		V
EN/HSD OR EN LOGIC				
EN/HSD or EN Shutdown Current	Max $I_{EN/HSD}$ for $V_{EN/HSD}$ < +0.8V or V_{EN} < +0.8V	0.5	3.0	µA
Logic High	V_{VL} = V_{V+} = +4.5 to +5.5V, 100mV hysteresis	1.5		V
Logic Low	V_{VL} = V_{V+} = +4.5 to +5.5V		0.8	V
POWER-OK OUTPUT				
Upper VTT, and VTTR Threshold	MAX8553	55	57	% V_{REFIN}
Lower VTT, and VTTR Threshold	MAX8553	43	45	% V_{REFIN}
Upper Threshold	MAX8554	0.646	0.698	V
Lower Threshold	MAX8554	0.504	0.552	V
POK Output Low Level	I_{SINK} = 2mA		0.4	V
POK Output High Leakage	V_{POK} = +5V		5	µA

Note 1: Consult factory for applications that require higher than 3.5V output.

Note 2: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX forced to 0V, BST forced to 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

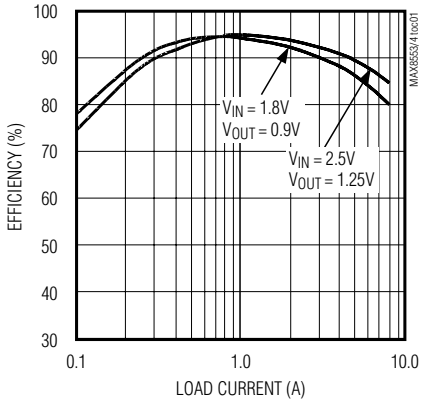
Note 3: Specifications to -40°C are guaranteed by design and are not production tested.

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

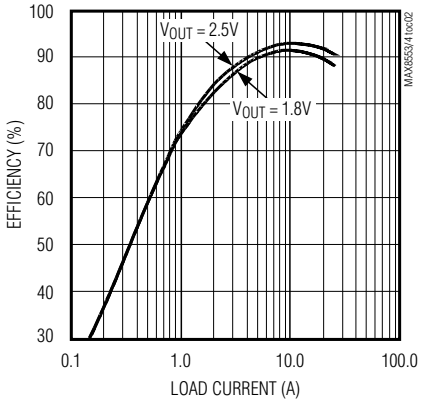
Typical Operating Characteristics

(V_{V+} = 12V, V_{OUT} = 1.8V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

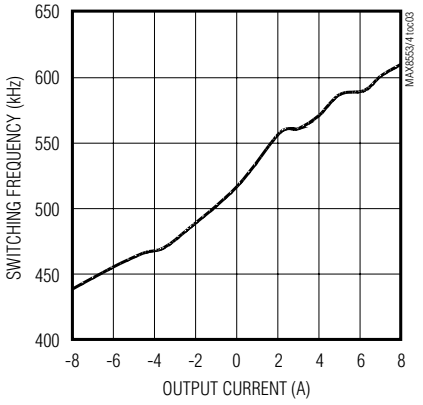
EFFICIENCY vs. LOAD CURRENT (CIRCUIT OF FIGURE 2)



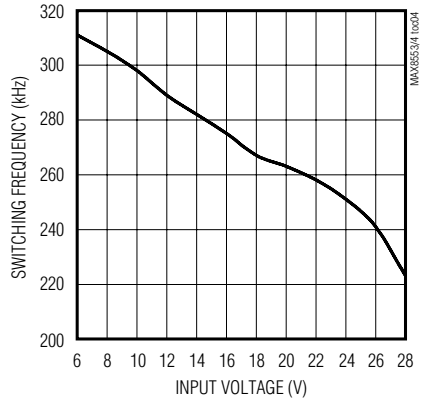
EFFICIENCY vs. LOAD CURRENT (CIRCUIT OF FIGURE 1)



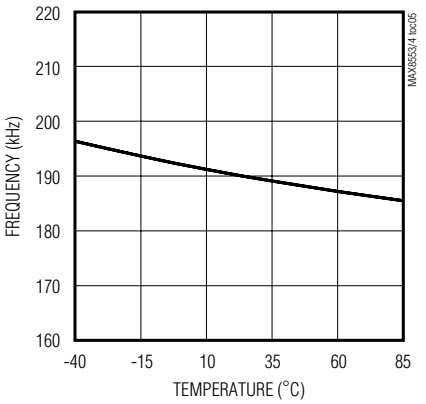
SWITCHING FREQUENCY vs. OUTPUT CURRENT (CIRCUIT OF FIGURE 2)



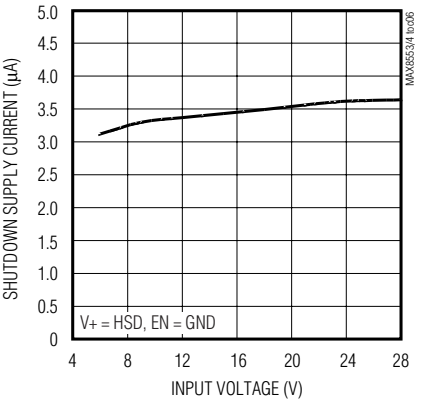
SWITCHING FREQUENCY vs. INPUT VOLTAGE (CIRCUIT OF FIGURE 3)



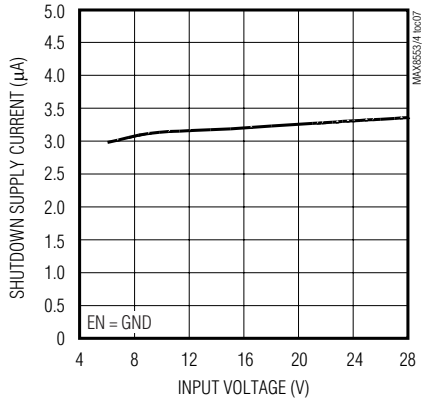
FREQUENCY vs. TEMPERATURE



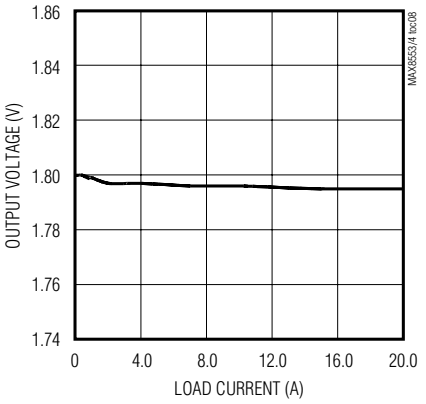
MAX8554 SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



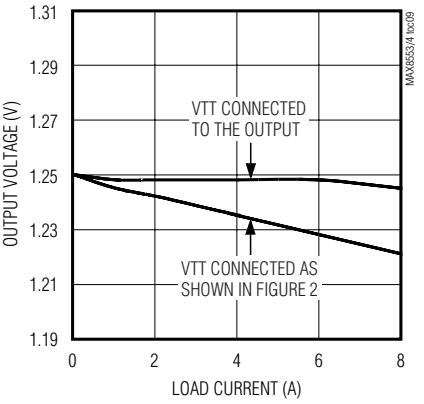
MAX8553 SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



LOAD REGULATION (CIRCUIT OF FIGURE 1)



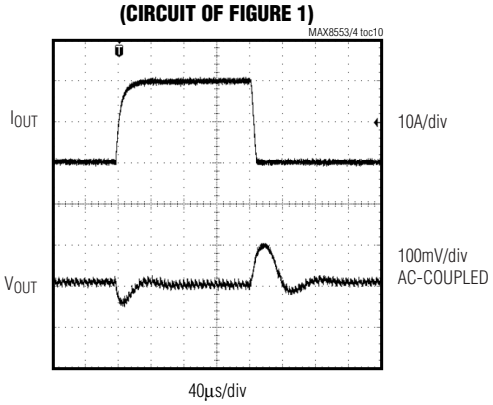
LOAD REGULATION (CIRCUIT OF FIGURE 2)



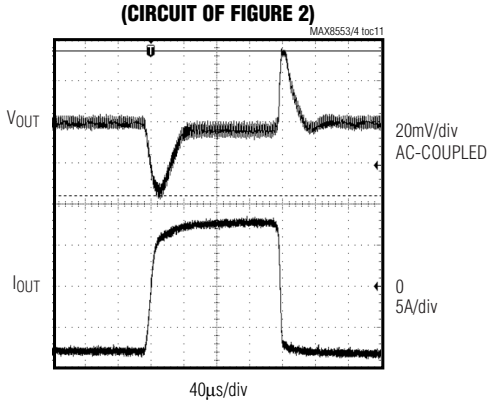
Typical Operating Characteristics (continued)

(V_{V+} = 12V, V_{OUT} = 1.8V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT 0A TO 20A TO 0A (CIRCUIT OF FIGURE 1)

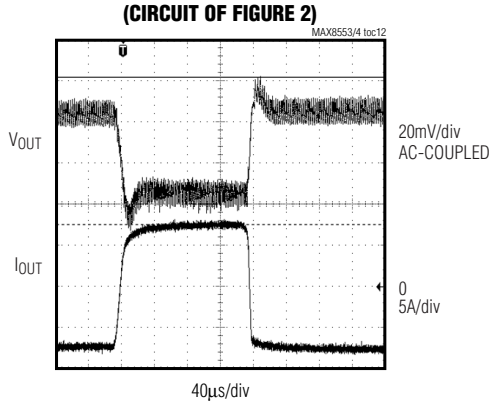


LOAD TRANSIENT -8A TO +8A TO -8A (CIRCUIT OF FIGURE 2)



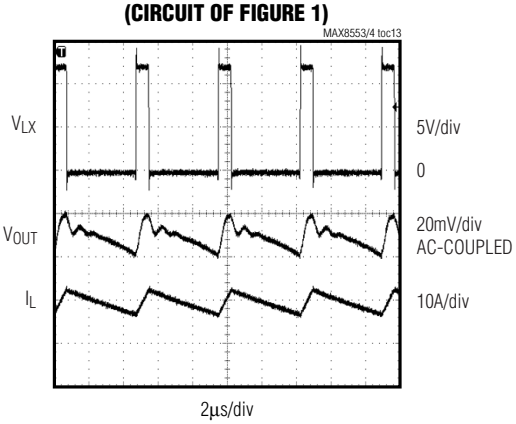
VTT CONNECTED TO THE OUTPUT

LOAD TRANSIENT -8A TO +8A TO -8A (CIRCUIT OF FIGURE 2)



VTT CONNECTED AS SHOWN IN FIGURE 2

SWITCHING WAVEFORMS WITH 20A LOAD (CIRCUIT OF FIGURE 1)

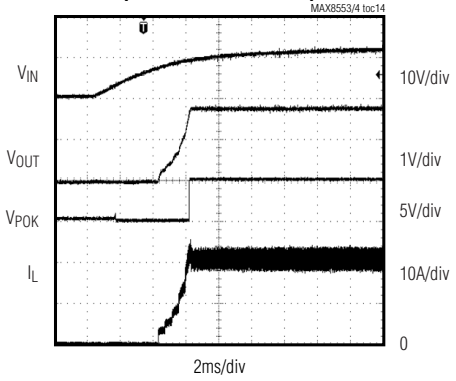


4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

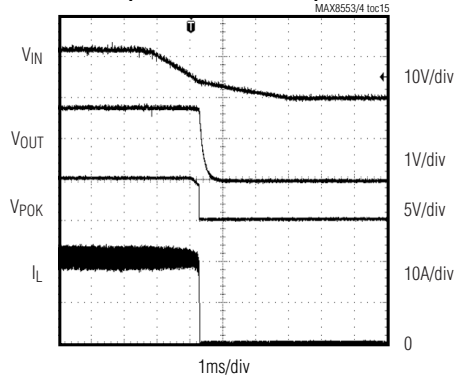
Typical Operating Characteristics (continued)

(V_{V+} = 12V, V_{OUT} = 1.8V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

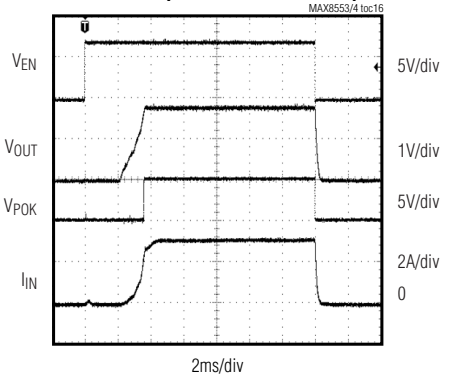
POWER-UP WAVEFORMS WITH 20A LOAD (CIRCUIT OF FIGURE 1)



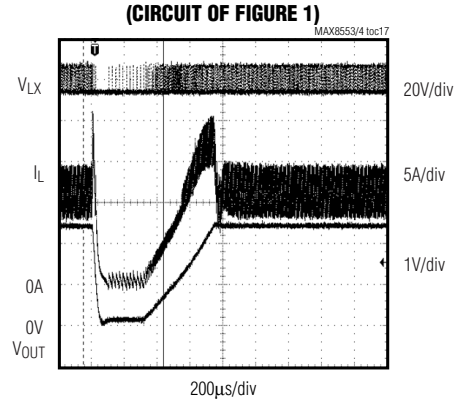
POWER-DOWN WAVEFORMS WITH 20A LOAD (CIRCUIT OF FIGURE 1)



STARTUP/SHUTDOWN WAVEFORMS WITH 20A LOAD (CIRCUIT OF FIGURE 1)



SHORT CIRCUIT AND RECOVERY (CIRCUIT OF FIGURE 1)

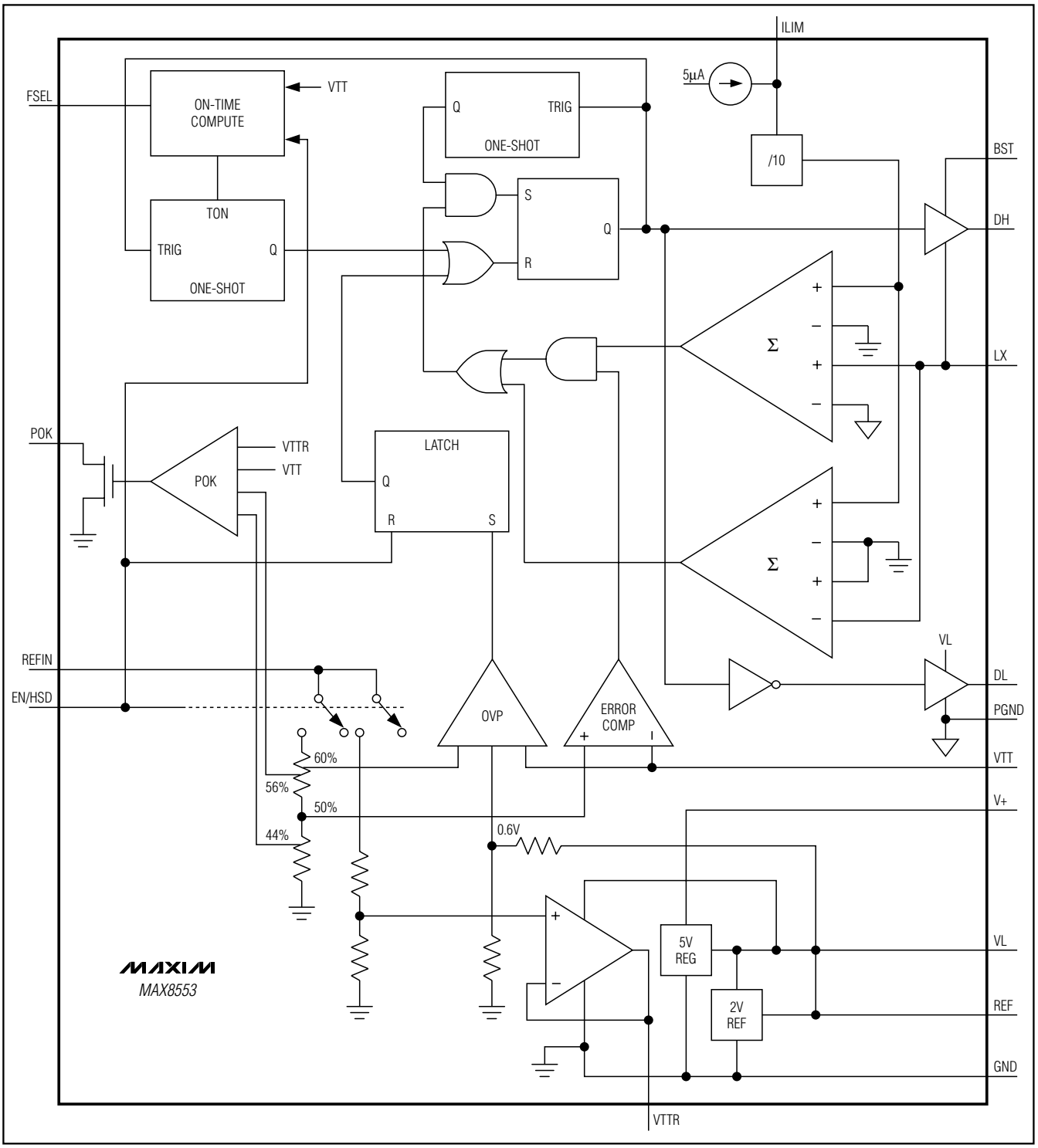


Pin Description

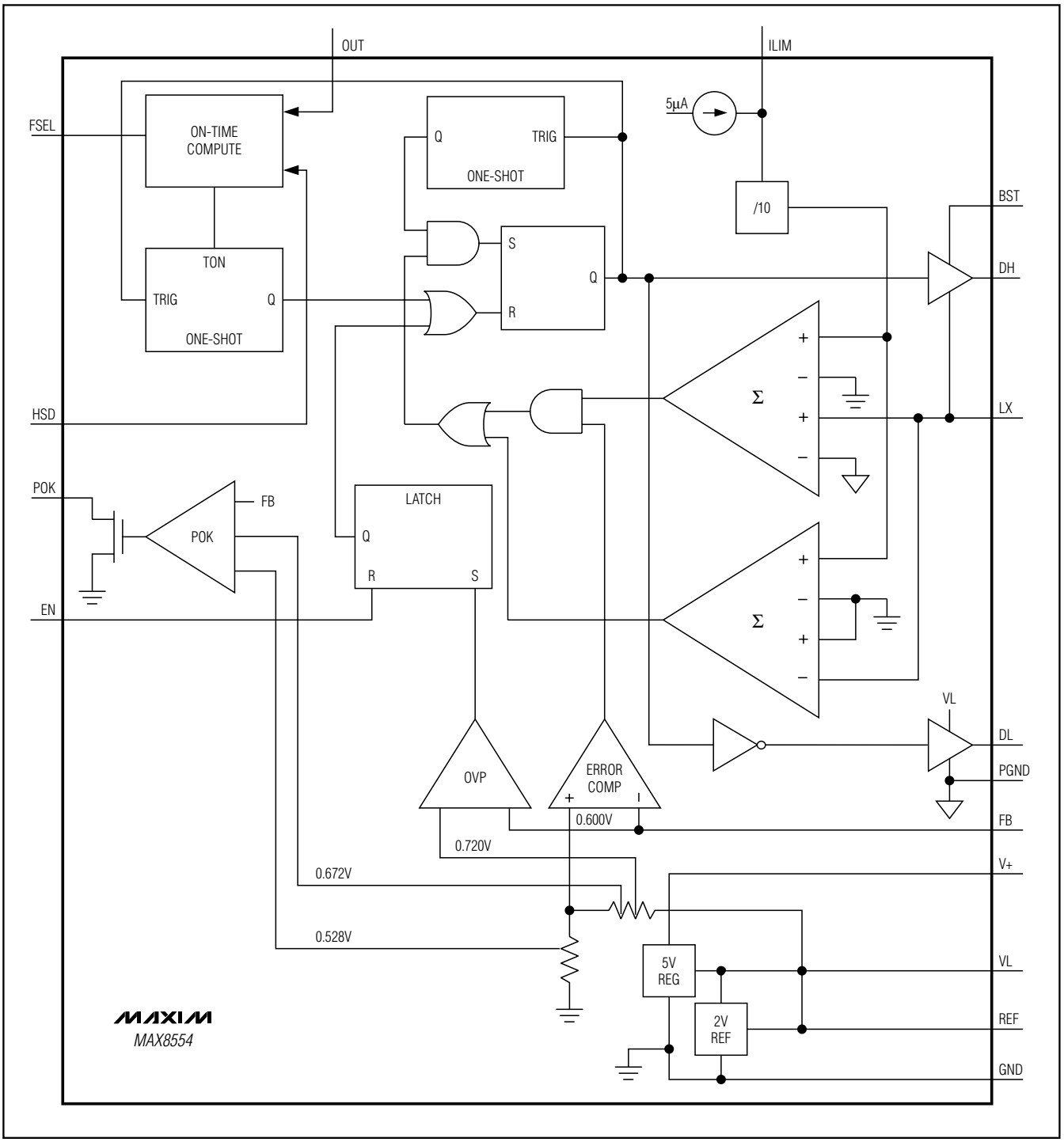
PIN	MAX8553	MAX8554	FUNCTION
1	EN/HSD	—	Enable/High-Side Drain. Connect to the high-side N-channel MOSFET drain through a 5.1kΩ resistor for normal operation. Connect to GND for low-power shutdown (Figure 2). If the enable function is not used, connect EN/HSD directly to the high-side N-channel MOSFET drain.
	—	HSD	High-Side Drain. Connect to the high-side N-channel MOSFET drain for normal operation.
2	REFIN	—	Reference Input. An applied voltage at REFIN sets V_{VTT} and V_{VTTR} to 1/2 V_{REFIN}. REFIN voltage range is from 0 to +3.6V.
	—	EN	Enable. Drive EN high to enable the output. Drive EN low to shut down the IC. If the enable function is not used, connect EN to V+.
3	POK	POK	Power-OK Output. POK is an open-drain output and is logic high when both VTT and VTTR are within 12% of regulation. POK is pulled low in shutdown.
4	VTT	—	VTT Feedback Input. Connect to VTT output.
	—	FB	Output Feedback. Connect to the center of a resistor-divider between the output and ground to set the output voltage. FB threshold is 0.6V.
5	ILIM	ILIM	Current-Limit Threshold Adjustment. Connect a resistor from ILIM to GND to set the current-limit threshold, or connect ILIM to VL for the default setting. See the *Setting the Current Limit* section.
6	FSEL	FSEL	Frequency Select. Selects the switching frequency. See Tables 1 and 2 for configuration of FSEL.
7	REF	REF	Reference. Connect a 0.22µF or greater capacitor from REF to GND.
8	GND	GND	Ground
9	VTTR	—	VTTR Reference Output. Connect a 1µF or greater capacitor from VTTR to GND. VTTR is capable of sourcing and sinking up to 25mA.
	—	OUT	Output Voltage. Connect directly to the output. OUT senses the output voltage to determine the on-time for the high-side switching MOSFET.
10	V+	V+	Input Supply Voltage. Supply input for the VL regulator. Bypass with a 0.22µF or greater capacitor.
11	VL	VL	Internal Regulator Output. Connect a 2.2µF or greater capacitor from VL to GND. VL can be connected to V+ if the operating range is from +4.5V to +5.5V.
12	DL	DL	Low-Side MOSFET Gate Drive. Connect to the gate of the low-side N-channel MOSFET. DL is low in shutdown or in undervoltage lockout.
13	PGND	PGND	Power Ground
14	BST	BST	Bootstrapped Supply. Drives high-side N-channel MOSFET. Connect a 0.1µF or greater capacitor from BST to LX.
15	DH	DH	High-Side MOSFET Gate Drive. Connect to the high-side N-channel MOSFET gate. DH is low in shutdown or in undervoltage lockout.
16	LX	LX	Inductor Switching Node

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

Functional Diagrams



Functional Diagrams (continued)



4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

Typical Application Circuits

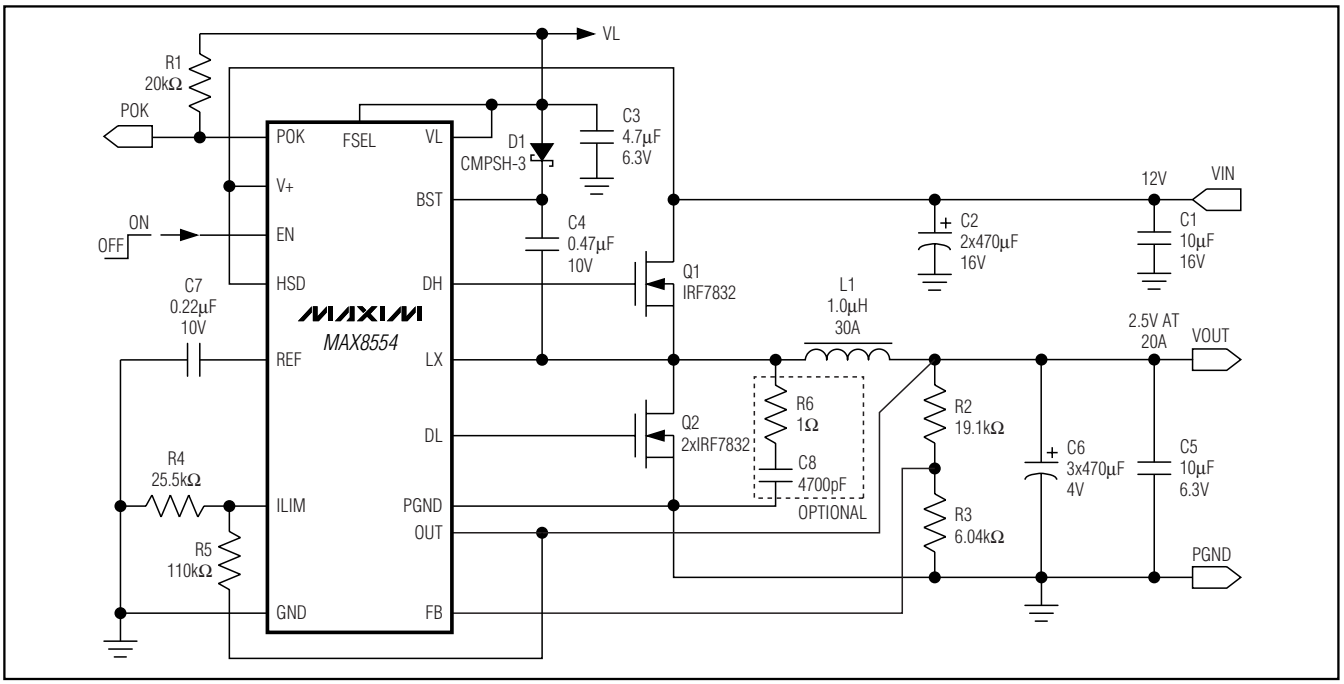


Figure 1. Typical Application Circuit 1: 12V Input, 2.5V Output at Up to 20A with 200kHz Switching Frequency

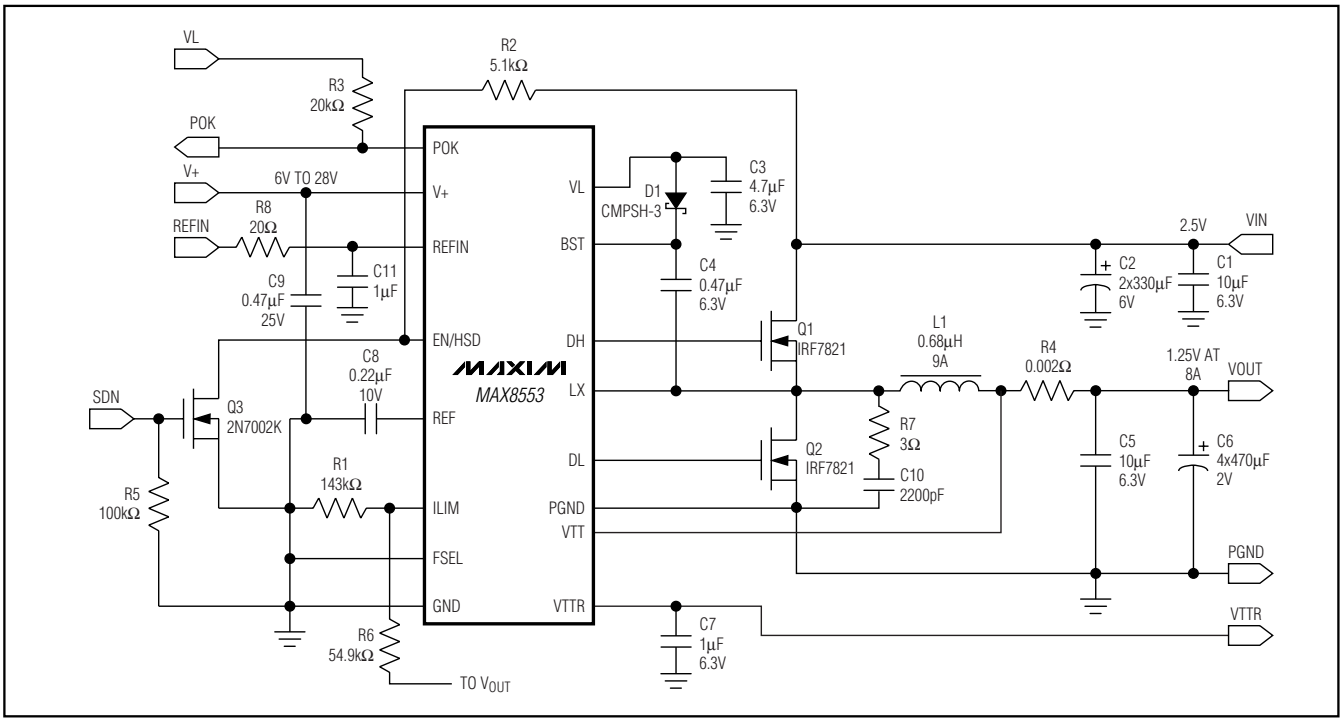


Figure 2. Typical Application Circuit 2: 2.5V Input, 1.25V VTT at Up to 8A, and 1.25V VTTR at Up to 25mA with 550kHz Switching

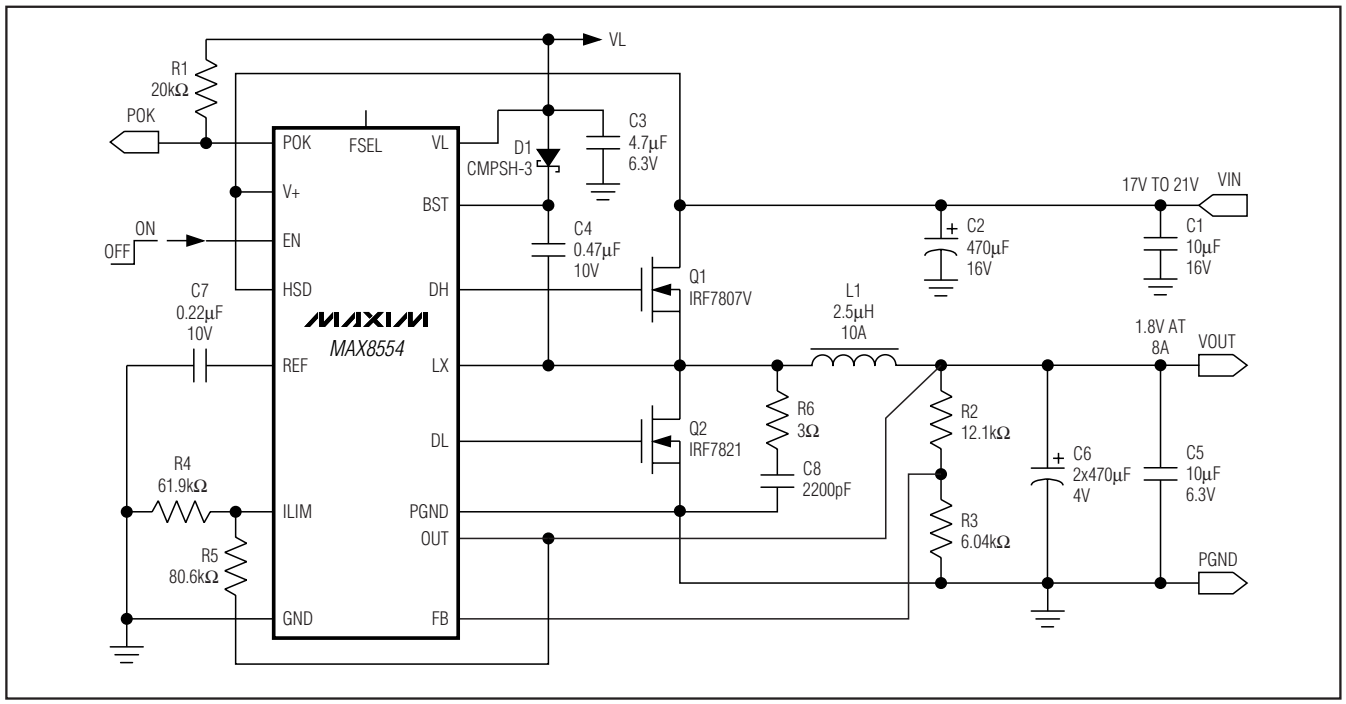


Figure 3. Typical Application Circuit 3: 19V Input, 1.8V Output at Up to 8A with 300kHz Switching Frequency

Detailed Description

Internal Linear Regulator

An internal regulator produces the +5V supply (VL) that powers the PWM controller, MOSFET driver, logic, reference, and other blocks within the IC. This +5V low-dropout (LDO) linear regulator supplies up to 35mA for MOSFET gate-drive and external loads. For supply voltages between +4.5V and +5.5V, connect VL to V+. This bypasses the VL regulator, which improves efficiency and allows the IC to function at lower input voltages.

On-Time One-Shot and Switching Frequency

The heart of the PWM is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to both input and output voltages. The high-side switch on-time is inversely proportional to the input voltage as measured by the EN/HSD (HSD for the MAX8554) input, and is directly proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The switching frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band. Also, with a constant switching frequency, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The general formula for the MAX8553 on-time (t_{ON}) is:

$$t_{ON} = K \times N \times \frac{1}{V_{EN/HSD}} \times V_{OUT}$$

where $V_{EN/HSD}$ and V_{OUT} are the voltages measured at EN/HSD and the output, respectively, and K = 1.7µs. The value of N depends on the configuration of FSEL and is listed in Table 1.

For the MAX8554, the general formula for on-time (t_{ON}) is:

$$t_{ON} = K \times N \times \frac{1}{V_{HSD}} \times V_{OUT}$$

where V_{HSD} and V_{OUT} are the voltages measured at HSD and the output, respectively, and K = 1.7µs. The value of N depends on the configuration of FSEL and is listed in Table 2.

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Table 1. Configuration of FSEL (MAX8553)

FSEL CONNECTED TO	N	t_{ON} (µs)	FREQUENCY (kHz)	CONDITION
Ground	1.07	0.91	550	V_{OUT} / $V_{EN/HSD}$ = 0.5
REF	1.33	1.15	400	V_{OUT} / $V_{EN/HSD}$ = 0.5
Floating	2.00	1.70	300	V_{OUT} / $V_{EN/HSD}$ = 0.5
VL	3.00	2.55	200	V_{OUT} / $V_{EN/HSD}$ = 0.5

Table 2. Configuration of FSEL (MAX8554)

FSEL CONNECTED TO	N	t_{ON} (µs)	FREQUENCY (kHz)	CONDITION
Ground	1.07	0.37	550	V_{HSD} = 12V, V_{OUT} = 2.5V
REF	1.33	0.49	400	V_{HSD} = 12V, V_{OUT} = 2.5V
Floating	2.00	0.71	300	V_{HSD} = 12V, V_{OUT} = 2.5V
VL	3.00	1.02	200	V_{HSD} = 12V, V_{OUT} = 2.5V

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The actual switching frequency, which is given by the following equation, varies slightly due to the voltage drop across the on-resistance of the MOSFETs and the DC resistance of the output inductor:

$$f_S = \frac{D}{t_{ON}} \cong \frac{1}{K \times N}$$

where D is the duty cycle:

$$D = \frac{V_{OUT} + I_O(R_{DSONL} + R_{DC})}{V_{HSD} + I_O(R_{DSONL} - R_{DSONH})}$$

where I_O is the output current, R_{DSONL} is the on-resistance of the low-side MOSFET, R_{DSONH} is the on-resistance of the high-side MOSFET, and R_{DC} is the DC resistance of the output inductor. The ideal switching frequency for V_{REFIN} = 2.5V is about 550kHz. Switching frequency increases for positive (sourcing) load current and decreases for negative (sinking) load current, due to the changing voltage drop across the low-side MOSFET, which changes the inductor-current discharge ramp rate. The on-times guaranteed in the *Electrical Characteristics* are also influenced by switching delays caused by the loading effect of the external power MOSFETs.

The switching frequency can also be adjusted to a value other than the preset frequencies by adding a resistor voltage-divider at HSD. See the *Adjusting the Switching Frequency* section.

VTTR Reference (MAX8553 Only)

The MAX8553's VTTR output is capable of sourcing or sinking up to 25mA of current. The VTTR output voltage is one-half of the voltage applied to REFIN. Bypass VTTR with at least a 1µF ceramic capacitor.

Voltage Reference

The voltage at REF is nominally 2.00V. Connect a 0.22µF ceramic bypass capacitor between REF and GND.

EN and HSD (MAX8554 Only)

EN is a logic input used to enable or shut down the MAX8554. Drive EN high or connect to V+ to enable the output. Drive EN low to place the MAX8554 in low-power shutdown mode, reducing input current to less than 5µA (typ).

HSD senses the input voltage at the drain of the high-side MOSFET, which is used to set the high-side MOSFET on-time. For normal operation, connect HSD to the drain of the high-side MOSFET.

EN/HSD Function (MAX8553 Only)

In order to reduce pin count and package size, the MAX8553 features a dual-function input pin, EN/HSD. When EN/HSD is pulled to ground, the internal circuitry powers off, reducing current consumption to less than 5µA (typ). To enable normal operation, connect EN/HSD to the drain of the high-side MOSFET through a 5.1kΩ resistor (Figure 2). In this configuration, EN/HSD becomes an input that monitors the high-side MOSFET drain voltage (converter input voltage) and uses that measurement to calculate the appropriate on-time for the converter. If the enable function is not used, connect EN/HSD directly to the high-side MOSFET drain.

Predischarge Mode

The MAX8553/MAX8554 discharge the output to GND before the digital soft-start begins. When EN/HSD (EN) is pulled high, the MAX8553 (MAX8554) starts an internal counter, and forces V_{DL} to V_{VL}. This discharges the output to GND through the low-side MOSFET. If the output voltage is above ground before enable, the output voltage goes slightly negative due to energy stored in the output LC. If the load cannot tolerate a negative voltage, place a power Schottky diode from the output to PGND (anode to PGND) to act as a reverse-polarity clamp. The period for this discharge mode is 1.7ms. Both the buck controller and the VTTR buffer are turned off during this period. After the predischarge period, both the buck controller and the VTTR buffer are turned on and go through soft-start.

Digital Soft-Start

The digital soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge current. The MAX8553/MAX8554 divide the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach the regulation within 425µs, soft-start enters the second phase and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached (after 1.7ms) or when the output reaches the nominal regulation voltage, whichever occurs first. Adding a capacitor in parallel with the external ILIM resistor creates a continuously adjustable analog soft-start function. If the foldback current-limiting feature is implemented in the application circuit, the maximum current limit is also a function of the output voltage and the resistors connected to ILIM.

Power-Good Output (POK)

POK is the open-drain output of the internal window comparators that continuously monitor VTT and VTTR for the MAX8553 and FB for the MAX8554. POK is actively held low in shutdown, and becomes high impedance when the outputs are within 12% of their respective nominal regulation voltage.

Overvoltage Protection (OVP)

When the buck output voltage rises above 120% of the nominal regulation voltage, the OVP circuit sets the fault latch, shuts down the PWM controller, and immediately pulls DH low and forces DL high. The negative current limit is also disabled. This turns on the low-side MOSFET, which rapidly discharges the output capacitors and clamps the output to ground. Note that immediately latching DL high can cause the output voltage to go slightly negative due to energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode from the output to PGND (anode to PGND) to act as a reverse-polarity clamp. Cycle EN or input power to reset the latch.

Overcurrent Protection

The current-limit circuit employs a unique “valley” current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current (Figure 4). Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, the inductor value, and the input voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 110% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted. The current-limit threshold can be adjusted with an external resistor (R_{ILIM}) at ILIM. A precision 5µA pullup current source at ILIM sets a voltage drop on this resistor, adjusting the current-limit threshold from approximately 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10 the voltage seen at ILIM. Therefore, choose R_{ILIM} equal to 2kΩ/mV of the current-limit threshold. The threshold defaults to 100mV when ILIM is connected to VL. The logic threshold for switchover to the 100mV default value is approximately V_{VL} - 1V. The adjustable current limit can accommodate various MOSFETs. Alternately, foldback current limit can also be implemented by adding a resistor from ILIM to V_{OUT}. See the *Setting the Current Limit* section.

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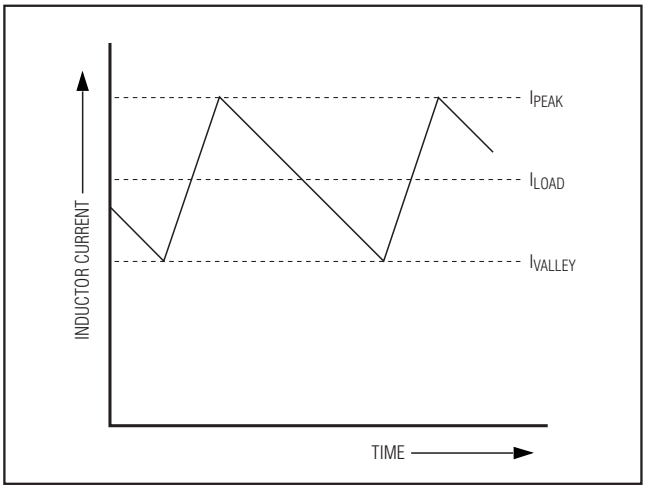

Figure 4. Inductor-Current Waveform

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by LX and PGND. The IC must be mounted close to the low-side MOSFET with short, direct traces making a Kelvin-sense connection to the source and drain terminals. See the *PC Board Layout* section.

Voltage Positioning

The Quick-PWM control architecture responds virtually instantaneously to transient load changes and eliminates the control loop delay of conventional PWM controllers. Therefore, a large portion of the voltage deviation during a step load change is from the ESR (equivalent series resistance) of the output capacitors. For DDR termination applications, the maximum allowed voltage deviation is ±40mV for any output load transition from sourcing current to sinking current. Passive voltage positioning adjusts the converter's output voltage based on its load current to optimize transient response and minimize the required output capacitance.

Voltage positioning is implemented by connecting a low ohmic resistor (R4) as shown in Figure 2.

MOSFET Drivers

The DH and DL drivers are optimized to drive MOSFETs that can deliver up to 25A output current. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX8553/MAX8554 can interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 squares to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the MAX8553/MAX8554). This adaptive dead-time delay is in addition to a fixed delay of 30ns (typ). The dead time at the other edge (DH turning off) is determined by a fixed 32ns (typ) internal delay.

Design Procedure

Setting the Output Voltage

For the MAX8553, the output voltage, V_{VTT}, is always 50% of V_{REFIN}.

For the MAX8554, the output voltage can be adjusted from 600mV to 3.5V using a resistive voltage-divider (R2 and R3 in Figures 1 and 3). To set the voltage, choose a value for R3 in the range of 1kΩ to 10kΩ, then solve for R2 using the following equation:

$$R2 = R3 \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} is 0.6V.

Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak inductor current (I_{PEAK}), and DC resistance (R_{DC}). A good compromise between size and efficiency is to set the inductor peak-to-peak ripple current equal to 30% of the maximum load current, thus LIR = 0.3. The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost and also improve transient response but reduce efficiency and increase output voltage ripple due to higher peak currents. Higher inductance increases efficiency by reducing the RMS current.

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor's current saturation rating must exceed the

peak inductor current at the maximum-defined load current ($I_{LOAD(MAX)}$):

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Output-Capacitor Selection

The key selection parameters for the output capacitor are the actual capacitance value, the ESR, the equivalent series inductance (ESL), and the voltage-rating requirements, which affect the overall stability, output ripple voltage, and transient response.

The worst-case output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and ESL caused by the current into and out of the capacitor. This can be approximated by:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple due to the ESR is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

The output voltage ripple due to the output capacitance is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

The output voltage ripple due to the ESL of the output capacitor is:

$$V_{RIPPLE\ (ESL)} = (V_{IN} \times ESL) / (L+ESL)$$

I_{P-P} is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

After a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD} + ESL x di/dt and the controllers respond within 100ns and try to regulate back to the nominal output value.

Solid polymer or OSCON electrolytic capacitors are recommended due to their low ESR and ESL at the switching frequency. Higher output-current applications require multiple output capacitors connected in parallel to meet the output ripple-voltage requirements. Do not exceed the capacitor's voltage or ripple-current ratings.

Output-Capacitor Stability Consideration

Stability is determined by the value of the ESR zero relative to the switching frequency. To ensure stability, the following condition must be met:

$$f_{ESR} < \frac{f_S}{\pi}$$

where f_S is the switching frequency and:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection. The source impedance to the input supply largely determines the value of C_{IN}. High source impedance requires high input capacitance. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value of 1/2 I_{LOAD}, which occurs when V_{IN} is twice V_{OUT}.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

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Setting the Current Limit

Constant Current Limit

The adjustable current limit accommodates MOSFETs with a wide range of on-resistance values. The current-limit threshold is adjusted with an external resistor connected from ILIM to GND ($R_{ILIM\_}$). The adjustment range is 50mV to 200mV measured across the low-side MOSFET. The value of R_{ILIM} is calculated using the following formula:

$$R_{ILIM} = 10 \times \frac{I_{VALLEY}}{5\mu A} \times R_{DS(ON)}$$

where I_{VALLEY} is the valley current limit and $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET. To avoid reaching the current at a lower current than expected, use the maximum value for $R_{DS(ON)}$ at elevated junction temperature. Refer to the MOSFET manufacturer's data sheet for maximum values.

Foldback Current Limit

Foldback current limit is used to reduce power dissipation during overload and short-circuit conditions. This is accomplished by lowering the current-limit threshold as the output voltage drops due to the overload.

To use foldback current limit, connect a resistor (R_{FOBK}) from ILIM to the output, and connect a resistor (R_{ILIM}) from ILIM to GND (Figure 5). The values of R_{ILIM} and R_{FOBK} are calculated as follows:

First, select the percentage of foldback, P_{FB}. This percent corresponds to the current limit when V_{OUT} equals zero divided by the current limit when V_{OUT} equals its nominal voltage. Typical values range from 15% to 30%. To solve for the resistor values, use the following equations:

$$R_{FOBK} = \frac{P_{FB} \times V_{OUT}}{5\mu A(1 - P_{FB})}$$

$$R_{ILIM} = \frac{10 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB}) \times R_{FOBK}}{V_{OUT} - (10 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB}))}$$

If R_{ILIM} results in a negative number, select another low-side MOSFET with lower $R_{DS(ON)}$ or increase P_{FB} or a combination of both for the best compromise of cost, efficiency, and lower short-circuit power dissipation.

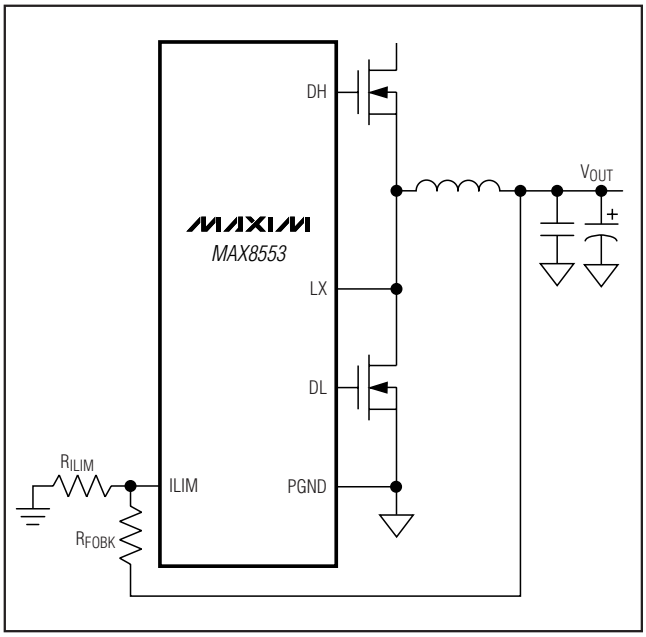


Figure 5. Setting the Foldback Current Limit with Two Resistors, R_{ILIM} and R_{FOBK}

Adjusting the Switching Frequency

The switching frequency of the MAX8553/MAX8554 can be lowered from the value set by FSEL by adding a resistor voltage-divider to EN/HSD (HSD) as shown in Figure 6. This voltage-divider lowers the voltage the IC measures on EN/HSD (HSD), which increases the on-time. The switching frequency with the added resistor-divider is calculated as follows:

$$f_S \cong \frac{1}{K \times N} \times \frac{R2}{R1 + R2}$$

where K = 1.7µs and N is given in Tables 1 and 2. To set the frequency, select a value for R2 between 10kΩ and 100kΩ, then calculate R1 from the following equation:

$$R1 = \frac{1}{K \times N} \times \frac{R2}{f_S} - R2$$

With the minimum input voltage, make sure that the voltage present at EN/HSD (HSD) is greater than 1.5V when the resistor-divider is used:

$$\frac{V_{IN(MIN)} \times R2}{R1 + R2} > 1.5V$$

Setting Voltage Positioning

The droop resistor, R_{DRP} (R4) in Figure 2, in series with the output inductor before the output capacitor, sets the droop voltage, V_{DRP}. Choose R_{DRP} such that the output voltage at the maximum load current, including ripple, is just above the lower limit of the output tolerance:

$$R_{DRP} < \frac{V_{OUT(TYP)} - V_{OUT(MIN)} - V_{RIPPLE} / 2}{I_{OUT(MAX)}}$$

R_{DRP} introduces some power dissipation, which is given by:

$$P_{D(DRP)} = R_{DRP} \times \left(I_{OUT(MAX)}\right)^2$$

R_{DRP} should be chosen to handle this power dissipation.

Power MOSFET Selection

The MAX8553/MAX8554 drive external, logic-level, N-channel MOSFETs as the circuit-switch elements. The key selection parameters are:

On-resistance ($R_{DS(ON)}$): The lower, the better.

Maximum drain-to-source voltage (V_{DSS}): This should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.

Gate charges (Q_G, Q_{GD}, Q_{GS}): The lower, the better.

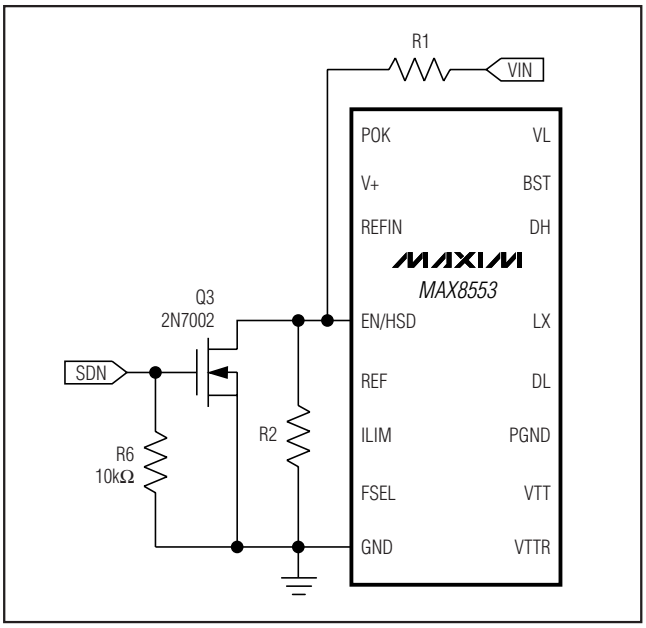


Figure 6. A resistor-divider (R1 and R2) is used to lower the switching frequency.

Choose the MOSFETs with rated $R_{DS(ON)}$ at V_{GS} = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has a conduction loss equal to switching loss at nominal input voltage and maximum output current (see below). For the low-side MOSFET, make sure that it does not spuriously turn on because of the dV/dt caused by the high-side MOSFET turning on, as this would result in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{GD} to Q_{GS} ratio have higher immunity to dV/dt.

For proper thermal-management design, calculate the power dissipation at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for low-side MOSFET, worst case is at $V_{IN(MAX)}$; for high-side MOSFET, it could be either at $V_{IN(MIN)}$ or $V_{IN(MAX)}$). The high-side MOSFET and low-side MOSFET have different loss components due to the circuit operation. The low-side MOSFET operates as a zero voltage switch; therefore, major losses are: the channel conduction loss (P_{LSCC}), the body-diode conduction loss (P_{LSDC}), and the gate-drive loss (P_{LSDR}):

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I_{LOAD}\right)^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{LSDC} = 2 \times I_{LOAD} \times V_F \times t_{DT} \times f_S$$

where V_F is the body-diode forward-voltage drop, t_{DT} is the dead time (~30ns), and f_S is the switching frequency.

Because of the zero-voltage switch operation, low-side MOSFET gate-drive loss occurs as a result of charging and discharging the input capacitance (C_{ISS}). This loss is distributed among the average DL gate driver's pullup and pulldown resistance, R_{DL} (~1.2Ω), and the internal gate resistance (R_{GATE}) of the MOSFET (~2Ω). The drive power dissipated is given by:

$$P_{LSDR} = C_{ISS} \times \left(V_{GS}\right)^2 \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DL}}$$

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{HSCC}), the VI overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current.

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times (I_{LOAD})^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_S \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$$

where I_{GATE} is the average DH driver output current determined by:

$$I_{GATE} = \frac{2.5V}{R_{DH} + R_{GATE}}$$

where R_{DH} is the high-side MOSFET driver's on-resistance (1.4Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (~2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

where $V_{GS} = V_{VL} = 5V$.

When the MAX8553 is sinking current, the high-side MOSFET operates as a zero-voltage switch and the low-side MOSFETs operate as a nonzero-voltage switch.

In addition to the losses above, allow about 20% more for additional losses due to MOSFET output capacitances and low-side MOSFET body-diode reverse recovery charge dissipated in the high-side MOSFET that is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source, or add resistors in series with DH and DL to slow down the switching transitions. Adding series resistors increases the power dissipation of the MOSFET, so ensure that this does not overheat the MOSFET.

Control IC Power Dissipation

Power dissipation in the MAX8553/MAX8554 IC is primarily due to the on-chip MOSFETs' gate drivers (DH and DL). This power dissipation depends on the gate charge of the external MOSFETs used. Power dissipation in the MAX8553 also depends on the VTTR load current (I_{VTTR}). Use the following equation to calculate the power dissipation:

$$P_D = (V_{V+}) \times \left[f_S \times (Q_{GH} + Q_{GL}) + I_{VTTR} \right]$$

where Q_{GH} and Q_{GL} are the total gate charge of the high-side and low-side MOSFETs, respectively. Select the switching frequency and V_{V+} correctly to ensure the power dissipation does not exceed the package power-dissipation requirement.

Applications Information

PC Board Layout

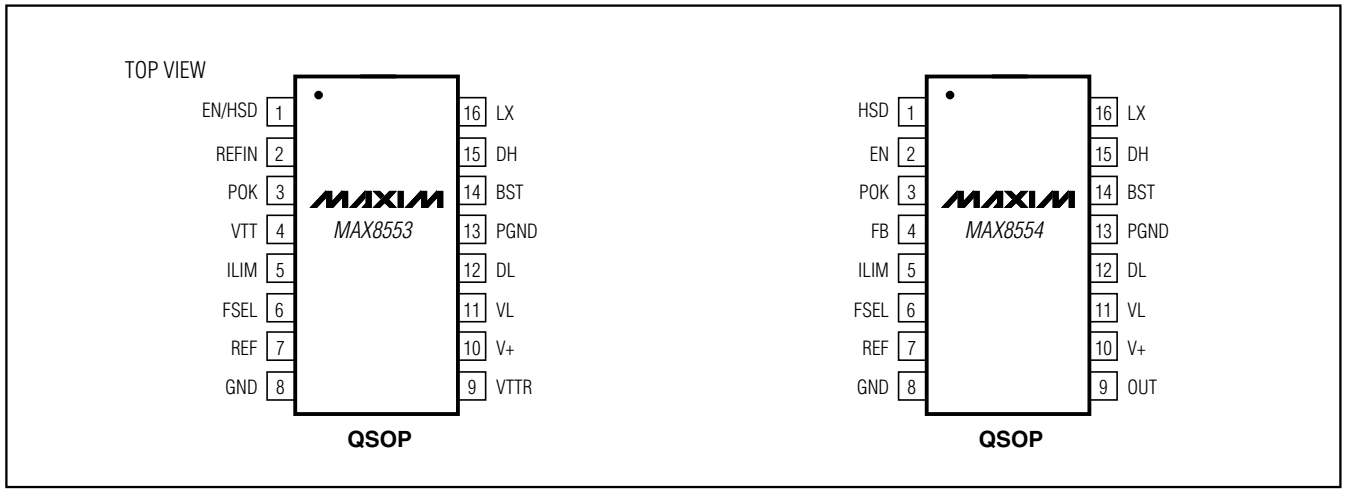
A properly designed PC board layout is important in any switching regulator. The switching power stage requires particular attention. If possible, mount all the power components on the top-side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, low-jitter operation.
2) Connect GND and PGND together at a single point.
3) Keep the power traces and load connections short. This practice is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can noticeably enhance full-load efficiency. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) LX and PGND connections to the low-side MOSFET for current limiting must be made using Kelvin-sense connections in order to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this can be done by routing power to the MOSFETs from

outside using the top copper layer, while tying in PGND and LX inside (underneath) the 8-pin SO package.

5) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
6) It may be desirable to deliberately introduce some trace length (droop resistance) between the FB inductor node and the output filter capacitor to meet the stability criteria ($f_{ESR} < f_S / \pi$).
7) Place feedback resistors as close as possible to the IC.
8) Route high-speed switching nodes away from sensitive analog nodes.
9) Make all pin-strap control input connections (ILIM, etc.) to GND or VL close to the chip, and do not connect to PGND.

Pin Configurations



Chip Information

TRANSISTOR COUNT: 2827

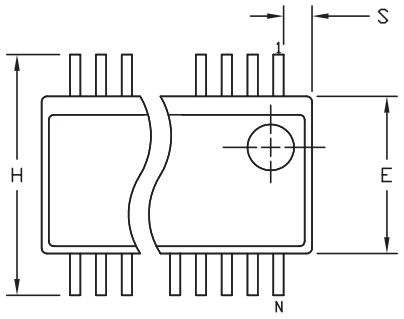
PROCESS: BiCMOS

4.5V to 28V Input, Synchronous PWM Buck Controllers for DDR Termination and Point-of-Load Applications

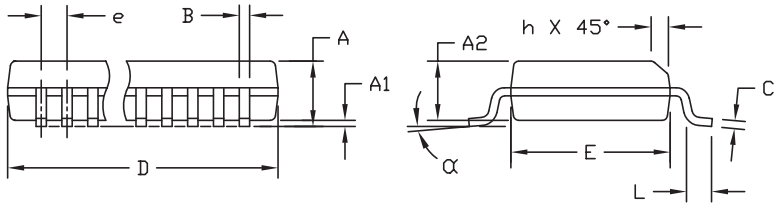
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

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