



Low-Power, Serial, 12-Bit DACs with Voltage Output

MAX5174/MAX5176

General Description

The MAX5174/MAX5176 low-power, serial, voltage-output, 12-bit digital-to-analog converters (DACs) feature a precision output amplifier in a space-saving 16-pin QSOP package. The MAX5174 operates from a single +5V supply, and the MAX5176 operates from a single +3V supply. Both devices draw only 280 μ A of supply current, which reduces to 1 μ A in shutdown. In addition, the programmable power-up reset feature allows for a user-selectable output voltage state of either 0 or mid-scale.

The 3-wire, digital, serial interface is compatible with SPI™/QSPI™, and MICROWIRE™ standards. An input register followed by a DAC register provides a double-buffered input, allowing the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include software and hardware shutdown, shutdown lockout, a hardware clear pin, and a reference input capable of accepting DC and offset AC signals. These devices provide a programmable digital output pin for added functionality and a serial-data output pin for daisy-chaining. All logic inputs are TTL/CMOS compatible and are internally buffered with Schmitt triggers to allow direct interfacing to optocouplers.

The MAX5174/MAX5176 incorporate a proprietary on-chip circuit that keeps the output voltage virtually “glitch free,” limiting the glitches to a few millivolts during power-up.

Both devices are available in 16-pin QSOP packages and are specified for the extended (-40°C to +85°C) temperature range. The MAX5170/MAX5172 are pin-compatible 14-bit upgrades to the MAX5174/MAX5176. For 100% pin-compatible DACs with internal reference, see the 13-bit MAX5130/MAX5131 and the 12-bit MAX5120/MAX5121 data sheets.

Applications

- Industrial Process Controls
- Digital Offset and Gain Adjustment
- Motion Control
- Automatic Test Equipment (ATE)
- Remote Industrial Controls
- μ P-Controlled Systems

Functional Diagram appears at end of data sheet.

*SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*



Maxim Integrated Products 1

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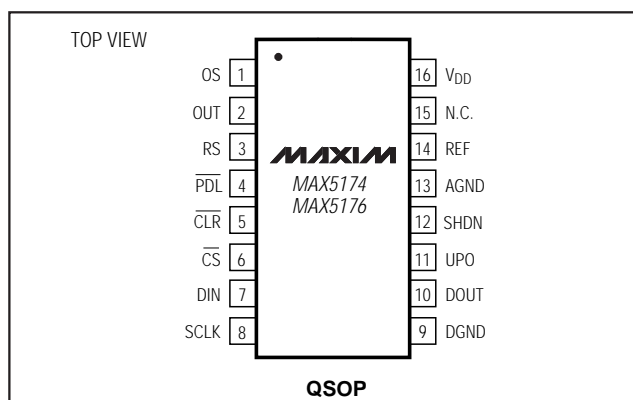
Features

- ◆ ± 1 LSB INL
- ◆ 1 μ A Shutdown Current
- ◆ “Glitch Free” Output Voltage at Power-Up
- ◆ Single-Supply Operation
 - +5V (MAX5174)
 - +3V (MAX5176)
- ◆ Full-Scale Output Range
 - +2.048V (MAX5176, VREF = +1.25V)
 - +4.096V (MAX5174, VREF = +2.5V)
- ◆ Rail-to-Rail® Output Amplifier
- ◆ Adjustable Output Offset
- ◆ Low THD (-80dB) in Multiplying Operation
- ◆ SPI/QSPI/MICROWIRE-Compatible 3-Wire Serial Interface
- ◆ Programmable Shutdown Mode and Power-Up Reset
- ◆ Buffered Output Capable of Driving 5k Ω || 100pF Loads
- ◆ User-Programmable Digital Output Pin Allows Serial Control of External Components
- ◆ 14-Bit Upgrades Available (MAX5170/MAX5172)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5174AE4E	-40°C to +85°C	16 QSOP	± 1
MAX5174BE4E	-40°C to +85°C	16 QSOP	± 2
MAX5176AE4E	-40°C to +85°C	16 QSOP	± 2
MAX5176BE4E	-40°C to +85°C	16 QSOP	± 4

Pin Configuration



Low-Power, Serial, 12-Bit DACs with Voltage Output

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND, DGND	-0.3V to +6.0V
AGND to DGND	-0.3V to +0.3V
Digital Inputs to DGND	-0.3V to +6.0V
DOUT, UPO to DGND	-0.3V to (V _{DD} + 0.3V)
OUT, REF to AGND	-0.3V to (V _{DD} + 0.3V)
OS to AGND	(AGND - 4.0V) to (V _{DD} + 0.3V)
Maximum Current into Any Pin	50mA

Continuous Power Dissipation (T _A = +70°C)	16-Pin QSOP (derate 8mW/°C above +70°C)	667mW
Operating Temperature Range		-40°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering, 10sec)		+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5174

(V_{DD} = +5V ±10%, V_{REF} = 2.5V, OS = AGND = DGND, R_L = 5kΩ, C_L = 100pF referenced to ground, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5174A			±1	LSB
		MAX5174B			±2	
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	V _{OS}				±10	mV
Gain Error	GE	R _L = ∞		-0.6	±4	LSB
		R _L = 5kΩ		-1.6	±8	
Power-Supply Rejection Ratio	PSRR			10	120	μV/V
Output Noise Voltage		f = 100kHz		1		LSBp-p
Output Thermal Noise Density				80		nV/√Hz
REFERENCE						
Reference Input Range	V _{REF}		0		V _{DD} - 1.4	V
Reference Input Resistance	R _{REF}		18			kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V _{REF} = 0.5Vp-p + 1.5V _{DC} , slew-rate limited		350		kHz
Reference Feedthrough		V _{REF} = 3.6Vp-p + 1.8V _{DC} , f = 1kHz, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V _{REF} = 2Vp-p + 1.5V _{DC} , f = 10kHz, code = FFF hex		82		dB
DIGITAL INPUTS						
Input High Voltage	V _{IH}		3			V
Input Low Voltage	V _{IL}				0.8	V
Input Hysteresis	V _{HYS}			200		mV
Input Leakage Current	I _{IN}	V _{IN} = 0 or V _{DD}		0.001	±1	μA
Input Capacitance	C _{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V _{OH}	I _{SOURCE} = 2mA		V _{DD} - 0.5		V
Output Low Voltage	V _{OL}	I _{SINK} = 2mA		0.13	0.4	V

Low-Power, Serial, 12-Bit DACs with Voltage Output

MAX5174/MAX5176

ELECTRICAL CHARACTERISTICS—MAX5174 (continued)

($V_{DD} = +5V \pm 10\%$, $V_{REF} = 2.5V$, OS = AGND = DGND, $R_L = 5k\Omega$, $C_L = 100pF$ referenced to ground, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/ μ s
Output Settling Time		To $\pm 0.5LSB$, from 10mV to full-scale		18		μ s
Output Voltage Swing (Note 3)			0		V_{DD}	V
OS Pin Input Resistance			80	120		$k\Omega$
Time Required to Exit Shutdown				40		μ s
Digital Feedthrough		$\overline{CS} = V_{DD}$, $f_{SCLK} = 100kHz$, $V_{SCLK} = 5Vp-p$		1		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current (Note 4)	I_{DD}			0.35	0.4	mA
Shutdown Current (Note 4)				1	10	μ A
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
\overline{CS} Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to \overline{CS} Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		40			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	$C_{LOAD} = 200pF$			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	$C_{LOAD} = 200pF$			80	ns
SCLK Rise to \overline{CS} Fall Delay	t_{CS0}		10			ns
\overline{CS} Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
\overline{CS} Pulse Width High	t_{CSW}		100			ns

Low-Power, Serial, 12-Bit DACs with Voltage Output

ELECTRICAL CHARACTERISTICS—MAX5176

($V_{DD} = +2.7V$ to $+3.6V$, $V_{REF} = 1.25V$, $OS = AGND = DGND$, $R_L = 5k\Omega$, $C_L = 100pF$ referenced to ground, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			12			Bits
Integral Nonlinearity (Note 5)	INL	MAX5176A			± 2	LSB
		MAX5176B			± 4	
Differential Nonlinearity	DNL				± 1	LSB
Offset Error (Note 2)	V_{OS}				± 10	mV
Gain Error	GE	$R_L = \infty$		-0.6	± 4	LSB
		$R_L = 5k\Omega$		-1.6	± 8	
Power-Supply Rejection Ratio	PSRR			10	120	$\mu V/V$
Output Noise Voltage		$f = 100kHz$		2		LSBp-p
Output Thermal Noise Density				80		nV/\sqrt{Hz}
REFERENCE						
Reference Input Range	V_{REF}		0		$V_{DD} - 1.4$	V
Reference Input Resistance	R_{REF}		18			$k\Omega$
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		$V_{REF} = 0.5V_{p-p} + 0.75V_{DC}$, slew-rate limited		350		kHz
Reference Feedthrough		$V_{REF} = 1.6V_{p-p} + 0.8V_{DC}$, $f = 1kHz$, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	$V_{REF} = 0.6V_{p-p} + 0.9V_{DC}$, $f = 10kHz$, code = FFF hex		78		dB
DIGITAL INPUT						
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	$V_{IN} = 0$ or V_{DD}		0.001	± 1	μA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	$I_{SOURCE} = 2mA$	$V_{DD} - 0.5$			V
Output Low Voltage	V_{OL}	$I_{SINK} = 2mA$		0.13	0.4	V

Low-Power, Serial, 12-Bit DACs with Voltage Output

MAX5174/MAX5176

ELECTRICAL CHARACTERISTICS—MAX5176 (continued)

($V_{DD} = +2.7V$ to $+3.6V$, $V_{REF} = 1.25V$, $OS = AGND = DGND$, $R_L = 5k\Omega$, $C_L = 100pF$ referenced to ground, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/ μs
Output Settling Time		To $\pm 0.5LSB$, from 10mV to full-scale		18		μs
Output Voltage Swing (Note 3)			0		V_{DD}	V
OS Pin Input Resistance			80	120		$k\Omega$
Time Required to Exit Shutdown				40		μs
Digital Feedthrough		$\overline{CS} = V_{DD}$, $DIN = 50kHz$; $f_{SCLK} = 100kHz$, $V_{SCLK} = 3Vp-p$		1		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current (Note 4)	I_{DD}			0.35	0.4	mA
Shutdown Current (Note 4)				1	10	μA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		150			ns
SCLK Pulse Width High	t_{CH}		75			ns
SCLK Pulse Width Low	t_{CL}		75			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS}		60			ns
SCLK Rise to \overline{CS} Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		60			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	$C_{LOAD} = 200pF$			200	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	$C_{LOAD} = 200pF$			200	ns
SCLK Rise to \overline{CS} Fall Delay	t_{CS0}		10			ns
\overline{CS} Rise to SCLK Rise Hold Time	t_{CS1}		75			ns
\overline{CS} Pulse Width High	t_{CSW}		150			ns

Note 2: Offset is measured at the code that comes closest to 10mV.

Note 3: Accuracy is better than 1 LSB for $V_{OUT} = 10mV$ to $V_{DD} - 180mV$. Guaranteed by PSR test on end points.

Note 4: $R_L =$ open and digital inputs are either V_{DD} or $DGND$.

Note 5: INL guaranteed between codes 20 and 4095.

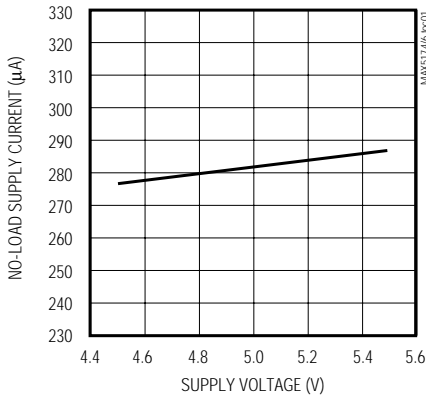
Low-Power, Serial, 12-Bit DACs with Voltage Output

Typical Operating Characteristics

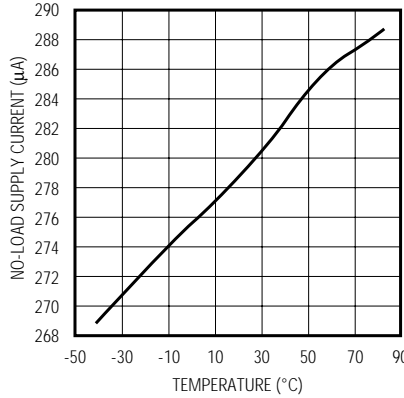
(MAX5174: $V_{DD} = +5V$, $V_{REF} = 2.5V$; MAX5176: $V_{DD} = +3V$, $V_{REF} = +1.25V$; $C_L = 100pF$, OS = AGND, code = FFF hex, $T_A = +25^\circ C$, unless otherwise noted.)

MAX5174

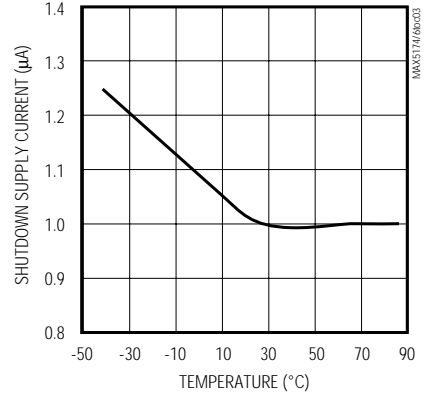
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



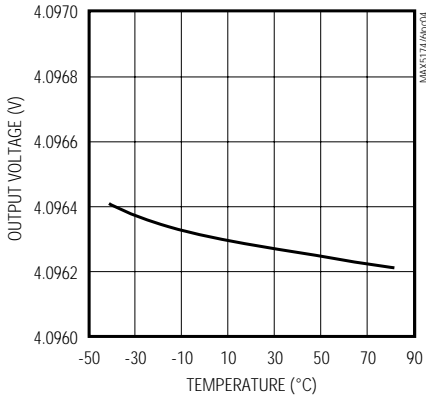
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



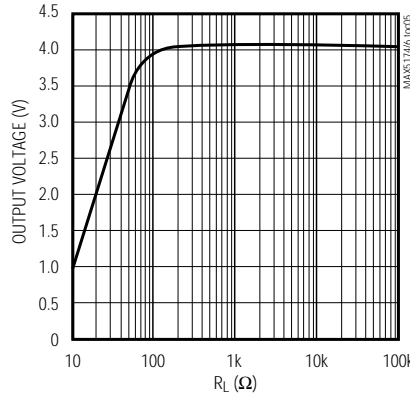
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



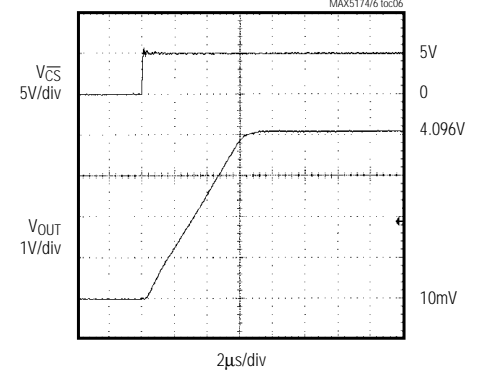
OUTPUT VOLTAGE vs. TEMPERATURE



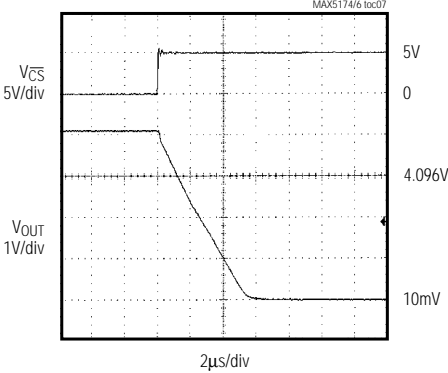
OUTPUT VOLTAGE vs. LOAD RESISTANCE



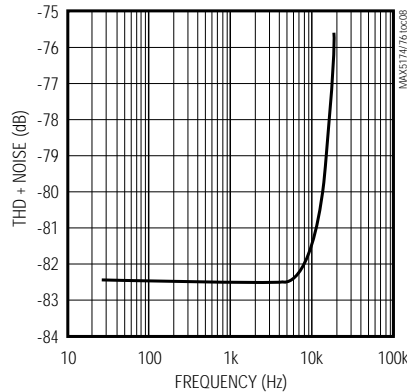
DYNAMIC RESPONSE



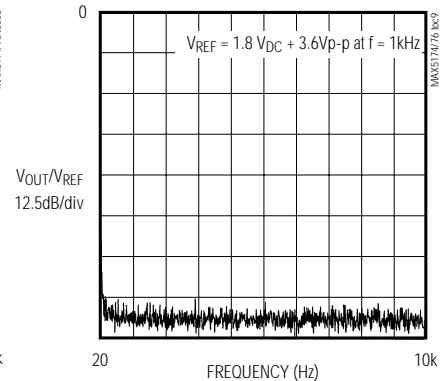
DYNAMIC RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



REFERENCE FEEDTHROUGH



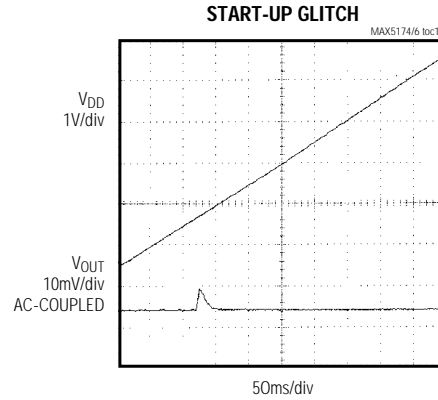
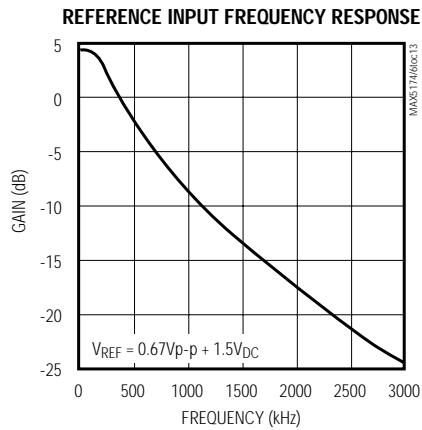
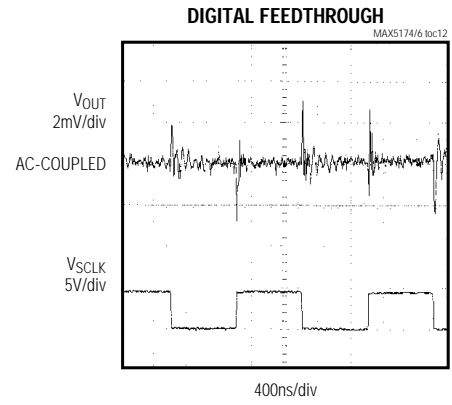
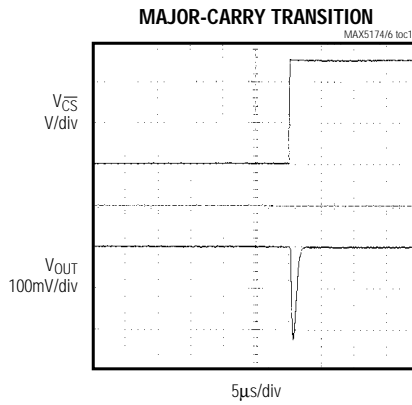
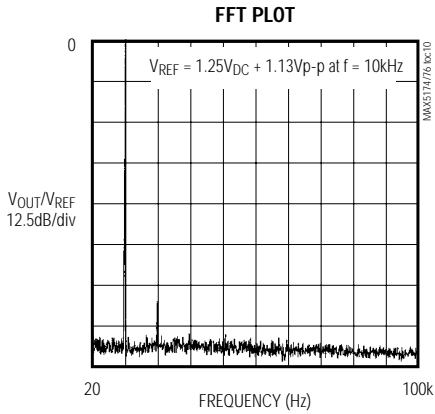
Low-Power, Serial, 12-Bit DACs with Voltage Output

MAX5174/MAX5176

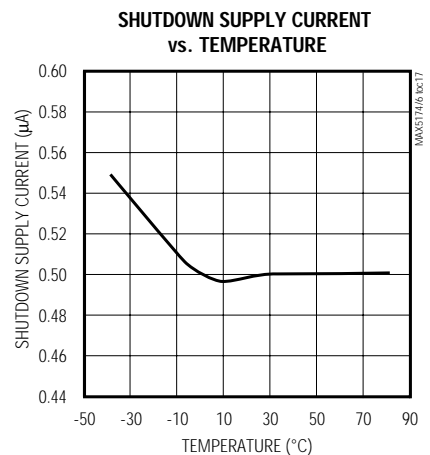
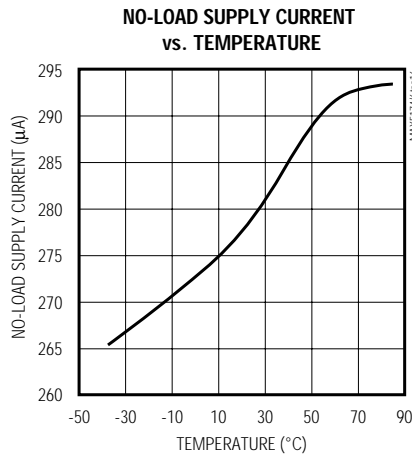
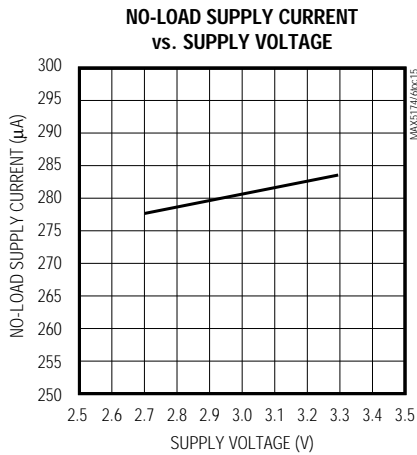
Typical Operating Characteristics (continued)

(MAX5174: $V_{DD} = +5V$, $V_{REF} = 2.5V$; MAX5176: $V_{DD} = +3V$, $V_{REF} = +1.25V$; $C_L = 100pF$, OS = AGND, code = FFF hex, $T_A = +25^\circ C$, unless otherwise noted.)

MAX5174



MAX5176



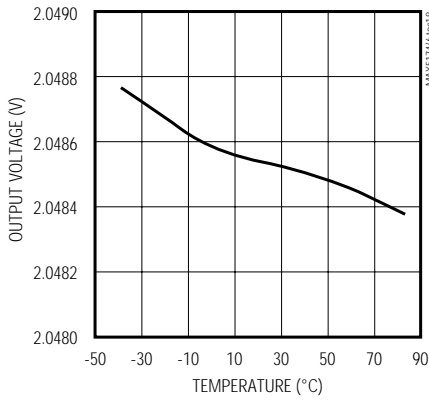
Low-Power, Serial, 12-Bit DACs with Voltage Output

Typical Operating Characteristics (continued)

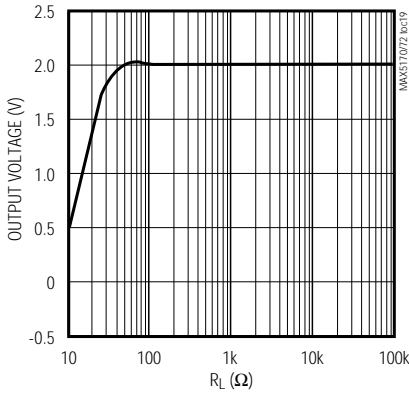
(MAX5174: $V_{DD} = +5V$, $V_{REF} = 2.5V$; MAX5176: $V_{DD} = +3V$, $V_{REF} = +1.25V$; $C_L = 100pF$, OS = AGND, code = FFF hex, $T_A = +25^\circ C$, unless otherwise noted.)

MAX5176

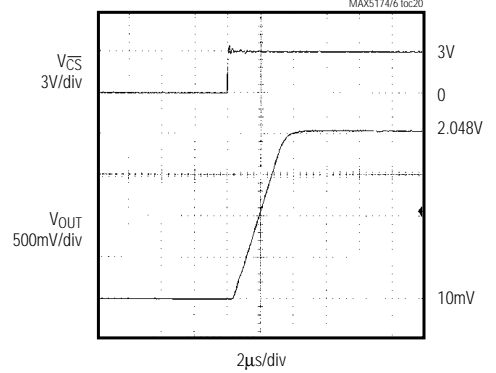
OUTPUT VOLTAGE vs. TEMPERATURE



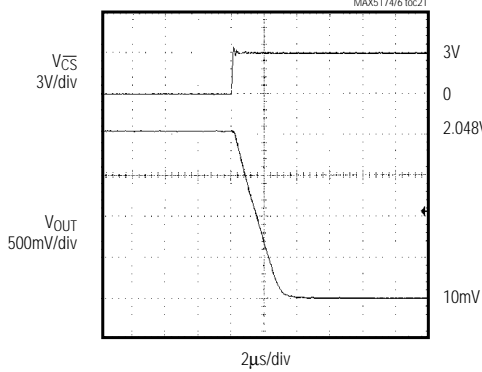
OUTPUT VOLTAGE vs. LOAD RESISTANCE



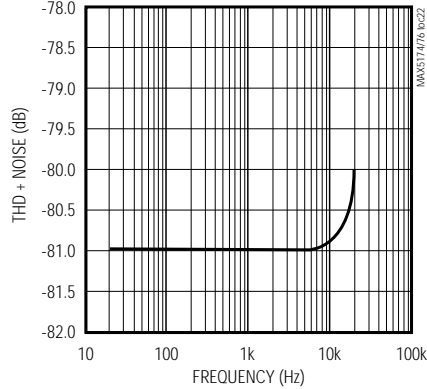
DYNAMIC RESPONSE



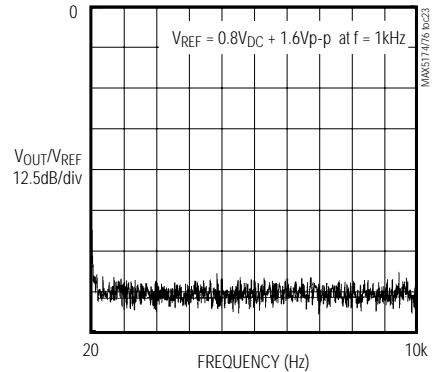
DYNAMIC RESPONSE



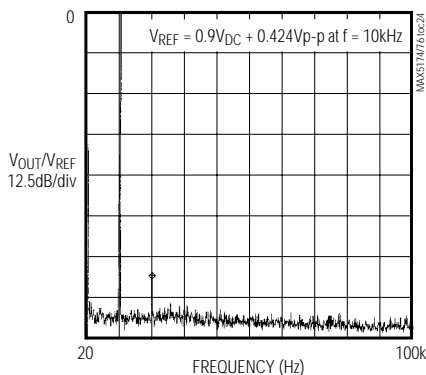
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



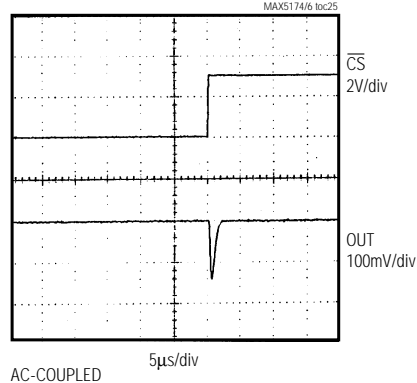
REFERENCE FEEDTHROUGH



FFT PLOT



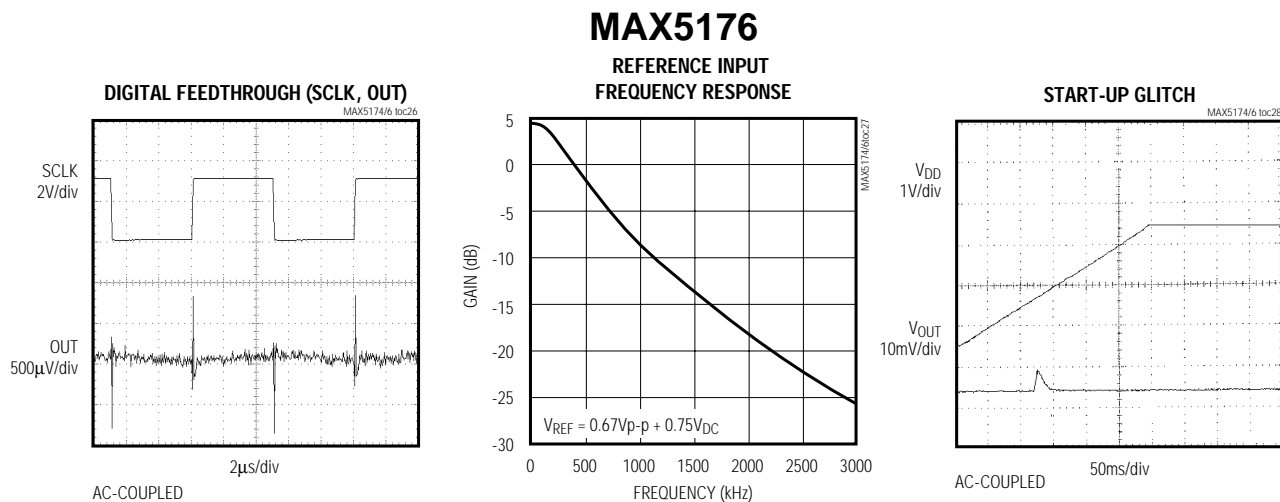
MAJOR-CARRY TRANSITION



Low-Power, Serial, 12-Bit DACs with Voltage Output

Typical Operating Characteristics (continued)

(MAX5174: $V_{DD} = +5V$, $V_{REF} = 2.5V$; MAX5176: $V_{DD} = +3V$, $V_{REF} = +1.25V$; $C_L = 100pF$, OS = AGND, code = FFF hex, $T_A = +25^\circ C$, unless otherwise noted.)



MAX5174/MAX5176

Pin Description

PIN	NAME	FUNCTION
1	OS	Offset Adjustment. Connect to AGND for no offset.
2	OUT	Voltage Output. High impedance when in shutdown. The output voltage is limited to V_{DD} .
3	RS	Reset Mode Select (digital input). Connect to V_{DD} to select midscale reset output voltage. Connect to DGND to select 0 reset output voltage.
4	\overline{PDL}	Power-Down Lockout. (digital input). Connect to V_{DD} to allow shutdown. Connect to DGND to disable software and hardware shutdown.
5	\overline{CLR}	Clear DAC. (digital input) Clears the DAC to either zero or midscale as determined by RS.
6	\overline{CS}	Chip-Select Input (digital input). DIN ignored when \overline{CS} is high.
7	DIN	Serial-Data Input (digital input). Data is clocked in on the rising edge of SCLK.
8	SCLK	Serial Clock Input (digital input).
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output. State is set by the serial input.
12	SHDN	Shutdown (digital input). Pulling SHDN high when $\overline{PDL} = V_{DD}$ places the chip in shutdown with a maximum shutdown current of $10\mu A$.
13	AGND	Analog Ground
14	REF	Reference Input. Maximum V_{REF} is $V_{DD} - 1.4V$.
15	N.C.	No Connection
16	V_{DD}	Positive Supply. Bypass to AGND with a $4.7\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor.

Low-Power, Serial, 12-Bit DACs with Voltage Output

Detailed Description

The MAX5174/MAX5176 12-bit, serial, voltage-output DACs operate with a 3-wire serial interface. These devices include a 16-bit shift register and a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, these devices employ a rail-to-rail output amplifier and internal trimmed resistors to provide a gain of +1.638V/V, maximizing the output voltage swing. The MAX5174/MAX5176's offset adjust pin allows for a DC shift in DAC outputs. The DACs are designed with an inverted R-2R ladder network (Figure 1) that produces a weighted voltage proportional to the reference voltage.

Reference Inputs

The reference input accepts both AC and DC values with a voltage range extending from 0 to $V_{DD} - 1.4V$. The following equation represents the resulting output voltage:

$$V_{OUT} = \frac{V_{REF} \cdot N \cdot \text{Gain}}{4096}$$

where N is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the internally set voltage gain (1.638V/V if OS = AGND). The maximum output voltage is V_{DD} . The reference pin has a minimum impedance of 18k Ω and is code dependent.

Output Amplifier

With OS connected to AGND, the output amplifier employs an internal trimmed resistor-divider, setting the gain to 1.638V/V and minimizing gain error. The output amplifier has a typical slew rate of 0.6V/ μ s, and settles to ± 0.5 LSB from a full-scale transition within 18 μ s when loaded with 5k Ω in parallel with 100pF. Loads less than 2k Ω degrade performance. For alternative output amplifier setups, refer to the *Applications Information* section.

Shutdown Mode

The MAX5174/MAX5176 feature a software- and hardware-programmable shutdown mode that reduces the typical supply current to 1 μ A. Enter shutdown by writing the appropriate input-control word as shown in Table 1 or by using the hardware shutdown. In shutdown mode, the reference input and amplifier output both become high impedance, and the serial interface remains active. Data in the input register is saved, allowing the MAX5174/MAX5176 to recall the prior output state when returning to normal operation. Exit shutdown by

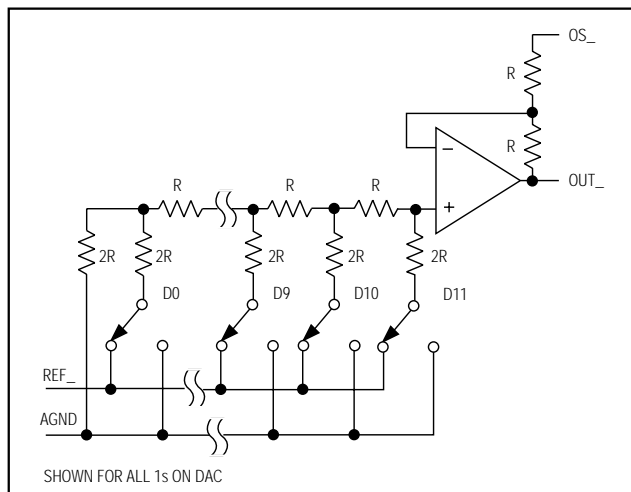


Figure 1. Simplified DAC Circuit Diagram

reloading the DAC register from the shift register, by simultaneously loading the input and DAC registers, or by toggling \overline{PDL} . When returning from shutdown wait 40 μ s for the output to settle.

Power-Down Lockout

Power-down lockout disables the software/hardware shutdown mode. A high-to-low transition on \overline{PDL} brings the device out of shutdown and returns the output to its previous state.

Shutdown

Pulling SHDN high while \overline{PDL} is high places the MAX5174/MAX5176 in shutdown. Pulling SHDN low will not return the device to normal operation. A high-to-low transition on \overline{PDL} or an appropriate command from the serial data line (see Table 1 for commands) is required to exit shutdown.

Serial-Interface

The MAX5174/MAX5176 3-wire serial interface is compatible with SPI and QSPI (Figure 2), and MICROWIRE (Figure 3) interface standards. The 16-bit serial input word consists of two control bits, 12 bits of data (MSB to LSB), and two sub-bits.

The control bits determine the MAX5174/MAX5176's response as outlined in Table 1. The MAX5174/MAX5176's digital inputs are double buffered, which allows any of the following:

- Loading the input register without updating the DAC register.
- Updating the DAC register from the input register.
- Updating the input and DAC registers simultaneously.

Low-Power, Serial, 12-Bit DACs with Voltage Output

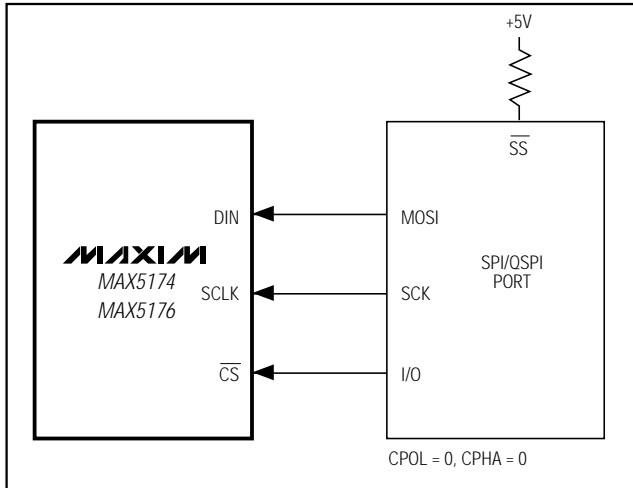


Figure 2. Connections for SPI and QSPI Standards

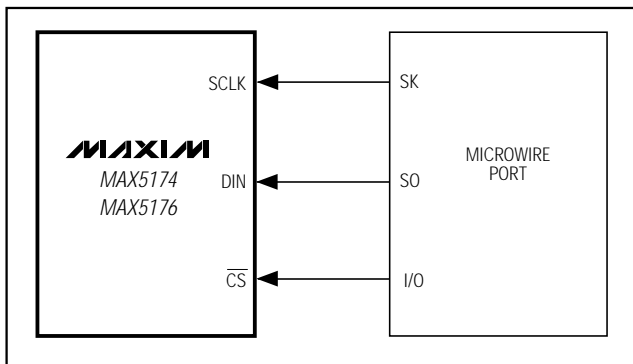


Figure 3. Connections for MICROWIRE

The MAX5174/MAX5176 accepts one 16-bit packet or two 8-bit packets sent while \overline{CS} remains low. The MAX5174/MAX5176 allow the following to be configured:

- Clock edge on which serial data output (DOUT) is clocked.
- State of the user-programmable logic output.
- Configuration of the reset state.

Specific commands for setting these are shown in Table 1.

The general timing diagram in Figure 4 illustrates how the MAX5174/MAX5176 acquires data. \overline{CS} must go low at least t_{CSS} before the rising edge of the serial clock (SCLK). With \overline{CS} low, data is clocked into the register on the rising edge of SCLK. The maximum serial clock frequency guaranteed for proper operation is 10MHz for the MAX5174 and 6MHz for the MAX5176. See Figure 5 for a detailed timing diagram of the serial interface.

Serial Data Output (DOUT)

The serial-data output (DOUT) is the internal shift register's output and allows for daisy-chaining of multiple devices as well as data readback (see *Applications Information*). By default upon start-up, data shifts out of DOUT on the serial clock's rising edge (Mode 0) and provides a lag of 16 clock cycles, thus maintaining SPI, QSPI, and MICROWIRE compatibility. However, if the device is programmed for Mode 1, then the output data lags DIN by 16.5 clock cycles and is clocked out on the serial clock's rising edge. During shutdown, DOUT retains its last digital state prior to shutdown.

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD			S1, S0	FUNCTION
C1	C0	D11.....D0		
0	0	12-bit DAC data	0 0	Load input register; DAC registers are unchanged.
0	1	12-bit DAC data	0 0	Load input register; DAC registers are updated (start-up DAC with new data).
1	0	xxxxxxxxxxxx	xx	Update DAC register from input register (start-up DAC with data previously stored in the input registers).
1	1	0 0 x x xxxx xxxx	xx	No operation (NOP).
1	1	0 1 x x xxxx xxxx	xx	Shut down DAC (provided $\overline{PDL} = 1$).
1	1	1 0 0 x xxxx xxxx	xx	UPO goes low (default).
1	1	1 0 1 x xxxx xxxx	xx	UPO goes high.
1	1	1 1 0 x xxxx xxxx	xx	Mode 1, DOUT clocked out on SCLK's rising edge.
1	1	1 1 1 x xxxx xxxx	xx	Mode 0, DOUT clocked out on SCLK's falling edge (default).

Low-Power, Serial, 12-Bit DACs with Voltage Output

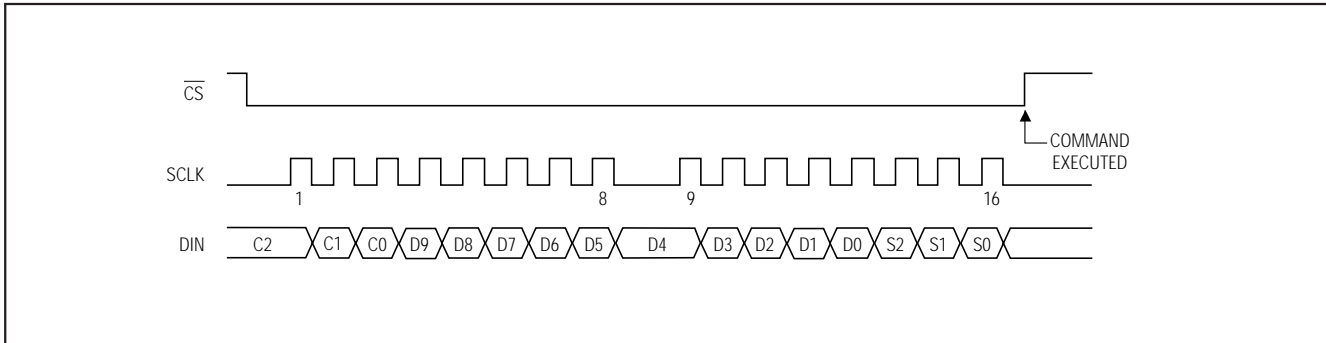


Figure 4. Serial-Interface Timing Diagram

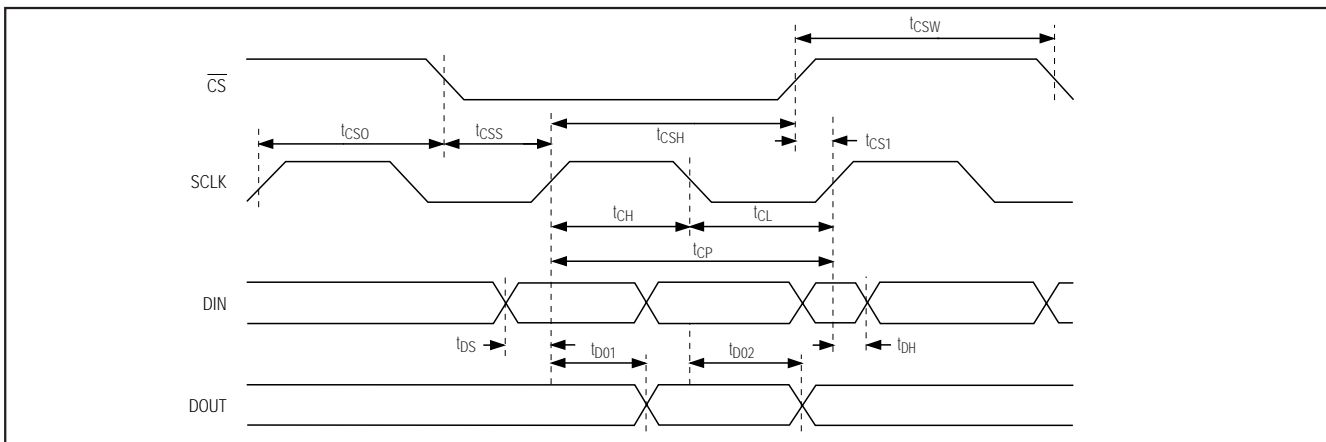


Figure 5. Detailed Serial-Interface Timing Diagram

User-Programmable Logic Output (UPO)

The user-programmable logic output (UPO) allows control of an external device through the serial interface, thereby reducing the number of microcontroller I/O pins required. During power-down, this output will retain its digital state prior to shutdown. When $\overline{\text{CLR}}$ is pulled low, UPO will reset to its programmed default state. See Table 1 for specific commands to control the UPO.

Reset (RS) and Clear ($\overline{\text{CLR}}$)

The MAX5174/MAX5176 offers a clear pin ($\overline{\text{CLR}}$), which resets the output voltage. If $\text{RS} = \text{DGND}$, then $\overline{\text{CLR}}$ resets the output voltage to 0. If $\text{RS} = \text{V}_{\text{DD}}$, then $\overline{\text{CLR}}$ resets the output voltage to mid-scale. In either case, $\overline{\text{CLR}}$ will reset UPO to its programmed default state.

Applications Information

Unipolar Output

Figure 6 shows the MAX5174/MAX5176 configured for unipolar, rail-to-rail operation with a gain of 1.638V/V.

Table 2 lists the codes for unipolar output voltages. The output voltage is limited to V_{DD} . Use the OS pin to introduce an offset voltage as shown in Figure 7 and described in the *Offset and Buffer Configurations* section.

Bipolar Output

Figure 8 shows the MAX5174/MAX5176 configured for bipolar output operation. The output voltage is given by the following equation (OS = AGND):

$$V_{\text{OUT}} = V_{\text{REF}} \left(\frac{2 \cdot N}{4096} - 1 \right)$$

where N represents the numeric value of the DAC's binary input code and V_{REF} is the voltage of the external reference. Table 3 shows digital codes and the corresponding output voltage for Figure 8's circuit.

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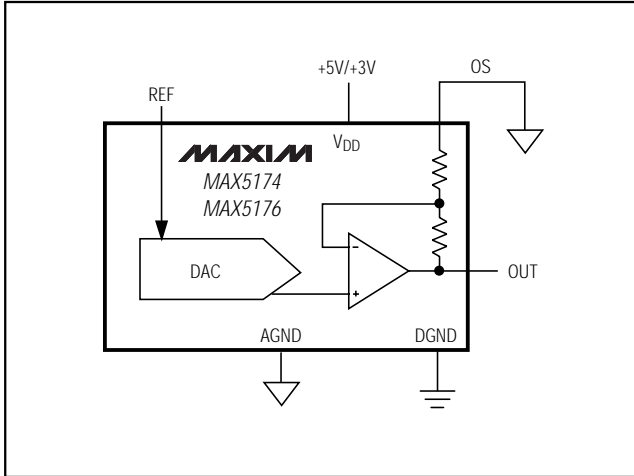


Figure 6. Unipolar Output Circuit (Rail-to-Rail)

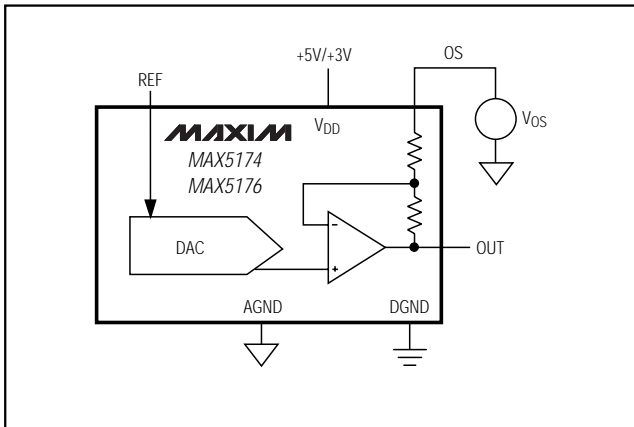


Figure 7. Setting OS for Output Offset

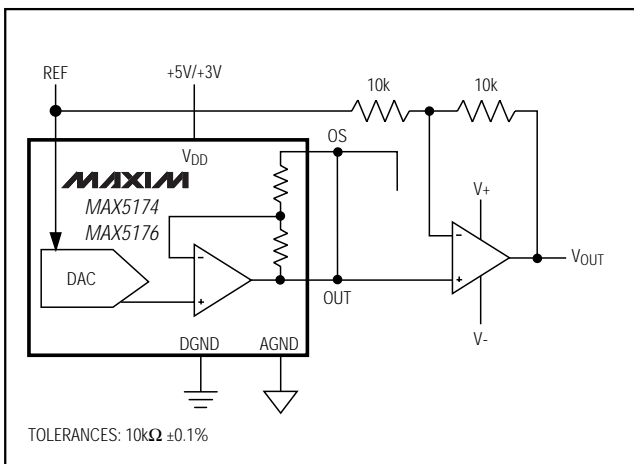


Figure 8. Bipolar Output Circuit

Offset and Buffer Configurations

The simple circuit of Figure 7 illustrates how to introduce an offset to the output voltage. The amount of offset introduced by a voltage at the OS pin is shown in the following equation:

$$V_{\text{OFFSET}} = V_{\text{OS}} \cdot (1 - \text{Gain})$$

where Gain = 1.638.

However, the total output voltage of the device cannot exceed V_{DD} , regardless of the voltage on the OS pin.

To set the gain of the output amplifier to 1, connect OS to OUT.

Daisy-Chaining Devices

The serial-data output pin (DOUT) allows multiple MAX5174/MAX5176s to be daisy-chained together as shown in Figure 9. The advantage of this is that only two lines are needed to control all the DACs. The disadvantage is that it takes n commands to program the DACs.

Figure 10 shows several MAX5174/MAX5176s sharing one common DIN signal line. In this configuration the data bus is common to all devices; however, more I/O lines are required because each device needs a dedicated $\overline{\text{CS}}$ line. The advantage of this configuration is that only one command is needed to program any DAC.

Table 2. Unipolar Code Table (Circuit of Figure 6)

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
11	1111 1111 11 (00)	$+V_{\text{REF}} (4095/4096) \cdot 1.638$
10	0000 0000 01 (00)	$+V_{\text{REF}} (2049/4096) \cdot 1.638$
10	0000 0000 00 (00)	$+V_{\text{REF}} (2048/4096) \cdot 1.638$
01	1111 1111 11 (00)	$+V_{\text{REF}} (2047/4096) \cdot 1.638$
00	0000 0000 01 (00)	$+V_{\text{REF}} (1/4096) \cdot 1.638$
00	0000 0000 00 (00)	0

Table 3. Bipolar Code Table (Circuit of Figure 8)

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
11	1111 1111 11 (00)	$+V_{\text{REF}} [(2 \cdot 4095/4096) - 1]$
10	0000 0000 01 (00)	$+V_{\text{REF}} [(2 \cdot 2049/4096) - 1]$
10	0000 0000 00 (00)	$+V_{\text{REF}} [(2 \cdot 2048/4096) - 1]$
01	1111 1111 11 (00)	$+V_{\text{REF}} [(2 \cdot 2047/4096) - 1]$
00	0000 0000 01 (00)	$+V_{\text{REF}} [(2 \cdot 1/4096) - 1]$
00	0000 0000 00 00	$-V_{\text{REF}}$

Low-Power, Serial, 12-Bit DACs with Voltage Output

Using an AC Reference

The MAX5174/MAX5176 accept references with AC components, as long as the reference voltage remains between 0 and $V_{DD} - 1.4V$. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must remain above AGND.

Power-Supply and Layout Considerations

Wire-wrap boards are not recommended. For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND pins together at the IC. The best ground connection is achieved by connecting the DAC's DGND and AGND

pins together and connecting that point to the system analog ground plane. This is useful because if the DAC's DGND is connected to the system digital ground, digital noise may infiltrate the DAC's analog portion.

Bypass the power supply with a $4.7\mu F$ capacitor in parallel with a $0.1\mu F$ capacitor to AGND. Minimize capacitor lead lengths to reduce inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation.

To maintain INL and DNL performance as well as gain drift, it is extremely important to provide the lowest possible reference output impedance at the DAC reference input pin. INL degrades if the series resistance on REF pin exceeds 0.1Ω . The same consideration must be made for the AGND pin.

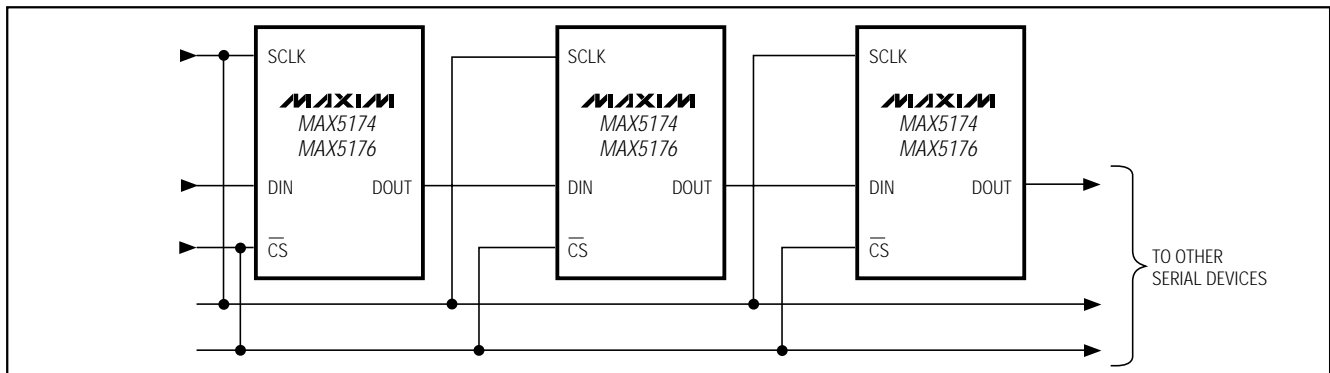


Figure 9. Daisy-Chaining MAX5174/MAX5176 Devices

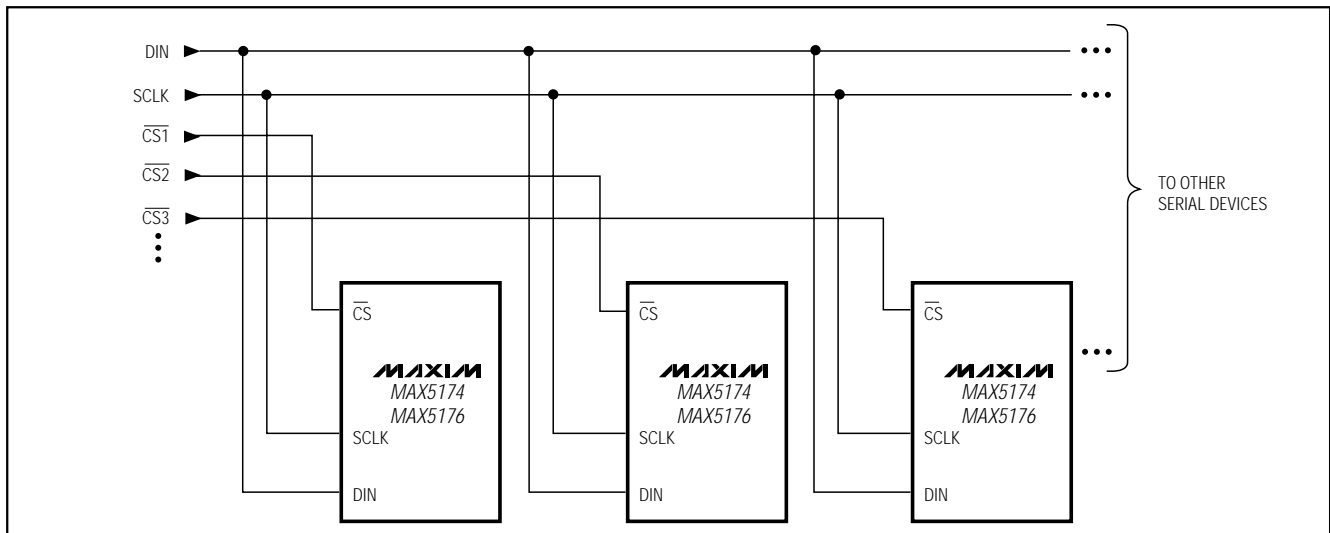


Figure 10. Multiple MAX5174/MAX5176s Sharing Common DIN and SCLK Lines

Low-Power, Serial, 12-Bit DACs with Voltage Output

Chip Information

TRANSISTOR COUNT: 3457

MAX5174/MAX5176

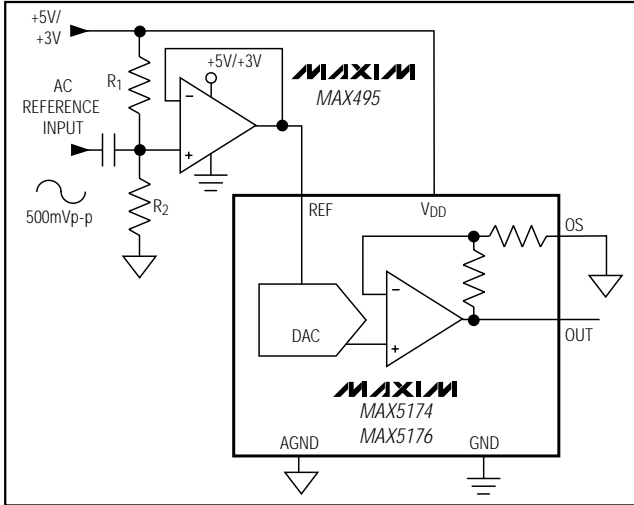
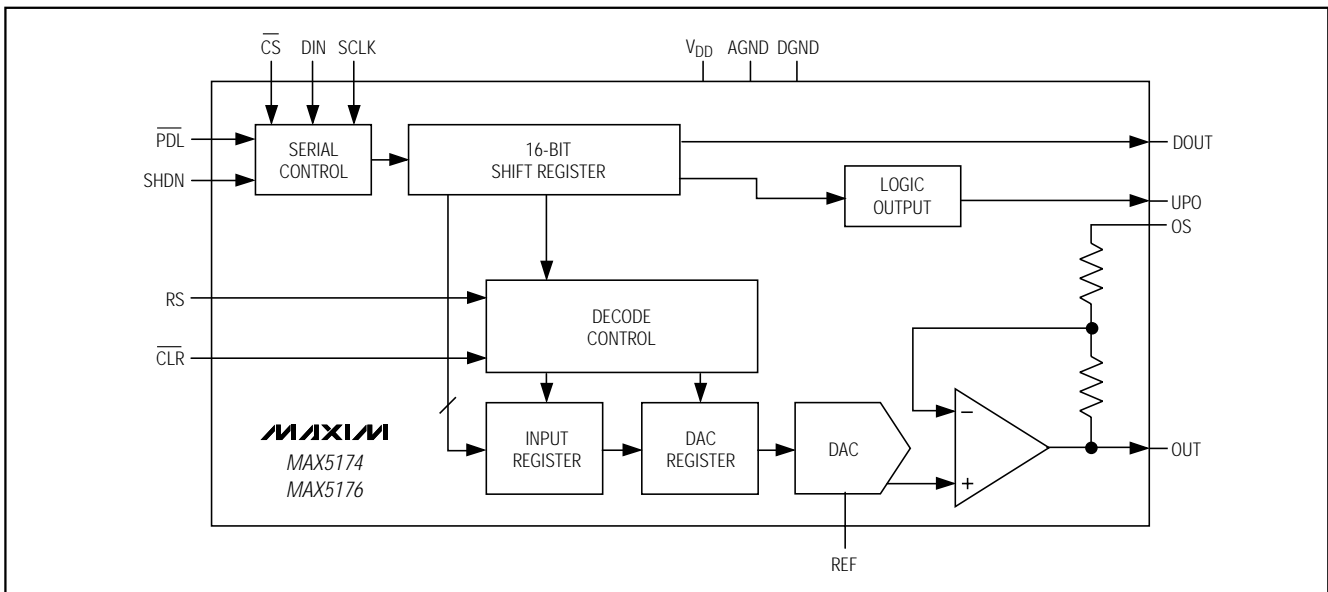


Figure 11. AC Reference Input Circuit

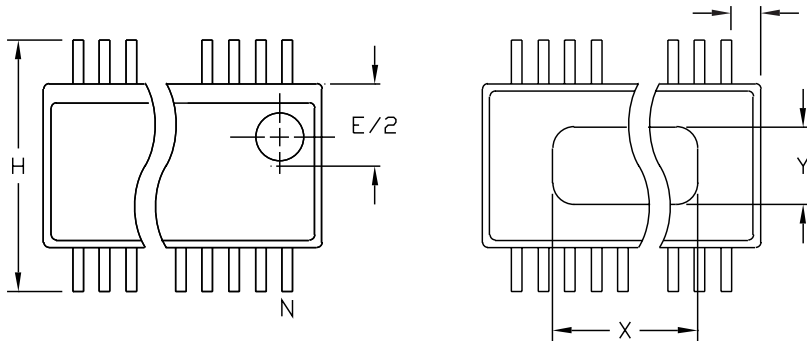
Functional Diagram



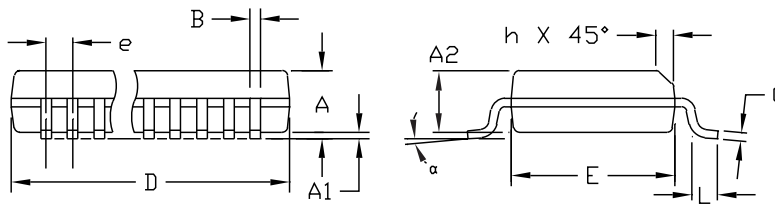
Low-Power, Serial, 12-Bit DACs with Voltage Output

Package Information

QSOP-EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°



VARIATIONS:

DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
D	.189	.196	4.80	4.98	16 AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20 AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSDP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

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[MCP47FVB04T-E/MQ](#) [MCP48FEB28T-E/MQ](#) [MCP48FVB28T-20E/ST](#) [MCP47FVB28T-20E/ST](#) [MCP47FEB24T-E/MQ](#) [MCP48FVB18T-20E/ST](#) [MCP47FEB14T-E/MQ](#) [MCP47FEB08T-E/MQ](#) [MCP48FVB08T-20E/ST](#) [MCP47FEB04T-E/MQ](#) [MCP47FVB04T-20E/ST](#)
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