19-4190; Rev 0; 7/08

EVALUATION KIT AVAILABLE

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

MAX17065

General Description

The MAX17065 provides the power-supply rails for active-matrix, organic light-emitting diode (OLED) displays.

The MAX17065 includes a step-up DC-DC converter, an inverting DC-DC converter, a regulated positive charge pump, a regulated negative charge pump, and a low-dropout linear regulator (LDO). Synchronous rectifiers are integrated into the IC, eliminating the need for external power components. An I²C interface is used to program the switching frequency, the operating mode, and the cycle-by-cycle current limit of the noninverting and step-up converters, as well as the output voltages of the inverting converter and the charge pumps. Efficiency of 94% can be achieved for the step-up and 83% for the inverting converter.

The MAX17065 is packaged into a space-efficient 28-pin, 4mm x 4mm TQFN package with an exposed backside pad (EP) to enhance thermal characteristics.

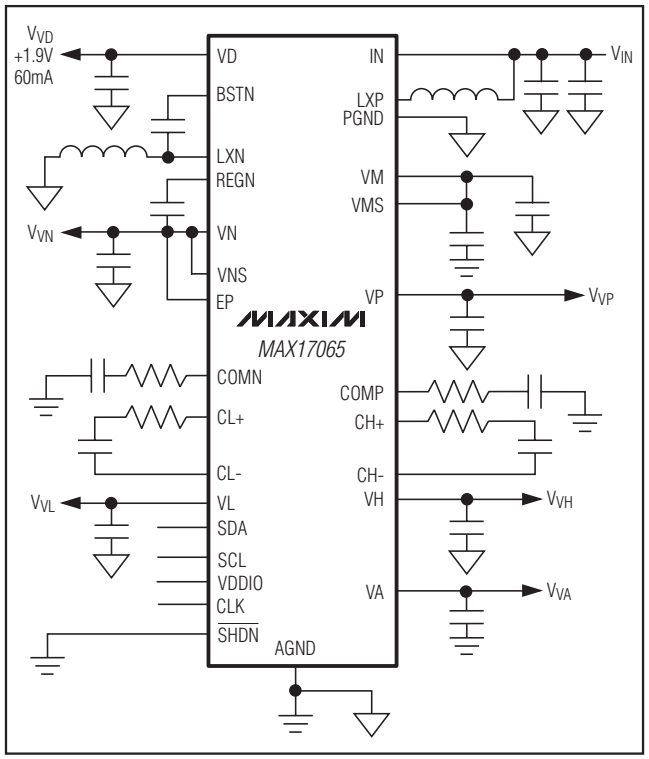
Applications

Cell Phones

Digital Still Cameras

MP3 Players

Minimal Operating Circuit



Features

- 2.3V to 4.5V Input Voltage Supply Range
- Fixed +5.35V Step-Up DC-DC Converter
- Adjustable -0.5V to -5.0V Inverting DC-DC Converter
- Adjustable 450mA/700mA Cycle-by-Cycle Current Limit for DC-DC Converters
- Selectable SKIP or Forced-PWM Mode for DC-DC Converters
- 600kHz/1.2MHz Selectable Fixed-Switching Frequency
- +5.5V to +9.0V Adjustable Positive-Regulated Charge Pump
- -5.0V to -0.5V Adjustable Negative-Regulated Charge Pump
- +1.9V 60mA LDO
- Integrated Synchronous Rectifiers
- True Shutdown™
- Output Undervoltage Shutdown with 100ms Timer
- Startup Sequence with 4ms Soft-Start
- 3µA (typ) Shutdown Supply Current
- Thermal Shutdown with 15ms Timer
- I²C Interface Control
- Greater than 90% Efficiency
- Small, 4mm x 4mm, 28-Pin Thin QFN

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17065ETI+	-40°C to +85°C	28 Thin QFN

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

ABSOLUTE MAXIMUM RATINGS

IN, SDA, SCL, VMS, VDDIO to AGND .....-0.3V to +6V
SHDN, CLK to AGND.....-0.3V to (V_{DDIO} + 0.3V)
COMP, COMN to AGND.....-0.3V to (V_{VMS} + 0.3V)
VD to AGND.....-0.3V to (V_{IN} + 0.3V)
LXP to PGND.....-0.3V to (V_{VM} + 0.3V)
VM to PGND .....-0.3V to +6V
VP to PGND.....(V_{VM} - 6V) to (V_{VM} + 6V)
VA to PGND.....-0.3V to (V_{VM} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
VN to PGND.....-9V to +0.3V
VNS to VN.....-0.3V to +0.3V
LXN to VN .....-0.3V to (V_{IN} + 0.3V)
REGN to VN.....-0.3V to +6V
BSTN to VN .....(V_{REGN} - 0.3V) to +18V
BSTN to LXN.....-0.3V to +6V
VH to PGND.....-0.3V to +14V
CH- to PGND .....-0.3V to (V_{VM} + 0.3V)
CH+ to PGND .....-0.3V to (V_{VH} + 6V)
VL to PGND .....-6V to +0.3V
CL+ to PGND .....-0.3V to (V_{VM} + 0.3V)
CL- to PGND .....(V_{VL} - 0.3V) to +0.3V
VD to AGND Short Circuit .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 20.8mW/°C above +70°C).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		2.3		4.5	V
IN Shutdown Supply Current + LXP Leakage Current	SHDN = low , V_{IN} = 4.5V, VD off, T_A = +25°C		3	7	µA
IN Standby Supply Current	VP, VN, VL, VH disabled, VD enabled, V_{IN} = 2.3V to 4.5V		300	600	µA
IN Undervoltage-Lockout (UVLO) Threshold	V_{IN} rising, typical hysteresis is 50mV	2.00	2.10	2.20	V
VD REGULATOR					
VD Output Voltage	V_{IN} = 2.3V to 4.5V, 0 < I_{LOAD} < 60mA	1.8	1.9	1.95	V
VD Undervoltage-Lockout Threshold	V_{VD} rising, typical hysteresis is 60mV	1.3	1.4	1.5	V
VD Short-Circuit Current		70		160	mA
STEP-UP REGULATOR					
VM Regulation Voltage	V_{IN} = 2.3V to 4.5V	5.25	5.35	5.45	V
VM Load Regulation	0 < I_{LOAD} < 120mA		0.1		%
VM Transconductance	ΔI = ±2.5µA at COMP, V_{VM} = 5.35V	20	35	70	µS
LXP Current-Sense Transresistance		0.5	0.75	1.0	V/A
VP-to-PGND Discharge Resistance	VP discharge mode		100	200	Ω
LXP-to-PGND On-Resistance	V_{VM} = 5.35V		0.25	0.5	Ω
LXP-to-VM On-Resistance	V_{VM} = 5.35V		0.5	1	Ω
LXP Current Limit	VSW register bit 5 = 1 (high value), duty = 38%	0.6	0.7	0.8	A
	VSW register bit 5 = 0 (low value), duty = 38%	0.36	0.45	0.54	
LXP-to-VM Zero-Crossing Threshold	Skip mode only		25		mA
LXP-to-IN Damping Switch Resistance	Skip mode, V_{VM} = 5.5V		100		Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LXP Negative Current Limit	Forced PWM only; it is a peak value; average value is (LXP negative current limit - $I_{RIPPLE}/2$)			-0.3		A
VM-to-VP On-Resistance	V_{VM} = 5.35V			0.4	0.8	Ω
VM-to-VA On-Resistance	V_{VM} = 5.35V			3	6	Ω
VP Leakage Current	V_{VP} = +8V, VM in regulation test mode, T_A = +25°C (Note 1)				10	µA
VM Soft-Start Time			3	4	5	ms
VP Soft-Start Time			3	4	5	ms
VA-to-PGND Discharge Resistance				100	200	Ω
VM-to-VA Impedance at Startup				100	200	Ω
VM-to-VA Delay to Low Impedance					1	ms
INVERTING REGULATOR						
VN Regulation Voltage Accuracy	V_{IN} = 2.3V to 4.5V with respect to the V_{VN} Table 9 voltage	V_{VN} = -0.5V	-7		+7	%
		V_{VN} = -1.0V, -1.5V or -2.0V	-4		+4	
		$V_{VN} \le$ -2.5V	-2		+2	
VN Load Regulation	0 < I_{LOAD} < 120mA			0.1		%
VN Transconductance	ΔI = ±2.5µA at COMN, V_{VN} = -4.5V		20	35	70	µS
LXN Current-Sense Transresistance			0.3	0.6	0.9	V/A
VN-to-PGND Discharge Resistance	VN discharge mode			120	250	Ω
LXN-to-IN On-Resistance	V_{VM} = 5.35V, V_{BSTN} - V_{LXN} = 4.5V			0.5	1	Ω
LXN-to-VN On-Resistance	V_{VM} = 5.35V			0.5	1	Ω
LXN Current Limit	VSW register bit 4 = 1 (high value), duty = 80%		0.6	0.7	0.8	A
	VSW register bit 4 = 0 (low value), duty = 80%		0.36	0.45	0.54	
LXN-to-VN Zero Crossing	Skip mode only			20		mA
LXN Negative Current Limit	Forced PWM only; it is a peak value; average value is (LXN negative current limit - $I_{RIPPLE}/2$)			-0.3		A
VN + VNS Leakage Current	V_{VN} = V_{VNS} = -8V, test mode, T_A = +25°C (Note 1)				20	µA
LXN-to-PGND Damping Switch Resistance				100		Ω
VN Soft-Start Time			3	4	5	ms
OSCILLATOR						
LXN, LXP Switching Frequency	V_{IN} = 3.3V	FSET = 1	1080	1200	1320	kHz
		FSET = 0	540	600	660	
LXN, LXP Maximum Duty Cycle			80	85	90	%
CLx, CHx Switching Frequency	V_{VH} = +6V, V_{VL} = -4V, FSET = 0		270	300	330	kHz
	V_{VH} = +6V, V_{VL} = -4V, FSET = 1		540	600	660	

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE PUMPS						
VH Adjustable Voltage Range	See Table 7 for output settings		5.5		9.0	V
VL Adjustable Voltage Range	See Table 8 for output settings (Note 3)		-5.0		-0.5	V
CH-, CL+ to VM, CH-, CL+ to PGND On-Resistance				4	8	Ω
CH+ to VM, CH+ to VH, CL- to VL, CL- to PGND On-Resistance				10	25	Ω
VH Voltage-Regulation Threshold	With respect to the V_{VH} Table 7 voltage, V_{VM} = 5.35V		-2		+2	%
VL Voltage-Regulation Threshold	With respect to the V_{VL} Table 8 voltage, V_{VM} = 5.35V	V_{VL} = -0.5V	-10		+10	%
		V_{VL} = -1.0V	-5		+5	
		V_{VL} = -1.5V or -2	-4		+4	
		$V_{VL} \le$ -2.5V	-2		+2	
VL Discharge Resistance				100	200	Ω
VH Discharge Resistance				100	200	Ω
VH Leakage Current	V_{VH} = +9V, test mode, T_A = +25°C (Note 1)				10	µA
VL Leakage Current	V_{VL} = -5.0V, test mode, T_A = +25°C (Note 1)				10	µA
VH Soft-Start Time			3	4	5	ms
VL Soft-Start Time			3	4	5	ms
PROTECTION						
VMS UVP Threshold Voltage	VMS falling, $V_{VMS} > V_{IN}$		4	4.2	4.4	V
VA UVP Threshold Voltage	V_A falling		4.15	4.37	4.59	V
VMS-to-V_{IN} Disable Threshold Voltage	VMS rising, typical hysteresis is 90mV		-0.35	-0.2	-0.1	V
VNS UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VNS rising	V_{VN} = -0.5V to -1.5V	27	60	90	%
		$V_{VN} \le$ -2.0V	74	80	85	
VH UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VH falling		75	80	85	%
VL UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VL rising	V_{VL} = -0.5V to -1.5V	27	60	90	%
		$V_{VL} \le$ -2.0V	74	80	85	
UVP Shutdown Delay			100	120	145	ms
Thermal Shutdown	Hysteresis = 20°C			160		°C
Thermal-Shutdown Delay			12	15	18	ms

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (SDA, SCL)					
I²C Frequency Range		10		100	kHz
SDA, SCL Input Logic-High Voltage		0.7 x V_{VD}			V
SDA, SCL Input Logic-Low Voltage				0.3 x V_{VD}	V
SDA, SCL Pullup Resistance to VD		5	10	20	kΩ
SDA Pulldown Current	V_{SDA} = 0.4V	10			mA
VDDIO Operating Voltage Range	V_{SDA} = 0.4V	1.6		5.5	V
VDDIO UVLO Threshold Voltage		1.2	1.4	1.6	V
VDDIO Bias Current	V_{CLK} = 0 or VDDIO, $\overline{SHDN}$ = open			2	µA
$\overline{SHDN}$, CLK Input Logic-High Voltage		0.7 x V_{VDDIO}			V
$\overline{SHDN}$, CLK Logic Input Logic-Low Voltage				0.3 x V_{VDDIO}	V
$\overline{SHDN}$ Pulldown Resistance		50	100	200	kΩ

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		2.3		4.5	V
IN Standby Supply Current	VP, VN, VL, VH disabled, VD enabled, V_{IN} = 2.3V to 4.5V			600	µA
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis is 50mV	2.05		2.20	V
VD REGULATOR					
VD Output Voltage	V_{IN} = 2.3V to 4.5V, 0 < I_{LOAD} < 60mA	1.8		1.95	V
VD Undervoltage-Lockout Threshold	V_{VD} rising, typical hysteresis is 60mV	1.25		1.6	V
VD Short-Circuit Current		55		180	mA

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP REGULATOR						
VM Regulation Voltage	V_{IN} = 2.3V to 4.5V		5.25		5.45	V
VM Transconductance	ΔI = ±2.5µA at COMP, V_{VM} = 5.35V		20		70	µS
LXP Current-Sense Transresistance			0.5		1.0	V/A
VP-to-PGND Discharge Resistance	VP discharge mode				200	Ω
LXP-to-PGND On-Resistance	V_{VM} = 5.35V				0.5	Ω
LXP-to-VM On-Resistance	V_{VM} = 5.35V				1	Ω
LXP Current Limit	VSW register bit 5 = 1 (high value), duty = 38%		0.6		0.8	A
	VSW register bit 5 = 0 (low value), duty = 38%		0.36		0.54	
LXP Negative Current Limit	Forced PWM only; it is a peak value; average value is (LXP negative limit - I_{RIPPLE}/2)		-0.3		-0.1	A
VM-to-VP On-Resistance	V_{VM} = 5.35V				0.8	Ω
VM-to-VA On-Resistance	V_{VM} = 5.35V		3		6	Ω
VM Soft-Start Time			3		5	ms
VP Soft-Start Time			3		5	ms
VA-to-PGND Discharge Resistance			100		200	Ω
VM-to-VA Impedance at Startup			100		200	Ω
VM-to-VA Delay to Low Impedance					1	ms
INVERTING REGULATOR						
VN Regulation Voltage Accuracy	V_{IN} = 2.3V to 4.5V with respect to the V_{VN} Table 9 voltage	V_{VN} = -0.5V	-7		+7	%
		V_{VN} = -1.0V, -1.5V or -2.0V	-4		+4	
		$V_{VN} \le$ -2.5V	-2		+2	
VN Transconductance	ΔI = ±2.5µA at COMN, V_{VN} = -4.5 V		20		70	µS
LXN Current-Sense Transresistance			0.3		0.9	V/A
VN-to-PGND Discharge Resistance	VN discharge mode				250	Ω
LXN-to-IN On-Resistance	V_{VM} = 5.35V, V_{BSTN} - V_{LXN} = 4.5V				1	Ω
LXN-to-VN On-Resistance	V_{VM} = 5.35V				1	Ω
LXN Current Limit	VSW register bit 4 = 1 (high value), duty = 80%		0.6		0.8	A
	VSW register bit 4 = 0 (low value), duty = 80%		0.345		0.54	
VN Soft-Start Time			3		5	ms

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR						
LXN, LXP Switching Frequency	V_{IN} = 3.3V	FSET = 1	1080		1320	kHz
		FSET = 0	540		660	
LXN, LXP Maximum Duty Cycle			80		90	%
CLx, CHx Switching Frequency	V_{VH} = 6V, V_{VL} = -4V, FSET = 0		270		330	kHz
	V_{VH} = 6V, V_{VL} = -4V, FSET = 1		540		660	
CHARGE PUMPS						
VH Adjustable Range	See Table 7 for output settings		5.5		9.0	V
VL Adjustable Range	See Table 8 for output settings (Note 3)		-5.0		-0.5	V
CH-, CL+ to VM, CH-, CL+ to PGND On-Resistance					8	Ω
CH+ to VM, CH+ to VH, CL- to VL, CL- to PGND On-Resistance					25	Ω
VH Voltage-Regulation Threshold	Typical values as per Table 7, V_{VM} = 5.35V		-2		+2	%
VL Voltage-Regulation Threshold	With respect to the V_{VL} Table 8 voltage, V_{VM} = 5.35V	V_{VL} = -0.5V	-10		+10	%
		V_{VL} = -1	-5		+5	
		V_{VL} = -1.5V or -2	-4		+4	
		V_{VL} = -2.5V or -4.5	-2		+2	
VL Discharge Resistance					200	Ω
VH Discharge Resistance					200	Ω
VH Soft-Start Time			3		5	ms
VL Soft-Start Time			3		5	ms
PROTECTION						
VMS UVP Threshold Voltage	VMS falling, $V_{VMS} > V_{IN}$		4.2		4.4	V
VA UVP Threshold Voltage	VA falling		4.15		4.59	V
VMS-to-IN Disable Threshold Voltage	VMS rising, typical hysteresis is 90mV		-0.35	-0.2	-0.1	V
VNS UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VNS rising	V_{VN} = -0.5V to -1.5V	27		90	%
		$V_{VN} \le$ -2.0V	74		85	
VH UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VH falling		75		85	%
VL UVP Threshold-Voltage Tolerance	With respect to the regulation voltage, VL rising	V_{VL} = -0.5V to -1.5V	27		90	%
		$V_{VL} \le$ -2.0V	74		85	
UVP Shutdown Delay			100		145	ms
Thermal-Shutdown Delay			12		18	ms

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VP, VN, VL, VH enabled, default output values set according to Tables 7, 8, 9, skip mode enabled, V_{VM} = 5.5V, V_{VN}, V_{VH}, V_{VL} set 50mV beyond their regulation points (not switching), V_{IN} = 3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

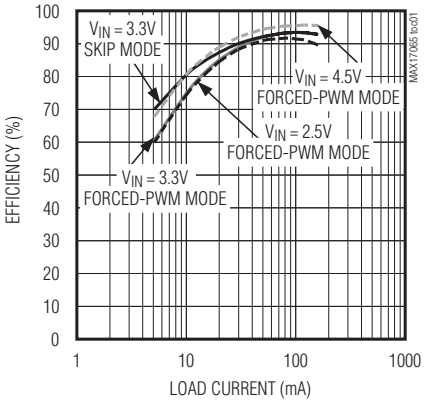
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (SDA, SCL)					
I²C Frequency Range		10		100	kHz
SDA, SCL Input Logic-High Voltage		0.7 x V_{VD}			V
SDA, SCL Input Logic-Low Voltage				0.3 x V_{VD}	V
SDA, SCL Pullup Resistance to VD		5		20	kΩ
SDA Pulldown Current	V_{SDA} = 0.4V	10			mA
VDDIO Voltage Range		1.6		5.5	V
VDDIO UVLO Threshold Voltage	VDDIO falling, typical hysteresis is 50mV	1.2		1.6	V
VDDIO Bias Current	V_{CLK} = 0 or V_{VDDIO}, $\overline{SHDN}$ unconnected			2	µA
$\overline{SHDN}$, CLK Input Logic-High Voltage		0.7 x V_{VDDIO}			V
$\overline{SHDN}$, CLK Input Logic-Low Voltage				0.3 x V_{VDDIO}	V
$\overline{SHDN}$ Pulldown Resistance		50		200	kΩ

Note 1: The 10µA leakage current at VN, VP, VH, VL is guaranteed only when the switching regulators are disabled. See Table 12.
Note 2: The T_A = -40°C specifications are guaranteed by design, not production tested.
Note 3: VL output current cannot exceed 1mA when VL is set at -5V.

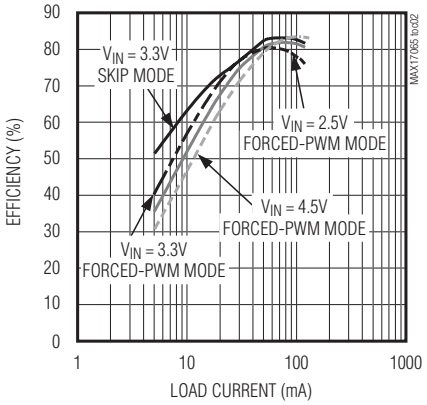
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

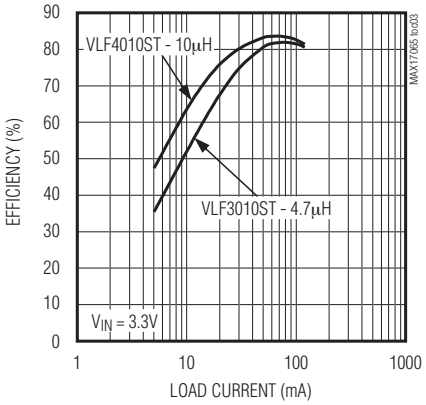
VM EFFICIENCY vs. LOAD CURRENT (f_{LXP} = 1.2MHz)



VN EFFICIENCY vs. LOAD CURRENT (f_{LXN} = 1.2MHz)



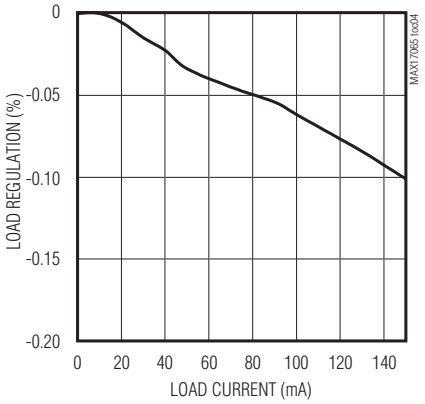
VN EFFICIENCY vs. LOAD CURRENT (f_{LXN} = 1.2MHz/FORCED-PWM MODE)



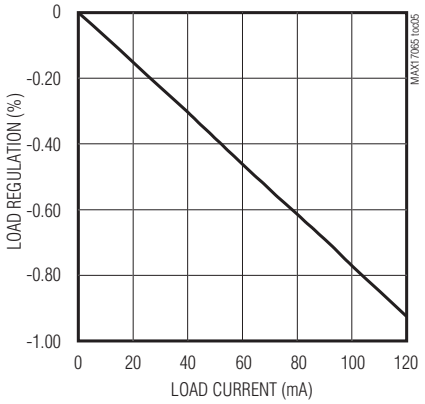
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

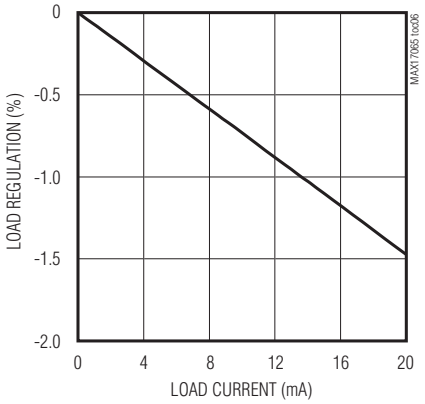
VM OUTPUT LOAD REGULATION (V_{IN} = 3.3V)



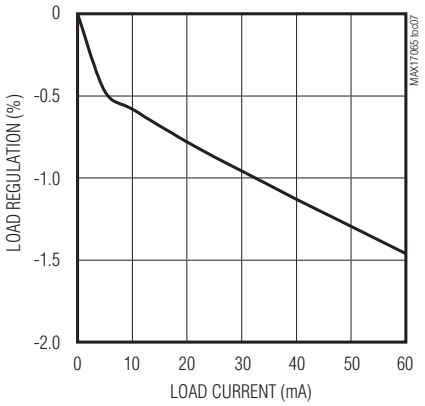
VP OUTPUT LOAD REGULATION (V_{IN} = 3.3V)



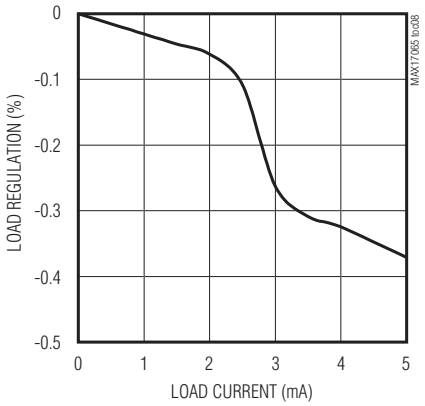
VA OUTPUT LOAD REGULATION (V_{IN} = 3.3V)



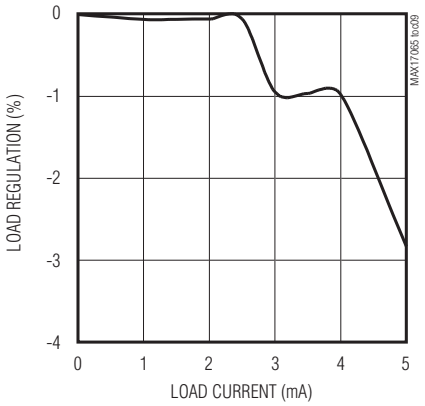
VD OUTPUT LOAD REGULATION (V_{IN} = 3.3V)



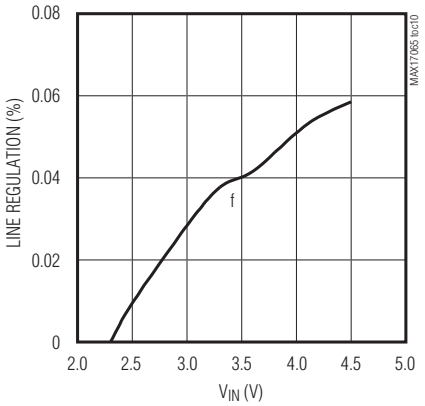
VH OUTPUT LOAD REGULATION (V_{VH} = 6.5V, C_{CH} = 2.2nF, R_{CH} = 47Ω)



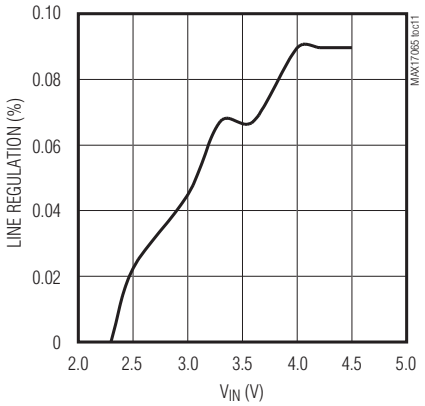
VL OUTPUT LOAD REGULATION (V_{VL} = 4.0V, C_{CL} = 10nF, R_{CL} = 47Ω)



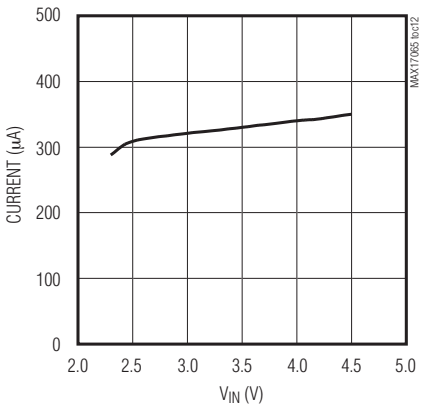
VP OUTPUT LINE REGULATION (I_{VP} = 120mA)



VN OUTPUT LINE REGULATION (V_{IN} = -4.5V, I_{VN} = 120mA)



IN STANDBY SUPPLY CURRENT

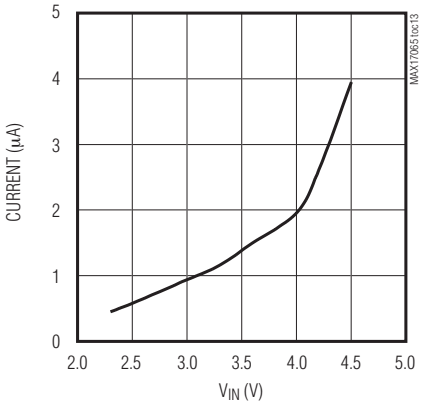


Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

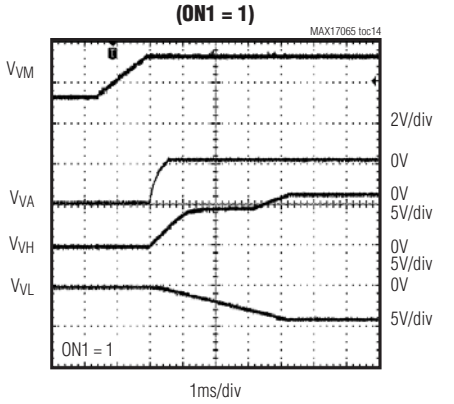
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

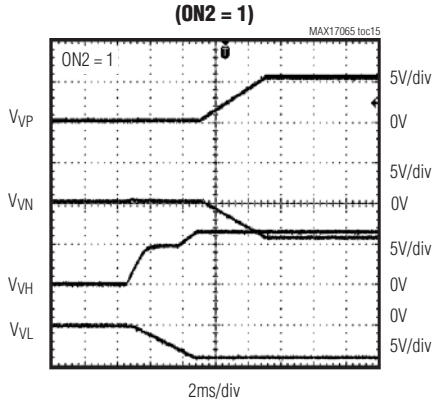
IN SHUTDOWN SUPPLY CURRENT



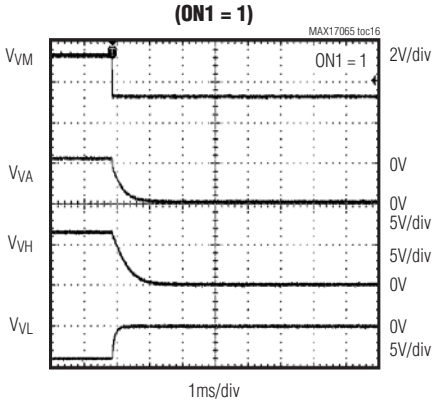
VM, VA, VH, AND VL STARTUP (ON1 = 1)



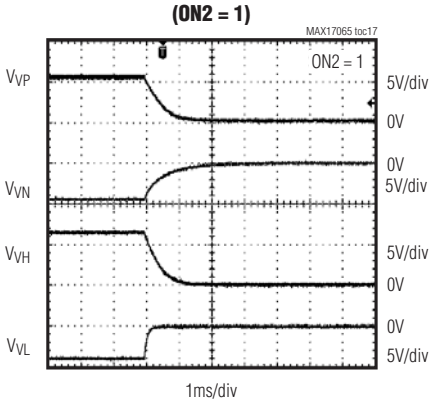
VH, VL, VP, AND VN STARTUP (ON2 = 1)



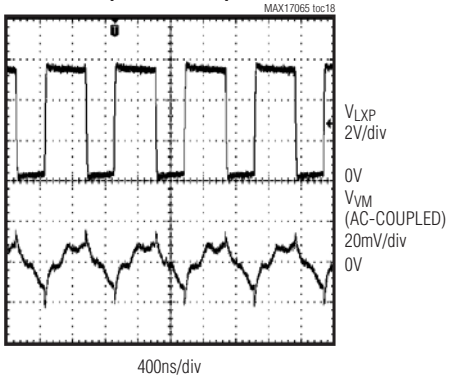
VM, VA, VH, AND VL SHUTDOWN (ON1 = 1)



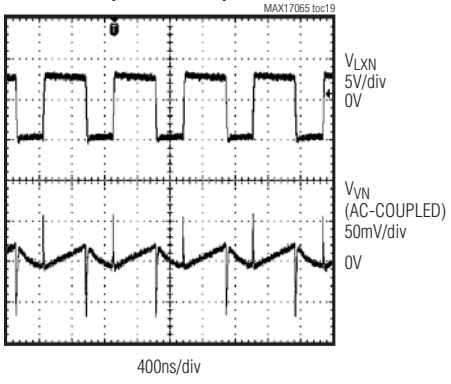
VH, VL, VP, AND VN SHUTDOWN (ON2 = 1)



LXP SWITCHING WAVEFORM (I_{VM} = 150mA)



LXN SWITCHING WAVEFORM (I_{VN} = 120mA)



Pin Description

PIN	NAME	FUNCTION
1	SDA	I²C-Compatible Serial Bidirectional Data Line. Internally connected to VD with a 10kΩ resistor.
2	CLK	External Wake-Up CMOS Oscillator. The fourth rising CLK pulse edge starts the IC. The CLK input frequency range is 10kHz to 10MHz.
3	VDDIO	Supply Voltage for CLK and $\overline{SHDN}$ Input Logic
4	VD	1.9V Low-Dropout Linear Regulator Output. Connect a 4.7µF capacitor to AGND.
5	AGND	Analog GND
6	$\overline{SHDN}$	Shutdown Control Input. Connect $\overline{SHDN}$ to VDDIO to force VD to be always on. This pin is internally pulled down to AGND through a 100kΩ resistor. Connect $\overline{SHDN}$ to AGND or open for shutdown. The MAX17065 can exit from the shutdown after the fourth rising CLK pulse edge.
7	COMN	Compensation Pin for the Inverting Converter Error Amplifier. Connect a series RC from COMN to AGND. Typical values are 33kΩ and 470pF.
8	VNS	Inverting Converter Voltage Sense. Connect to the VN output capacitor.
9	REGN	Regulated Supply that Provides V_{VN} + 5V for the Synchronous DMOS of the Inverting Converter. Bypass with a 0.1µF capacitor to VN.
10	VN	Inverting Converter Output. Connect a 4.7µF capacitor to PGND for 1.2MHz operating frequency.
11	BSTN	Boost Supply that Provides V_{LXN} + 5V for the DMOS of the Inverting Converter. Bypass with a 0.1µF capacitor to LXN.
12	LXN	Inverting Converter Switching Node. Connect inductor here and minimize trace area for lowest EMI.
13	IN	Supply Pin. Bypass IN with a minimum 10µF ceramic capacitor directly to PGND.
14	PGND	Power GND
15	N. C.	No Connection. Not internally connected.
16	LXP	Step-Up Converter Switching Node. Connect inductor here and minimize trace area for lowest EMI.
17	VM	Step-Up Converter Output. Connect a 4.7µF capacitor to PGND for 1.2MHz frequency operation.
18	VMS	Step-Up Converter Voltage Sense. Connect to the VM output capacitor. VMS also provides a clean power supply for internal precision circuitry. Bypass VMS to AGND with a 0.1µF capacitor.
19	VP	OLED Anode Voltage Supply. Powered from VM through an internal 0.4Ω MOSFET.
20	VA	Anode Voltage Supply. Powered from VM through an internal 3Ω MOSFET.
21	COMP	Compensation Pin for the Step-Up Converter Error Amplifier. Connect a series RC from COMP to AGND. Typical values are 33kΩ and 470pF.
22	VL	Negative Charge-Pump Output. Connect a 1µF capacitor to PGND.
23	CL-	Negative Charge-Pump Flying Capacitor Terminal. Connect 10nF + 100Ω between CL+ and CL- for typical application. See the Charge Pumps section in the *Electrical Characteristics* table for the capacitor selection.
24	CL+	Negative Charge-Pump Flying Capacitor Terminal. Connect 10nF +100Ω between CL+ and CL- for typical application. See the Charge Pumps section in the *Electrical Characteristics* table for the capacitor selection.
25	CH-	Positive Charge-Pump Flying Capacitor Terminal. Connect 2.2nF + 100Ω between CH+ and CH- for typical application. See the Charge Pumps section in the *Electrical Characteristics* table for the capacitor selection.
26	CH+	Positive Charge-Pump Flying Capacitor Terminal. Connect 2.2nF + 100Ω between CH+ and CH- for typical application. See the Charge Pumps section in the *Electrical Characteristics* table for the capacitor selection.
27	VH	Positive Charge-Pump Output. Connect a 1µF capacitor to PGND.
28	SCL	I²C-Compatible Clock Input and Output. Internally connected to VD with a 10kΩ resistor.
—	EP	Exposed Backside Pad. To ensure low thermal resistance, solder the backside pad to a copper plane that is **electrically connected to VN**. See the *PCB Layout and Grounding* section.

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

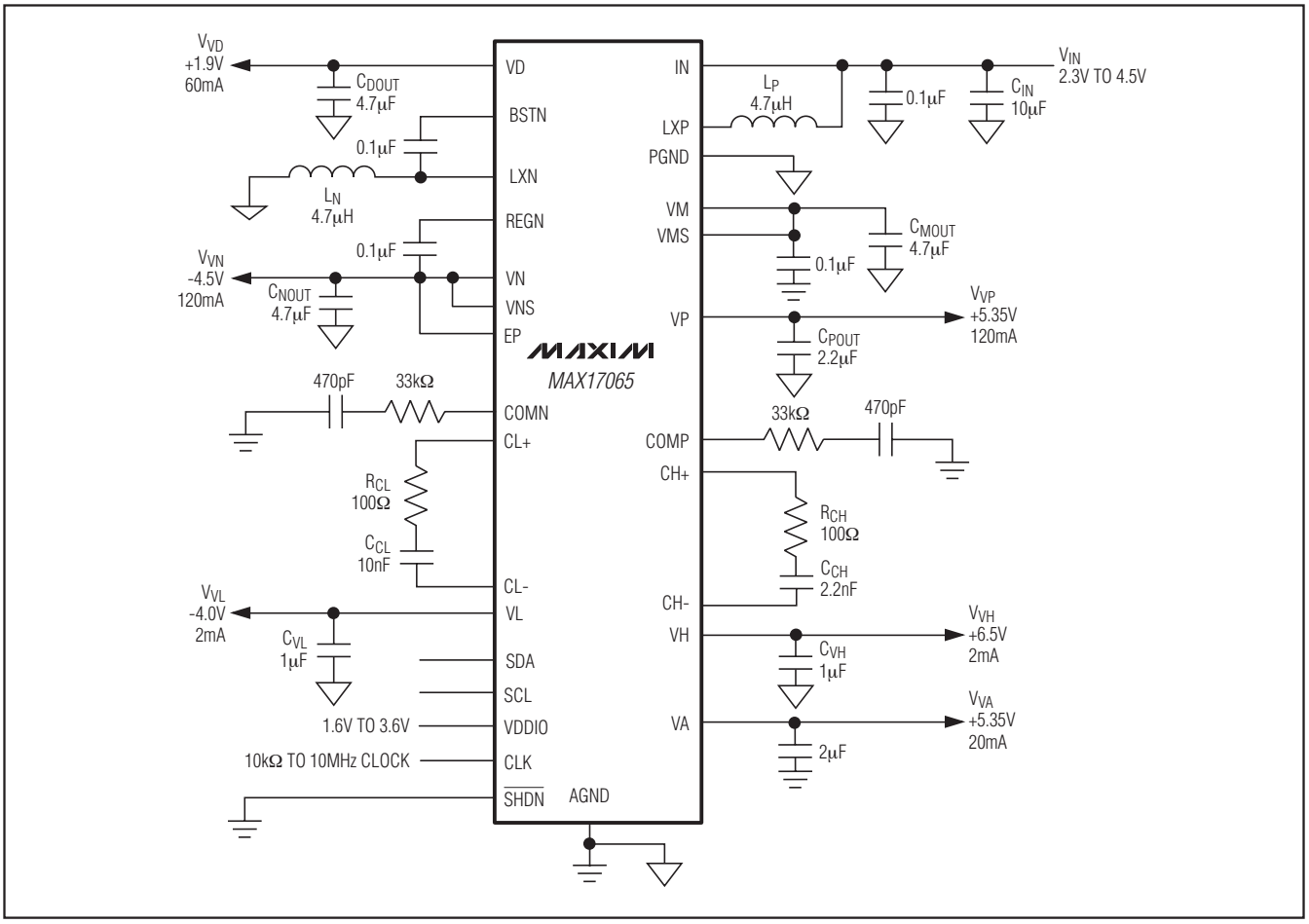


Figure 1. MAX17065 Typical Operating Circuit

Table 1. Component List

DESIGNATION	DESCRIPTION
C_{IN}	10µF ±10%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J106K Murata GRM188R60J106M
L_N	4.7µH, 0.75A, 0.15Ω inductor TDK VLF3010ST-4R7MR70
L_P	4.7µH, 0.75A, 0.15Ω inductor TDK VLF3010ST-4R7MR70 10µH, 0.8A, 0.25Ω inductor TDK VLF4010ST-100MR80
C_{MOUT}, C_{NOUT}, C_{DOUT}	4.7µF ±10%, 10V X5R ceramic capacitors (0805) Murata GRM219R61A475K TDK C2012X5R1A475K

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
TDK Corp.	847-803-	www.component.tdk.com

Typical Operating Circuit

The typical operating circuit of Figure 1 provides the power-supply rails for active-matrix OLED displays. Table 1 lists recommended components and Table 2 lists contact information for component suppliers.

Detailed Description

The MAX17065 provides all the power-supply rails for active-matrix OLED displays. It includes a step-up DC-DC converter, an inverting DC-DC converter, a regulated positive charge pump, a regulated negative charge pump, and a low-dropout linear regulator (LDO). Synchronous rectifiers are integrated into the device to minimize the number of external components, and to save circuit board space. Figure 2 is the MAX17065 functional diagram.

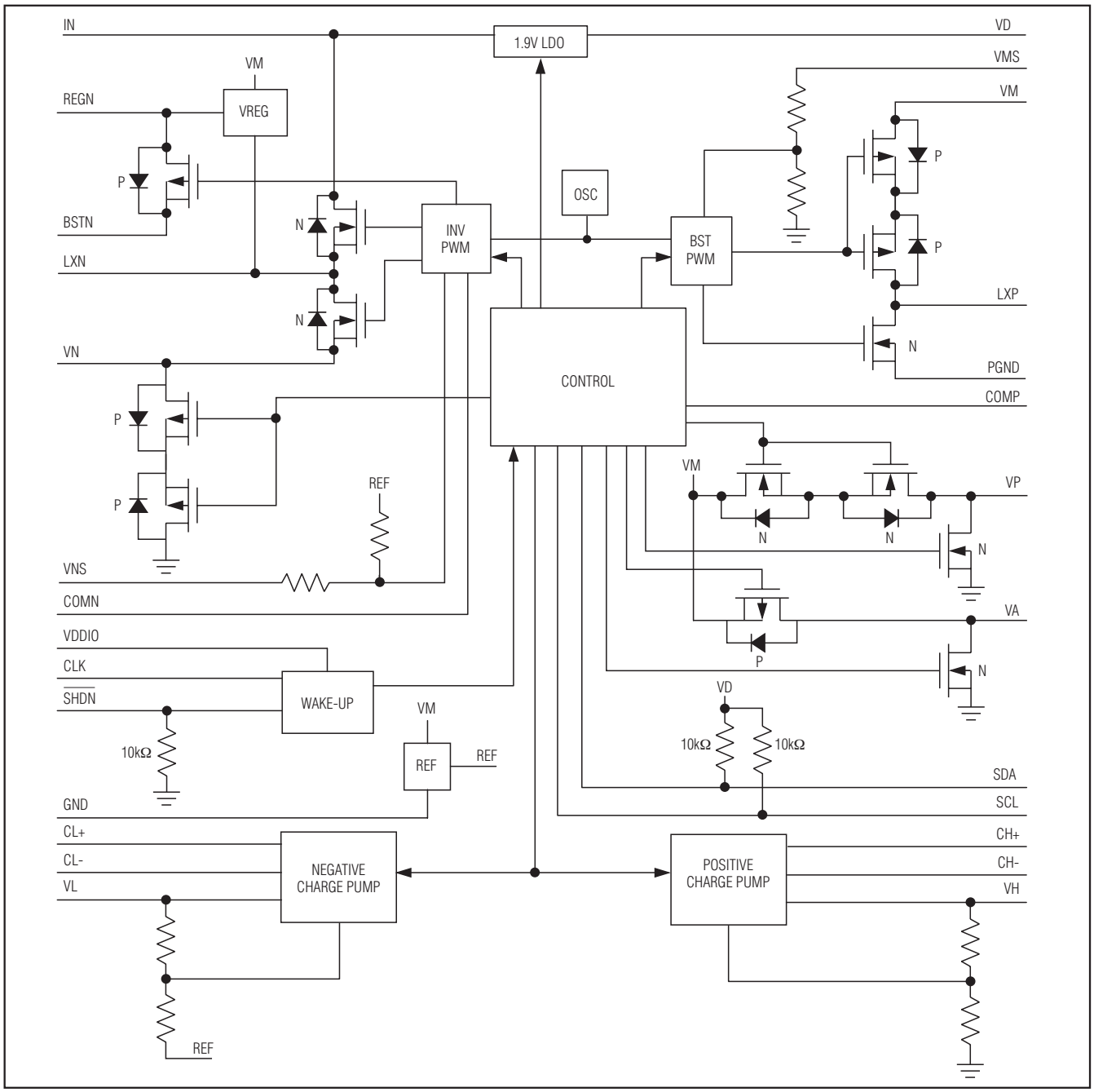


Figure 2. MAX17065 Functional Diagram

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

Step-Up Converter (VM)

The step-up converter provides a fixed output voltage of +5.35V and provides up to 150mA of output current used to power the anode voltage supply (VP), the analog voltage supply (VA), the positive charge pump (VH), the negative charge pump (VL), and some of the IC's internal circuitry through the step-up converter's output-voltage sense pin (VMS).

The I²C interface is used to select the switching frequency (600kHz or 1.2MHz), the operating mode (SKIP or forced PWM), and the cycle-by-cycle current limit (450mA or 700mA) of the step-up converter. Efficiency of 94% can be achieved. Because of the slope compensation used to stabilize the feedback loop, the inductor current limit depends on the duty cycle. The current limit is determined by the following equation:

$$I_{LP(LIM)} = I_{LP(LIM)\_EC} + 0.2A \times (0.38 - Duty)$$

where $I_{LP(LIM)\_EC}$ is the current limit specified at 38% duty cycle (see the *Electrical Characteristics*). The current-limit comparator delay is 60ns (typ) and the actual peak inductor current is increased by the delay.

Anode Voltage Supply (VP)

The anode voltage supply is created by connecting the output of the step-up converter VM directly to VP through an internal 0.4Ω (typ) MOSFET. VP can deliver up to 120mA to the OLED's anode.

Analog Voltage Supply (VA)

The analog voltage supply is created by connecting the output of the step-up converter VM directly to VA through an internal 3Ω (typ) MOSFET. The VA voltage is kept within 100mV from the VM regulated output. VA can deliver up to 20mA.

Inverting Converter (VN)

The inverting converter can be adjusted to provide an output voltage range of -5.0V to -0.5V and can deliver an output current up to 120mA. The I²C interface is used to set the output voltage, the switching frequency (600kHz or 1.2MHz), the operating mode (SKIP or forced PWM), and the cycle-by-cycle current limit (450mA or 700mA). An efficiency of 84% can be achieved. Because of the slope compensation used to stabilize the feedback loop, the inductor current limit depends on the duty cycle. The current limit is determined by the following equation:

$$I_{LN(LIM)} = I_{LN(LIM)\_EC} + 0.25A \times (0.8 - Duty)$$

where $I_{LN(LIM)\_EC}$ is the current limit specified at 80% duty cycle (see the *Electrical Characteristics*). The current-limit comparator delay is 60ns (typ) and the actual peak inductor current is increased by the delay.

Positive Charge-Pump Regulator (VH)

The positive charge-pump regulator is programmable through the I²C interface to provide an output voltage range of +5.0V to +9.0V and can provide an output current up to 2mA. The positive charge-pump regulator has an on-demand switching architecture to save power loss at light-load current. Figure 3 is the positive charge-pump regulator control block diagram.

Negative Charge-Pump Regulator (VL)

The negative charge-pump regulator is programmable through the I²C interface to provide an output voltage range of -5.0V to -0.5V and can provide an output current up to 2mA. Like the positive charge-pump regulator, the negative charge-pump regulator has an on-demand switching architecture to save power loss at light-load current as well. Figure 4 shows the negative charge-pump regulator control block diagram.

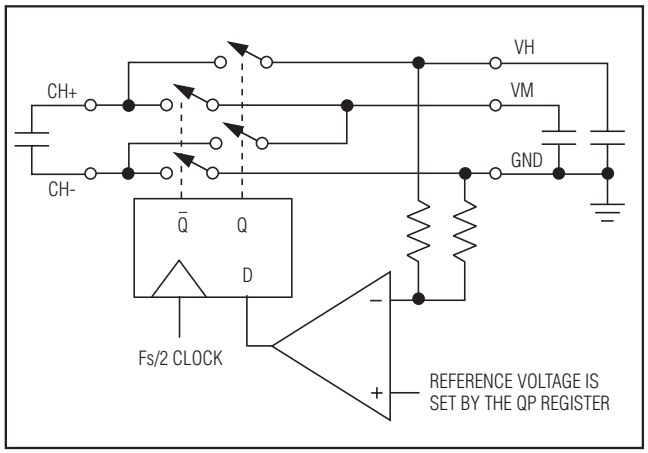


Figure 3. Positive Charge-Pump Regulator Control Block Diagram

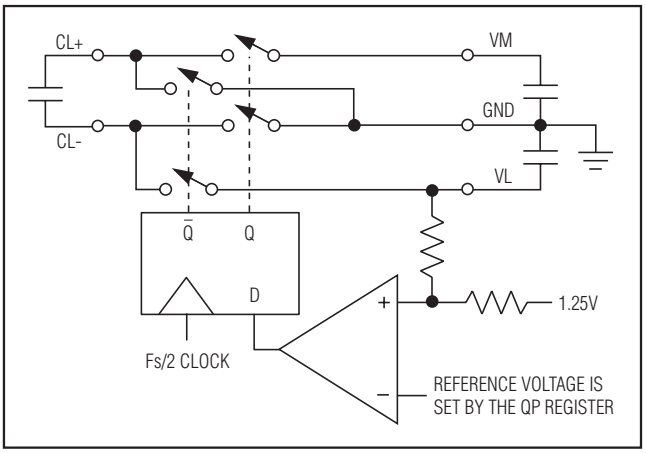


Figure 4. Negative Charge-Pump Regulator Block Diagram

Low-Dropout Linear Regulator (VD)

The LDO provides a fixed output voltage of 1.9V and can deliver up to 60mA. The LDO is active whenever the input voltage is higher than the input UVLO threshold if $\overline{SHDN}$ is connected to VDDIO. If $\overline{SHDN}$ is connected to AGND or left unconnected, the LDO is started only when activity on the CLK pin is detected.

True Shutdown

The MAX17065 completely disconnects the VA, VP, and VN loads from the input when the outputs are turned off. For most step-up converters, the external rectifying diode and inductor form a DC current path from the battery to the output. This can drain the battery even in shutdown if a load remains connected at the step-up converter output. The MAX17065 internal switches shut off, disconnecting the load from the battery. This load disconnect is referred to as True Shutdown.

Output Undervoltage Fault Protection

The MAX17065 provides output undervoltage fault protection (UVP) for all outputs. When a UVP fault is detected for one of the outputs VA, VN, VH, and VL for 120ms (typ), all outputs except VD latch off. The fault status is set in the status register, which can be read through the I²C interface. When a VM UVP fault is detected, the VM-VP switch latches off after a 30µs delay. If the VM UVP condition continues for a period longer than 120ms (typ), all remaining outputs except VD are latched off. For all UVP faults except a VD UVP fault, the fault latch can be cleared by writing zero for ON1 and ON2 to the control register. Since the I²C bus is pulled up to VD through a 10kΩ resistor, a VD UVP fault cannot be cleared by writing to the control register and can only be cleared by cycling the input power (below the VIN - UVLO falling threshold) or by removing the CLK signal with $\overline{SHDN}$ = low.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor activates the fault-protection latch after 15ms (typ), which shuts down all outputs including VD, allowing the device to cool down. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Since VD is latched off during a thermal-overload protection fault, the fault cannot be cleared through the I²C bus since the I²C bus is pulled up to VD through a 10kΩ resistor. The fault is cleared by either cycling the input power (below the V_{IN} - UVLO falling threshold) or by removing the CLK signal with $\overline{SHDN}$ = low. See Table 3.

Table 3. Status of Each Output Due to a Fault Condition

FAULT			REACTION AFTER THE FAULT	
OVER-TEMPERATURE	VD	ANY OTHER OUTPUTS	VD	OTHER OUTPUTS
Fault	x	x	Off	Off
Good	Fault	x	Off	Off
Good	Goo	Fault	On	Off

I²C Interface (SDA, SCL)

The MAX17065 supports an I²C-compatible, 2-wire digital interface. SDA is the bidirectional data line and SCL is the clock line of the 2-wire interface corresponding, respectively, to SDA and SDL lines of the I²C bus. The MAX17065 uses the write-byte and read-byte protocols (Figures 5 and 6). The I²C protocols are documented in the I²C-bus specification and user manual and are available at http://www.nxp.com/. The MA17065 is a slave-only device and responds to the 7-bit address 0b0100111. The read and write commands can be distinguished by adding 1 more bit (R/$\overline{W}$ bit) to the end of the 7-bit slave address, with one indicating read, and zero indicating write. The MAX17065 has six registers: a device control register (0x00), a VQP register (0x01), a VSW register (0x02), a status register (0x03), an MFG register (0x04), and an IREG register (0x05).

WRITE BYTE FORMAT

ST	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	STOP
	7 bits			8 bits		8 bits		

READ BYTE FORMAT

ST	ADDRESS	WR	ACK	COMMAND	ACK	RST	ADDRESS	RD	ACK	DATA	///	STOP
	7 bits			8 bits			7 bits	1		8 bits		

Figure 5. I²C Protocols

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

Communication starts with the master signaling the beginning of a transmission with a START condition, which is a high-to-low transition on SDA while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition, which is a low-to-high transition on SDA while SCL is high. The bus is then free for another transmission. Figures 6 and 7 show the timing diagrams for signals on the 2-wire interface. The address byte, command byte, and data byte are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit words and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX17065 since either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. If the MAX17065 receives its correct slave address followed by R/W = 0, it expects to receive 1 or 2 bytes of information (depending on the protocol). If the device detects a START or STOP condition prior to clocking in the bytes of data, it considers this an error condition and disregards all the data. If the transmission is completed correctly, the registers are updated immediately after a STOP (or RESTART) condition. If the MAX17065 receives its correct slave address followed by R/W = 1, it expects to clock out the register data selected by the previous command byte.

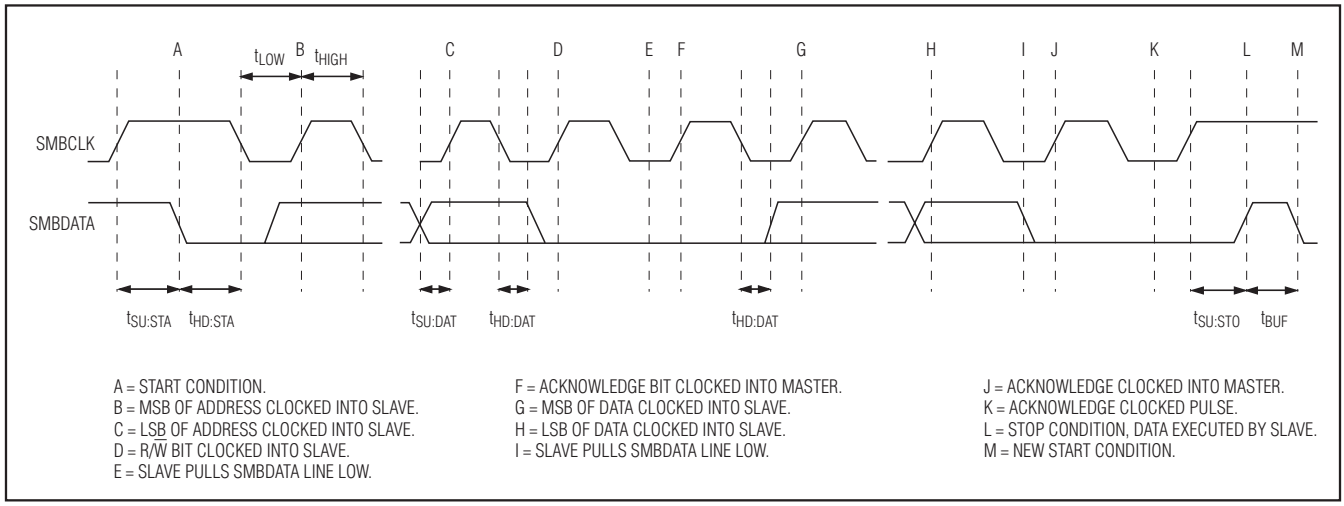


Figure 6. I²C Write Timing

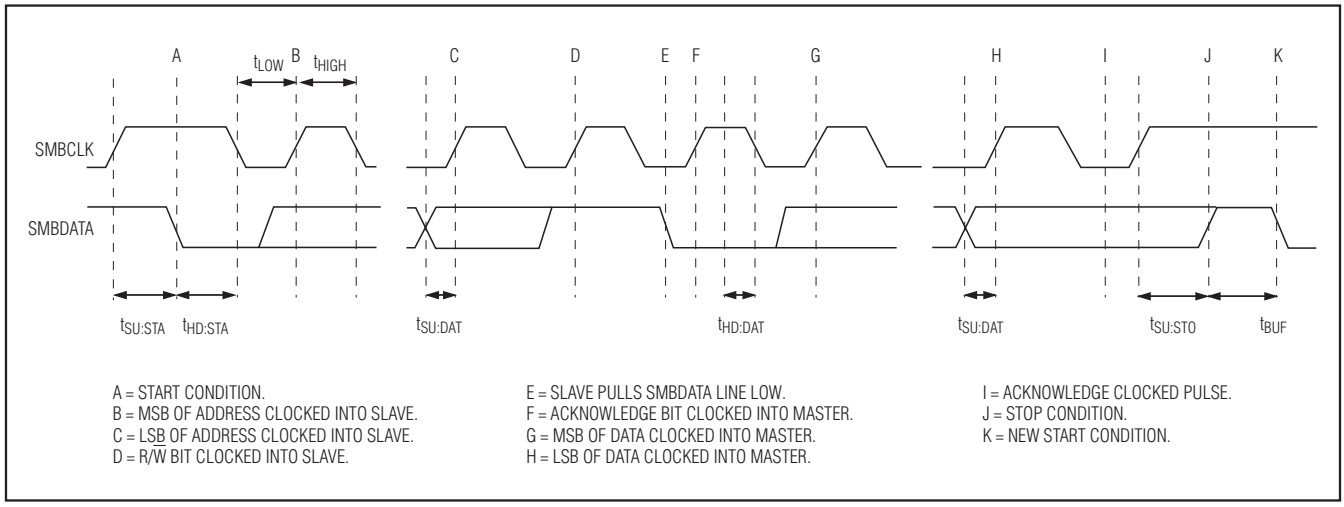


Figure 7. I²C Read Timing from the RESTART Condition

I²C Register Definitions

All MAX17065 registers are byte wide and accessible through the read/write byte protocols mentioned in the previous section. Their bit assignments are provided in the following sections with reserved bits containing a default value of zero. Table 4 summarizes the register assignments. During shutdown, the serial interface remains fully functional.

Control Register (0x00)

The control register enables and disables the VA, VH, VL, VP, and VN outputs. Also, the operating frequency and the mode of operation for the step-up and inverting converters are controlled by this register.

Output Enable and Fault Latch Reset

Setting ON1 to 1 enables VM to start up and the VA, VH, and VL outputs begin their soft-start procedures. Setting ON1 to 0 triggers a VA, VH, and VL shutdown sequence. Toggling ON1 to 0 has no effect if ON1 was previously set to 1 for less than 6ms or if ON2 is currently set to 1.

Setting ON2 to 1 enables the VP and VN soft-start procedure. Setting ON2 to 0 triggers the VP and VN shutdown sequence. Toggling ON2 to 0 has no effect if ON2 was previously set to 1 for less than 6ms. See Table 5.

Setting both ON1 and ON2 to 0 clears the fault latches (see the *Status Register (0x03)* section).

Step-Up and Inverting Converter Operating Mode

Set SKIP/PWM to 0 for forced PWM or to 1 for skip-mode operation of the step-up and inverting converters (VM and VN regulated outputs). If no value is written to SKIP/PWM, forced-PWM mode is selected by default (Table 6).

Step-Up and Inverting Converter Operating Frequency Selection

Setting the FSET bit chooses the switching frequency for the step-up and inverting converters (VM and VN regulated outputs). Set FSET to 0 for 600kHz operation or to 1 for 1.2MHz operation. If no value is written to FSET, the 600kHz frequency is selected by default. See Table 7.

VQP Register (0x01)

The VQP register is used to set both VL and VH output regulation voltages.

Table 4. Commands Description

COMMAND BYTE	REGISTER NAME	DATA-REGISTER BIT ASSIGNMENT							
		BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0x00	Control register	Reserve	FSET	$\overline{\text{SKIP}}$/PWM	Reserve	Reserve	Reserve	ON2	ON1
0x01	VQP register	VL3	VL2	VL1	VL0	Reserve	VH2	VH1	VH0
0x02	VSW register	TEST1	TEST0	IMAXP	IMAXN	VN3	VN2	VN1	VN0
0x03	Status register	VA fault	Reserve	Reserve	Reserve	VL fault	VH fault	VN fault	VM fault
0xFE	MFG register	0	1	0	0	1	1	0	1
0xFF	IDREG	0	1	0	0	1	1	1	1

Table 5. ON2 and ON1

ON2	ON1	VA OUTPUT	VH, VL OUTPUTS	VP, VN OUTPUT	NOTES
0	0	OFF	OFF	OFF	Clears fault latch.
0	1	ON	ON	OFF	—
1	0	ON	ON	ON	VP/VN are turned on after when VH/VL soft-start is completed.
1	1	ON	ON	ON	VP/VN are turned on after when VH/VL soft-start is completed.

Table 6. SKIP/PWM

SKIP/PWM	OPERATING MODE	NOTES
0	Forced PWM	Default condition
1	SKIP	—

Table 7. FSET

FSET	OPERATING FREQUENCY (MHz)	NOTES
0	0.6	Default condition
1	1.2	—

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

Positive Charge-Pump Regulation Voltage (VH)

Set the VH bits to program the VH regulation voltage according to Table 8.

Table 8. VH[2:0]

VH[2:0]	VH REGULATION VOLTAGE (V)	NOTES
0b000	5.5	Default condition
0b001	6.0	—
0b010	6.5	—
0b011	7.0	—
0b100	7.5	—
0b101	8.0	—
0b110	8.5	—
0b111	9.0	—

Negative Charge-Pump Regulation Voltage (VL)

Set the VL bits to program the VL regulation voltage according to Table 9.

Table 9. VL[3:4]

VL[3:4]	VN REGULATION VOLTAGE (V)	NOTES
0b0000	-0.5	Default condition
0b0001	-1.0	—
0b0010	-1.5	—
0b0011	-2.0	—
0b0100	-2.5	—
0b0101	-3.0	—
0b0110	-3.5	—
0b0111	-4.0	—
0b1000	-4.5	—
0b1001	-5.0	—

VSW Register (0x02)

The VSW register sets the VN regulation voltage and sets the maximum current limit for LXP and LXN. Also, this register can be programmed to disable the VH, VL, VP, and VN outputs such that they can be driven by external voltage sources.

VN Regulation Voltage

Set the VN bits to program the output voltage of VN according to Table 10.

LXN Peak Current Limit

The IMAXN bit is used to select the peak LXN current for the inverting converter. Setting IMAXN to 0 selects an LXN peak current limit of 450mA (typ), while setting

Table 10. VN[3:0]

VN[3:0]	VN REGULATION VOLTAGE (V)	NOTES
0b0000	-0.5	Default condition
0b0001	-1.0	—
0b0010	-1.5	—
0b0011	-2.0	—
0b0100	-2.5	—
0b0101	-3.0	—
0b0110	-3.5	—
0b0111	-4.0	—
0b1000	-4.5	—
0b1001	-5.0	—

IMAXN to 1 selects an LXN peak current limit of 700mA (typ). If no value is written to IMAXN, the LXN current limit is set to 450mA (typ) by default. See Table 11.

Table 11. IMAXN

IMAXN	OPERATING MODE (mA)	NOTES
0	450	Default condition
1	700	—

LXP Peak Current Limit

The IMAXP bit is used to select the peak LXP current for the step-up converter. Setting IMAXP to 0 selects an LXP peak current limit of 450mA (typ), while setting IMAXP to 1 selects an LXP peak current limit of 700mA (typ). If no value is written to IMAXP, the LXNP current limit is set to 450mA (typ) by default. See Table 12.

Table 12. IMAXP

IMAXP	OPERATING MODE (mA)	NOTES
0	450	Default condition
1	700	–

TEST Bits

Setting the TEST bits disables the VH, VL, VP, and VN outputs. In this mode, these outputs can be driven by external voltage sources. Maximum acceptable external voltages are +10V for VH, -5.5V for VL, +8V for VP, and -8V for VN.

When either of the 2 TEST bits is set to 1, all discharge functions are disabled. VA, VH, VL, VP, and VN are still controlled by ON1 and ON2 bits only when they are listed as allowed in Table 13.

Table 13. TEST1 and TEST0

TEST1	TEST0	VA OUTPUT	VH OUTPUT	VL OUTPUT	VP OUTPUT	VN OUTPUT	DISCHARGE
0	**0**	**Allowed**	**Allowed**	**Allowed**	**Allowed**	**Allowed**	**Yes**
0	1	Allowed	Allowed	Allowed	Not allowed	Not allowed	No
1	0	Allowed	Allowed	Allowed	Allowed	Not allowed	No
1	1	Allowed	Not allowed	Not allowed	Not allowed	Not allowed	No

Status Register (0x03)

This read-only register allows the fault status to be read through the I²C interface. The bits are 0 during normal operation and also when the outputs are disabled. During a fault condition, the corresponding fault bit is forced to 1 for any undervoltage condition occurring after a 120ms (typ) delay.

MFG and IDREG Registers (0xFE 0xFF)

These read-only registers contain the manufacturing ID and the chip revision.

Startup and Shutdown Sequence

Figure 8 shows the startup and shutdown sequence.

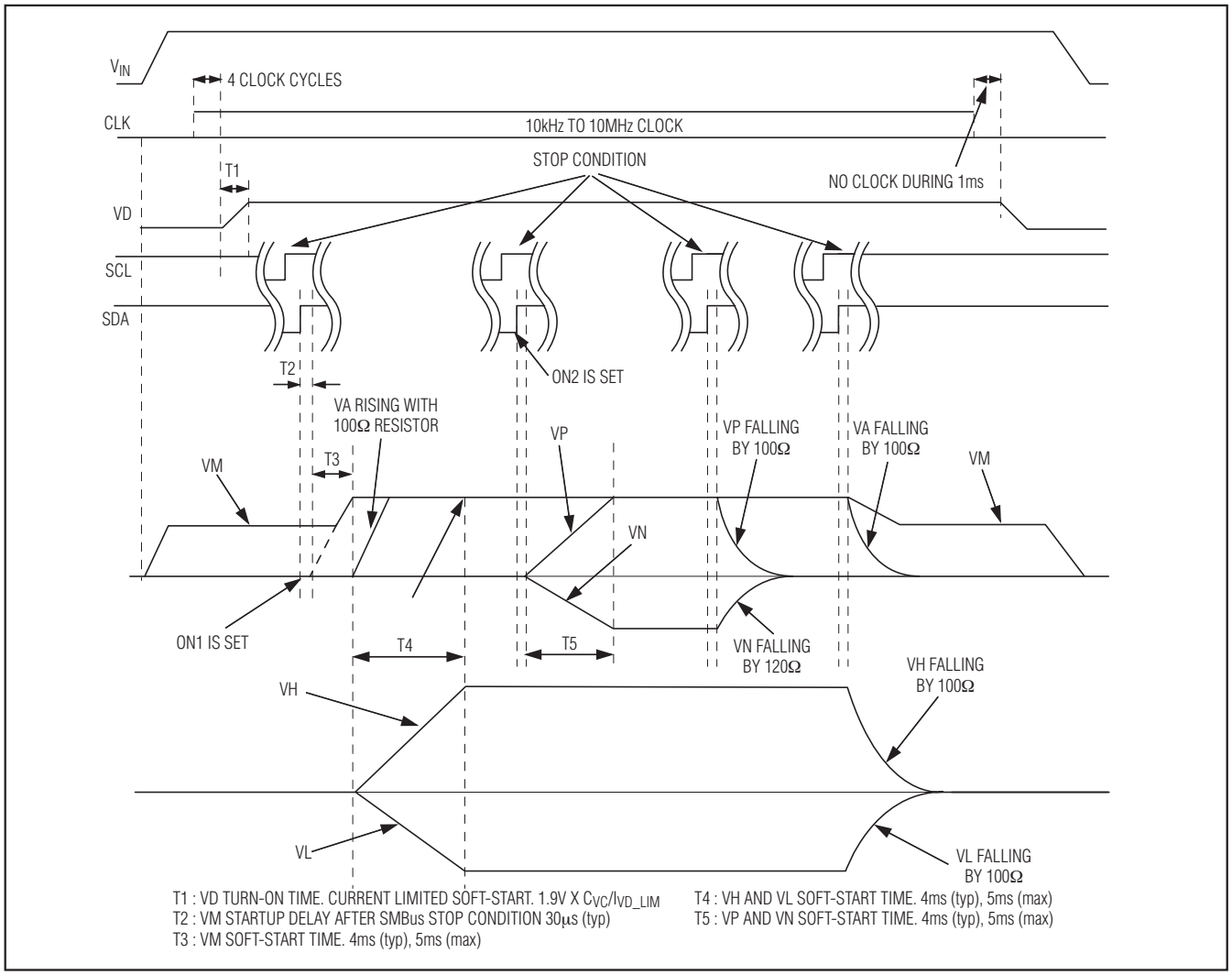


Figure 8. Startup and Shutdown Sequence

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

Table 14. Output States

V_{IN}	($\overline{SHDN}$)	ON2	ON1	STATE	VD	VM	VA	VH	VL	VP	VN
< UVLO	x	x	x	All OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
> UVLO	High	x	x	X	ON	Status defined by ON1 and ON2 as in the last 4 lines					
> UVLO	Low CLK idle	X	X	Shutdown	OFF	OFF	OFF	OFF	OFF	OFF	OFF
> UVLO	Low CLK active	L	L	Standby	ON	OFF	OFF	OFF	OFF	OFF	OFF
		L	H	VM, VA, VH/VL = ON		< UVLO	OFF	OFF	OFF	OFF	OFF
						> UVLO	ON	ON	ON	OFF	OFF
		H	L	VP/VN = ON		ON	ON	ON	ON	ON	ON
		H	H								

Design Procedure

Inductor Selections

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductors for the step-up and inverting converters. These factors influence the converters' efficiencies, maximum output-load capabilities, transient response times, and output voltage ripples. Physical size and cost are also important factors to be considered.

The maximum output currents, input voltages, output voltages, and switching frequencies determine the inductor values. Very-high-inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low-inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the required inductance, the maximum DC current, the inductor ripple current, and the peak inductor current using the following equations to choose an inductor value from an appropriate inductor family. The inductor's saturation current rating and the LXP and LXN current limits should exceed the peak currents calculated above. The inductor's DC current rating should exceed the maximum expected DC current. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Step-Up Converter Inductor (L_P)

Use the following procedure below to choose the inductor for the inverting converter. An example is provided below using a typical operating condition of:

- $V_{IN(TYP)}$ = 3.3V: The typical operating input voltage.
- $V_{IN(MIN)}$ = 2.3V: The minimum operating input voltage.
- $I_{VM(MAX)}$ = 150mA: The maximum output current for the step-up converter.
- $\eta_{(TYP)}$ = 0.9: The expected efficiency at the typical operating condition for the step-up converter.
- $\eta_{(MIN)}$ = 0.87: The worst-case efficiency expected at the minimum operating input voltage and maximum output current for the step-up converter.
- f_{SW} = 1.2MHz: The switching frequency for the inverting converter.

1) Calculate the required inductance:

$$L_P = \left(\frac{V_{IN(TYP)}}{5.35V}\right)^2 \left(\frac{5.35V - V_{IN(TYP)}}{I_{VM(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{(TYP)}}{LIR}\right)$$

$$= \left(\frac{3.3V}{5.35V}\right)^2 \left(\frac{5.35V - 3.3V}{0.150A \times 1.2 \times 10^6 Hz}\right)\left(\frac{0.9}{0.8}\right)$$

$$= 4.87 \times 10^{-6} H$$

Choose L_P = 4.7µH.

2) Calculate the maximum DC current in the inductor to select an inductor whose DC current rating is less than the maximum DC current calculated:

$$I_{LP(DC,MAX)} = \frac{I_{VM(MAX)} \times 5.35V}{V_{IN(MIN)} \times \eta_{(MIN)}} = \frac{0.150A \times 5.35V}{2.3V \times 0.87} = 401mA$$

3) Calculate the peak amplitude of the inductor current to choose an inductor with a saturation current rating less than the peak inductor current calculated. Also, use this result to verify that the peak inductor current amplitude is below the minimum current rating of LXN:

$$I_{P(PEAK)} = I_{LP(DC,MAX)} + \frac{V_{IN(MIN)} \times (5.35V - V_{IN(MIN)})}{2 \times L_P \times 5.35V \times f_{SW}} = 401mA + \frac{2.3V \times (5.35V - 2.3V)}{2 \times 4.7 \times 10^{-6} \times 5.35V \times 1.2 \times 10^{6}Hz} = 517mA$$

Inverting Converter Inductor (L_N)

Use the following procedure to choose the inductor for the inverting converter. An example is provided below using a typical operating condition of:

- $V_{IN(TYP)}$ = 3.3V: The typical operating input voltage.
- $V_{IN(MIN)}$ = 2.3V: The minimum operating input voltage.
- I_{VN} = -4.5V: The output voltage of the inverting converter.
- $V_{N(MAX)}$ = 120mA: The maximum output current for the inverting converter.
- $\eta_{(TYP)}$ = 0.9: The expected efficiency at the typical operating condition for the inverting converter.
- $\eta_{(MIN)}$ = 0.87: The worst-case efficiency expected at the minimum operating input voltage and maximum output current for the inverting converter.
- f_{SW} = 1.2MHz: The switching frequency for the inverting converter.

1) Calculate the required inductance:

$$L_N = \left(\frac{V_{IN(TYP)}}{(\eta_{(TYP)} \times V_{IN(TYP)}) + |V_{VN}|}\right)^2 \left(\frac{|V_{VN}| \times \eta_{(TYP)}}{f_{SW} \times I_{VN(MAX)} \times LIR}\right) = \left(\frac{3.3V}{(0.8 \times 3.3V) + |-4.5V|}\right)^2 \left(\frac{|-4.5V| \times 0.8}{1.2 \times 10^{6}Hz \times 0.120A \times 0.8}\right) = 6.67 \times 10^{-6}H$$

Choose L_N = 6.8µH for better efficiency or LN = 4.7µH for smaller physical inductor size.

2) Calculate the maximum DC current in the inductor to select an inductor whose DC current rating is less than the maximum DC current calculated:

$$I_{LN(DC,MAX)} = I_{VN(MAX)} \times \left[1 + \frac{|V_{VN}|}{\eta_{(MIN)} \times V_{IN(MIN)}}\right] = 0.120A \times \left[1 + \frac{|-4.5V|}{0.8 \times 2.3V}\right] = 0.413A$$

3) Calculate the peak amplitude of the inductor current to choose an inductor with a saturation current rating less than the peak inductor current calculated. Also, use this result to verify that the peak inductor current amplitude is below the minimum current rating of LXN:

$$I_{LN(PEAK)} = I_{LN(DC,MAX)} + \left(\frac{V_{IN(MIN)}}{2 \times L_N \times f_{SW}}\right)\left(\frac{|V_{VN}|}{V_{IN(MIN)} + |V_{VN}|}\right) = 0.413A + \left(\frac{2.3V}{2 \times 4.7 \times 10^{-6}H \times 1.2 \times 10^{6}Hz}\right)\left(\frac{|-4.5V|}{2.3 + |-4.5V|}\right) = 0.548A$$

VM and VN Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

For the step-up converter:

$$V_{VM\_RIPPLE} = V_{VM\_RIPPLE(C)} + V_{VM\_RIPPLE(ESR)}$$

$$V_{VM\_RIPPLE(C)} \approx \left(\frac{I_{VM}}{C_{MOUT} \times f_{SW}}\right)\left(\frac{5.35V - V_{IN}}{5.35V}\right)$$

and:

$$V_{VM\_RIPPLE(ESR)} \approx I_{LP(PEAK)} \times R_{ESR\_CMOUT}$$

where:

C_{MOUT} = The step-up converter's output capacitance.

$I_{LN(PEAK)}$ = The step-up converter's peak inductor current from the *Inductor Selections* section.

For the inverting converter:

$$V_{VN\_RIPPLE} = V_{VN\_RIPPLE(C)} + V_{VN\_RIPPLE(ESR)}$$

$$V_{VN\_RIPPLE(C)} \approx \left(\frac{I_{VN}}{C_{NOUT} \times f_{SW}}\right)\left(\frac{|V_{VN}|}{V_{IN} + |V_{VN}|}\right)$$

and:

$$V_{VN\_RIPPLE(ESR)} \approx I_{LN(PEAK)} R_{ESR\_CAP\_CNOUT}$$

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

where:

C_{NOUT} = The inverting converter's output capacitance.

$I_{LN(PEAK)}$ = The inverting converter's peak inductor current from the *Inductor Selections* section.

For ceramic capacitors, the output-voltage ripple is typically dominated by the capacitors. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Loop Compensation Components

The MAX17065 regulators are current-mode converters and are inherently stable with the suggested design values in the *Typical Application Circuit* (Figure 1). Since the right-half plane zeros of the step-up and the inverting converters are pushed to very high frequencies due to the low output currents of these converters, the compensation networks at COMP and COMN are needed mainly to improve line-and-load regulation.

If further transient-response improvements are necessary, try varying the resistors in 20% steps and the capacitors in 50% steps from the suggested values used in the *Typical Application Circuit* (Figure 1) while observing the effect on the transient-response waveforms. For typical application, the compensation resistors are chosen between 10kΩ to 100kΩ.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the *Typical Applications Circuit* (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the *Typical Applications Circuit* (Figure 1).

Charge-Pump Capacitor Selection

The flying capacitor C_{CH} and series resistor R_{CH} that are connected between the CH+ and CH- pins and the flying capacitor C_{CL} and series resistor R_{CL} connected between the CL+ and CL- are what determines the maximum current that can be delivered by the charge pumps. Increasing C_{CH} and C_{CL} indefinitely in an attempt to increase the output-current capability of the charge pumps is eventually limited due to the resistance of the internal switches for the charge pumps in addition to the added series resistors R_{CH} and R_{CL}.

The *Typical Application Circuit* (Figure 1) uses 100Ω for both R_{CH} and R_{CL} in order to reduce the noise susceptibility that can affect the performance of the charge pumps. Reducing R_{CH} and R_{CL} can increase the current capability, but reduces the noise immunity of the charge pumps. The maximum output current of the charge pumps is determined by:

$$I_{VH(MAX)} = \frac{(2 \times V_{VM}) - V_{VH}}{\frac{1}{f_{CLK} \times C_{CH}} + (2 \times R_{SW(MAX)}) + (4 \times R_{CH})}$$

$$I_{VL(MAX)} = \frac{V_{VM} - |V_{VL}|}{\frac{1}{f_{CLK} \times C_{CL}} + (2 \times R_{SW(MAX)}) + (4 \times R_{CL})}$$

and the output-voltage ripple for the charge pumps is determined by:

$$VH_{RIPPLE} = \frac{C_{CH}}{C_{VH} + C_{CH}} \times \left((2 \times V_{VM}) - V_{VH}\right)$$

$$VL_{RIPPLE} = \frac{C_{CL}}{C_{VL} + C_{CL}} \times \left(V_{VM} - |V_{VL}|\right)$$

where:

V_{VM} = The output voltage of the step-up converter.

V_{VH} = The output voltage of the positive charge pump.

V_{VL} = The output voltage of the negative charge pump.

f_{CLK} = The operating frequency of the charge pumps.

(f_{CLK} = 1/2 the operating frequency selected for the step-up and inverting converters).

$R_{SW(MAX)}$ = The internal charge-pump switch resistances (use 56Ω).

For V_{VH} = 6.5V, f_{CLK} = 1/2 x 1.2MHz, and using the R_{CH}, C_{CH}, and C_{VH} from the *Typical Application Circuit* (Figure 1), the maximum current the positive charge pump can deliver is:

$$I_{VH(MAX)} = \frac{(2 \times 5.35V) - 6.5V}{\frac{1}{600kHz \times 2.2nF} + (2 \times 56\Omega) + (4 \times 100\Omega)} = 3.3mA$$

and the positive charge-pump output voltage ripple is:

$$VH_{RIPPLE} = \frac{2.2nF}{1\mu F + 2.2nF} \times \left((2 \times 5.35V) - 6.5V\right) = 9.2mV$$

For V_{VL} = -4.0V, f_{CLK} = 1/2 x 1.2MHz, and using the R_{CL}, C_{CL}, and C_{VL} from the *Typical Application Circuit* (Figure 1), The maximum current the negative charge pump can deliver is:

$$I_{VL(MAX)} = \frac{5.35V - |-4.0V|}{\frac{1}{600kHz \times 10nF} + (2 \times 56\Omega) + (4 \times 100\Omega)} = 2.0mA$$

and the negative charge-pump output voltage ripple is:

$$VL_{RIPPLE} = \frac{10nF}{1\mu F + 10nF} \times \left(5.35V - |-4.0V|\right) = 13.4mV$$

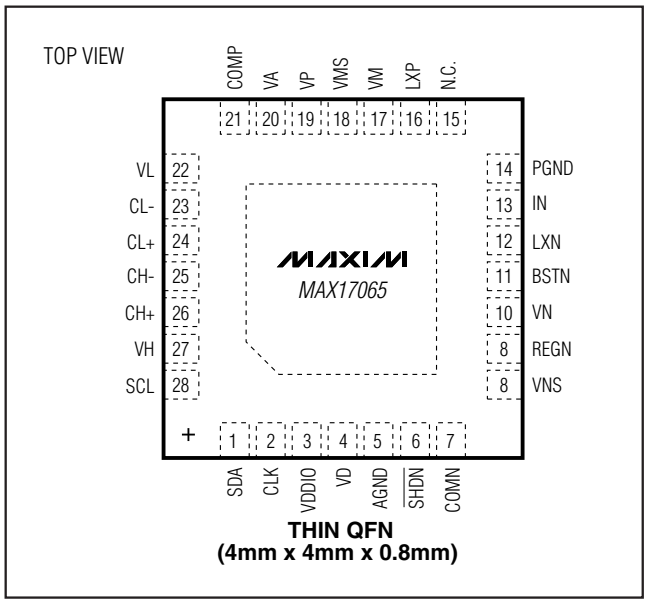
PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Place the 0.1µF and the 10µF input capacitors as close as possible to the IN pin such that the trace connecting one end of the capacitors to the IN pin and the trace connecting the other end of the capacitors to the PGND pin is as short as possible.
2) Place the step-up converter inductor such that the traces connecting the inductor to the LXP pin and the input capacitors are as short as possible.
3) Connect the output capacitors of VM, VP, VA, VH, VN, and VL as close as possible to their respective pins. Create a power ground plane (PGND) such that the other end of these capacitors and the PGND pin can connect to this plane directly.
4) Connect the output capacitor of VD and the 0.1µF bypass capacitor for VMS as close as possible to their respective pins. Create an analog ground plane (AGND) such that the other end of these capacitors and the AGND pin can connect to this plane directly. Connect the capacitors of COMN and COMP to the AGND plane also.
5) Place the inverting converter inductor such that the trace connecting the inductor to the LXN pin and the distance the inductor current has to travel through the PGND plane to the PGND pin are as short as possible.
6) Make a single connection between the AGND and PGND planes together at a point closest to the PGND pin only. Make no other connections between these two ground planes. If vias are needed to make this connection, use multiple vias instead of a single via to help reduce the resistance and the inductance attributed by the vias and place the vias close to the PGND pin such that the AGND plane can connect to the PGND plane at a point closest to the PGND pin.
7) Create a plane for VN and connect the entire backside paddle to this plane. Try to maximize the area of this plane to help improve the IC's thermal performance.
8) Care should be taken to avoid running traces that carry any noise-sensitive signals near LXP or LXN or high-current traces.
9) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
10) Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias instead of single vias to help reduce the resistance and the inductance attributed by the vias.
11) Refer to the MAX17065 Evaluation Kit for an example of a proper board layout.

Dual SMPS Outputs, LDO, and Dual Charge Pumps with I²C Interface for OLED

Pin Configuration



THIN QFN
(4mm x 4mm x 0.8mm)

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2844-1	**21-0139**

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