

Features

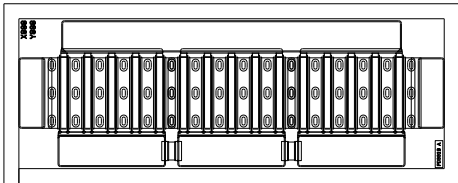
- Small Signal Gain: 15 dB @ 4 GHz
- PSAT: 45 W
- Drain Efficiency: 65% @ 3.5 GHz
- 28 V Operation
- High Breakdown Voltage
- High Temperature Operation
- Up to 6 GHz Operation
- High Efficiency

Applications

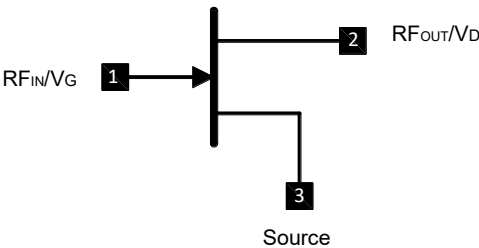
- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms
- Radar, Electronic Warfare

Description

The WST4300D is a gallium nitride (GaN) high electron mobility transistor (HEMT). GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity, and higher thermal conductivity. GaN HEMTs offer greater power density and wider bandwidths compared to Si and GaAs transistors.



Functional Schematic



Pin Configuration

Pin #	Pin Name	Function
1	RF _{IN} / V _G	RF Input / Gate
2	RF _{OUT} / V _D	RF Output / Drain
3	Source	Ground / Source

Ordering Information

Part Number	MOQ Increment
WST4300D	bulk
WST4300D-GP4	10 pc Gel-Pak

- Restrictions on Hazardous Substances, compliant to current RoHS EU directive.
- Proprietary RF Large Signal Models Available for ADS and MWO

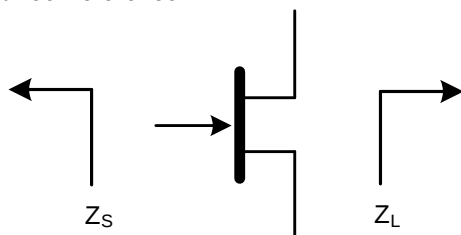
CW Load-Pull Performance: Reference Plane at Device Bond Pads

For Engineering Evaluation Only – This data does not Modify MACOM's Datasheet Limits.

Frequency (GHz)	Z_{SOURCE} (Ω)	Maximum Output Power				
		$V_{\text{DS}} = 28 \text{ V}$, $I_{\text{DQ}} = 0.5 \text{ A}$, $T_c = 25^\circ\text{C}$, P_{SAT}				
		Z_{LOAD} (Ω)	Gain (dB)	Pout (dBm)	Pout (W)	η_D (%)
0.5	$1.8 + j5.2$	$4.7 + j5.0$	20	49.5	89.13	77
1	$1.6 + j2.9$	$3.9 + j3.8$	18	49.5	89.13	76
2	$1.4 + j1.7$	$3.5 + j3.0$	15	49.5	89.13	74
4	$1 + j1.2$	$2.5 + j2.7$	10.5	49	79.43	64
6	$0.7 + j0.8$	$2 + j2.1$	8.2	48.7	74.13	55

Frequency (GHz)	Z_{SOURCE} (Ω)	Maximum Drain Efficiency				
		$V_{\text{DS}} = 28 \text{ V}$, $I_{\text{DQ}} = 0.45 \text{ A}$, $T_c = 25^\circ\text{C}$, P_{SAT}				
		Z_{LOAD} (Ω)	Gain (dB)	Pout (dBm)	Pout (W)	η_D (%)
0.5	$1.8 + j5.2$	$6.3 + j6.0$	19	48.5	70.79	80
1	$1.6 + j2.9$	$4.7 + j5.7$	17	48.5	70.79	80
2	$1.4 + j1.7$	$3.2 + j4.6$	14	48.5	70.79	80
4	$1 + j1.2$	$1.8 + j3.7$	9.8	48.3	67.61	71
6	$0.7 + j0.8$	$1.5 + j3.0$	7.7	48.2	66.07	63

Impedance Reference



Z_{SOURCE} = Measured impedance presented to the input of the device at bond pad reference plane.

Z_{LOAD} = Measured impedance presented to the output of the device at bond pad reference plane.

DC Electrical Specifications at $T_C = +25^\circ\text{C}$

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Gate Threshold Voltage	$V_{DS} = 10\text{ V}, I_D = 10.8\text{ mA}$	V_T	-2.6	-2.0	-1.6	V
Gate Quiescent Voltage	$V_{DS} = 28\text{ V}, I_D = 500\text{ mA}$	V_{GSQ}	—	-1.8	—	V
Saturated Drain Current	$V_{GS} = 6\text{ V}, V_{GS} = 2.0\text{ V}$	I_{DSS}	10.8	12.9	—	A
Drain-Source Breakdown Voltage	$V_{DS} = -8\text{ V}, I_D = 10.8\text{ mA}$	V_{BDS}	84	—	—	V
On Resistance	$V_{DS} = 0.05\text{ V}, V_{GS} = 0\text{ V}$	R_{ON}	0.1	0.11	—	Ω
Gate Forward Voltage	$V_{DS} = 0\text{ V}, I_D = 10.8\text{ }\mu\text{A}$	$V_{G(ON)}$	0.4		—	V

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
Drain-Source Voltage	84 V
Gate Voltage	-10, +2 V
Drain Current	4.5 A
Gate Current	11 mA
Storage Temperature	-55°C to +150°C
Mounting Temperature	+320°C, 30 seconds
Junction Temperature ^{3,4}	+225°C
Operating Temperature	-40°C to +85°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Operating at nominal conditions with $T_J \leq +225\text{ C}$ will ensure $MTTF > 1 \times 10^6$ hours.
- Junction Temperature (T_J) = $T_C + \Theta_{jc} * (V * I)$
Typical thermal resistance (Θ_{jc}) = 2.1°C/W for CW.
a) For $T_C = +25^\circ\text{C}$,
 $T_J = 115^\circ\text{C}$ @ $P_{DISS} = 43\text{ W}$
b) For $T_C = +85^\circ\text{C}$,
 $T_J = 175^\circ\text{C}$ @ $P_{DISS} = 43\text{ W}$

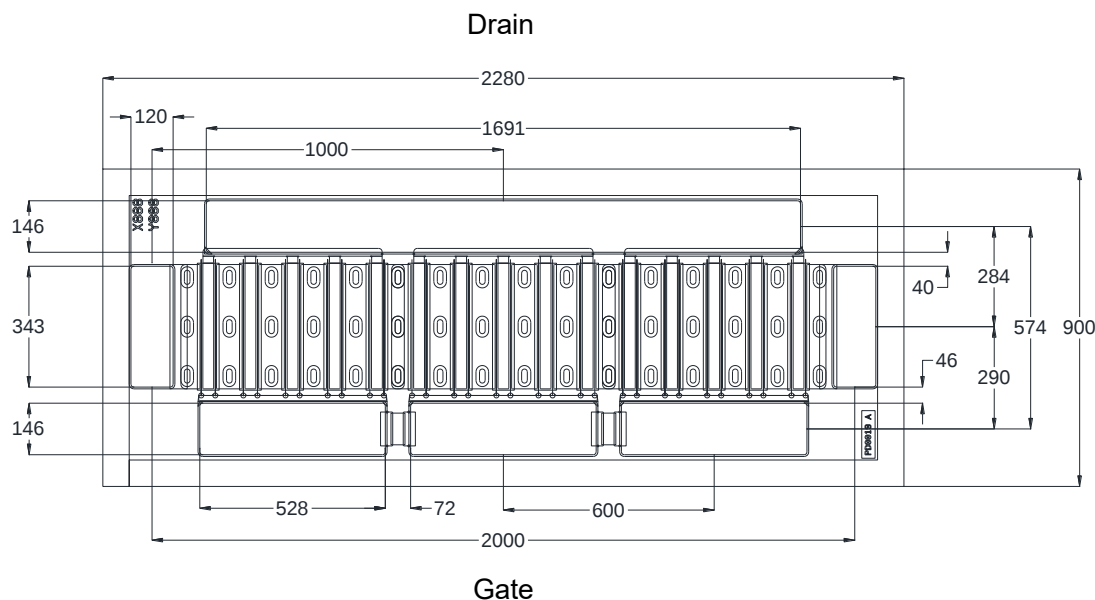
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Die Dimensions (units in microns)



Assembly Notes:

- Recommended solder is AuSn (80/20) solder. Refer to website for the Eutectic Die Bond Procedure application note.
- Vacuum Collet is the preferred method of pick-up.
- Die thickness is 3 mils.
- The backside of the die is the Source (ground) contact.
- Die back side gold plating is 5 microns thick minimum.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- Gold wire must be used for connections.
- Use the die label (XXX-YYY) for correct orientation.

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