



SN74LS163(LX) Presettable Synchronous 4-bit Binary Counter; Synchronous Reset

Product Specification

Specification Revision History:

Version	Date	Description
2022-06-A1	2022-06	New
2023-04-B1	2023-04	Update the template



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1、General Description

The SN74LS163 is a synchronous presettable binary counter with an internal look-ahead carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action. It causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW after the next positive-going transition on the clock input (CP). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

The CP to TC propagation delay and CEP to CP set-up time determine the maximum clock frequency for the cascaded counters according to the following formula:

$$f_{\max} = 1 / (t_{p(\max)}(\text{CP to TC}) + t_{\text{SU}}(\text{CEP to CP}))$$

Features:

- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Synchronous reset
- Positive-edge triggered clock
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16



Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74LS163N(LX)	DIP16	SN74LS163N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm



Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74LS163DR(LX)	SOP16	LS163	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74LS163PW(LX)	TSSOP16	LS163	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

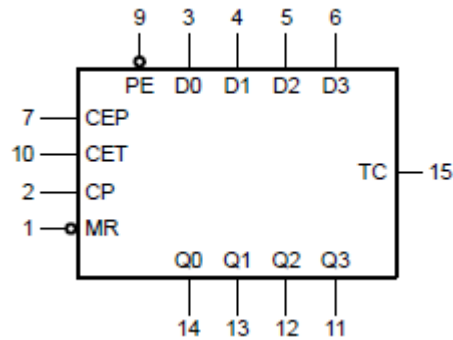


Figure 1. Logic symbol

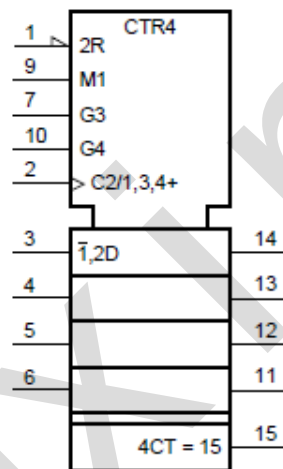


Figure 2. IEC logic symbol

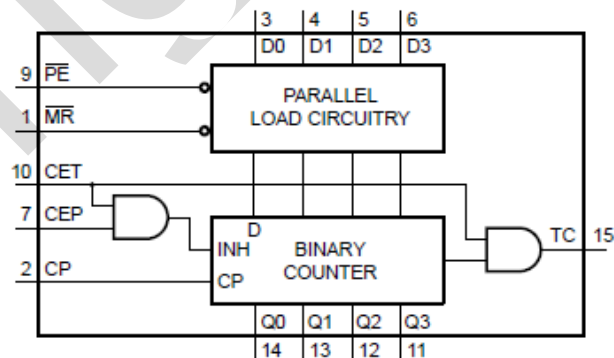


Figure 3. Functional diagram

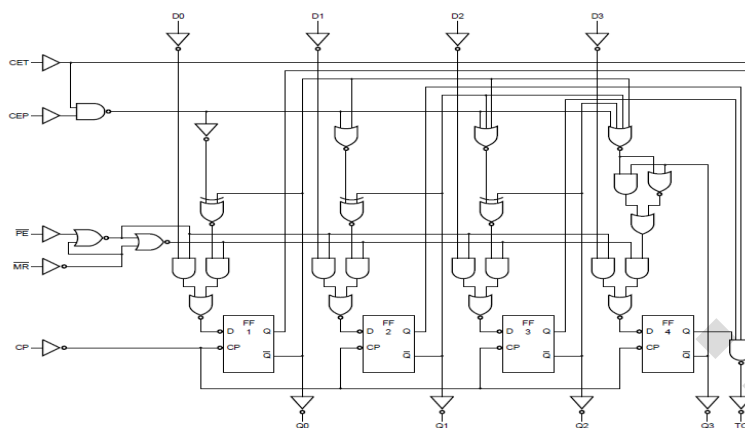


Figure 4. Logic diagram

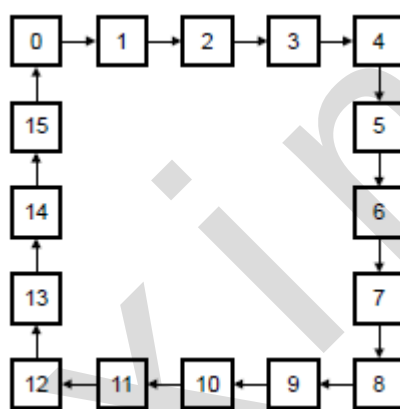


Figure 5. State diagram

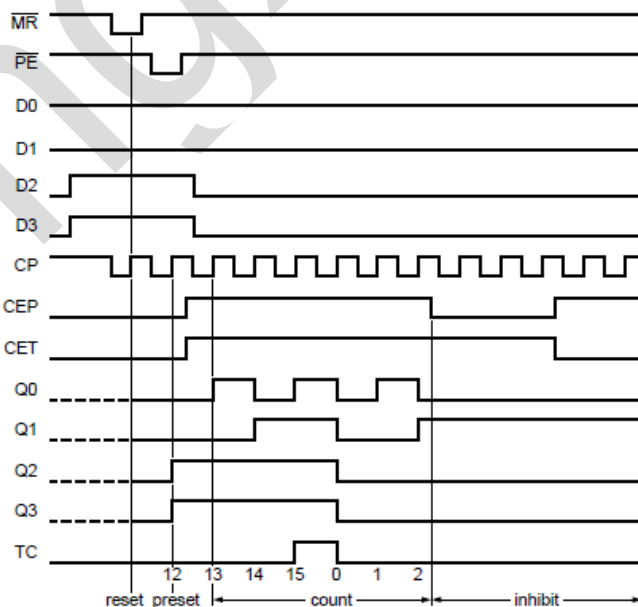
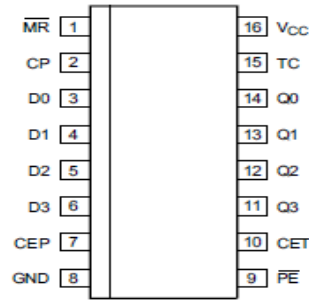


Figure 6. Typical timing sequence



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	MR	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable input
8	GND	ground (0V)
9	PE	parallel enable input (active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V _{CC}	supply voltage

2.4、Function Table

Operating mode	Input						Output	
	MR	CP	CEP	CET	PE	Dn	Qn	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	L
count	h	↑	h	h	h	X	count	[2]
hold (do nothing)	h	X	l	X	h	X	q _n	L
	h	X	X	l	h	X	q _n	L

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;



q=lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.

[2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$	-	± 25	mA
supply current	I_{CC}	-	-	+50	mA
ground current	I_{GND}	-	-50	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	°C



3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	2.1	1.35	V
		V _{CC} =6.0V		-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.48	5.81	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.26	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
input capacitance	C _I	-		-	3.5	-	pF



3.3.2、DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.34	-	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.33	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA



3.3.3、DC Characteristics 3

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.7	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.2	-	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.4	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.4	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	160	uA



3.3.4、AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $\text{GND}=0\text{V}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	55	185 ns
			$V_{CC}=4.5\text{V}$	-	20	37 ns
			$V_{CC}=5.0\text{V}$; $C_L=15\text{pF}$	-	17	- ns
			$V_{CC}=6.0\text{V}$	-	16	31 ns
		CP to TC; see Figure 8	$V_{CC}=2.0\text{V}$	-	69	215 ns
			$V_{CC}=4.5\text{V}$	-	25	43 ns
			$V_{CC}=5.0\text{V}$; $C_L=15\text{pF}$	-	21	- ns
			$V_{CC}=6.0\text{V}$	-	20	37 ns
		CET to TC; see Figure 9	$V_{CC}=2.0\text{V}$	-	36	120 ns
			$V_{CC}=4.5\text{V}$	-	13	24 ns
			$V_{CC}=5.0\text{V}$; $C_L=15\text{pF}$	-	11	- ns
			$V_{CC}=6.0\text{V}$	-	10	20 ns
transition time	t_t	see Figure 8 and Figure 9	$V_{CC}=2.0\text{V}$	-	19	75 ns
			$V_{CC}=4.5\text{V}$	-	7	15 ns
			$V_{CC}=6.0\text{V}$	-	6	13 ns
pulse width	t_w	CP HIGH or LOW; see Figure 8	$V_{CC}=2.0\text{V}$	80	17	- ns
			$V_{CC}=4.5\text{V}$	16	6	- ns
			$V_{CC}=6.0\text{V}$	14	5	- ns
set-up time	t_{su}	$\overline{\text{MR}}$, Dn to CP; see Figure 10, 11	$V_{CC}=2.0\text{V}$	80	22	- ns
			$V_{CC}=4.5\text{V}$	16	8	- ns
			$V_{CC}=6.0\text{V}$	14	6	- ns
		$\overline{\text{PE}}$ to CP; see Figure 10	$V_{CC}=2.0\text{V}$	80	17	- ns
			$V_{CC}=4.5\text{V}$	16	6	- ns
			$V_{CC}=6.0\text{V}$	14	5	- ns
		CEP, CET to CP; see Figure 12	$V_{CC}=2.0\text{V}$	175	58	- ns
			$V_{CC}=4.5\text{V}$	35	21	- ns
			$V_{CC}=6.0\text{V}$	30	17	- ns
hold time	t_h	Dn, $\overline{\text{PE}}$, CEP, CET, $\overline{\text{MR}}$ to CP; see Figure 10, 11, 12	$V_{CC}=2.0\text{V}$	0	-14	- ns
			$V_{CC}=4.5\text{V}$	0	-5	- ns
			$V_{CC}=6.0\text{V}$	0	-4	- ns
maximum frequency	f_{max}	CP; see Figure 8	$V_{CC}=2.0\text{V}$	5	15	- MHz
			$V_{CC}=4.5\text{V}$	27	46	- MHz
			$V_{CC}=5.0\text{V}$; $C_L=15\text{pF}$	-	51	- MHz
			$V_{CC}=6.0\text{V}$	32	55	- MHz
power dissipation capacitance	C_{PD}	$f_i=1\text{MHz}$; $V_{CC}=5.0\text{V}$; $V_I=\text{GND to } V_{CC}$	-	33	-	pF



Note:

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
 [2] t_t is the same as t_{THL} and t_{TLH} .
 [3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

3.3.5、AC Characteristics 2

($T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, GND=0V, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	230 ns
			$V_{CC}=4.5\text{V}$	-	-	46 ns
			$V_{CC}=6.0\text{V}$	-	-	39 ns
		CP to TC; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	270 ns
			$V_{CC}=4.5\text{V}$	-	-	54 ns
			$V_{CC}=6.0\text{V}$	-	-	46 ns
		CET to TC; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	150 ns
			$V_{CC}=4.5\text{V}$	-	-	30 ns
			$V_{CC}=6.0\text{V}$	-	-	26 ns
transition time	t_t	see Figure 8 and Figure 9	$V_{CC}=2.0\text{V}$	-	-	95 ns
			$V_{CC}=4.5\text{V}$	-	-	19 ns
			$V_{CC}=6.0\text{V}$	-	-	16 ns
pulse width	t_w	CP HIGH or LOW; see Figure 8	$V_{CC}=2.0\text{V}$	100	-	- ns
			$V_{CC}=4.5\text{V}$	20	-	- ns
			$V_{CC}=6.0\text{V}$	17	-	- ns
set-up time	t_{su}	$\overline{\text{MR}}$, Dn to CP; see Figure 10, 11	$V_{CC}=2.0\text{V}$	100	-	- ns
			$V_{CC}=4.5\text{V}$	20	-	- ns
			$V_{CC}=6.0\text{V}$	17	-	- ns
		$\overline{\text{PE}}$ to CP; see Figure 10	$V_{CC}=2.0\text{V}$	100	-	- ns
			$V_{CC}=4.5\text{V}$	20	-	- ns
			$V_{CC}=6.0\text{V}$	17	-	- ns
		CEP, CET to CP; see Figure 12	$V_{CC}=2.0\text{V}$	220	-	- ns
			$V_{CC}=4.5\text{V}$	44	-	- ns
			$V_{CC}=6.0\text{V}$	37	-	- ns
hold time	t_h	Dn, $\overline{\text{PE}}$, CEP, CET $\overline{\text{MR}}$ to CP; see Figure 10, 11, 12	$V_{CC}=2.0\text{V}$	0	-	- ns
			$V_{CC}=4.5\text{V}$	0	-	- ns
			$V_{CC}=6.0\text{V}$	0	-	- ns
maximum frequency	f_{max}	CP; see Figure 8	$V_{CC}=2.0\text{V}$	4	-	- MHz
			$V_{CC}=4.5\text{V}$	22	-	- MHz
			$V_{CC}=6.0\text{V}$	26	-	- MHz



Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

3.3.6、AC Characteristics 3

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, GND=0V, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74LS163						
propagation delay	t_{pd}	CP to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	280 ns
			$V_{CC}=4.5\text{V}$	-	-	56 ns
			$V_{CC}=6.0\text{V}$	-	-	48 ns
		CP to TC; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	320 ns
			$V_{CC}=4.5\text{V}$	-	-	65 ns
			$V_{CC}=6.0\text{V}$	-	-	55 ns
		CET to TC; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	180 ns
			$V_{CC}=4.5\text{V}$	-	-	36 ns
			$V_{CC}=6.0\text{V}$	-	-	31 ns
transition time	t_t	see Figure 8 and Figure 9	$V_{CC}=2.0\text{V}$	-	-	110 ns
			$V_{CC}=4.5\text{V}$	-	-	22 ns
			$V_{CC}=6.0\text{V}$	-	-	19 ns
pulse width	t_w	CP HIGH or LOW; see Figure 8	$V_{CC}=2.0\text{V}$	120	-	- ns
			$V_{CC}=4.5\text{V}$	24	-	- ns
			$V_{CC}=6.0\text{V}$	20	-	- ns
set-up time	t_{su}	$\overline{\text{MR}}$, Dn to CP; see Figure 10, 11	$V_{CC}=2.0\text{V}$	120	-	- ns
			$V_{CC}=4.5\text{V}$	24	-	- ns
			$V_{CC}=6.0\text{V}$	20	-	- ns
		$\overline{\text{PE}}$ to CP; see Figure 10	$V_{CC}=2.0\text{V}$	120	-	- ns
			$V_{CC}=4.5\text{V}$	24	-	- ns
			$V_{CC}=6.0\text{V}$	20	-	- ns
		CEP, CET to CP; see Figure 12	$V_{CC}=2.0\text{V}$	265	-	- ns
			$V_{CC}=4.5\text{V}$	53	-	- ns
			$V_{CC}=6.0\text{V}$	45	-	- ns
hold time	t_h	Dn, $\overline{\text{PE}}$, CEP, CET $\overline{\text{MR}}$ to CP; see Figure 10, 11, 12	$V_{CC}=2.0\text{V}$	0	-	- ns
			$V_{CC}=4.5\text{V}$	0	-	- ns
			$V_{CC}=6.0\text{V}$	0	-	- ns
maximum frequency	f_{max}	CP; see Figure 8	$V_{CC}=2.0\text{V}$	4	-	- MHz
			$V_{CC}=4.5\text{V}$	18	-	- MHz
			$V_{CC}=6.0\text{V}$	21	-	- MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

4、Testing Circuit

4.1、AC Testing Circuit

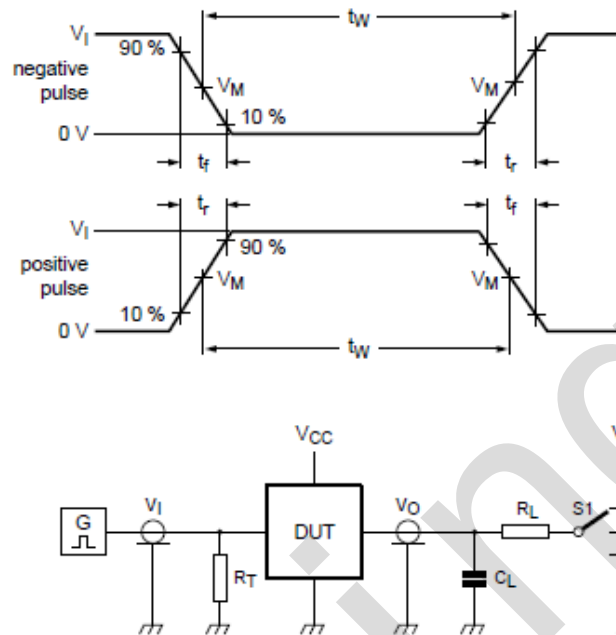


Figure 7. Test circuit for measuring switching times

Definitions for test circuit:

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

S1=Test selection switch

4.2、AC Testing Waveforms

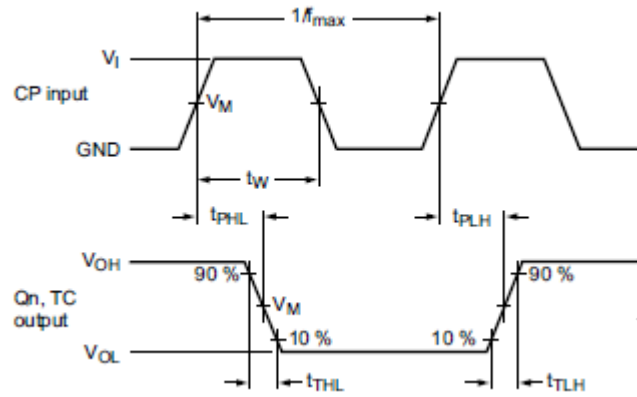


Figure 8. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

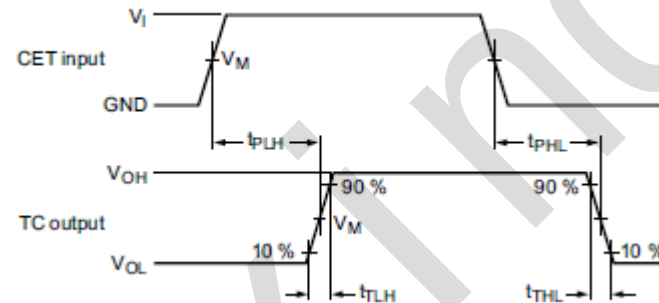


Figure 9. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times

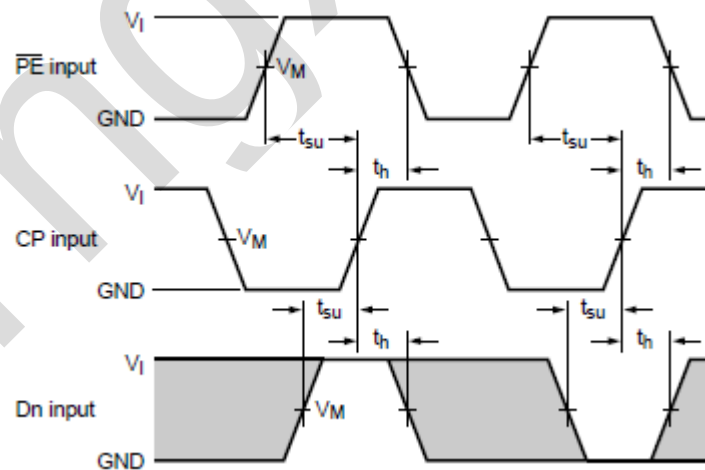


Figure 10. The data input (Dn) and parallel enable input (PE) set-up and hold times

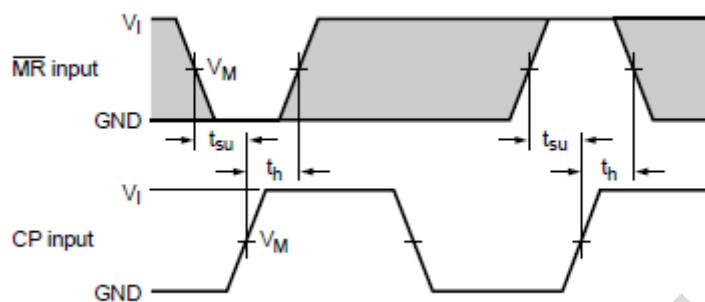


Figure 11. The master reset (MR) set-up and hold times

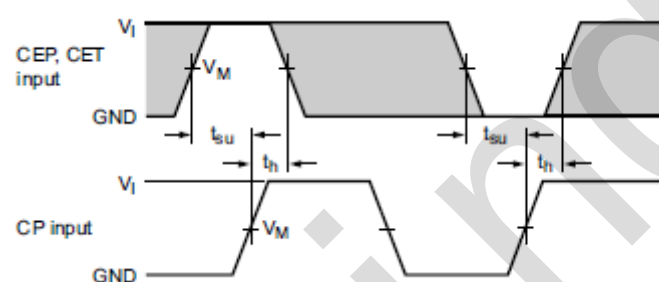


Figure 12. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

4.3、Measurement Points

Input		Output
V_I	V_M	V_M
GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

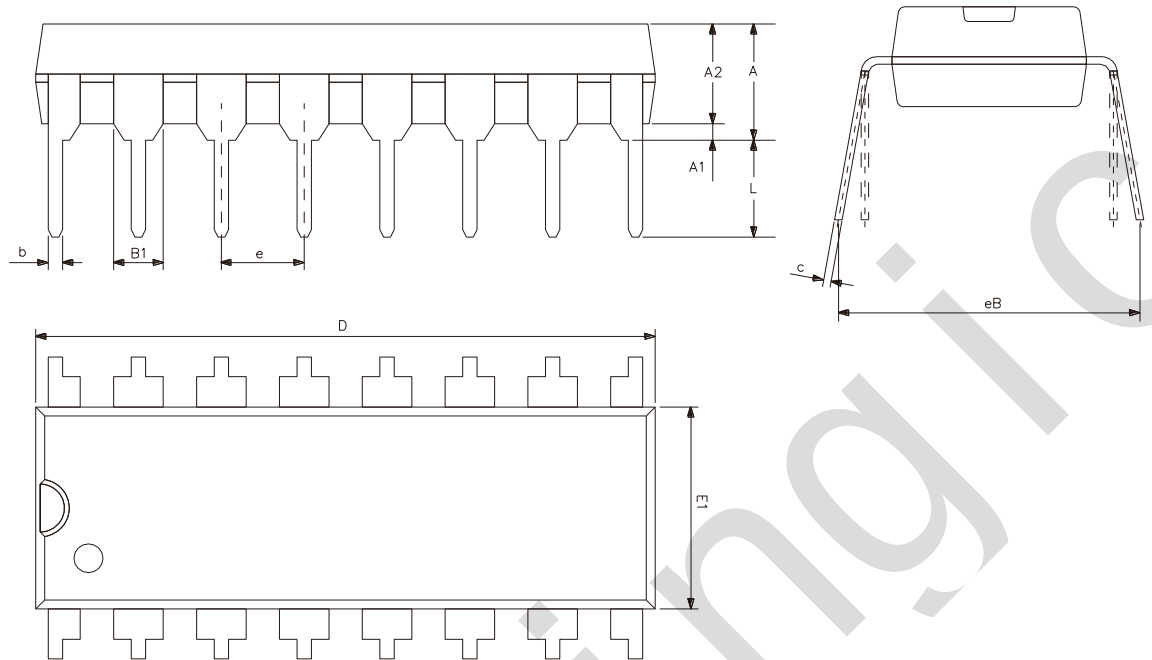
4.4、Test Data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6ns	15pF, 50pF	1kΩ	open



5、Package Information

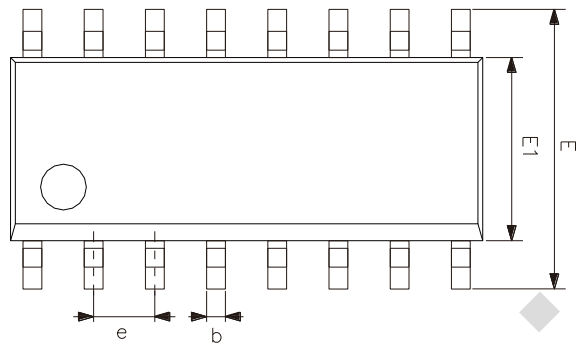
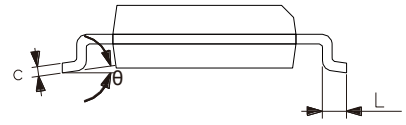
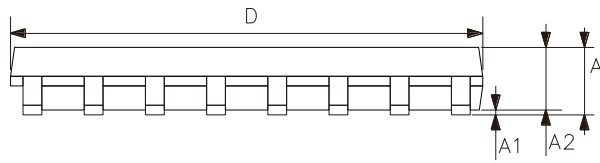
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



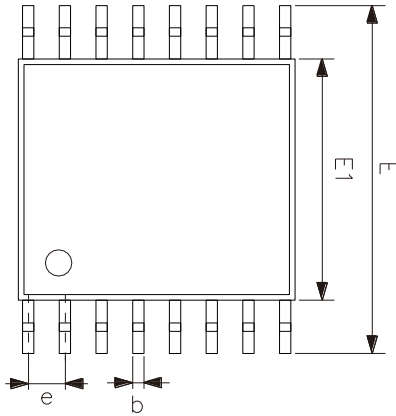
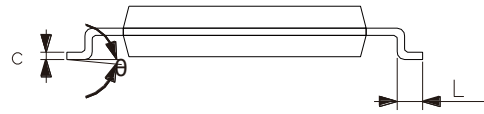
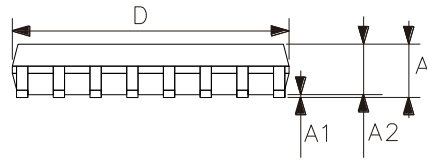
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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