

HX313C9FWK2/8

8GB (4GB 512M x 64-Bit x 2 pcs.)
DDR3-1333 CL9 240-Pin DIMM Kit



DESCRIPTION

HyperX HX313C9FWK2/8 is a kit of two 512M x 64-bit (4GB) DDR3-1333 CL9 SDRAM (Synchronous DRAM) 1Rx8 memory modules, based on eight 512M x 8-bit DDR3 FBGA components per module. Total kit capacity is 8GB. Each module kit has been tested to run at DDR3-1333 at latency timing 9-9-9 at 1.5V. The JEDEC standard electrical and mechanical specifications are as follows:

SPECIFICATIONS

CL(IDD)	9 cycles
Row Cycle Time (tRCmin)	49.125ns (min.)
Refresh to Active/Refresh Command Time (tRFCmin)	260ns (min.)
Row Active Time (tRASmin)	36ns (min.)
Maximum Operating Power	TBD W* (per module)
UL Rating	94 V - 0
Operating Temperature	0° C to 85° C
Storage Temperature	-55° C to +100° C

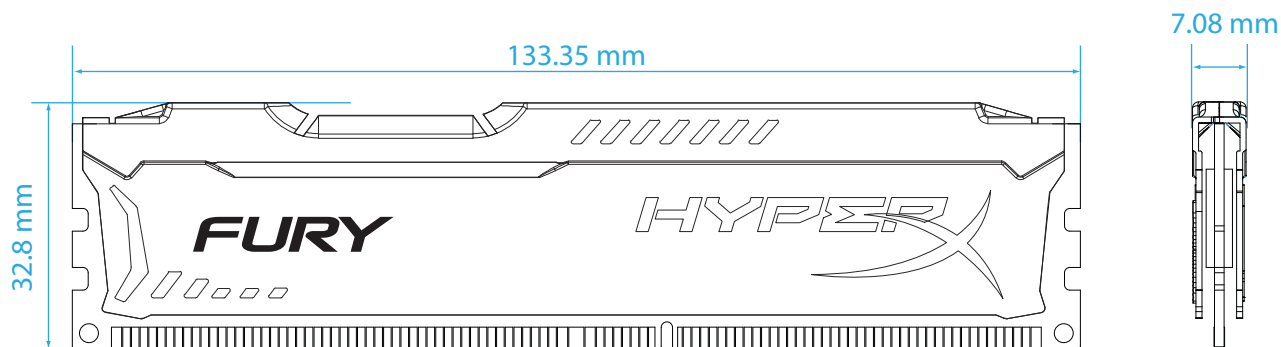
*Power will vary depending on the SDRAM used.

FEATURES

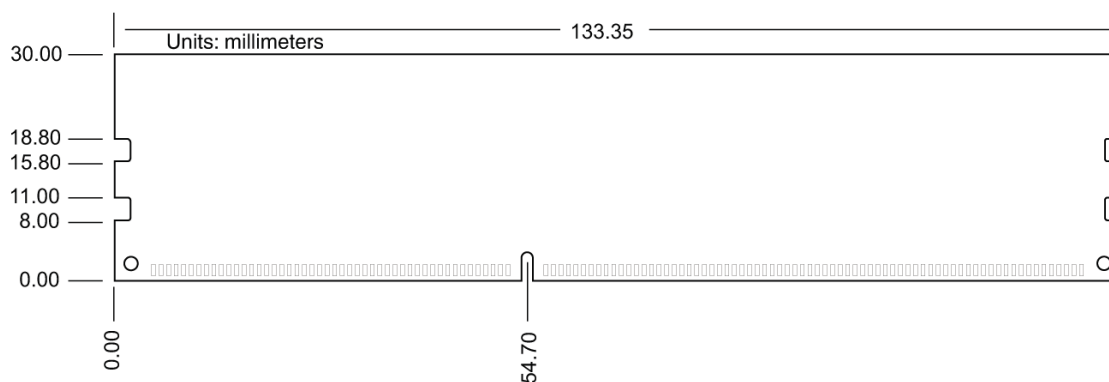
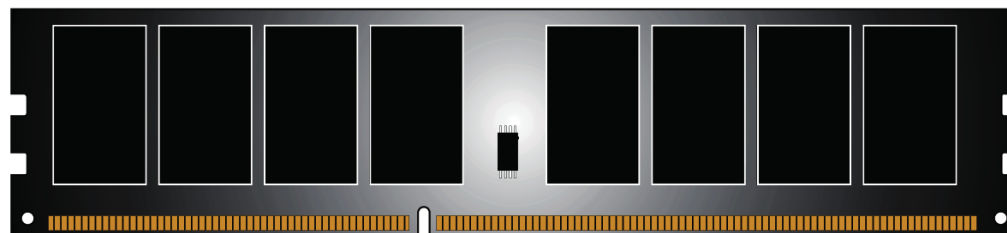
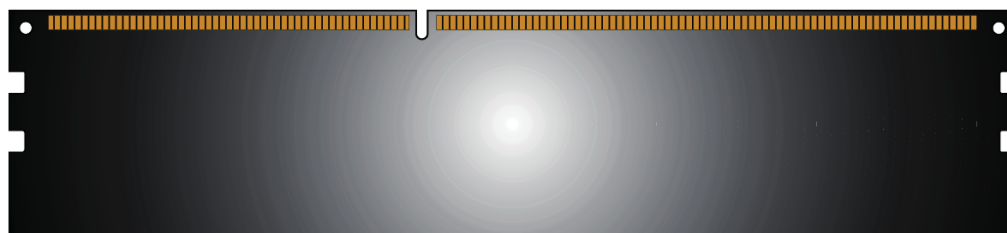
- JEDEC standard 1.5V (1.425V ~1.575V) Power Supply
- VDDQ = 1.5V (1.425V ~ 1.575V)
- 667MHz fCK for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 9, 8, 7, 6
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm $\pm$ 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE $\leq$ 95°C
- Asynchronous Reset
- Height 1.291" (32.80mm) w/heatsink, single sided component

Continued >>

MODULE WITH HEAT SPREADER



MODULE DIMENSIONS



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