

Ideal Diode and Load Switch Controller with Reverse Input Protection

Features

- 4.2V to 60V Wide Input Operating Range
 - Reverse Voltage Protection to $-60V$ Requirements with a Suitable TVS Diode
 - ESD Ratings
 - HBM: $\pm 2kV$
 - CDM: $\pm 750V$
 - Internal Charge Pump for External High-Side N-Channel MOSFET Driving
 - Controller and MOSFET Driver Suitable for:
 - Single MOSFET for Reverse Protection
 - Two Back-to-Back MOSFETs, one for Reverse Protection and the other for Load Switching and Inrush Control
 - 1.5A/15 μA Sink/Source Current Capability of MOSFET Gate Driver
 - EN Pin to Enable/Disable the Controller
 - 1 μA Shutdown Current
 - 110 μA Operating Quiescent Current
 - 230ns Reverse Protection Response Time
- Small 6 Pin SOT23 Package (2.9mm x 1.6mm)

Applications

- Reverse Power Supply Protection
- Telecom/Server/Networking Systems
- Battery and System Protection
- Redundant Power Systems
- Industrial and Medical Systems

Typical Application

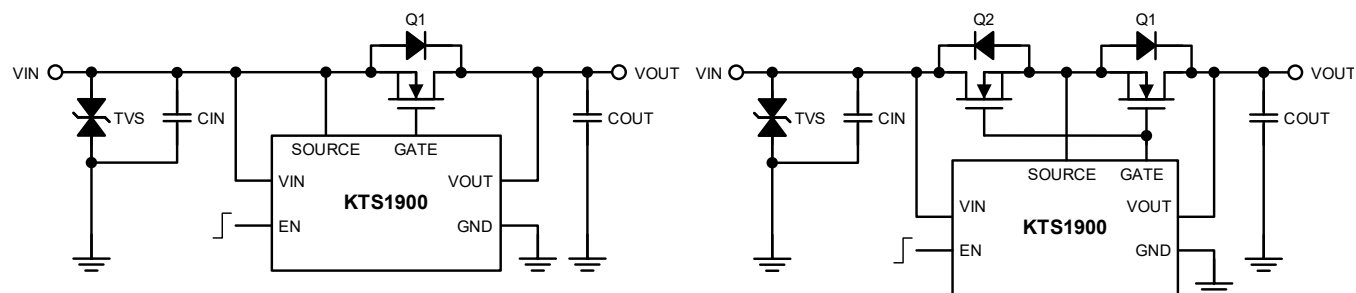


Figure 1. (a) Ideal Diode Controller Application

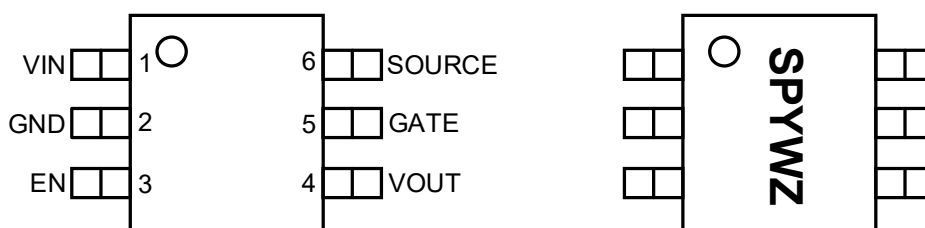
(b) Load Switch Controller Application

Ordering Information

Part Number	Marking ¹	Operating Temperature	Package
KTS1900GXAA-TA	SPYWZ	-40°C to +125°C	SOT23-6L

Pinout Diagram

SOT23-6



Top View
SOT23-6 2.9mm x 1.6mm x 1.45mm
SOT23 Package

Top Mark
SP = Device Code, YW = Date Code, Z = Serial Number

Pin Descriptions

Pin #	Name	Function
1	VIN	Supply voltage input. Connect pin to supply voltage VIN with a 2.2μF capacitor to ground. The VIN pin must be connected to the SOURCE pin in Ideal Diode mode. See the typical application schematic for details.
2	GND	Device ground.
3	EN	Enable control pin. EN pin is used to enable and disable the controller. EN pin can be also connected to VIN directly to enable the controller.
4	VOUT	Output voltage sense pin. Connect to the drain of the external N-channel MOSFET. Use 2.2μF from VOUT to ground
5	GATE	Gate drive. Connect to the gate of the external N-Channel MOSFETs.
6	SOURCE	Source pin. Connect to the source of the external N-Channel MOSFETs in Load Switch mode. SOURCE pin is also connected to VIN pin in single MOSFET application.

1. SP = Device Code, YW = Date Code, Z = Serial Number

Absolute Maximum Ratings²

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Description	Min.	Max.	Units
V _{IN}	VIN, EN, SOURCE to GND	-65	65	V
V _{OUT}	VOUT to GND	-0.3	65	V
V _{OUT}	VOUT to VIN	-65	80	V
V _{I-S}	VIN to SOURCE	-0.3	80	V
V _{O-S}	VOUT to SOURCE	-0.3	80	V
V _{GS}	GATE to SOURCE	-0.3	20	V
T _J	Operating Junction Temperature Range (T _J)	-40	150	°C
T _S	Storage Temperature Range (T _S)	-55	150	°C
T _{LEAD}	Maximum Soldering Temperature (at leads, 10 sec) (T _{LEAD})	-	250	°C

ESD Ratings³

Symbol	Description	Value	Units
V(ESD)	Human body model (HBM), all pins	±2000	V
Electrostatic Discharge	Charged device model (CDM), all pins	±750	V

Thermal Capabilities⁴

Symbol	Description	Value	Units
Θ _{JA}	Thermal Resistance – Junction to Ambient	120	°C/W
P _D	Maximum Continuous Power Dissipation at 25°C (T _J = 125°C)	833	mW
ΔP _D /ΔT	Derating Factor Above T _A = 25°C	-8.3	mW/°C

Recommended Operating Conditions⁵

Symbol	Description	Min.	Max.	Units
V _{IN}	VIN to GND	-60	60	V
V _{EN}	EN to GND	-60	60	V
V _{OUT}	VOUT to GND	-0.3	60	V
T _J	Operating Junction Temperature Range (T _J)	-40	125	°C

- Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
- ESD conform to JEDEC and IEC industry standards. Some pins may have higher performance.
- Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
- The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

Electrical Characteristics⁶

Typical values correspond to $T_A = 25^\circ\text{C}$. *Minimum* and *Maximum* specs are applied over the full operation junction temperature range of -40°C to 125°C , unless otherwise noted. SOURCE pin tied to VIN pin, VIN = 12V, $V_{EN} = 12\text{V}$ unless otherwise noted.

SUPPLY AND ENABLE

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Operating Input Voltage Range		4.2		60	V
	VIN Undervoltage Threshold	VIN Rising		3.8	4.1	V
		VIN Falling	2.65	3		V
I_Q	Operating Quiescent Current	EN = 12V		110	180	μA
I_{SHDN}	Shutdown Supply Current	EN = 0V		1	4	μA
EN	EN Logic High Threshold	EN Rising		1.24	1.32	V
	EN Logic Low Threshold	EN Falling	0.7	1.14		V
I_{EN}	EN Pin Sink Current	EN = 12V		3	5	μA

GATE DRIVER

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{GATE}	Gate Drive Voltage (GATE to SOURCE)	Full Conduction Mode, $V_{SOURCE} - V_{VOUT} = 100\text{mV}$	10	12	15	V
I_{GATE}	Gate Peak Source Current			15		μA
	Gate Peak Sink Current ⁷			1.5		A
T_{EN_DLY}	Gate Turn-On Delay Time			60	100	μs
$T_{REVERSE_DLY}$	Gate Turn-Off Delay Time			230		ns
$T_{RECOVERY}$	Recovery Delay from Forward Detection to Gate Turn ON ⁷			5		μs

SOURCE TO DRAIN VOLTAGE

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{SDREG}	Regulated Source to Drain Voltage (SOURCE-VOUT)		25	40	65	mV
V_{SDREV}	Source to Drain Voltage Threshold for Reverse Current Blocking		-24	-15	-2	mV

VOUT AND SOURCE PIN CURRENT

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{VOUT}	VOUT Pin Sink Current	Vout = 12V		1.5	2	μA
I_{SOURCE}	SOURCE Pin Sink Current ⁷	Vsource = 12V		5	10	μA

6. Device is guaranteed to meet performance specifications over the -40°C to $+125^\circ\text{C}$ operating temperature range by design, characterization and correlation with statistical process controls.

7. Guaranteed by design, characterization and statistical process control methods; not production tested.

Timing Diagrams

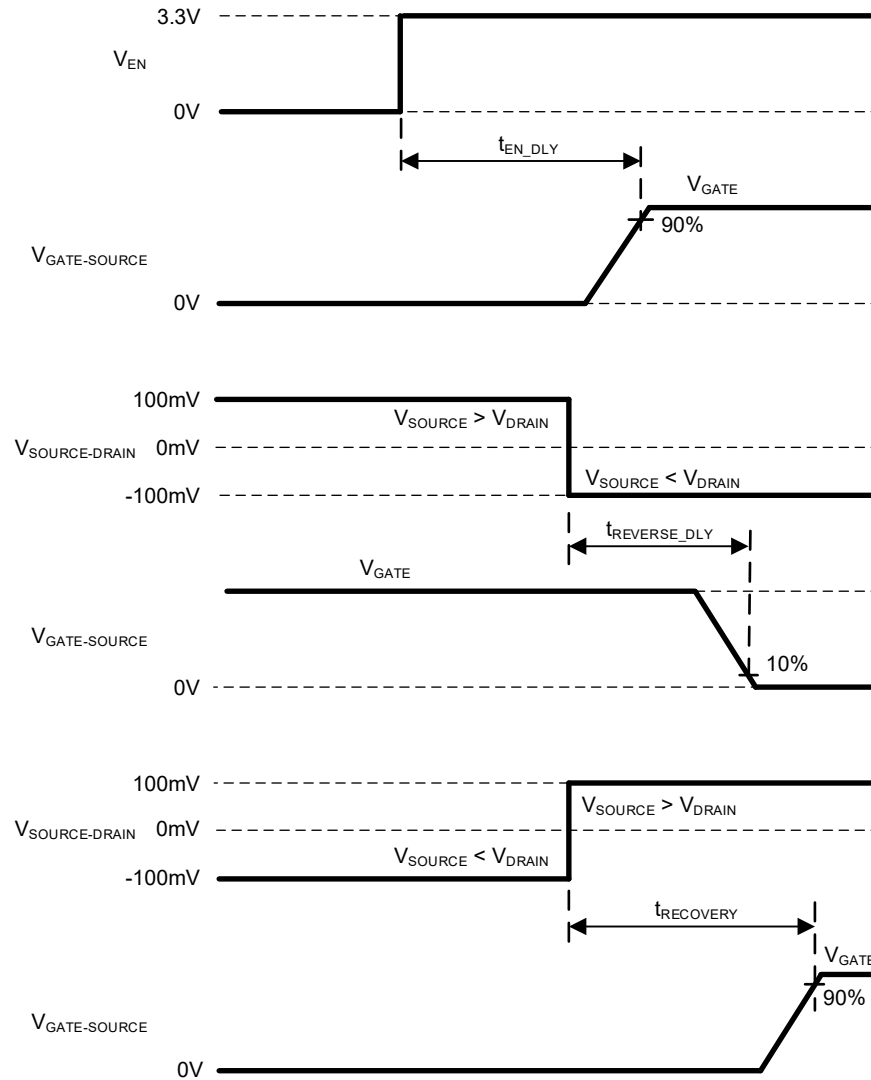
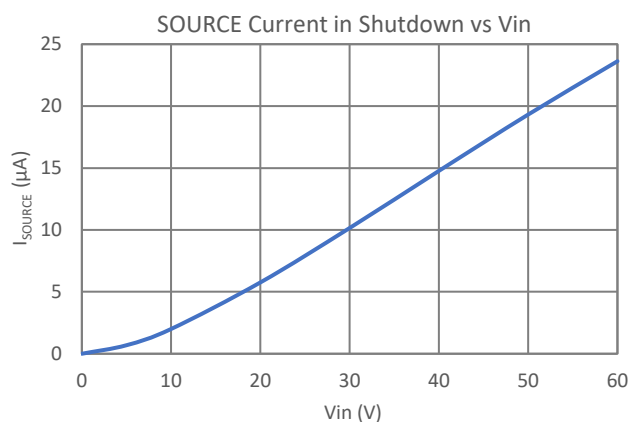
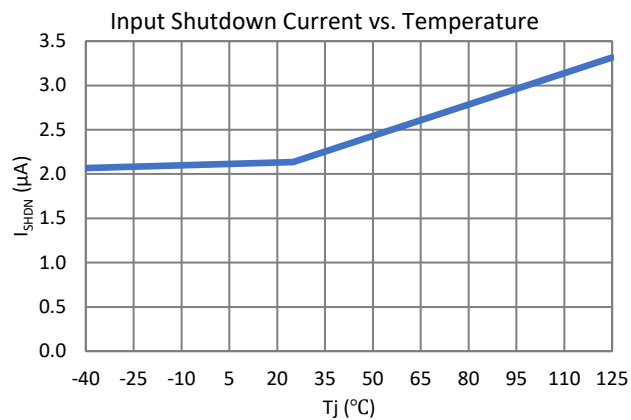
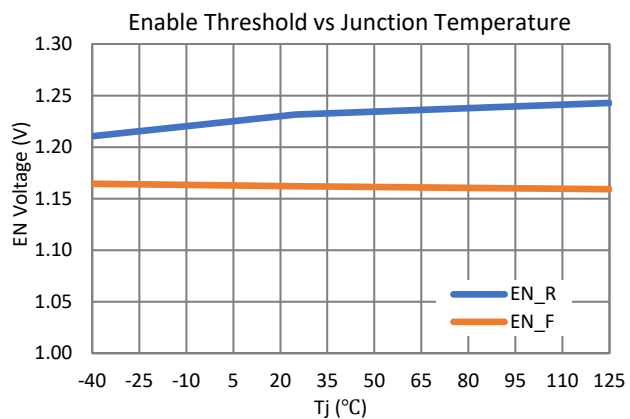
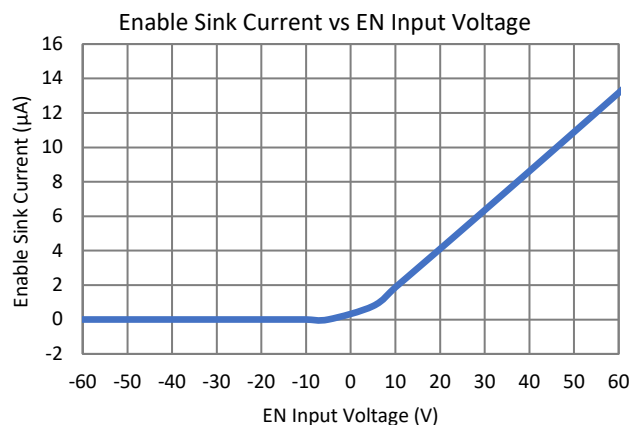
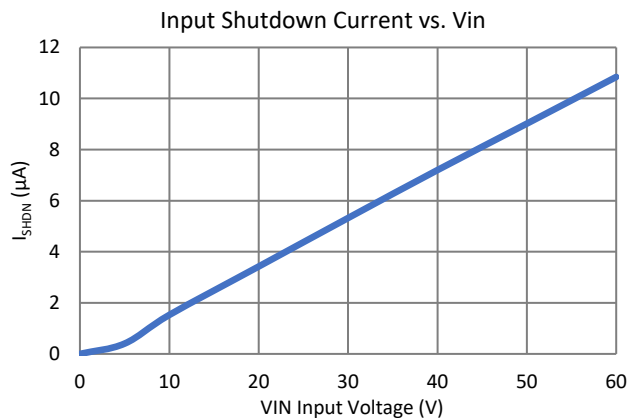
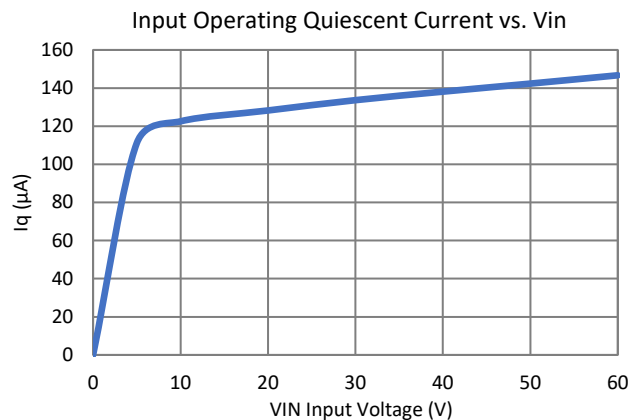


Figure 2. Timing Definition

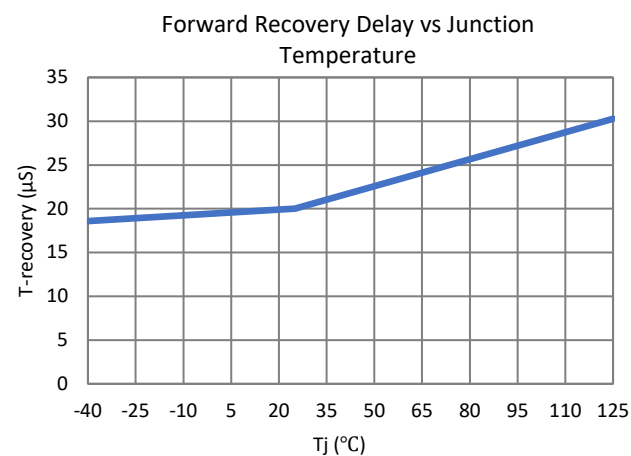
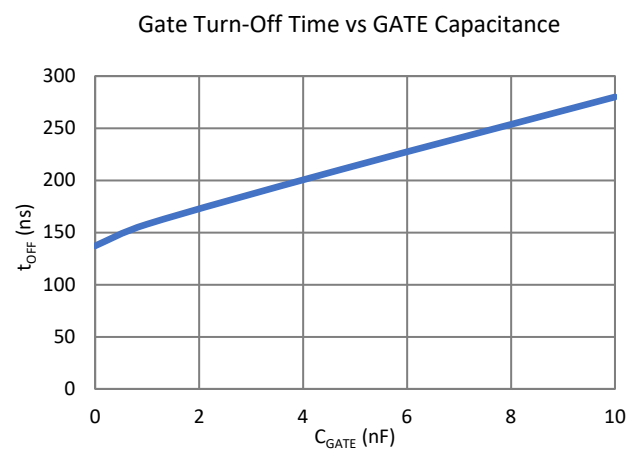
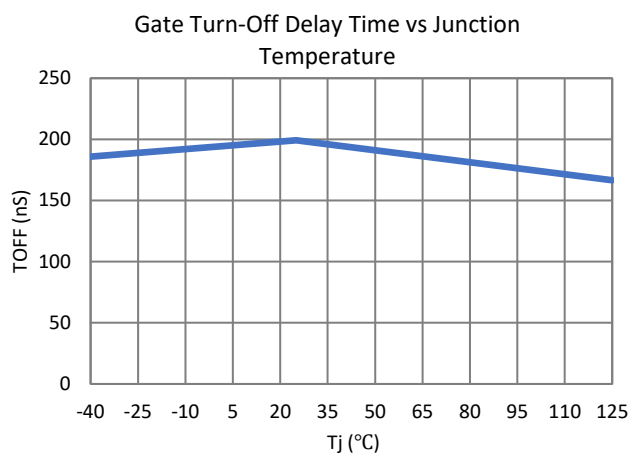
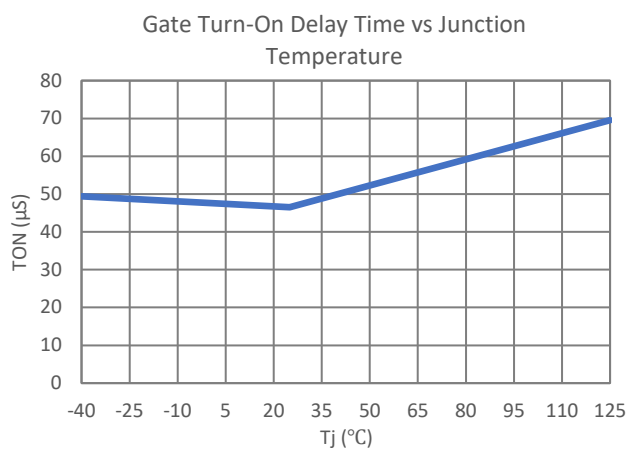
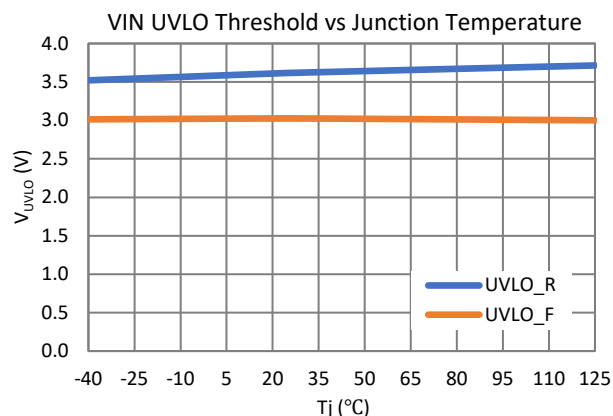
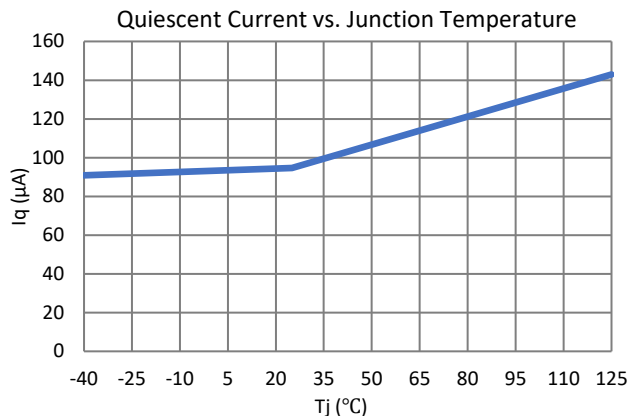
Typical Characteristics

$V_{IN} = 12V$, $T_A = 25^\circ C$, unless otherwise specified.



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Functional Block Diagram

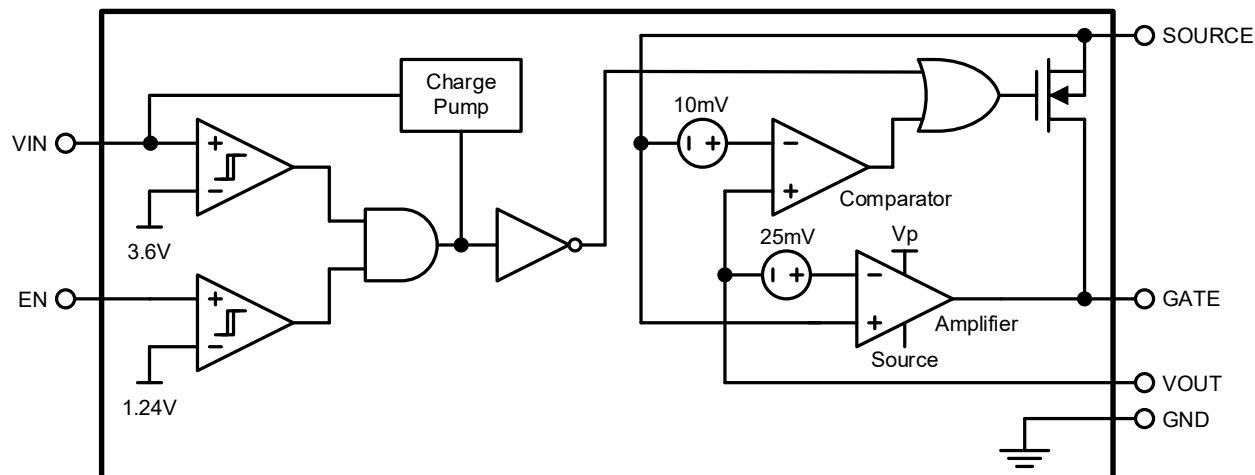


Figure 3. Functional Block Diagram

Application Information

Overview

To achieve an ideal diode function the KTS1900 controls an external N-MOSFET. An internal charge pump is used to supply NMOSFET gate driver turn on voltage. This ideal diode controller integrates a fast reverse current protection circuit. This protects the system from reverse current when there is a short or reverse polarity at VIN. In forward mode the KTS1900 also senses the source to drain voltage drop of the NMOSFET. The device linearly increases the GATE pin voltage to regulate the forward voltage drop to 40mV at light load. To keep the power loss at a minimum the GATE pin voltage increases with load current. This makes the KTS1900 ideal diode solution more efficient compared to traditional a Schottky diode. The forward voltage drop is regulated to avoid oscillation at light loads and minimize the power dissipation at higher currents. The KTS1900 also detects reverse current through the MOSFET. If the threshold is reached, the MOSFET is turned off with a 1.5 A GATE pull down current. The EN pin is also available to turn off the MOSFET(s) and minimize the current drawn by the controller down to 1μA in shutdown mode.

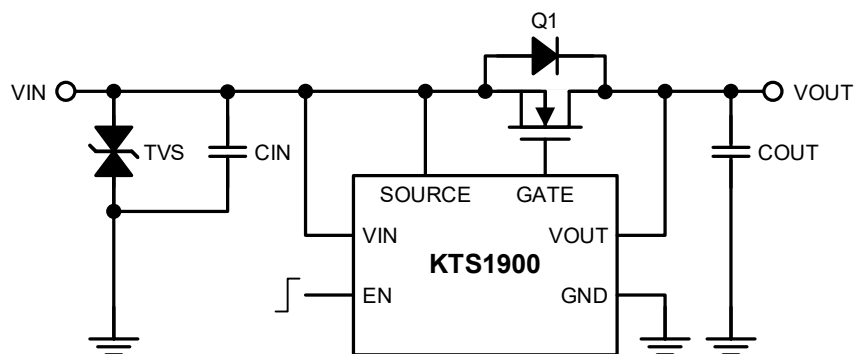


Figure 4. Typical Application

Linear Regulation Control

The table below shows that at light load the gate drive is reduced to regulate the source to drain voltage. At higher currents the MOSFET is driven to its lowest resistance. This results in a soft turn on and the lowest on-resistance R_{ON} at higher currents as listed in Table 1.

Table 1. Linear Regulation Control as Output Current Increases

I _{OUT} (A)	V _{GS} (V)	R _{ON} (mΩ)	P _{LOSS} (mW)
0.1	2.195	476.00	4.8
1	2.611	48.70	48.7
2	2.854	24.80	99.2
3	3.073	16.87	151.8
4	3.310	12.90	206.4
5	3.603	10.52	263.0
6	3.998	8.98	323.4
7	4.583	7.90	387.1
8	5.480	7.15	457.6
9	6.832	6.61	535.5
10	8.790	6.27	627.0
11	11.260	6.08	735.9
12	13.870	6.05	871.2
13	13.890	6.2	1047.8

Notes: V_{GS} is the MOSFET GATE to SOURCE voltage. P_{LOSS} is the MOSFET power loss.

Operational Waveform

The normal startup and shut down waveforms for the “ideal diode” configuration with 12V input are shown in Figure 5 and Figure 6.

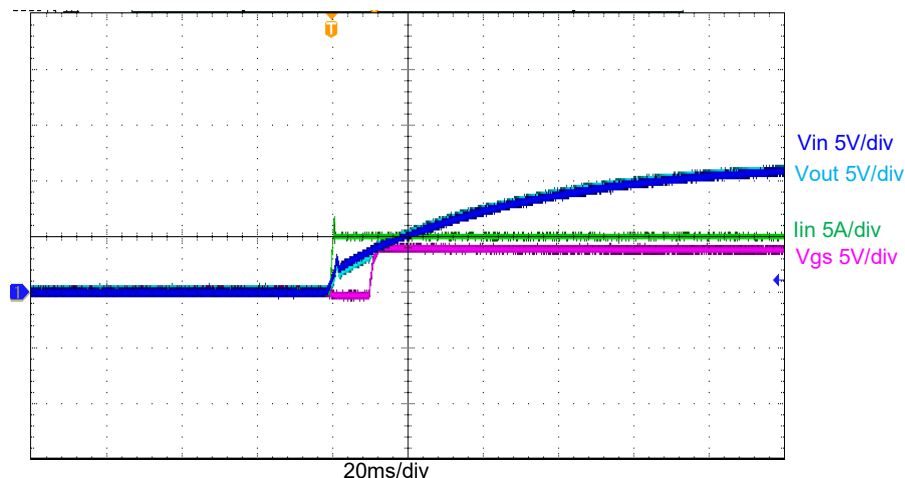


Figure 5. Start up with 12V Vin, and 5A Load

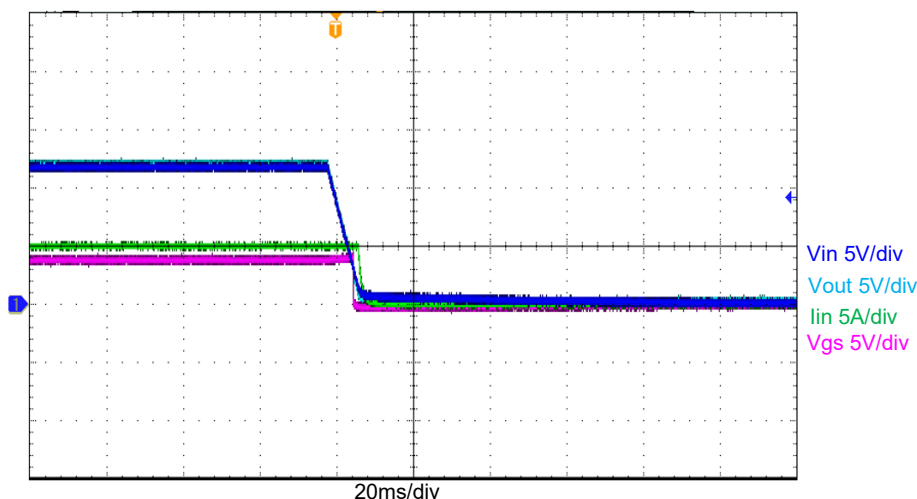


Figure 6. Turn off from 12V Vin, and 5A Load

Reverse Blocking

During input supply failure or micro-short conditions, very high reverse currents can flow in reverse direction, discharging the load capacitors used for VOUT holdup. KTS1900 features a very fast reverse current comparator and a strong gate driver to pull down the gate and turn off the MOSFET. The internal reverse comparator monitors the voltage across the MOSFET source and drain and if it exceeds the reverse current threshold, the GATE is pulled down to source with a fast response. Reverse current comparator delay, gate pulldown current and total gate capacitance determine how fast the MOSFET can be turned off. Figure 7 shows the fast reverse blocking when an input short happens. Once the MOSFET drain to source voltage exceeds the 15mV threshold

the device is turned off. With the MOSFET off the voltage on the body diode increases well beyond the 15mV latching the circuit off. This is shown in Figure 7. The circuit will remain off until the source to drain voltage is above 40mV across the body diode. This prevents the holdup capacitors on VOUT from discharging into the shorted input rail. The IIN trace in Figure 7 shows very little reverse let through current. This keeps the power supplies on the back-end circuits stable.

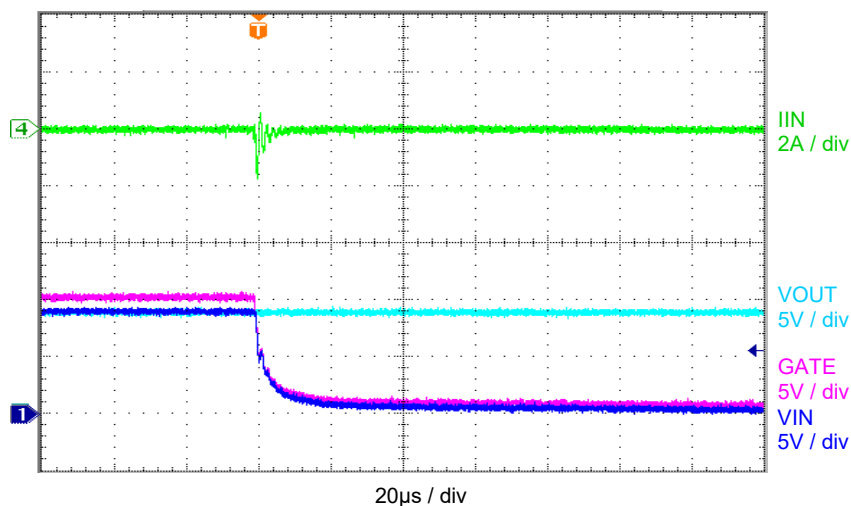


Figure 7. Reverse Blocking During Input Short

Reverse Polarity Protection

During maintenance of the battery or jump start of the vehicle, the battery can be connected in reverse polarity during reinstallation. If a battery is connected with a reversed polarity, the KTS1900 is rapidly turned off to protect the downstream circuits and components from damage. Figure 8 and Figure 9 show the VOUT stability when a reverse battery connection of -12V or -24V is applied at its VIN.

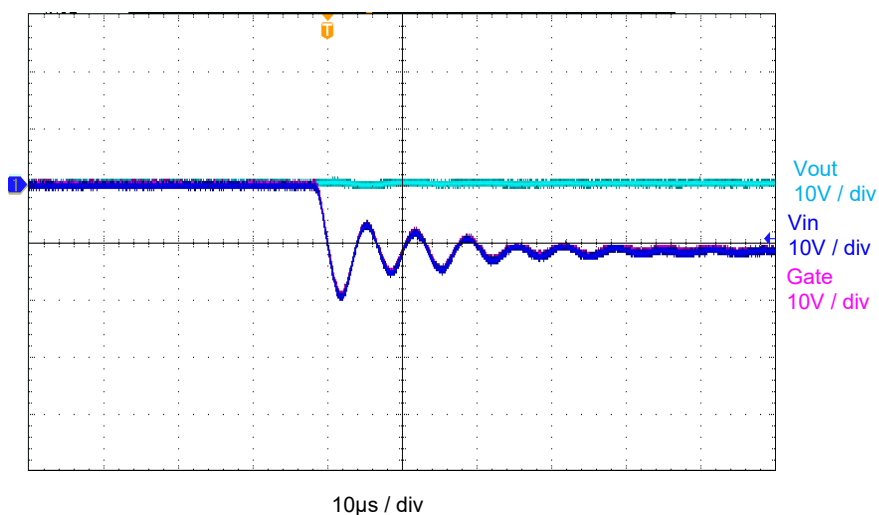


Figure 8. VIN Switch from 0 to -12V

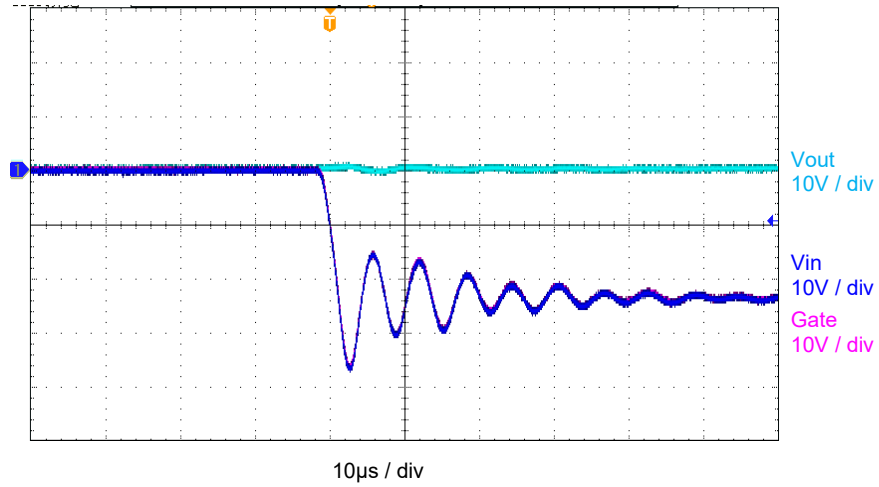


Figure 9. VIN Switch from 0 to -24V

OR-ing Power Supplies Application

In OR-ing power supplies application, two or more power supplies are needed to provide system redundancy or increase power capacity or both. Typically, in the N+1 configuration, more than one power supply source is paralleled with ideal diodes. A minimum 'N' supplies are required to power the load and additional supplies are added for redundancy in case of failed power supplies. The power supply with higher voltage provides most or all the current required by the load. To share loads equally, the power supplies DC set points are adjusted to match other units closely.

With external N-Channel MOSFETs, KTS1900 can be used in an OR-ing solution as shown in Figure 10. When an input supply failure happens, the KTS1900 quickly detects the reverse current and quickly pulls down the MOSFET gate, leaving the body diode of the MOSFET to block the reverse current flow. Redundant power supplies can then service the load.

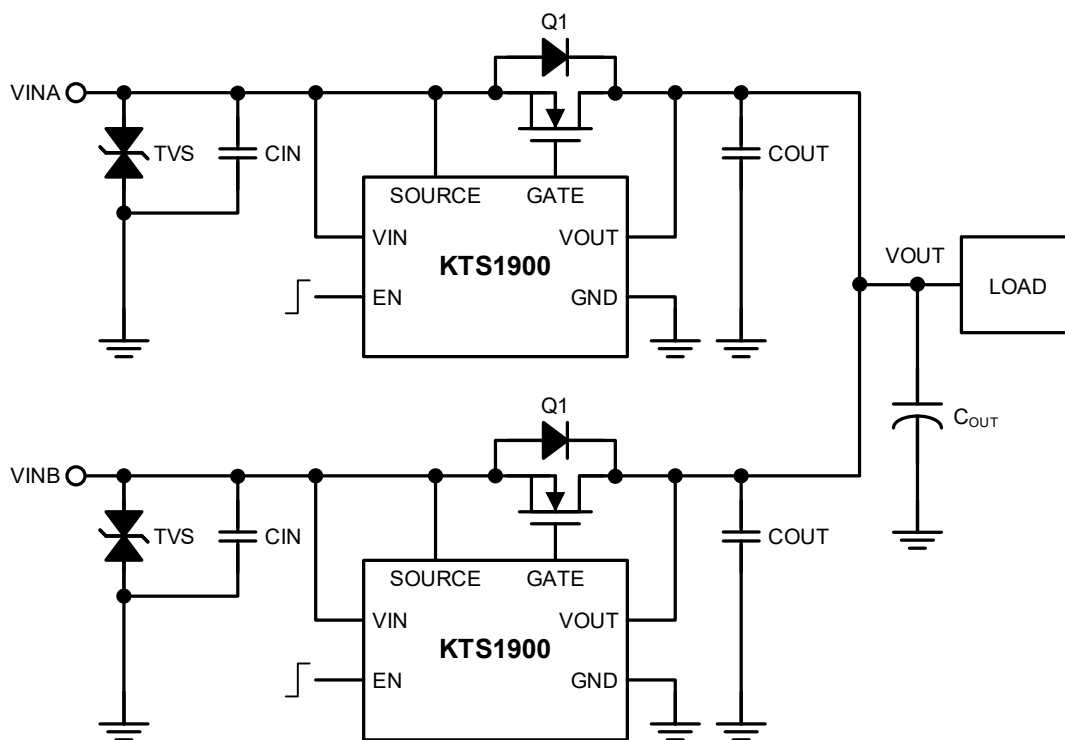


Figure 10. Typical OR-ing Application (Redundant Power Supplies)

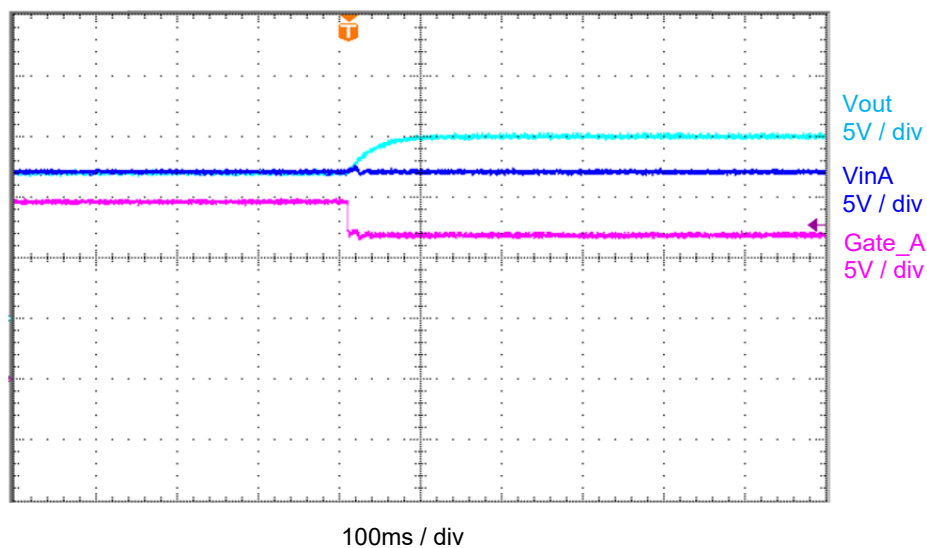


Figure 11. OR-Ing Performance VINB = 15V Step-up When VINA = 12V

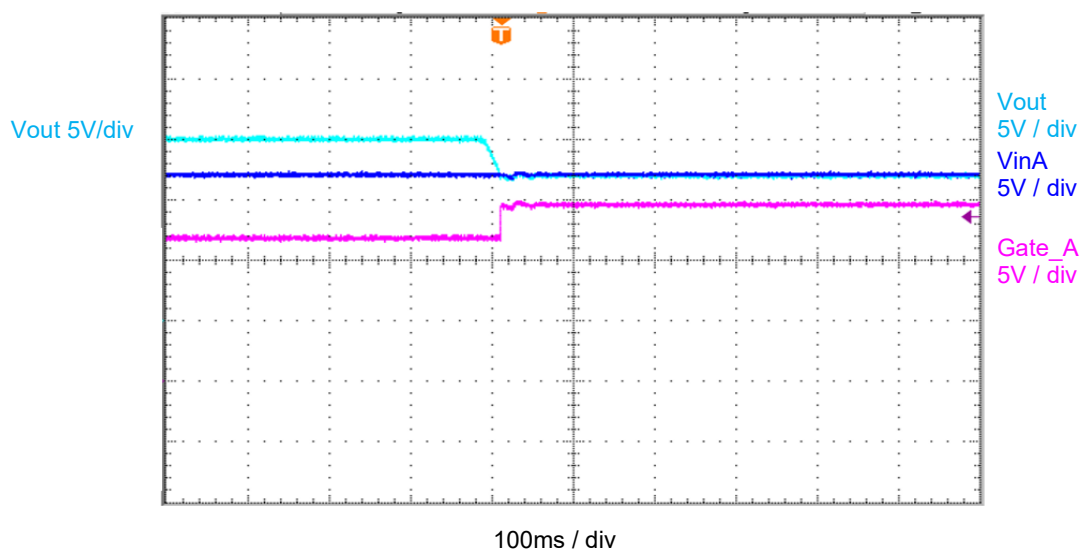


Figure 12. OR-Ing Performance VINB = 15V turns off When VINA = 12V

Load Switch Configuration

In load switch configuration, an additional MOSFET (Q2) can be used in the KTS1900 circuit to shut down the current to the load. In this case, Q1 acts as the ideal diode, while Q2 acts as a switch to control forward current flow. The circuit is shown in Figure 13. In addition, the back-to-back body diodes of two MOSFETs prohibit current flow, in both directions, when the MOSFETs are off. The turn on is inherently slow due to the low charge pump current of $15\mu\text{A}$ and the total gate capacitance.

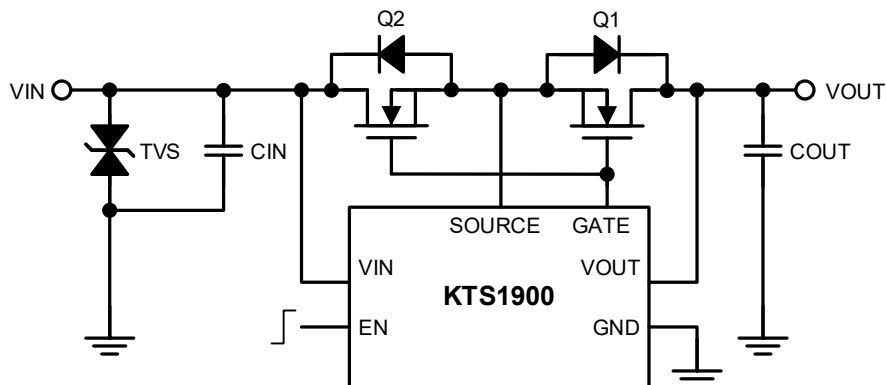


Figure 13. Load Switch Circuit Configuration with two MOSFETs

Operational Waveform

The normal turn on and off waveforms are shown in Figure 14 and Figure 15.

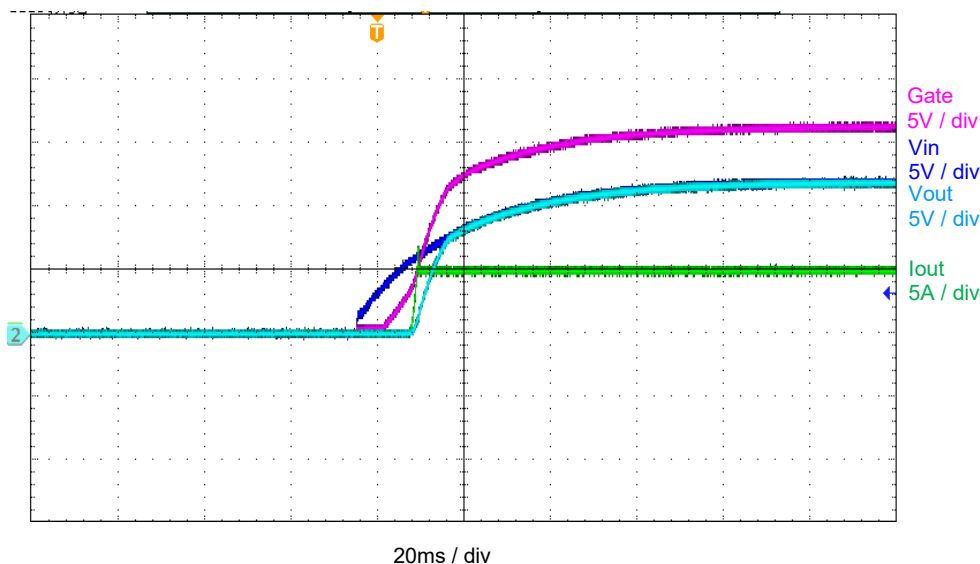


Figure 14. Start up at 12V Vin, and 5A Load

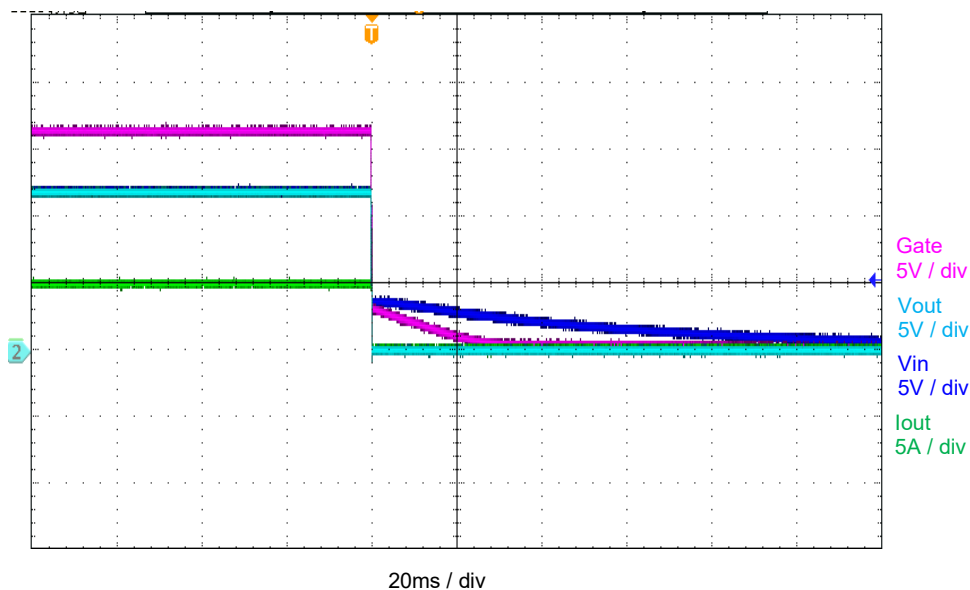


Figure 15. Turn off from 12V Vin, and 5A Load

Reverse Polarity Protection

To test the dynamic input reverse protection a -12V or -24V source is connected to the input of the KTS1900. Figure 16 and Figure 17 show that the VOUT remains at a constant 0V in this situation. This test shows that the KTS1900 can protect the load from negative input voltage.

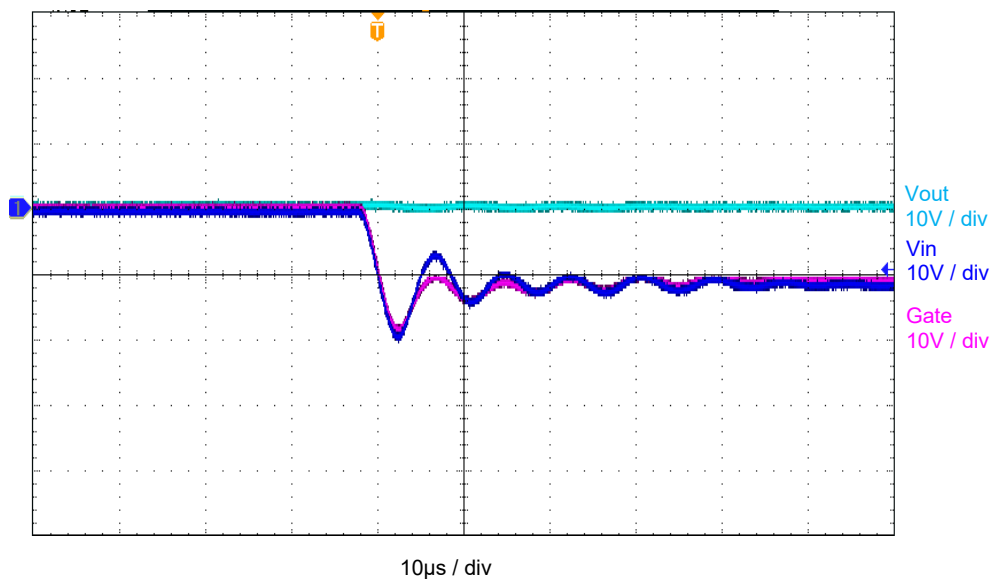


Figure 16. VIN Switch from 0V to -12V Reverse Protection

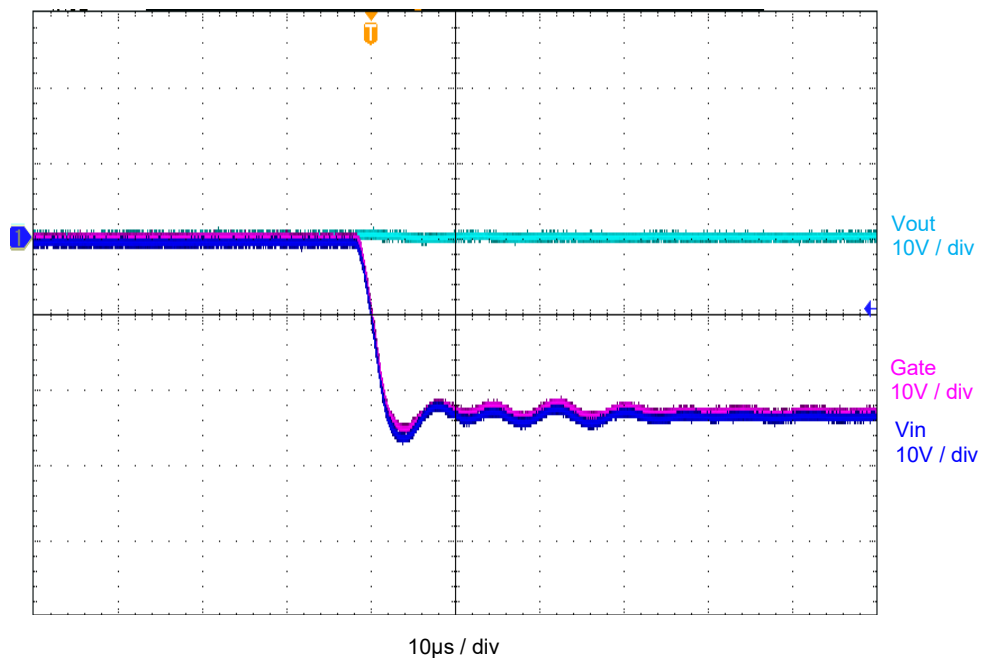


Figure 17. VIN Switch from 0V to -24V Reverse Protection

Input Voltage Short Protection

For input voltage short protection, VIN is switched from 12V to 0V, and VOUT keeps stable, with low reverse current as shown in Figure 18.

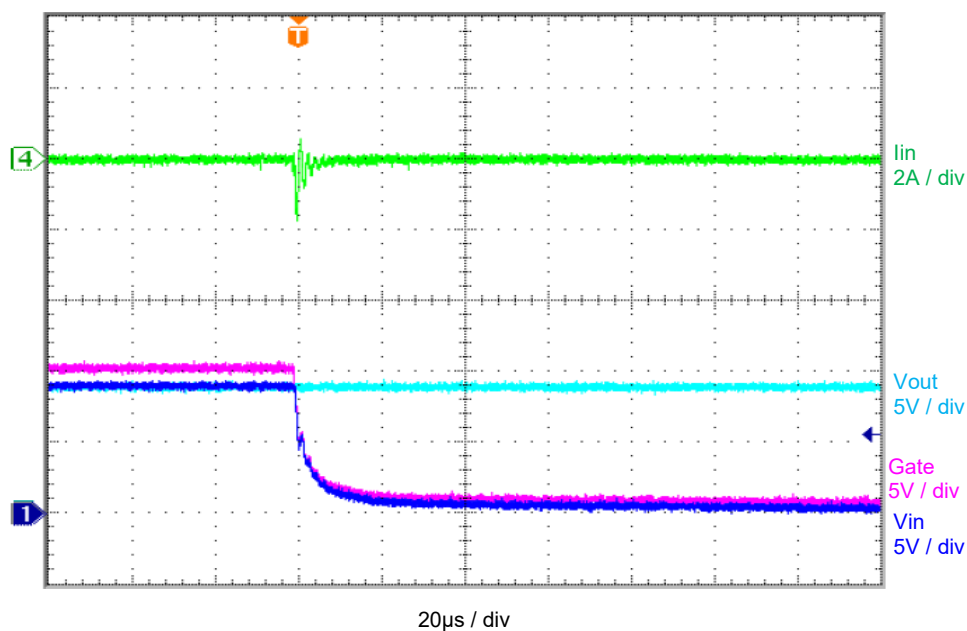


Figure 18. VIN Switch 12V to 0V Short Protection

ISO7637-2 Pulse Test

To ensure the compatibility of KTS1900 to conducted electrical transients for automotive applications; ISO7637-2 Pulse test is used as the reference with 12 V or 24 V electrical systems. This test is a simulation of transients due to supply disconnection from inductive loads. The test waveform details, and the related parameters are shown in Figure 19 and Table 2.

During dynamic reverse polarity conditions specified in ISO 7637-2 for 12 volt systems, a negative voltage transient is applied at the 12V battery supply line (VIN). A -150 volt transient is generated from a 10Ω generator impedance for 2ms. The 24 Volt system is hit with a -600V, 50Ω generator for 1ms. When the ISO 7637-2 test pulse is applied to VIN, the load current starts to reverse quickly and tries to pull the VOUT negative. KTS1900 detects the reverse current and turns OFF the MOSFET to block reverse current and prevent the VOUT from dropping. Downstream, bulk holdup capacitors, provide energy to the rest of the module during such transients. With a bi-direction TVS, the input voltage is clamped from exceeding the absolute maximum ratings of KTS1900 and N-MOSFET.

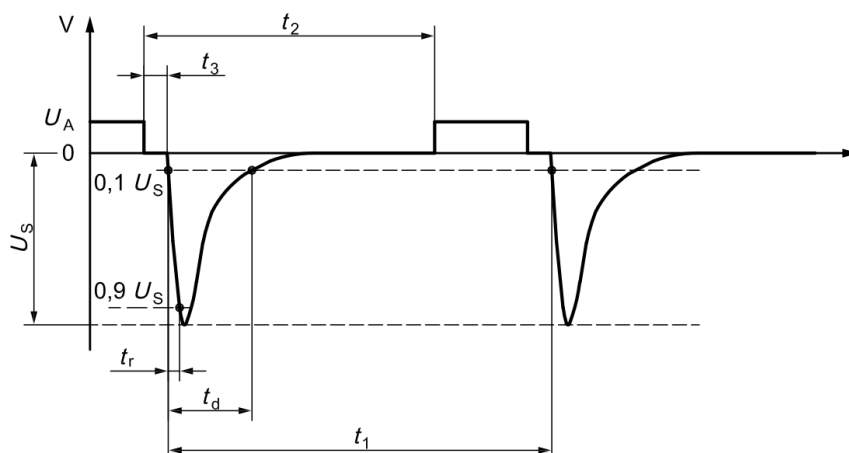


Figure 19. Test Pulse 1 Reference Waveform Details in ISO7637-2 Pulse Test Standard

Table 2. Parameters for Test Pulse 1 in ISO7637-2 Standard

Parameters	Nominal 12V System	Nominal 24V System
U_s	-75V to -150V	-300V to -600V
t_d	2ms	1ms
t_r	~1μs	~3μs
t_1	≥0.5s	
t_2	200ns	
t_3	<100μs	
t_1 shall be chosen such that it is the minimum time for the DUT to be correctly initialized before the application of the next pulse.		
t_3 Is the smallest possible time necessary between the disconnection of the supply source and the application of the pulse.		

Figure 20 shows the result of KTS1900 for -600V transient pulse test that can be used as the reference for 24V system. The large current spike seen in the lin trace is the conduction of the TVS diode. The Vin trace shows the input voltage is clamped to -40 Volts during the lin current spike.

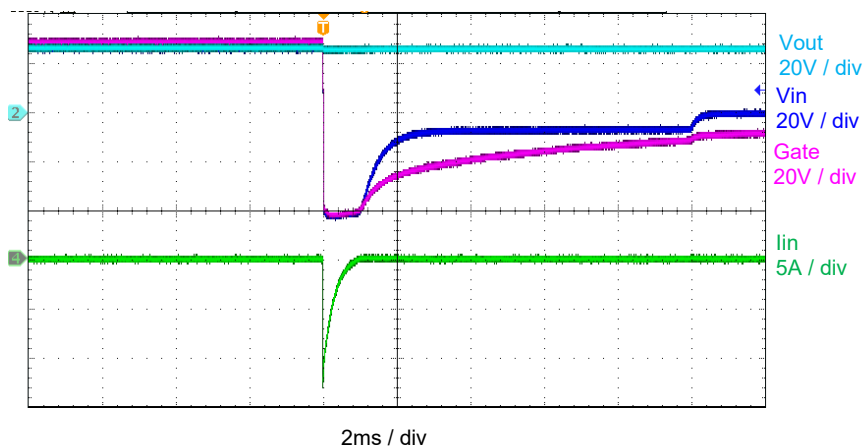
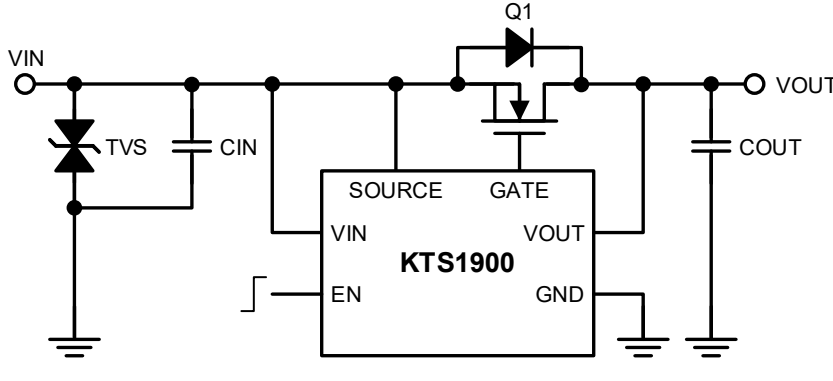
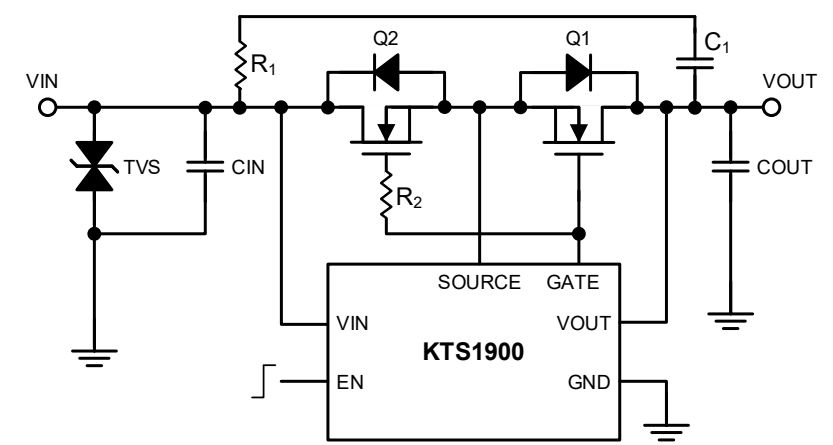


Figure 20. -600V Transient Results Based on ISO7367-2 Pulse Test

Typical Application Circuits

Ideal Diode Schematic	BOM
	TVS = SMBJ33CA-13-F DIODE, TVS, Bi, 33V, SMB Q1 = DMT6007LFG-13 MOSFET, N-CH, 60V, 15A CIN = 2.2μF, 100V, ±10%, X7R, 1210 COUT = 2.2μF, 100V, ±10%, X7R, 1210
Load Switch Schematic	BOM
	TVS = SMBJ33CA-13-F DIODE, TVS, Bi, 33V, SMB Q1 and Q2 = IPB027N10N3GATMA1 MOSFET, N-CH, 100V, 120A CIN = 2.2μF, 100V, ±10%, X7R, 1210 COUT = 2.2μF, 100V, ±10%, X7R, 1210 C1 = 10nF, 500V, ±20%, X7R, 1206 R1 = 100Ω, 1/2W, 5%, 1210 R2 = 10Ω, 1/8W, 5%, 0805

Recommended PCB Layout

The recommended KTS1900 PCB layout is optimized for low EMI, and good performance and follows the below PCB layout recommendations.

1. Connect a 2.2μF capacitor CIN as close as possible to the VIN and GND pins using wide metal traces and ground plane.
2. Connect the VIN, SOURCE and VOUT pins as close as possible to the MOSFET source and drain pins. With short and wide traces to minimize resistive losses.
3. Place surge suppressors and transient protection components as close as possible to the input of KTS1900 with short lead lengths.
4. Connect a 2.2μF capacitor, COUT, as close as possible to the GND and VOUT pins.
5. Check the creepage and clearance details and guidelines to determine the spacing between high voltage (VIN) and other nearby traces.

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[NCV459MNWTBG](#) [NCP4545IMNTWG-L](#) [NCV8412ASTT1G](#) [NCV8412ASTT3G](#) [FPF2260ATMX](#) [NCP45760IMN24RTWG](#)
[NCP45780IMN24RTWG](#) [NCP45540IMNTWG-L](#) [DK5V100R20S](#) [BTS7020-2EPA](#) [BTT6100-2ERA](#) [BTS71220-4ESA](#) [DK5V100R15M](#)
[AW32405CSR](#) [BTT6030-2ERA](#) [TLE75602-ESH](#) [BTS5200-4EKA](#) [DK5V45R25](#) [DK5V100R25S](#) [AW35206FOR](#) [BTS7120-2EPA](#) [BTT6030-1ERA](#) [DK5V60R10S](#) [DK5V45R25S](#) [DK5V45R15S](#) [DK5V100R15S](#) [WS3241C-12/TR](#) [WS4622C-4/TR](#) [SY7215ARDC](#) [BTT6200-4ESA](#)
[BTS7080-2EPA](#) [AW35122FDR](#) [AW35121FOR](#) [BTS7080-2EPZ](#) [BTT6050-1ERA](#) [ITS42K5DLDF](#) [BTS7012-2EPA](#) [BTT6020-1ERA](#)
[DK5V45R20S](#) [DK5V60R30S](#) [SQ24026DUC](#) [SK62606D8-ADJ](#) [XC8107XC05MR-G](#)