



6A, 5.5V Low On-Resistance Dual-Channel Load Switch

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW®7107S is a low on-resistance dual channel load switch with programmable turn-on rise time. It contains two N-channel MOSFETS that can provide 6A maximum continuous current per channel. Each channel can operate over an input voltage range of 0.8V to 5.5V.

Each channel can be independently controlled by a low-voltage control signal through EN1/EN2 pin. In JW7107S, a 200Ω load resistor is integrated for quick output discharge when load switch is turned off. The optional external capacitor connected to SS1/SS2 is used for output slew rate control.

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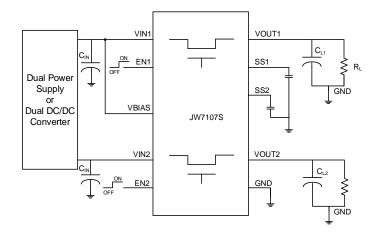
FEATURES

- Operating range : 0.8V ~ 5.5V
- Low quiescent current 80uA (both channels)
 60uA (single channels)
- Low on-resistance
- Integrated dual-channel
 up to 6A maximum load current per channel
- Low-voltage enable control
- Externally programmable rise time
- Quick output discharge
- Thermal shutdown
- Available in DFN3x2-14 package

APPLICATIONS

- Portable Computers
- Tablet PCs
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid-State Drives (SSD)

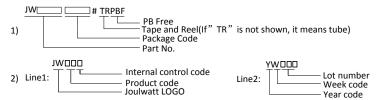
TYPICAL APPLICATION



ORDER INFORMATION

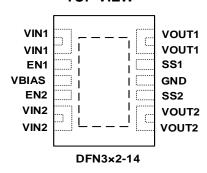
DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
NA/7107CDENIC#TDDDE	DEN2v2 14	JWFN□
JW7107SDFNC#TRPBF	DFN3×2-14	YW□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING¹⁾

VIN1,2 PIN Voltage	0.3V to 7V
VOUT1,2 PIN Voltage	0.3V to 7V
EN1,2 PIN Voltage	0.3V to 7V
(SS1,2-VOUT1,2) PIN Voltage	0.3V to 6.5V
VBIAS Voltage	0.3V to 7V
Maximum Continuous Switch Current Per Channel	6A
Maximum Pulsed Switch Current Per Channel, Pulse<300us 3% duty cycle	8A
Junction Temperature ²⁾	150°C
Lead Temperature	260°C
Storage Temperature	65°C to +150°C
ESD Susceptibility (Human Body Model)	2kV
Continuous Power Dissipation(T ₄ =+25°C) DFN3×2-14	2W

RECOMMENDED OPERATING CONDITIONS³⁾

VIN1,2 PIN Voltage	3.0	BV to V _{BIAS}
EN1,2 PIN Voltage	(0V to 5.5V
VBIAS Voltage	2.	5V to 5.5V
Operating Junction Temperature	40°	C to 125°C
THERMAL PERFORMANCE ⁴⁾	$oldsymbol{ heta}_{\!\scriptscriptstyle J\!A}$	$ heta_{Jc}$
DFN3x2-14	52.3	6.9°C/W

Note:

- 2) The JW7107S includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

¹⁾ Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

JW7107S

ELECTRICAL CHARACTERISTICS

Item	Symbol	Con	dition	Min.	Тур.	Max.	Units	
POWER SUPPLIES AN	ND CURRENTS							
V _{BIAS} quiescent current (both channels)	I _{IN(VBIAS-ON)}	$I_{OUT1} = I_{OUT2} = 0mA$ $V_{IN1,2} = V_{EN1,2} = V_{BIAS} =$	5.0V		50	55	uA	
V _{BIAS} quiescent current (single channel)	I _{IN(VBIAS-ON)}	$I_{OUT1} = I_{OUT2} = 0$ mA, V_{EN} $V_{IN1,2} = V_{EN1} = V_{BIAS} = 5$	_		38	45	uA	
V _{BIAS} shutdown current	I _{IN(VBIAS-OFF)}	V _{EN1,2} =0V, V _{OUT1,2} =0V			0.1	1	uA	
V _{IN1,2} off-state supply current (per channel)	I _{IN(VIN-OFF)}	V _{EN1,2} =0V V _{OUT1,2} =0V		0.1	1	uA		
EN pin input leakage current	I _{EN}	V _{EN} = 5.5 V				1	uA	
RESISTANCE CHARAG	CTERISTICS							
ON-state resistance (per channel)			V _{IN} = 5.0V		17	21		
	R _{on}	$I_{OUT} = -200$ mA $V_{BIAS} = 5.0$ V	V _{IN} = 3.3V		17	21	- mΩ	
			V _{IN} = 1.8V		17	21		
			V _{IN} = 1.5V		17	21		
			V _{IN} = 1.2V		17	21		
			V _{IN} = 0.8V		17	21		
Output pull-down resistance	R _{PD}	V _{IN} =5.0V, V _{EN} =0V, V _{OUT} =0.5V			200		Ω	
$V_{BIAS} = 2.5V$, typical	values are fo	or $T_A = 25^{\circ}$ C, unless	otherwise stated	<u> </u>				
$V_{BIAS} = 2.5V$, typical Item	values are fo		otherwise stated	Min.	Тур.	Max.	Units	
	Symbol	Con			Тур.	Max.	Units	
Item POWER SUPPLIES AN	Symbol	Con	dition		Typ. 35	Max.	Units uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current	Symbol ND CURRENTS	Condition $I_{OUT1} = I_{OUT2} = 0$ mA	2.5V _{N2} =0V					
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current (single channel)	Symbol ND CURRENTS I _{IN(VBIAS-ON)}	Constitution $I_{OUT1} = I_{OUT2} = 0$ mA $V_{IN1,2} = V_{EN1,2} = V_{BIAS} = I_{OUT1} = I_{OUT2} = 0$ mA, V_{EN}	2.5V _{N2} =0V		35	40	uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current (single channel) V _{BIAS} shutdown current V _{IN1,2} off-state supply	Symbol ND CURRENTS I _{IN(VBIAS-ON)} I _{IN(VBIAS-ON)}	Cond $I_{OUT1} = I_{OUT2} = 0mA$ $V_{IN1,2} = V_{EN1,2} = V_{BIAS} =$ $I_{OUT1} = I_{OUT2} = 0mA, V_{EN}$ $V_{IN1,2} = V_{EN1} = V_{BIAS} = 2$	2.5V _{N2} =0V		35	40	uA uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current (single channel) V _{BIAS} shutdown current V _{IN1,2} off-state supply current (per channel) EN pin input leakage	Symbol ND CURRENTS I _{IN(VBIAS-ON)} I _{IN(VBIAS-ON)} I _{IN(VBIAS-OFF)}	Condition I $I_{OUT1} = I_{OUT2} = 0$ mA $V_{IN1,2} = V_{EN1,2} = V_{BIAS} = I_{OUT1} = I_{OUT2} = 0$ mA, $V_{EN1,2} = V_{EN1} = V_{BIAS} = 2$ $V_{EN1,2} = 0$ V, $V_{OUT1,2} = 0$ V $V_{EN1,2} = 0$ V	2.5V 2.5V 2.5V		35 27 0.1	40 35 1	uA uA uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current (single channel) V _{BIAS} shutdown current V _{IN1,2} off-state supply current (per channel) EN pin input leakage current	Symbol ND CURRENTS I _{IN(VBIAS-ON)} I _{IN(VBIAS-OFF)} I _{IN(VIN-OFF)} I _{EN}	I _{OUT1} = I _{OUT2} = 0mA V _{IN1,2} = V _{EN1,2} = V _{BIAS} = I _{OUT1} = I _{OUT2} = 0mA, V _{EN} V _{IN1,2} = V _{EN1} = V _{BIAS} = 2 V _{EN1,2} =0V, V _{OUT1,2} = 0V V _{EN1,2} =0V V _{OUT1,2} =0V	2.5V 2.5V 2.5V		35 27 0.1	40 35 1	uA uA uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current (both channels) V _{BIAS} quiescent current (single channel) V _{BIAS} shutdown current V _{IN1,2} off-state supply current (per channel) EN pin input leakage current RESISTANCE CHARAC	Symbol ND CURRENTS I _{IN(VBIAS-ON)} I _{IN(VBIAS-OFF)} I _{IN(VIN-OFF)} I _{EN}	I _{OUT1} = I _{OUT2} = 0mA V _{IN1,2} = V _{EN1,2} = V _{BIAS} = I _{OUT1} = I _{OUT2} = 0mA, V _{EN} V _{IN1,2} = V _{EN1} = V _{BIAS} = 2 V _{EN1,2} =0V, V _{OUT1,2} = 0V V _{OUT1,2} =0V V _{OUT1,2} = 0V	2.5V 2.5V 2.5V		35 27 0.1	40 35 1	uA uA uA	
Item POWER SUPPLIES AN V _{BIAS} quiescent current	Symbol ND CURRENTS I _{IN(VBIAS-ON)} I _{IN(VBIAS-OFF)} I _{IN(VIN-OFF)} I _{EN}	I _{OUT1} = I _{OUT2} = 0mA V _{IN1,2} = V _{EN1,2} = V _{BIAS} = I _{OUT1} = I _{OUT2} = 0mA, V _{EN} V _{IN1,2} = V _{EN1} = V _{BIAS} = 2 V _{EN1,2} =0V, V _{OUT1,2} = 0V V _{EN1,2} =0V V _{OUT1,2} =0V	2.5V N ₂ =0V .5V V _{IN1,2} = 2.5V		35 27 0.1 0.1	40 35 1 1	uA uA uA	

		I		V 12V			10	25	
				V _{IN} = 1.2V			19	25	
0				$V_{IN}=0.8V$			18	24	
Output pull-down resistance	R_{PD}	V _{IN} =2.	5V, V _{EN} =0V, V _{OUT} =	=0.5V			200		Ω
EN CHARACTERISTICS	<u> </u>								
EN high level voltage	V _{ENH}	\/=0	8V to 5V			1.2			V
EN low level voltage	VENH	1	8V to 5V			1.2		0.5	V
OVER TEMPERATURE PR		V IN-O.	0 10 3 1					0.0	
Thermal shutdown									Т
threshold ⁵⁾	T _{SD}	V _{IN} =5.	V_{IN} =5.0V, V_{EN} =5V				155		°C
Thermal shutdown	T _{HYS}						25		°C
hysteresis ⁵⁾	THYS						23		
Item	Symbo	l	Condi	tion	Min.	Тур.	Ma	ax.	Units
$V_{IN} = V_{EN} = V_{BIAS} = 5 V$, 7	$T_A = 25^{\circ}\text{C}$ (unle	ss othe	rwise noted)						
Turn-on time	t _{ON}					1383			
Turn-off time	t _{OFF}					2.5			
V _{OUT} rise time	t _R		$R_L = 10\Omega, C_L = 0.1 \mu F$			1736			μs
V _{OUT} fall time	t _F		C _{SS} = 1nF			2			
EN delay time	t _D		1		515				
$V_{IN} = 0.8 \text{ V}, V_{EN} = V_{BIAS} =$	$= 5 \text{ V}, T_A = 25\%$	C (unles	s otherwise note	ed)					
Turn-on time	t _{ON}					511			
Turn-off time	t _{OFF}					2.5			
V _{OUT} rise time	t _R		$R_L = 10\Omega, C_L = 0.1 \mu F$		336			μs	
V _{OUT} fall time	t _F		$C_{SS} = 1$	C _{SS} = 1n F		1.7			
EN delay time	t _D					343			
$V_{IN} = 2.5 \text{ V}, V_{EN} = 5 \text{ V}, V_{EN}$	$T_{BIAS} = 2.5 \text{ V, } T_A$	= 25°C	(unless otherwi	se noted)	•				
Turn-on time	t _{on}					2150	T		
Turn-off time	t _{OFF}					3.4			
V _{OUT} rise time	t _R		$R_L = 10\Omega, C_L$			2350			μs
V _{OUT} fall time	t _F		C _{SS} = 1	n F		2			
EN delay time	t _D					1000			
$V_{IN} = 0.8 \text{ V}, V_{EN} = 5 \text{ V}, V_{EN}$	$T_{BIAS} = 2.5 \text{ V, } T_{A}$	= 25°C	(unless otherwi	se noted)					
Turn-on time	t _{on}				T	1260			
Turn-off time	t _{OFF}] _			3.8			
V _{OUT} rise time	t _R		$R_L = 10\Omega, C$			850			μs
V _{ouт} fall time	t _F		C _{SS} = 1	пЕ		2			
EN delay time	t _D		1			816			

Note:

5) Guaranteed by design

Parameter Measurement Information

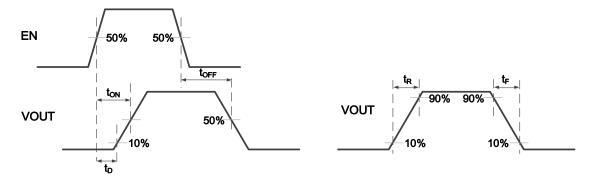
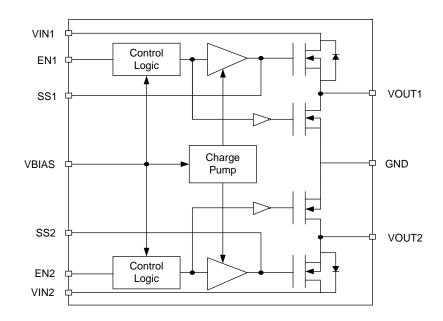


Figure 1. Timing Waveforms

PIN DESCRIPTION

Pin DFN3×2-14	Name	Description
		Switch 1 input.
1、2	VIN1	Recommended voltage range for this pin is 0.8V to V _{BIAS} to obtain optimal on-resistance.
		Bypass capacitor is also need to minimize VIN dip during turn-on of the channel.
3	EN1	Active high switch 1 control input. Do not leave floating.
4	VBIAS	Bias voltage.
4	VDIAS	Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
5	EN2	Active high switch 2 control input. Do not leave floating.
		Switch 2 input.
6、7	VIN2	Recommended voltage range for this pin is 0.8V to V _{BIAS} to obtain optimal on-resistance.
		Bypass capacitor is also need to minimize VIN dip during turn-on of the channel.
8、9	VOUT2	Switch 2 output.
10	SS2	Slew rate control of switch 2.
10	332	Capacitor connected to this pin should be rated no less than 15V.
11	GND	Ground
12	SS1	Slew rate control of switch 1.
12	331	Capacitor connected to this pin should be rated no less than 15V.
13、14	VOUT1	Switch 1 output.
Thermal Pad		Thermal pad (exposed center pad) must be connected to GND.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ON/OFF Control

EN high with 1.2V or high GPIO voltage enables the switch. The EN pin is compatible with standard logic threshold. This pin must be tied either high or low for proper functionality.

VIN and VBIAS Voltage Range

VBIAS is recommended to work within the range from 2.5V to 5.5V. For optimal on-resistance performance of load switch, make sure VIN ≤ VBIAS. Otherwise, the device will exhibit greater on-resistance than that in Electrical Characteristics. Resistance curves of a typical device at different temperature and VIN are shown as below.

Input Capacitor (Optional)

A 1-µF or higher ceramic capacitor is recommended to be placed between VIN1/VIN2 and GND to reduce the voltage drop caused by inrush current when switch turns on to charge a full-discharged load capacitor. A higher values capacitor can further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to put an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, an input capacitor greater than output capacitor is highly recommended. So the output can be discharged more quickly than input when the power supply is off. An input capacitor to output ratio of 10 to 1 is recommended. A larger output capacitor makes the initial turn-on transient smoother. In order to prevent the output from dropping, the output capacitor must be large enough to supply a fast transient load.

Over-Temperature Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults occurs. The JW7107S implements a thermal sensing circuit to monitor the operating junction temperature. Once the die temperature rises to approximately +155°C, the thermal protection feature activates as follows: The internal thermal sense circuitry turns the power switch off to prevent the power switch from damage. Once the junction temperature drops to 130°C, the MOSFET restart to work.

Power Sequencing

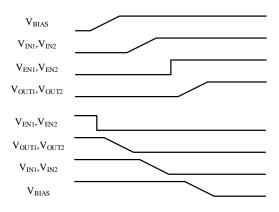


Figure 2. Power Sequencing

The charge pump block will stop working when VBAIS is Low. The voltage of charge pump cannot discharge without VBIAS. So EN shutdown before VBIAS is recommended and also VBIAS startup before EN and keep it high level is recommended.

PCB Guidelines

Good PCB helps improving the performance of JW7107S:

- For best performance, all traces should be as short as possible.
- For best efficiency, the input and output decoupling capacitors should be placed as close to the device as possible, so that the

parasitic impact can be minimized. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Device Functional Modes

Table1. Device Functional Modes

ENx	VINx to VOUTx	VOUTx to GND				
L	OFF	ON				
Н	ON	OFF				

JW7107S JouIWati

APPLICATION INFORMATION

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value. The inrush current presents a constant value controlled by the device. It can be calculated as below:

 $I_{inrush} = C \times dV/dt$

Where,

C - output capacitance

dV - output voltage

dt - rise time

Take a 3.3V case as an example. The parameters are shown in the table2.

Table2. Design Parameter

DESIGN PARAMETER	VALUE
Input voltage	3.3V
Bias voltage	5V
Load capacitance (CL)	22µF
Maximum acceptable inrush current	400mA

To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5µs.

JW7107S offer adjusted rise time for VOUT. So the user can control the inrush current during turn-on period. The appropriate rise time can be calculated using the following equation.

400 mA = 22 μ F × 3.3 V/dt dt = 181.5 μ s

Adjustable Rise Time

The rise time of each channel in JW7107S can be adjusted individually by external capacitors connected between SS and GND pins. To ensure desired performance, a capacitor with a minimum voltage rating of 15 V should be placed on the SS1/SS2 pin.

The approximate rise time of VOUT measured on a typical device at VBIAS = 5V is shown in table 3. Rise time can be calculated by multiplying the input voltage by the slew rate. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition, and the EN pin is used to enable the device.

Table3:

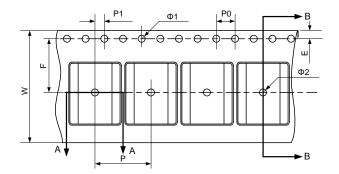
	RISE TIME (RISE TIME (μ s) 10% - 90%, CL = 0.1 μ F, CIN = 1 μ F, RL = 10 Ω									
SSx (pF)	TYPICAL VALUES at 25°C, VBIAS = 5V, 25V X7R 10% CERAMIC CAP										
	0.8	0.8 1.05 1.5 1.8 2.5V 3.3V 5V									
0	54.8	64.4	78.8	86.8	102.8	118	164				
220	120	143	186	217	291	360	518				
470	181	223	298	352	466	588	876				
1000	330	414	548	660	888	1156	1744				
2200	656	840	1160	1368	1872	2384	3656				
4700	1408	1760	2440	2888	3936	5100	7860				
10000	2940	3700	5120	5980	8280	10720	16360				

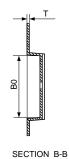
TAPE AND REEL INFORMATION

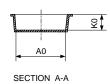
	UNIT: mr
ness Width W4	
tess Width W4 W2 ±2 9.5±2 60±2	

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Carrier Tape UNIT: mm







Note:
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

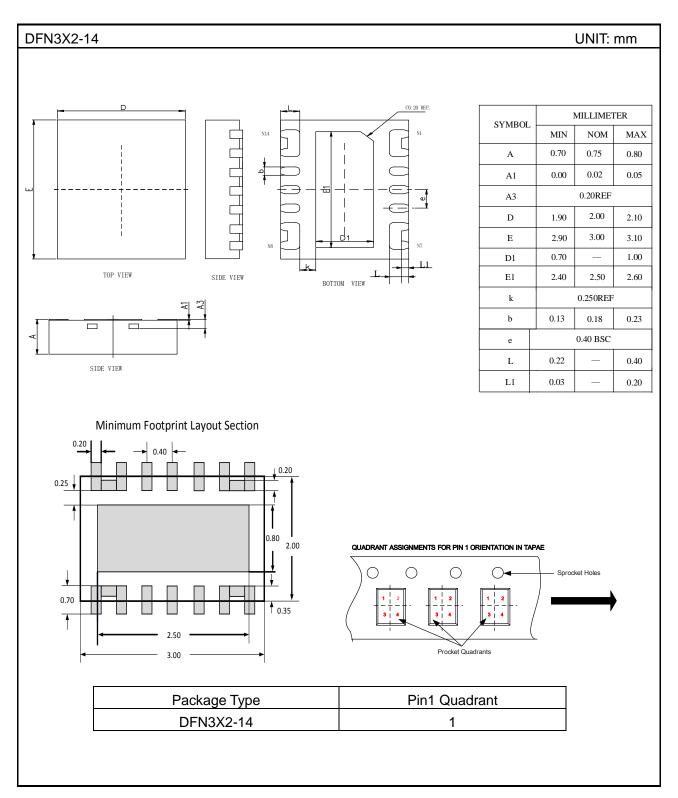
Package ₽	P0 <i>₽</i>	P1 ₽	P €	A0 ₽	B0 ₽	W≠	T o	K0 ₽	Ф1₽	Ф2 🕫	E₽	F≠
DFN3 x 2-14 ₽	4.0±0.1 ₽	2.0±0.1 ₽	4.0±0.1 ₽	2.30±0.2 ₽	3.20±0.2 ₽	8.0±0.3₽	0.30±0.2 ₽	1.00±0.20 ₽	1.55±0.10 ₽	1.00±0.1 ₽	1.75±0.1 ₽	3.50±0.1 ₽

2021/01/11

JW7107S

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PACKAGE OUTLINE



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KTS1640QGDV-TR KTS1641QGDV-TR BTS500101TADATMA2 NCV459MNWTBG NCP4545IMNTWG-L NCV8412ASTT1G

NCV8412ASTT3G FPF2260ATMX SLG5NT1765V SLG5NT1757V SLG59M1557VTR BD2222G-GTR NCP45780IMN24RTWG

NCP45540IMNTWG-L TPNTJD1155LT1G FDC6324L-TP FDC6326L-TP TPS11869DH-T1-E3 SI1865DDL FDC6330L-TP U6210

U25135 U62153 U6513BS U62133 U6773H U62143S U6315BS U6513B U6110 SL3405S BTS7040-2EPA SY6282ACC WS3222D-8/TR DP25136C DK5V100R20C