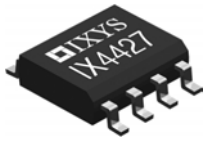
IXYS
INTEGRATED CIRCUITS DIVISION



IX4426-IX4427-IX4428
1.5-Ampere Dual Low-Side Ultrafast MOSFET Drivers

Features

- 1.5A Peak Output Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Operating Temperature Range
- Latch-up Protected to 1.5A
- TTL and CMOS Compatible Inputs
- Fast Rise and Fall Times
- Low Power Consumption

Applications

- MOSFET Driver
- Switching Power Supplies
- Motor Controls
- DC to DC Converters
- Pulse Transformer Driver

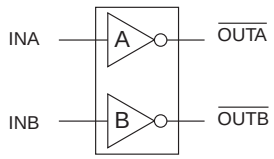
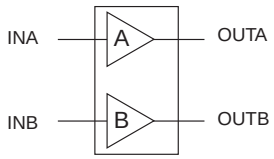
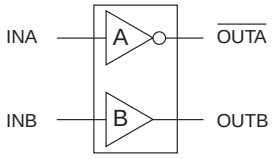
Description

The IX4426, IX4427, and IX4428 are dual high-speed, low-side gate drivers. Each of the two outputs can source and sink 1.5A of peak current with rise and fall times of less than 10ns. The inputs of each driver are TTL and CMOS compatible, and are virtually immune to latch-up. Low propagation delay times and fast, matched rise and fall times make the IX4426, IX4427, and IX4428 ideal for high-frequency and high-power applications.

The IX4426 is configured as a dual inverting driver; the IX4427 is configured as a dual non-inverting driver; and the IX4428 is configured with one inverting driver and one non-inverting driver. All three devices are available in a standard 8-pin SOIC package (N suffix) and an 8-pin DFN package (M suffix).

Pb RoHS e3

Ordering Information

Logic Configuration	Part Number	Package Type	Packing Method	Quantity
	IX4426N	8-Pin SOIC	Tube	100
	IX4426NTR	8-Pin SOIC	Tape & Reel	2000
	IX4426MTR	8-Pin DFN	Tape & Reel	2000
	IX4427N	8-Pin SOIC	Tube	100
	IX4427NTR	8-Pin SOIC	Tape & Reel	2000
	IX4427MTR	8-Pin DFN	Tape & Reel	2000
	IX4428N	8-Pin SOIC	Tube	100
	IX4428NTR	8-Pin SOIC	Tape & Reel	2000
	IX4428MTR	8-Pin DFN	Tape & Reel	2000

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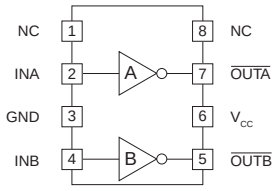
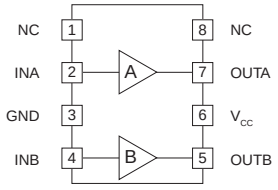
1 Specifications

1.1 Pin Configurations

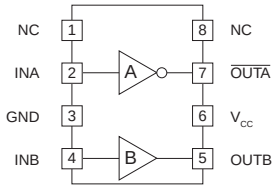
IX4426



IX4427



IX4428



1.2 Pin Definitions

Pin Name	Description
INA	Channel A Logic Input
INB	Channel B Logic Input
OUTA $\overline{OUTA}$	Channel A Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
OUTB $\overline{OUTB}$	Channel B Output - Sources or sinks current to turn on or turn off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	No Connection

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	35	V
Input Voltage	V_{IN}	-5.0	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±1.5	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless otherwise specified, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	4.5	30	V
Operating Temperature Range	T_A	-40	+125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 18V.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	-	V_{IH}	2.4	-	-	V
Input Voltage, Low	-	V_{IL}	-	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	-	±1	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	4	8	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	2	4	
Latch-Up Protection	With Reverse Current	I	>500	-	-	mA
Rise Time	V_{CC}=18V, C_{LOAD}=1000pF	t_R	-	10	20	ns
Fall Time	V_{CC}=18V, C_{LOAD}=1000pF	t_F	-	8	20	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=1000pF	t_{on}	-	35	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=1000pF	t_{off}	-	35	60	
Power Supply Current	V_{INA}=V_{INB}=3V	I_{CC}	-	2.5	4	mA
	V_{INA}=V_{INB}=0V		-	0.6	0.8	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 18V.

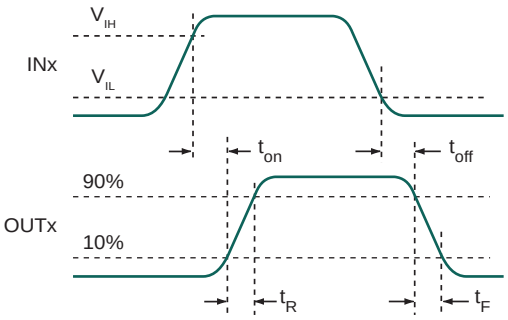
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	-	V_{IH}	2.4	-	V
Input Voltage, Low	-	V_{IL}	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	±1	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	12	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	8	
Latch-Up Protection	With Reverse Current	I	>500	-	mA
Rise Time	V_{CC}=18V, C_{LOAD}=1000pF	t_R	-	30	ns
Fall Time	V_{CC}=18V, C_{LOAD}=1000pF	t_F	-	30	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=1000pF	t_{on}	-	70	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=1000pF	t_{off}	-	70	
Power Supply Current	V_{INA}=V_{INB}=3V	I_{CC}	-	6	mA
	V_{INA}=V_{INB}=0V		-	1	

1.7 Thermal Characteristics

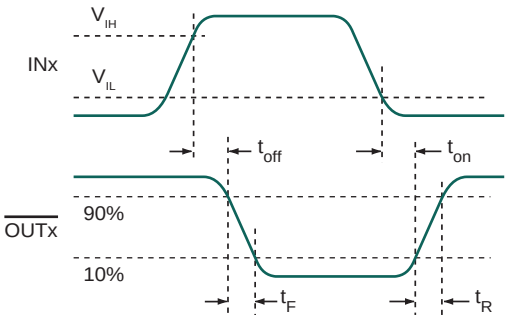
Package	Parameter	Symbol	Rating	Units
8-Pin SOIC	Thermal Resistance, Junction-to-Ambient	θ_{JA}	120	°C/W
8-Pin DFN	Thermal Resistance, Junction-to-Ambient	θ_{JA}	68	°C/W

2 IX4426-27-28 Performance

2.1 Timing Diagrams

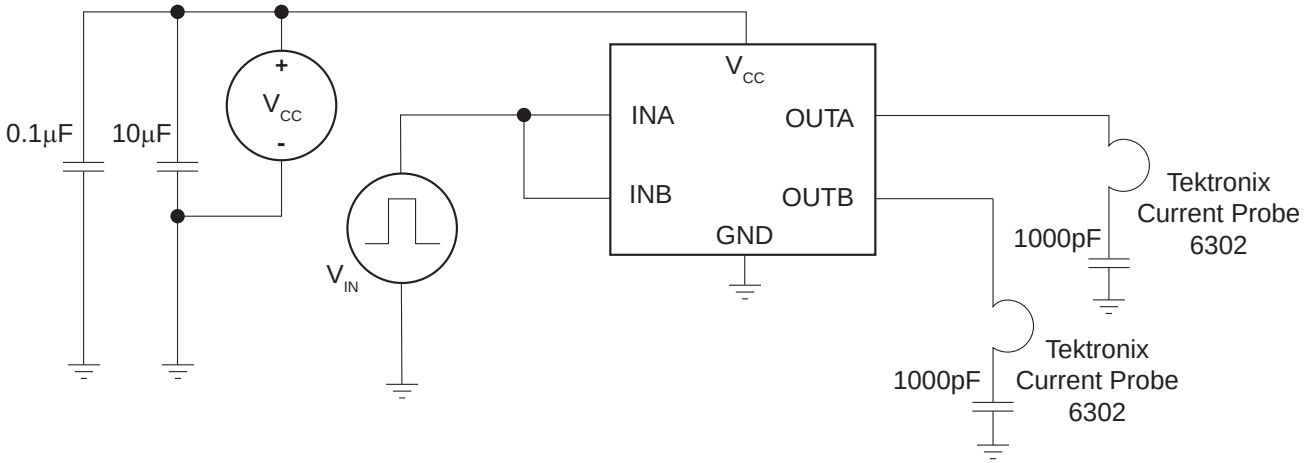


Non-Inverting Driver Waveforms



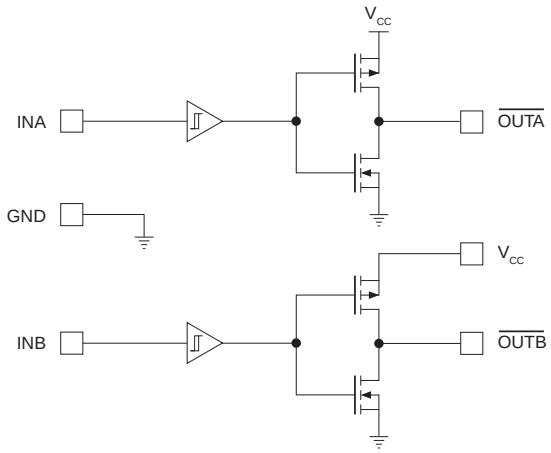
Inverting Driver Waveforms

2.2 Characteristics Test Diagram



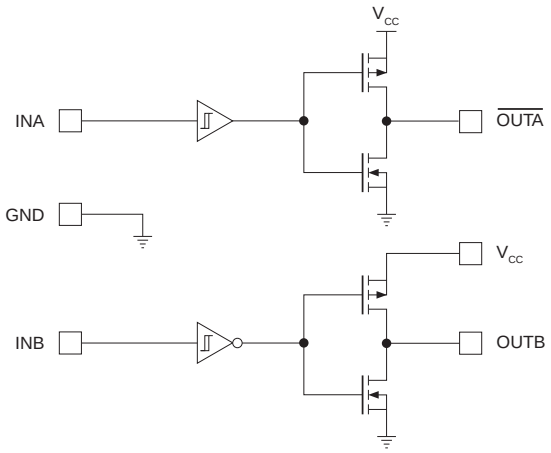
3 Block Diagrams & Truth Tables

3.1 IX4426



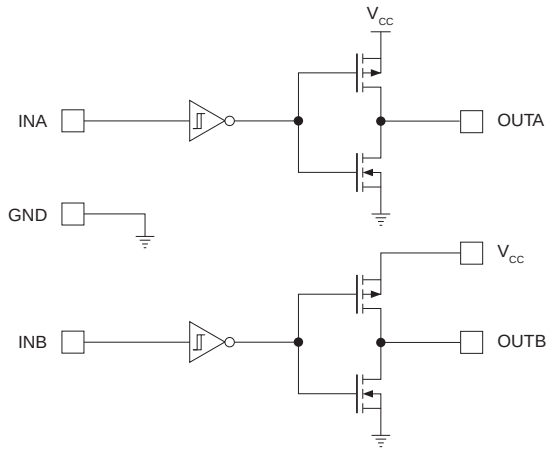
IN_X	$\overline{OUT}_X$
0	1
1	0

3.2 IX4428



INA	$\overline{OUTA}$
0	1
1	0
INB	**OUTB**
0	0
1	1

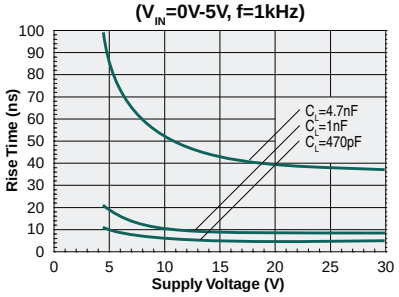
3.3 IX4427



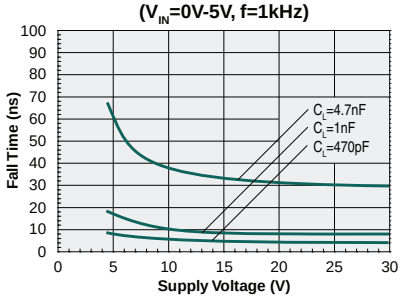
IN_X	OUT_X
0	0
1	1

4 Performance Data

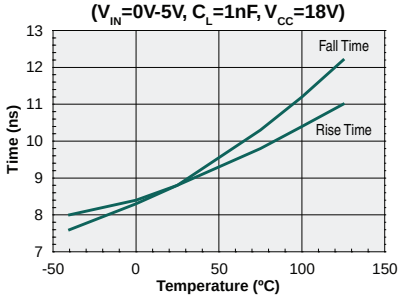
Rise Time vs. Supply Voltage (V_{IN}=0V-5V, f=1kHz)



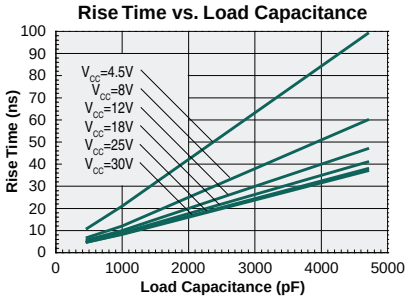
Fall Time vs. Supply Voltage (V_{IN}=0V-5V, f=1kHz)



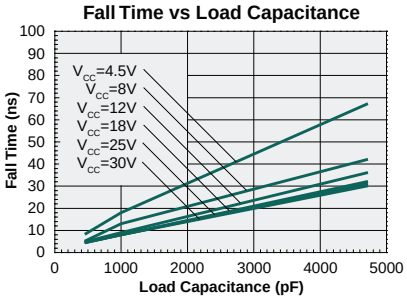
Rise Time & Fall Time vs. Temperature (V_{IN}=0V-5V, C_L=1nF, V_{CC}=18V)



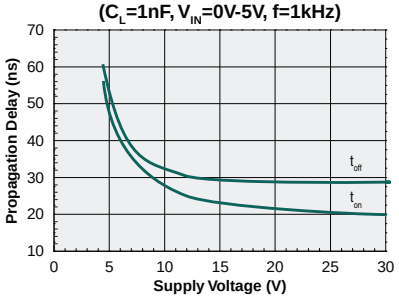
Rise Time vs. Load Capacitance



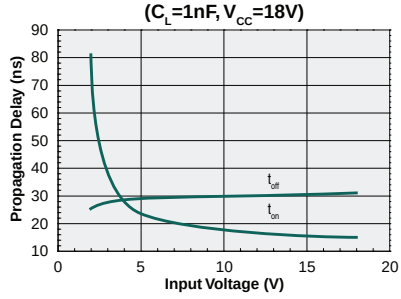
Fall Time vs Load Capacitance



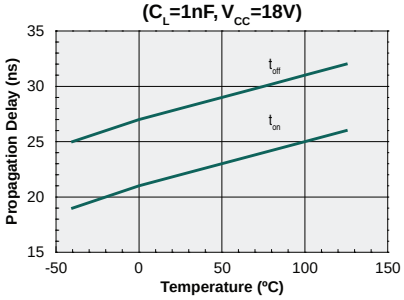
Propagation Delay vs. Supply Voltage (C_L=1nF, V_{IN}=0V-5V, f=1kHz)



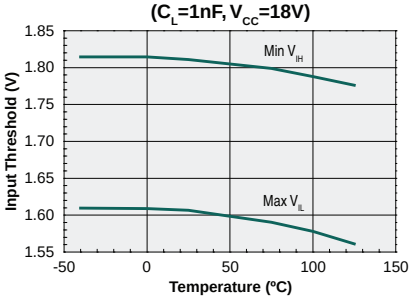
Propagation Delay vs. Input Voltage (C_L=1nF, V_{CC}=18V)



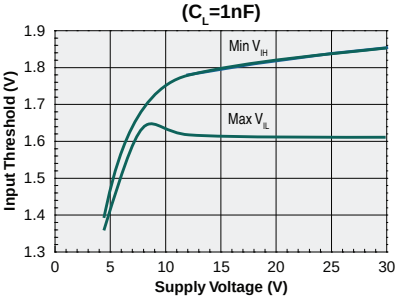
Propagation Delay vs. Temperature (C_L=1nF, V_{CC}=18V)



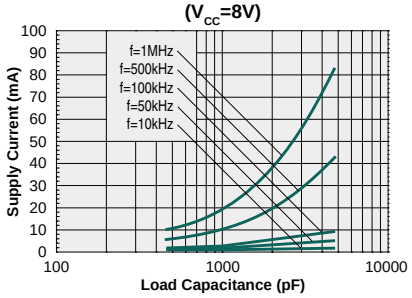
Input Threshold vs. Temperature (C_L=1nF, V_{CC}=18V)



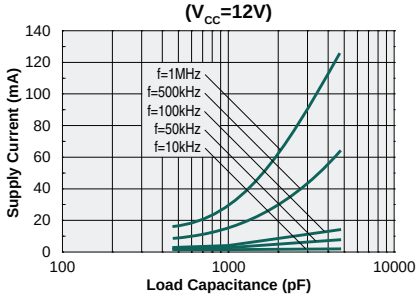
Input Threshold vs. Supply Voltage (C_L=1nF)



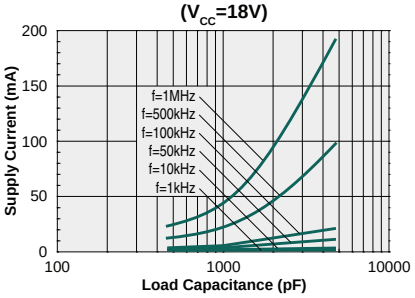
Supply Current vs. Load Capacitance A&B Outputs Active (V_{CC}=8V)



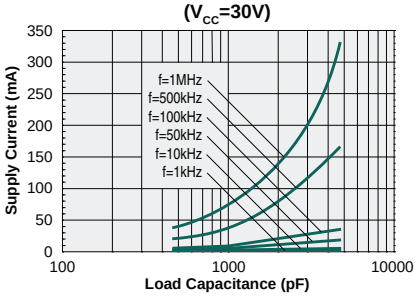
Supply Current vs. Load Capacitance A&B Outputs Active (V_{CC}=12V)



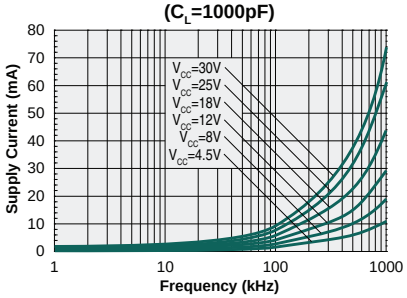
Supply Current vs. Load Capacitance A&B Outputs Active (V_{CC}=18V)



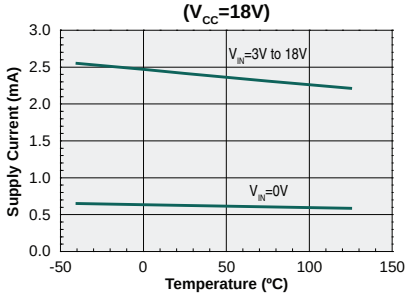
Supply Current vs. Load Capacitance A&B Outputs Active (V_{CC}=30V)



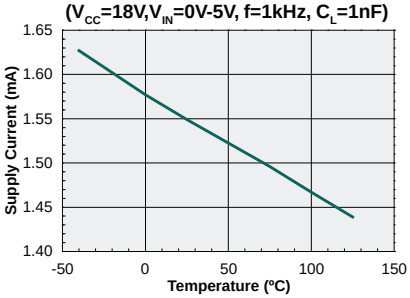
Supply Current vs. Frequency A&B Outputs Active (C_L=1000pF)



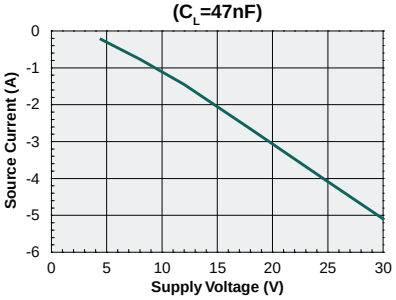
Quiescent Supply Current vs. Temperature (V_{CC}=18V)



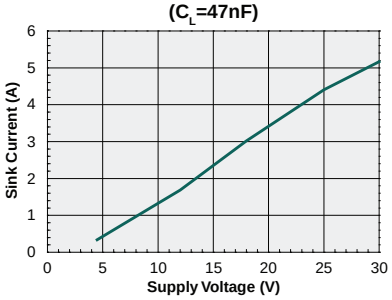
Dynamic Supply Current vs. Temperature Both Outputs Active (V_{CC}=18V,V_{IN}=0V-5V, f=1kHz, C_L=1nF)



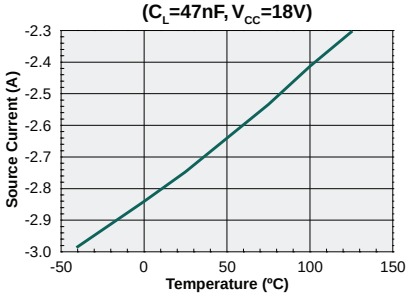
Output Source Current vs. Supply Voltage (C_L=47nF)



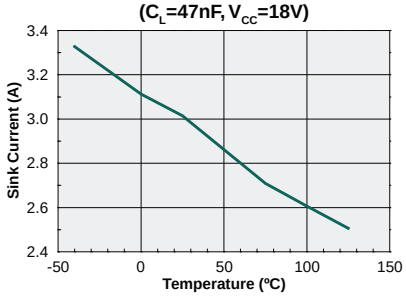
Output Sink Current vs. Supply Voltage (C_L=47nF)



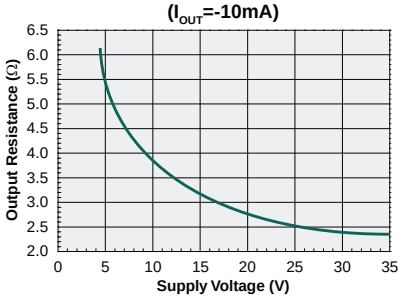
Output Source Current vs. Temperature (C_L=47nF, V_{CC}=18V)



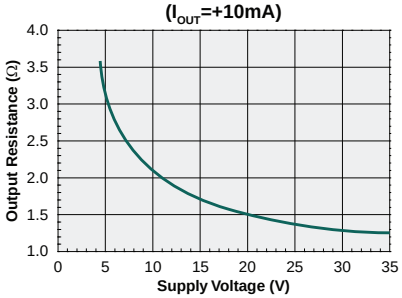
Output Sink Current vs. Temperature (C_L=47nF, V_{CC}=18V)



High-State Output Resistance vs. Supply Voltage (I_{OUT}=-10mA)



Low-State Output Resistance vs. Supply Voltage (I_{OUT}=+10mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4426 / IX4427 / IX4428 All Versions	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Reflow Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

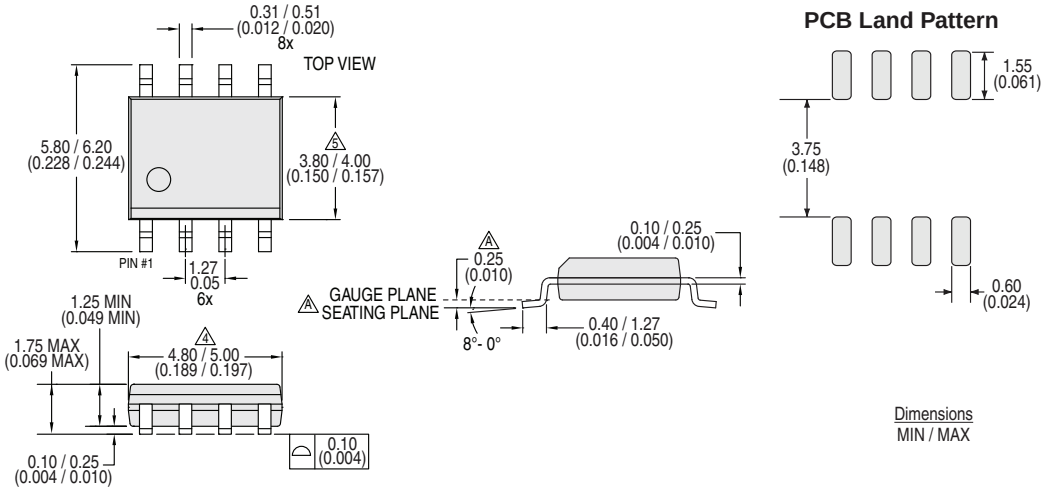
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX4426 / IX4427 / IX4428 All Versions	260°C	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

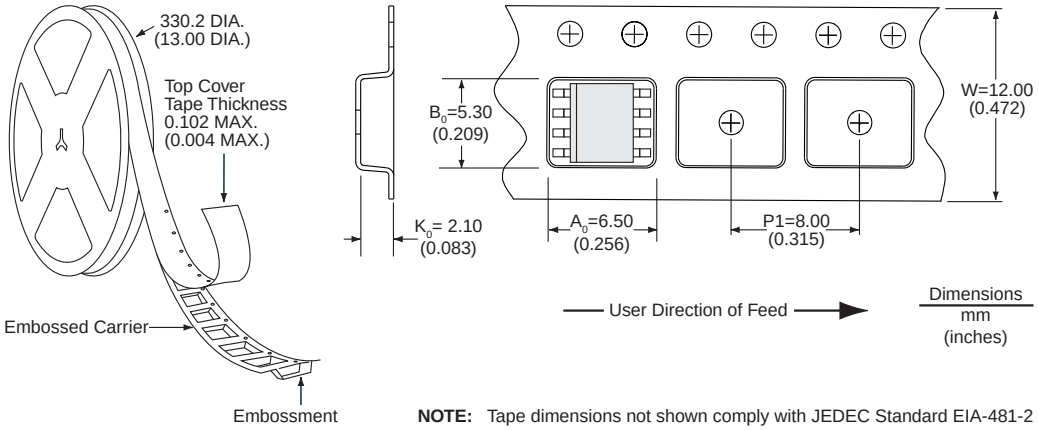
5.5 Mechanical Dimensions

5.5.1 "N" Package (8-Pin SOIC)



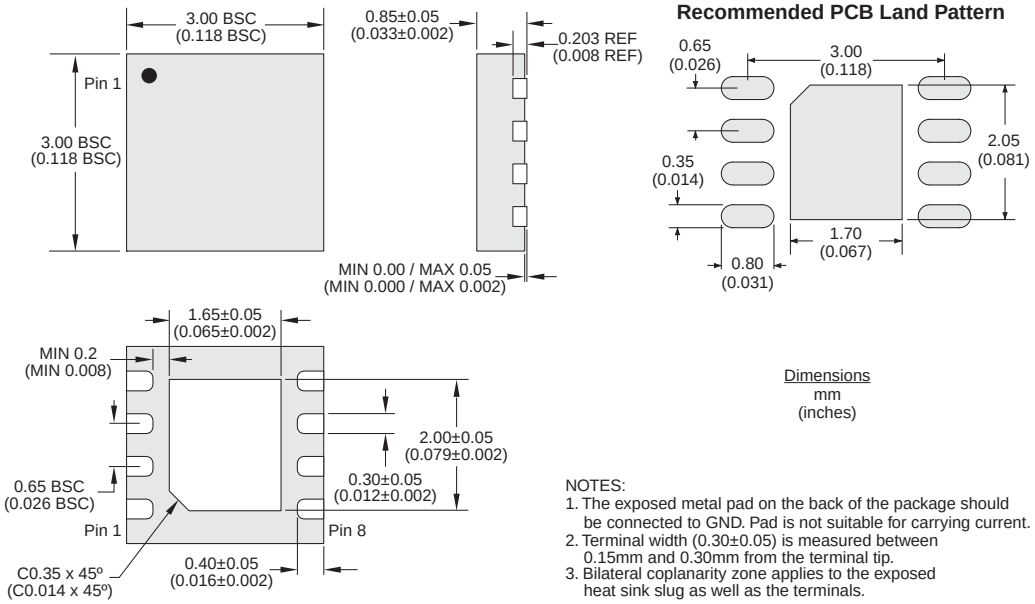
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

5.5.2 "N" Package Tape & Reel



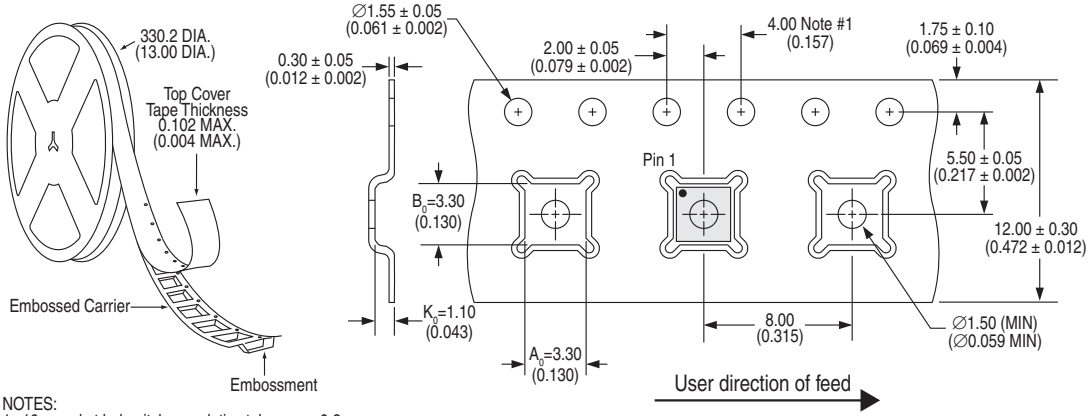
NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

5.5.3 "M" Package (8-Pin DFN)



NOTES:
1. The exposed metal pad on the back of the package should be connected to GND. Pad is not suitable for carrying current.
2. Terminal width (0.30±0.05) is measured between 0.15mm and 0.30mm from the terminal tip.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

5.5.4 "M" Package Tape & Reel



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm
3. Material black Advantek Polystyrene
4. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
5. K0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to the sprocket hole measured as true position of pocket, not pocket hole
7. Cover tape width 9.3±0.1mm

For additional information please visit our website at: www.ixysic.com

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