

**512Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with ECC**

**KEY FEATURES**

- High-speed access time: 8ns, 10ns, 20ns
- Single power supply
  - 1.65V-2.2V V<sub>DD</sub> (IS61WV51216EEALL)
  - 2.4V-3.6V V<sub>DD</sub> (IS61/64WV51216EEBLL)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
  - ERR1 pin indicates 1-bit error detection and correction.
  - ERR2 pin indicates 2-bit error detection
- Package Available:
  - 44-pin TSOP (Type II)
  - 48-pin TSOP (Type I)
  - 48-ball mini BGA (6mm x 8mm)
  - 54 pin TSOP (Type II)
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

**DESCRIPTION**

The ISSI IS61/64WV51216EEALL/BLL are high-speed, low power, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology and implemented ECC function to improve reliability.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yield high-performance and highly reliable devices.

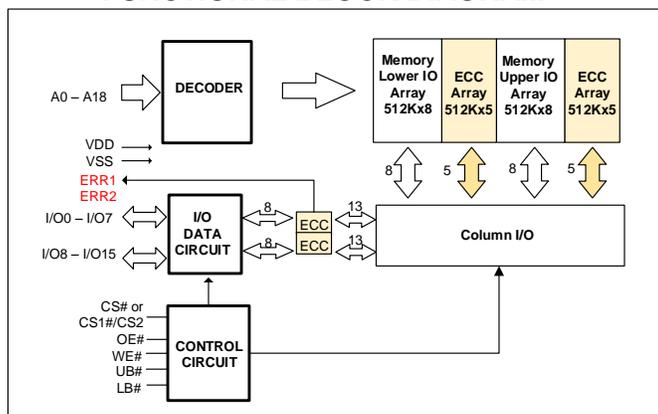
When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The devices are packaged in the JEDEC standard 44-pin TSOP (TYPE II), 48-pin mini BGA (6mm x 8mm), 48-pin TSOP (TYPE I), and 54-pin TSOP (TYPE II)

**FUNCTIONAL BLOCK DIAGRAM**



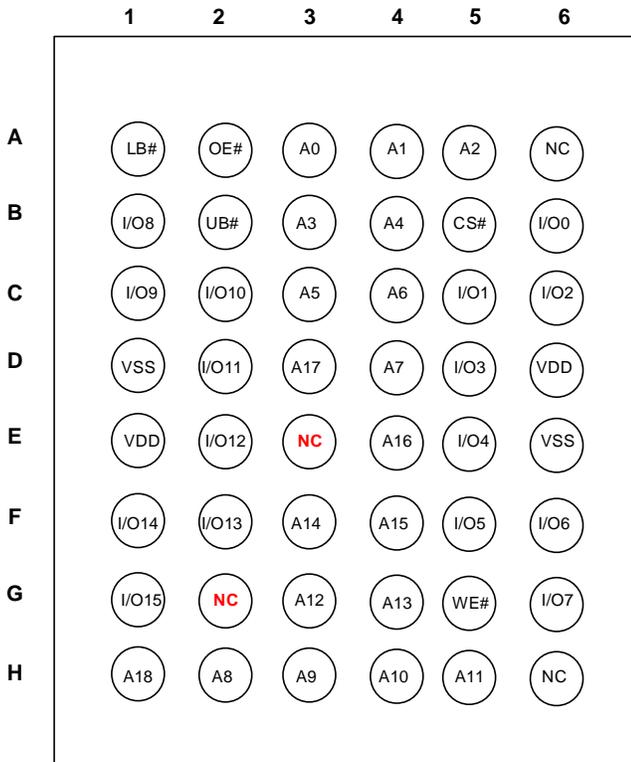
Copyright © 2019 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

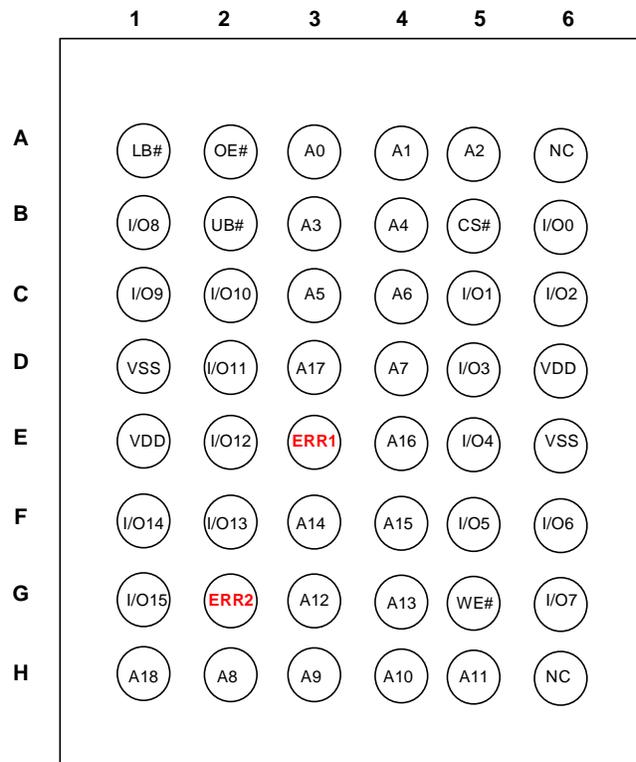
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATIONS**

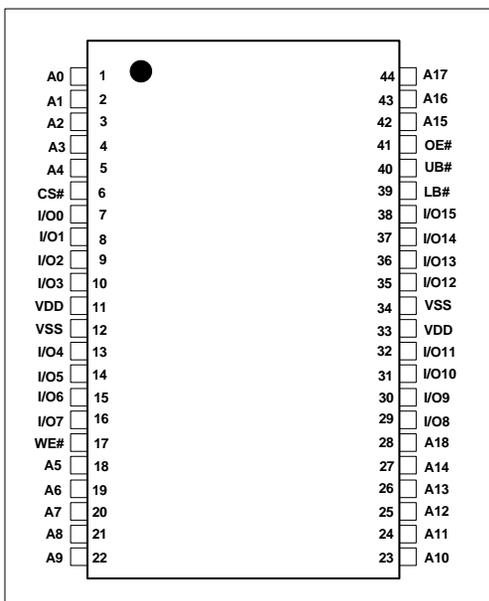
**48-Pin mini BGA(6mm x 8mm)**



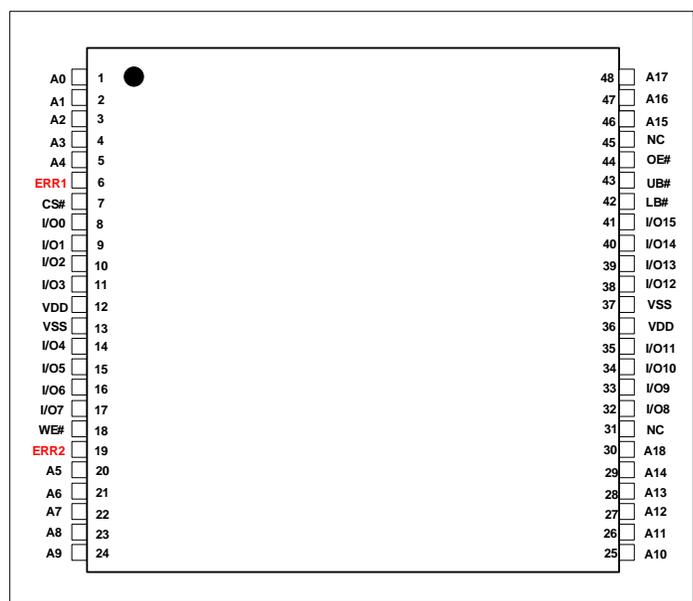
**48-Pin mini BGA (6mm x 8mm), ERR1/2**



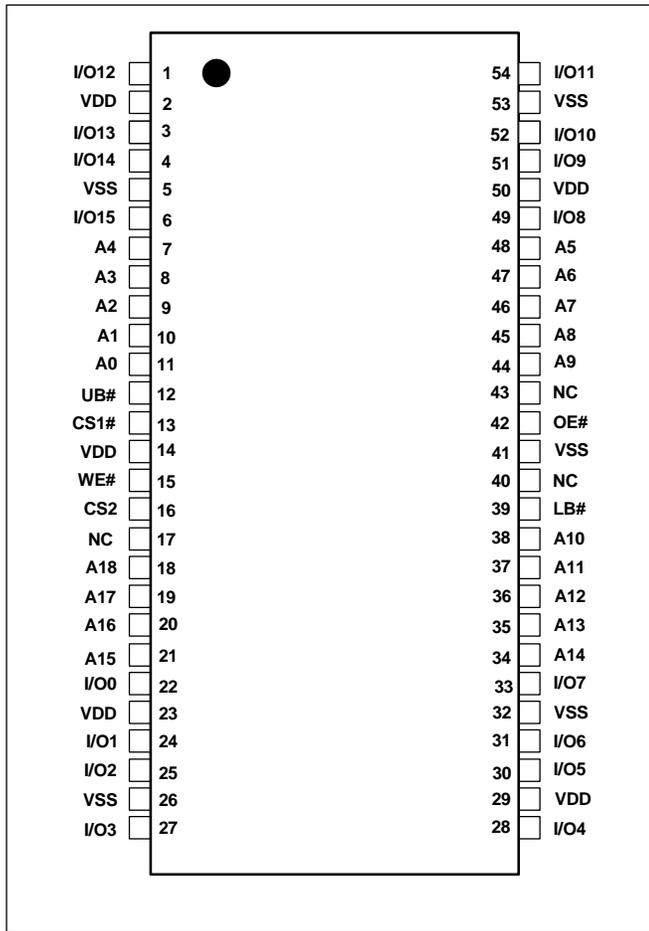
**44-Pin TSOP-II**



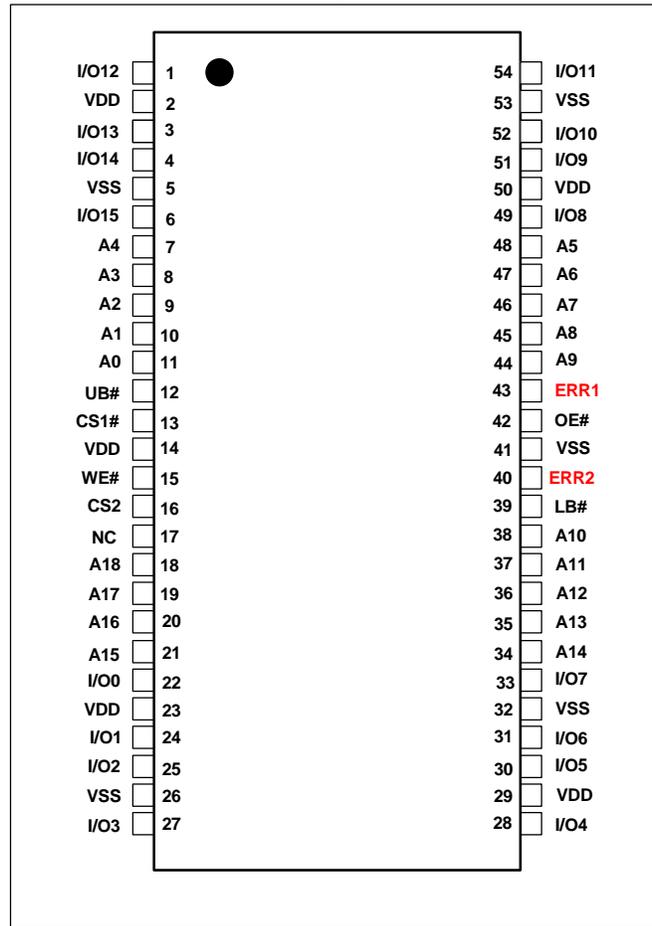
**48-Pin TSOP-I, ERR1/ERR2**



54-Pin TSOP-II



54-Pin TSOP-II, ERR1/ERR2



## PIN DESCRIPTIONS

|                 |   |
|-----------------|---|
| A0-A18          | Address Inputs                              |
| I/O0-I/O15      | Data Inputs/Outputs                         |
| CS# or CS1#/CS2 | Chip Enable Input                           |
| OE#             | Output Enable Input                         |
| WE#             | Write Enable Input                          |
| LB#             | Lower-byte Control (I/O0-I/O7)              |
| UB#             | Upper-byte Control (I/O8-I/O15)             |
| ERR1            | 1-bit Error Detection and Correction Signal |
| ERR2            | 2-bit ERR Detection Signal                  |
| NC              | No Connection                               |
| VDD             | Power                                       |
| VSS             | Ground                                      |

## FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

### STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

### WRITE MODE

Write operation issues with Chip selected (CS#) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

### READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

### ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct 1-bit error per byte or detect multi-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates multi-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

### ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

| ERR1   | ERR2   | DQ pin     | Status                  | Remark  |
|--------|--------|------------|-------------------------|---|
| 0      | 0      | Valid Q    | No Error                |   |
| 1      | 0      | Valid Q    | 1-Bit Error only        | 1-bit error per byte detected and corrected   |
| 0      | 1      | In-Valid Q | Multi-Bit Error only    | No 1-bit error. Multi-bit error per byte detected (out of 2 bytes)                            |
| 1      | 1      | In-Valid Q | 1-bit & Multi-bit error | 1-bit error detected and corrected at one byte, and multi-bit error detected at another byte. |
| High-Z | High-Z | Valid D    | Non-Read                | Write operation or Output Disabled  |

**TRUTH TABLE**

| Mode            | CS# | WE# | OE# | LB# | UB# | I/O0-I/O7 | I/O8-I/O15 | VDD Current                         |
|-----------------|-----|-----|-----|-----|-----|-----------|------------|-------------------------------------|
| Not Selected    | H   | X   | X   | X   | X   | High-Z    | High-Z     | I <sub>SB1</sub> , I <sub>SB2</sub> |
| Output Disabled | L   | H   | H   | L   | X   | High-Z    | High-Z     | ICC, ICC1                           |
|                 | L   | X   | X   | H   | H   | High-Z    | High-Z     |                                     |
| Read            | L   | H   | L   | L   | H   | DOUT      | High-Z     | ICC, ICC1                           |
|                 | L   | H   | L   | H   | L   | High-Z    | DOUT       |                                     |
|                 | L   | H   | L   | L   | L   | DOUT      | DOUT       |                                     |
| Write           | L   | L   | X   | L   | H   | DIN       | High-Z     | ICC, ICC1                           |
|                 | L   | L   | X   | H   | L   | High-Z    | DIN        |                                     |
|                 | L   | L   | X   | L   | L   | DIN       | DIN        |                                     |

**Note:**

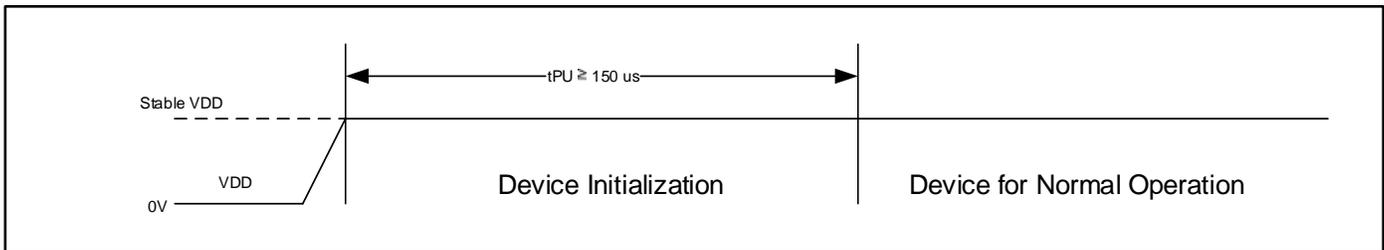
1. CS# = H means CS1#=HIGH, and CS2= LOW in Dual Chip Select Device.

**POWER UP INITIALIZATION**

The device includes on-chip voltage sensor used to launch POWER-UP initialization process.

When VDD reaches stable level, the device requires 150us of t<sub>PU</sub> (Power-Up Time) to complete its self-initialization process.

When initialization is complete, the device is ready for normal operation.



## ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Parameter                            | Value                          | Unit |
|-------------------|--------------------------------------|--------------------------------|------|
| V <sub>term</sub> | Terminal Voltage with Respect to VSS | -0.5 to V <sub>DD</sub> + 0.5V | V    |
| V <sub>DD</sub>   | V <sub>DD</sub> Related to VSS       | -0.3 to 4.0                    | V    |
| t <sub>Stg</sub>  | Storage Temperature                  | -65 to +150                    | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.0                            | W    |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### PIN CAPACITANCE <sup>(1)</sup>

| Parameter                 | Symbol           | Test Condition  | Max | Units |
|---------------------------|------------------|---|-----|-------|
| Input capacitance         | C <sub>IN</sub>  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = V <sub>DD</sub> (typ) | 6   | pF    |
| DQ capacitance (IO0–IO15) | C <sub>I/O</sub> |   | 8   | pF    |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

### OPERATING RANGE<sup>(1)</sup>

| Range           | Ambient Temperature | IS61WV51216EEALL<br>VDD (20ns) | IS61WV51216EEBLL<br>VDD (8, 10ns) | IS64WV51216EEBLL<br>VDD (10ns) |
|-----------------|---------------------|--------------------------------|-----------------------------------|--------------------------------|
| Industrial      | -40°C to +85°C      | 1.65V – 2.2V                   | 2.4V – 3.6V                       | –                              |
| Automotive (A3) | -40°C to +125°C     | –                              | –                                 | 2.4V – 3.6V                    |

Note:

1. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>DD</sub>(min) and 200 μs wait time after V<sub>DD</sub> stabilization.

### THERMAL CHARACTERISTICS <sup>(1)</sup>

| Parameter  | Symbol           | Rating | Units |
|--|------------------|--------|-------|
| Thermal resistance from junction to ambient (airflow = 1m/s) | R <sub>θJA</sub> | TBD    | °C/W  |
| Thermal resistance from junction to pins                     | R <sub>θJB</sub> | TBD    | °C/W  |
| Thermal resistance from junction to case                     | R <sub>θJC</sub> | TBD    | °C/W  |

Note:

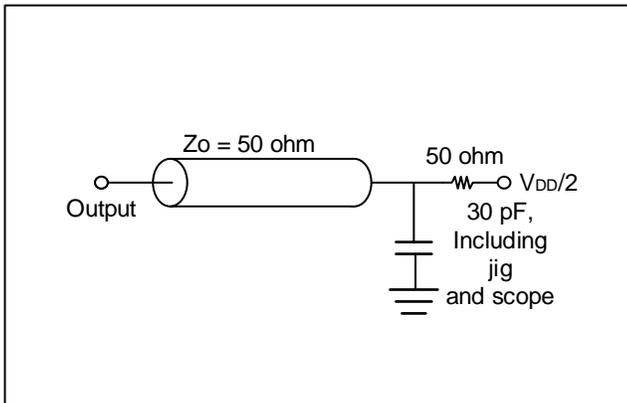
1. These parameters are guaranteed by design and tested by a sample basis only.

**AC TEST CONDITIONS (OVER THE OPERATING RANGE)**

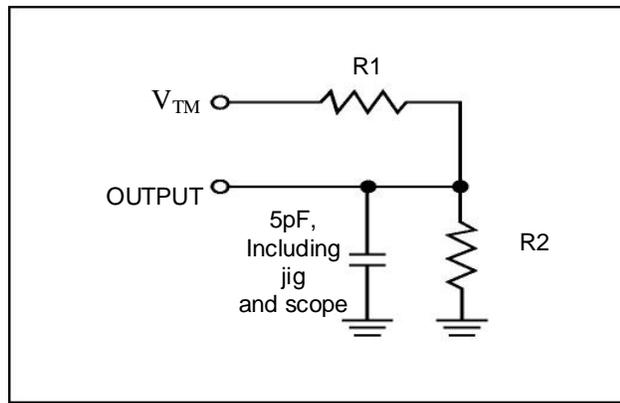
| Parameter                     | Unit<br>(1.65V~2.2V)    | Unit<br>(2.4V~3.6V)  |
|-------------------------------|-------------------------|----------------------|
| Input Pulse Level             | 0V to $V_{DD}$          | 0V to $V_{DD}$       |
| Input Rise and Fall Time      | 1.5 ns                  | 1.5 ns               |
| Output Timing Reference Level | $\frac{1}{2} V_{DD}$    | $\frac{1}{2} V_{DD}$ |
| R1 (ohm)                      | 13500                   | 319                  |
| R2 (ohm)                      | 10800                   | 353                  |
| $V_{TM}$ (V)                  | 1.8V                    | 3.3V                 |
| Output Load Conditions        | Refer to Figure 1 and 2 |                      |

**AC TEST LOADS**

**FIGURE 1**



**FIGURE 2**



## DC ELECTRICAL CHARACTERISTICS

### DC ELECTRICAL CHARACTERISTICS (OVER THE OPERATING RANGE)

VDD = 1.65V – 2.2V

| Symbol                           | Parameter           | Test Conditions   | Min. | Max.                  | Unit |
|----------------------------------|---------------------|---|------|-----------------------|------|
| V <sub>OH</sub>                  | Output HIGH Voltage | I <sub>OH</sub> = -0.1 mA                                 | 1.4  | —                     | V    |
| V <sub>OL</sub>                  | Output LOW Voltage  | I <sub>OL</sub> = 0.1 mA                                  | —    | 0.2                   | V    |
| V <sub>IH</sub> ( <sup>1</sup> ) | Input HIGH Voltage  |   | 1.4  | V <sub>DD</sub> + 0.2 | V    |
| V <sub>IL</sub> ( <sup>1</sup> ) | Input LOW Voltage   |   | -0.2 | 0.4                   | V    |
| I <sub>LI</sub>                  | Input Leakage       | GND < V <sub>IN</sub> < V <sub>DD</sub>                   | -1   | 1                     | μA   |
| I <sub>LO</sub>                  | Output Leakage      | GND < V <sub>IN</sub> < V <sub>DD</sub> , Output Disabled | -1   | 1                     | μA   |

Notes:

- V<sub>ILL</sub>(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
- V<sub>IHH</sub>(max) = V<sub>DD</sub> + 1.0V AC (pulse width < 10ns). Not 100% tested.

### DC ELECTRICAL CHARACTERISTICS (OVER THE OPERATING RANGE)

VDD = 2.4V – 3.6V

| Symbol                           | Parameter           | Test Conditions   | Min.  | Max. | Unit                  |   |
|----------------------------------|---------------------|---|---|------|-----------------------|---|
| V <sub>OH</sub>                  | Output HIGH Voltage | 2.4V ~ 2.7V   | V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA | 2.0  | —                     | V |
|                                  |                     | 2.7V ~ 3.6V   | V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA | 2.2  |                       |   |
| V <sub>OL</sub>                  | Output LOW Voltage  | 2.4V ~ 2.7V   | V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.0 mA  | —    | 0.4                   | V |
|                                  |                     | 2.7V ~ 3.6V   | V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA  | —    | 0.4                   |   |
| V <sub>IH</sub> ( <sup>1</sup> ) | Input HIGH Voltage  | 2.4V ~ 2.7V   |   | 2.0  | V <sub>DD</sub> + 0.3 | V |
|                                  |                     | 2.7V ~ 3.6V   |   | 2.0  |                       |   |
| V <sub>IL</sub> ( <sup>1</sup> ) | Input LOW Voltage   | 2.4V ~ 2.7V   |   | -0.3 | 0.6                   | V |
|                                  |                     | 2.7V ~ 3.6V   |   | -0.3 | 0.8                   |   |
| I <sub>LI</sub>                  | Input Leakage       | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>                   | -2  | 2    | μA                    |   |
| I <sub>LO</sub>                  | Output Leakage      | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub> , Output Disabled | -2  | 2    | μA                    |   |

Note:

- V<sub>IL</sub>(min) = -0.3V DC ; V<sub>IL</sub>(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.  
V<sub>IH</sub>(max) = V<sub>DD</sub> + 0.3V DC ; V<sub>IH</sub>(max) = V<sub>DD</sub> + 2.0V AC (pulse width 2.0ns). Not 100% tested..

**POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)**

| Symbol | Parameter  | Test Conditions  | Grade               | -8<br>Max. | -10<br>Max. | -20<br>Max | Unit |
|--------|--|--|---------------------|------------|-------------|------------|------|
| ICC    | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = MAX, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>   | Com.                | 90         | 85          | 80         | mA   |
|        |  |  | Ind.                | 100        | 95          | 90         |      |
|        |  |  | Auto.               | -          | 135         | -          |      |
| ICC1   | Operating Supply Current                         | V <sub>DD</sub> = MAX,<br>I <sub>OUT</sub> = 0 mA, f = 0   | Com.                | 80         | 80          | 80         | mA   |
|        |  |  | Ind.                | 90         | 90          | 90         |      |
|        |  |  | Auto.               | -          | 110         | -          |      |
| ISB1   | TTL Standby Current (TTL Inputs)                 | V <sub>DD</sub> = MAX,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>CS# ≥ V <sub>IH</sub> , f = 0                      | Com.                | 40         | 40          | 40         | mA   |
|        |  |  | Ind.                | 50         | 50          | 50         |      |
|        |  |  | Auto.               | -          | 60          | -          |      |
| ISB2   | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = MAX,<br>CS# ≥ V <sub>DD</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0 | Com.                | 30         | 30          | 30         | mA   |
|        |  |  | Ind.                | 40         | 40          | 40         |      |
|        |  |  | Auto.               | -          | 50          | -          |      |
|        |  |  | Typ. <sup>(2)</sup> | 10         |             |            |      |

Notes:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V<sub>DD</sub> = 3.0V/1.8V, T<sub>A</sub> = 25 °C and not 100% tested.

## AC CHARACTERISTICS (OVER OPERATING RANGE)

### READ CYCLE AC CHARACTERISTICS

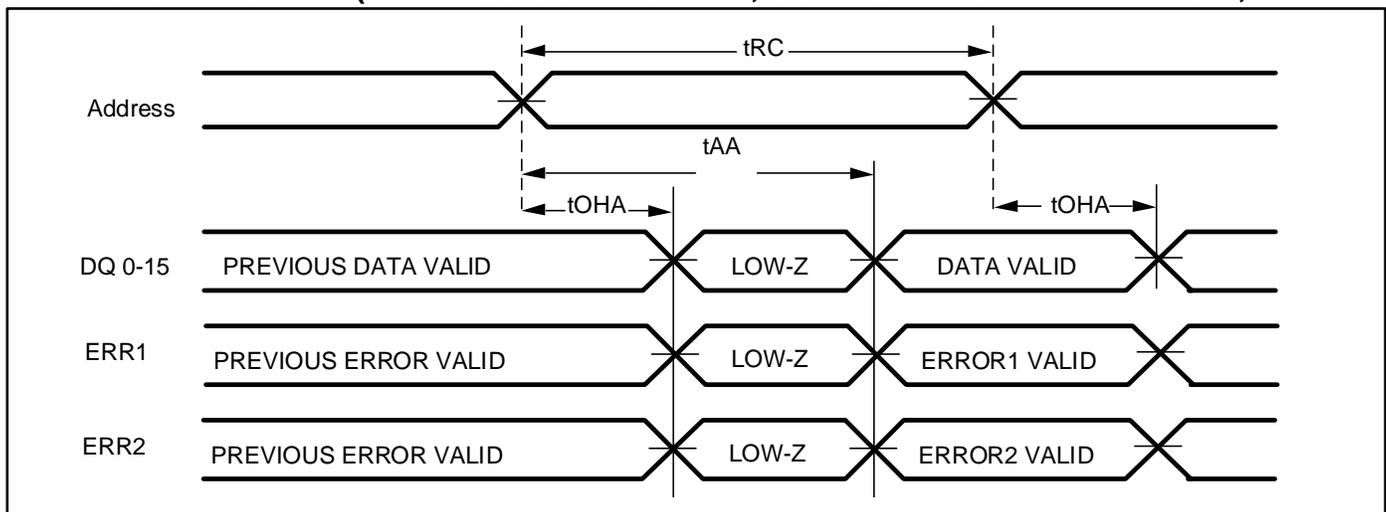
| Parameter                 | Symbol | -8 <sup>(1)</sup> |     | -10 <sup>(1)</sup> |     | -20 <sup>(1)</sup> |     | unit | notes |
|---------------------------|--------|-------------------|-----|--------------------|-----|--------------------|-----|------|-------|
|                           |        | Min               | Max | Min                | Max | Min                | Max |      |       |
| Read Cycle Time           | tRC    | 8                 | -   | 10                 | -   | 20                 | -   | ns   |       |
| Address Access Time       | tAA    | -                 | 8   | -                  | 10  | -                  | 20  | ns   |       |
| Output Hold Time          | tOHA   | 2.5               | -   | 2.5                | -   | 2.5                | -   | ns   |       |
| CS# Access Time           | tACE   | -                 | 8   | -                  | 10  | -                  | 20  | ns   |       |
| OE# Access Time           | tDOE   | -                 | 5.5 | -                  | 6   | -                  | 8   | ns   |       |
| OE# to High-Z Output      | tHZOE  | 0                 | 4   | 0                  | 5   | 0                  | 8   | ns   | 2     |
| OE# to Low-Z Output       | tLZOE  | 0                 | -   | 0                  | -   | 0                  | -   | ns   | 2     |
| CS# to High-Z Output      | tHZCE  | 0                 | 4   | 0                  | 5   | 0                  | 8   | ns   | 2     |
| CS# to Low-Z Output       | tLZCE  | 3                 | -   | 3                  | -   | 3                  | -   | ns   | 2     |
| UB#, LB# Access Time      | tBA    | -                 | 5.5 | -                  | 6   | -                  | 8   | ns   |       |
| UB#, LB# to High-Z Output | tHZB   | 0                 | 4   | 0                  | 5   | 0                  | 8   | ns   | 2     |
| UB#, LB# to Low-Z Output  | tLZB   | 0                 | -   | 0                  | -   | 0                  | -   | ns   | 2     |

Notes:

1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of  $V_{DD}/2$ , input pulse levels of 0V to  $V_{DD}$  and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

## AC WAVEFORMS

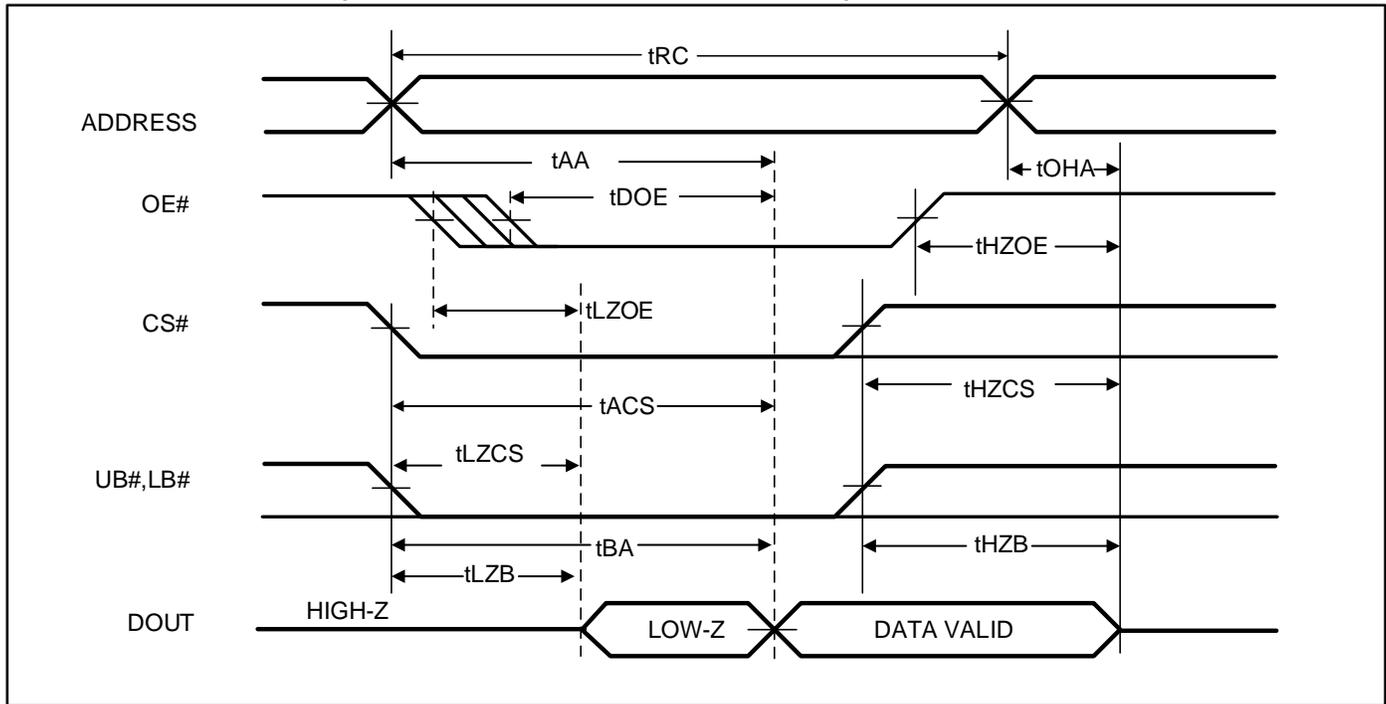
### READ CYCLE NO. 1<sup>(1,2)</sup> (ADDRESS CONTROLLED, CS# = OE# = UB# = LB# = LOW, WE# = HIGH)



Notes:

1. The device is continuously selected.
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

READ CYCLE NO. 2<sup>(1)</sup> (OE# CONTROLLED, WE# = HIGH)



Note:

1. Address is valid prior to or coincident with CS# LOW transition.

## WRITE CYCLE AC CHARACTERISTICS

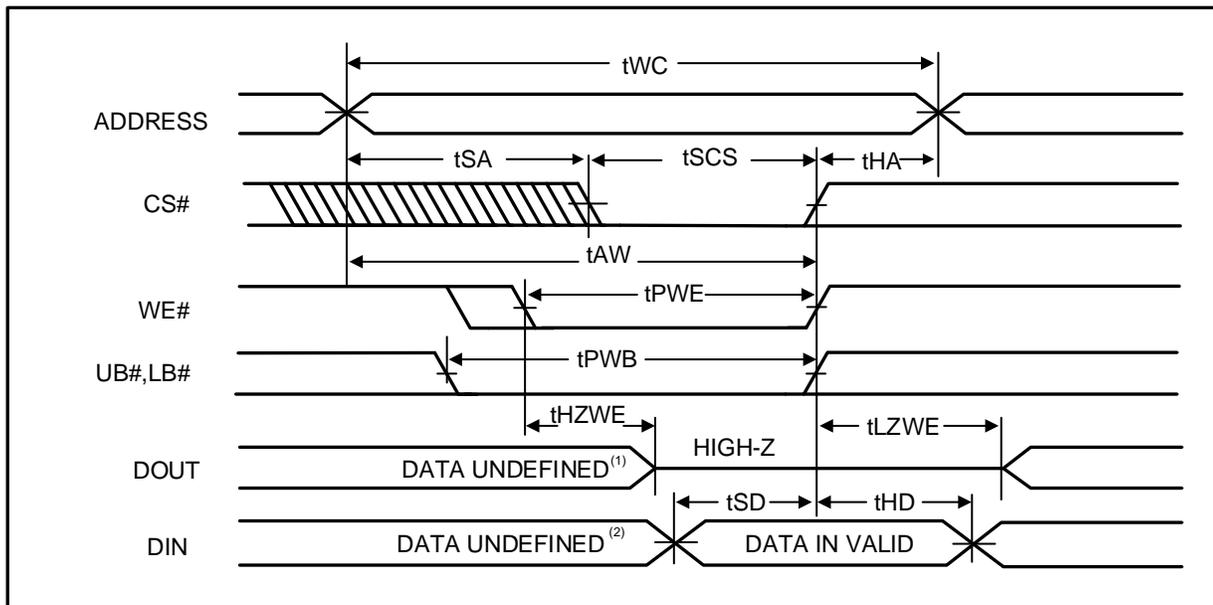
| Parameter                       | Symbol | -8 <sup>(1)</sup> |     | -10 <sup>(1)</sup> |     | -20 <sup>(1)</sup> |     | unit | notes |
|---------------------------------|--------|-------------------|-----|--------------------|-----|--------------------|-----|------|-------|
|                                 |        | Min               | Max | Min                | Max | Min                | Max |      |       |
| Write Cycle Time                | tWC    | 8                 | -   | 10                 | -   | 20                 | -   | ns   |       |
| CS# to Write End                | tSCS   | 6.5               | -   | 8                  | -   | 12                 | -   | ns   |       |
| Address Setup Time to Write End | tAW    | 6.5               | -   | 8                  | -   | 12                 | -   | ns   |       |
| UB#,LB# to Write End            | tPWB   | 6.5               | -   | 8                  | -   | 12                 | -   | ns   |       |
| Address Hold from Write End     | tHA    | 0                 | -   | 0                  | -   | 0                  | -   | ns   |       |
| Address Setup Time              | tSA    | 0                 | -   | 0                  | -   | 0                  | -   | ns   |       |
| WE# Pulse Width                 | tPWE1  | 6.5               | -   | 8                  | -   | 12                 | -   | ns   |       |
| WE# Pulse Width (OE# = LOW)     | tPWE2  | 8                 | -   | 10                 | -   | 17                 | -   | ns   | 2     |
| Data Setup to Write End         | tSD    | 5                 | -   | 6                  | -   | 9                  | -   | ns   |       |
| Data Hold from Write End        | tHD    | 0                 | -   | 0                  | -   | 0                  | -   | ns   |       |
| WE# LOW to High-Z Output        | tHZWE  | -                 | 3.5 | -                  | 4   | -                  | 9   | ns   |       |
| WE# HIGH to Low-Z Output        | tLZWE  | 2                 | -   | 2                  | -   | 3                  | -   | ns   |       |

Notes:

- 1 The internal write time is defined by the overlap of CS# = LOW, UB# or LB# = LOW, and WE# = LOW. All conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
- 2 tPWE > tHZWE + tSD when OE# is LOW.

## AC WAVEFORMS

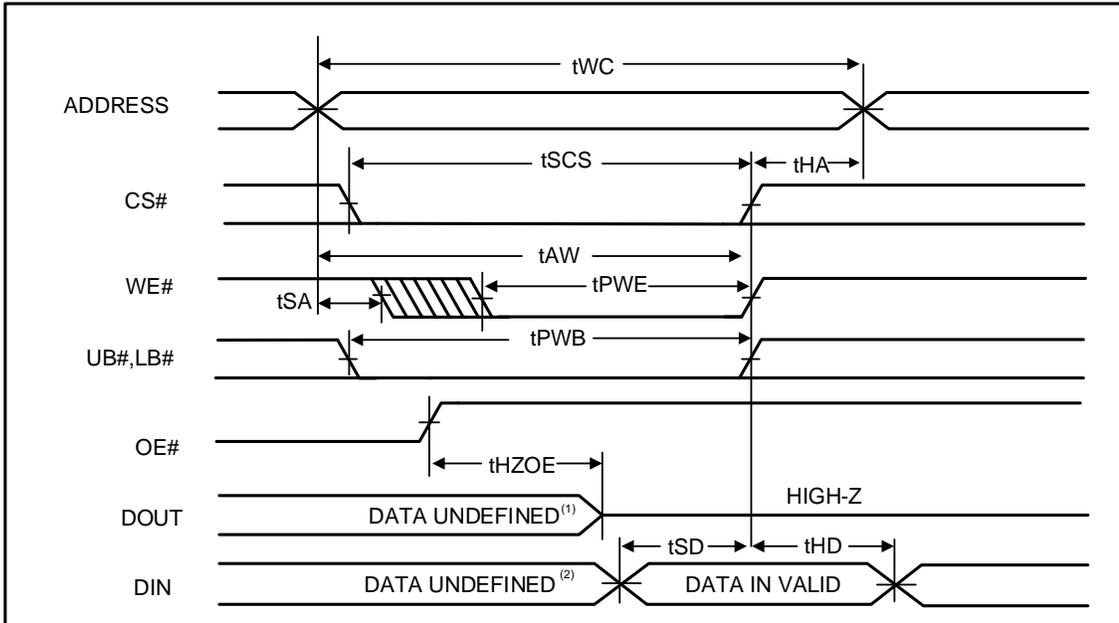
### WRITE CYCLE NO. 1 (CS# CONTROLLED, OE# = HIGH OR LOW)



Note:

- 1 tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle.

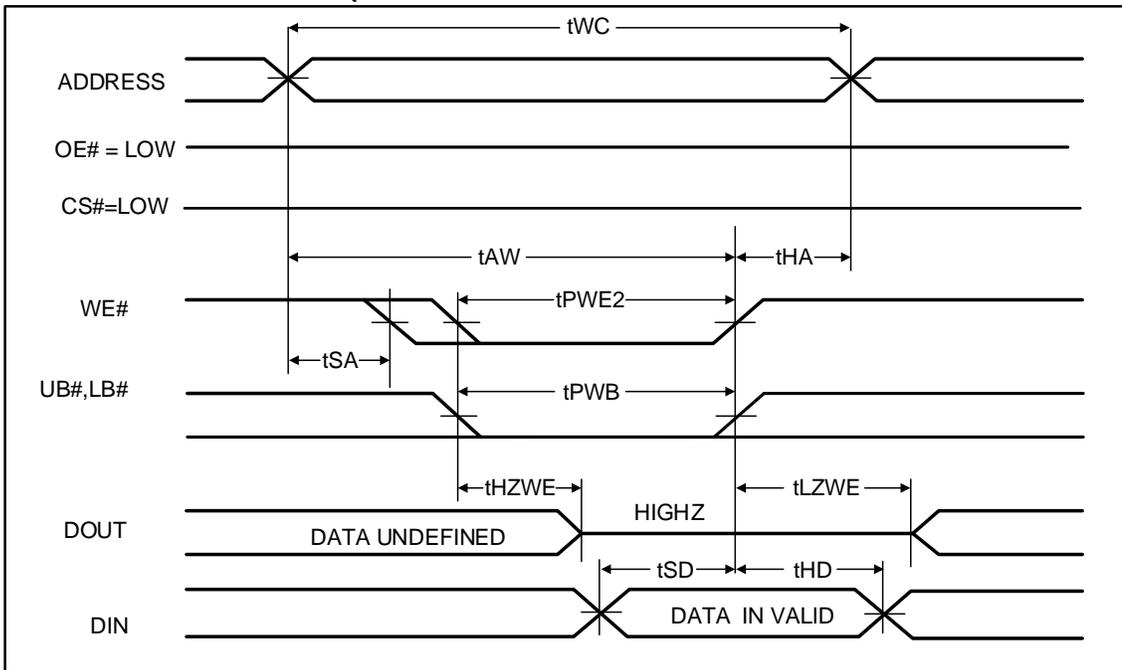
**WRITE CYCLE NO. 2<sup>(1,2)</sup> (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)**



Notes:

1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

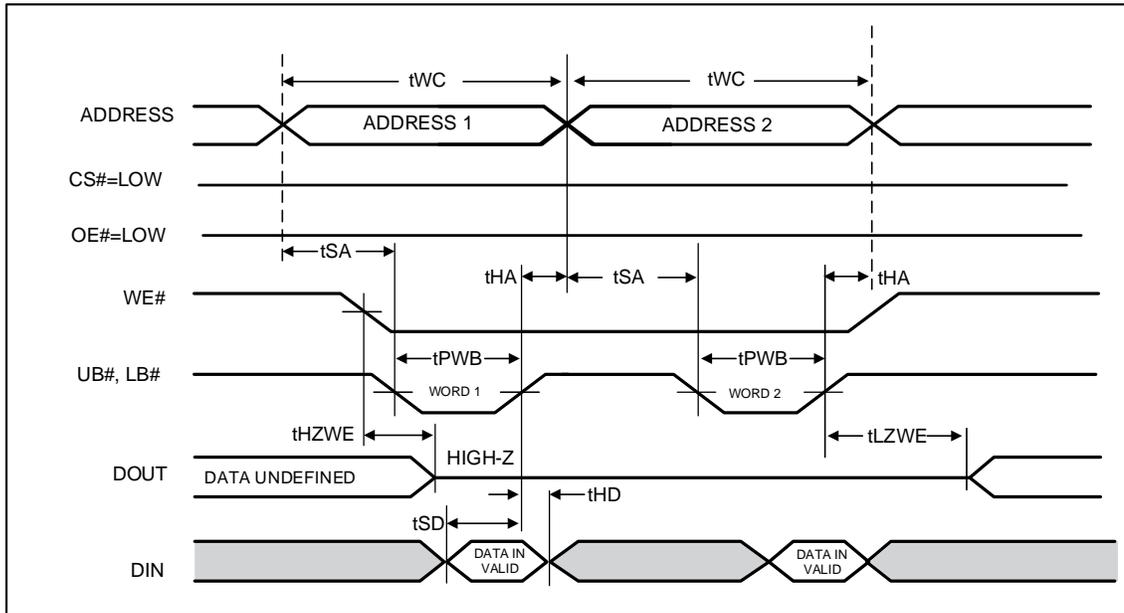
**WRITE CYCLE NO. 3<sup>(1)</sup> (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)**



Note:

3. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4<sup>(1, 2, 3)</sup> (UB# & LB# Controlled, CS# = OE# = LOW)



Notes:

- 1 If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
- 2 Due to the restriction of note1, OE# is recommended to be HIGH during write period.
- 3 WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

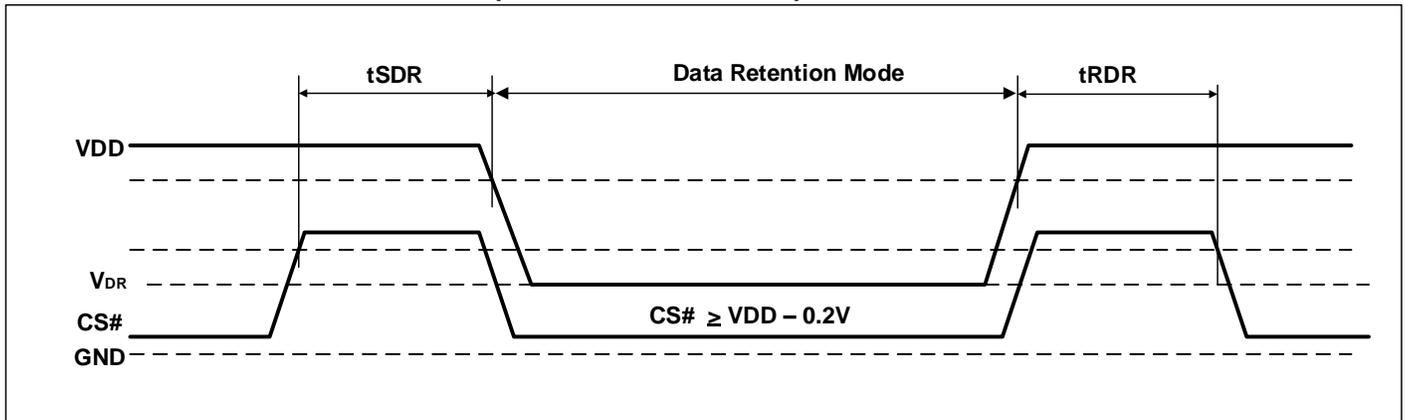
## DATA RETENTION CHARACTERISTICS

| Symbol           | Parameter                          | Test Condition   | OPTION                          | Min.            | Typ. <sup>(2)</sup> | Max. | Unit |
|------------------|------------------------------------|--|---------------------------------|-----------------|---------------------|------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform  | V <sub>DD</sub> = 2.4V to 3.6V  | 2.0             |                     | 3.6  | V    |
|                  |                                    |  | V <sub>DD</sub> = 1.65V to 2.2V | 1.2             |                     | 3.6  |      |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = V <sub>DR</sub> (min),<br>CS# ≥ V <sub>DD</sub> - 0.2V | Com.                            | -               | 10                  | 30   | mA   |
|                  |                                    |  | Ind.                            | -               | -                   | 40   |      |
|                  |                                    |  | Auto                            | -               | -                   | 50   |      |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform  |                                 | 0               | -                   | -    | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform  |                                 | t <sub>RC</sub> | -                   | -    | ns   |

Note:

1. If CS# ≥ V<sub>DD</sub>-0.2V, all other inputs including UB# and LB# must meet this condition.
2. CS#=H means CS1#=HIGH, and CS2=LOW in Dual Chip Select Device
3. Typical values are measured at V<sub>DD</sub> = V<sub>DR</sub> (Min), T<sub>A</sub> = 25 °C and not 100% tested.

## DATA RETENTION WAVEFORM (CS# CONTROLLED)



## ORDERING INFORMATION

### Industrial Range: -40°C to +85°C, Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No.          | Package                                      |
|------------|-------------------------|--|
| 20         | IS61WV51216EEALL-20BLI  | mini BGA (6mm x 8mm), Lead-free              |
| 20         | IS61WV51216EEALL-20B2LI | mini BGA (6mm x 8mm), ERR1/2 Pins, Lead-free |
| 20         | IS61WV51216EEALL-20TLI  | 44 TSOP (Type II), Lead-free                 |
| 20         | IS61WV51216EEALL-20T2LI | 48 TSOP (Type I), ERR1/2 Pins, Lead-free     |

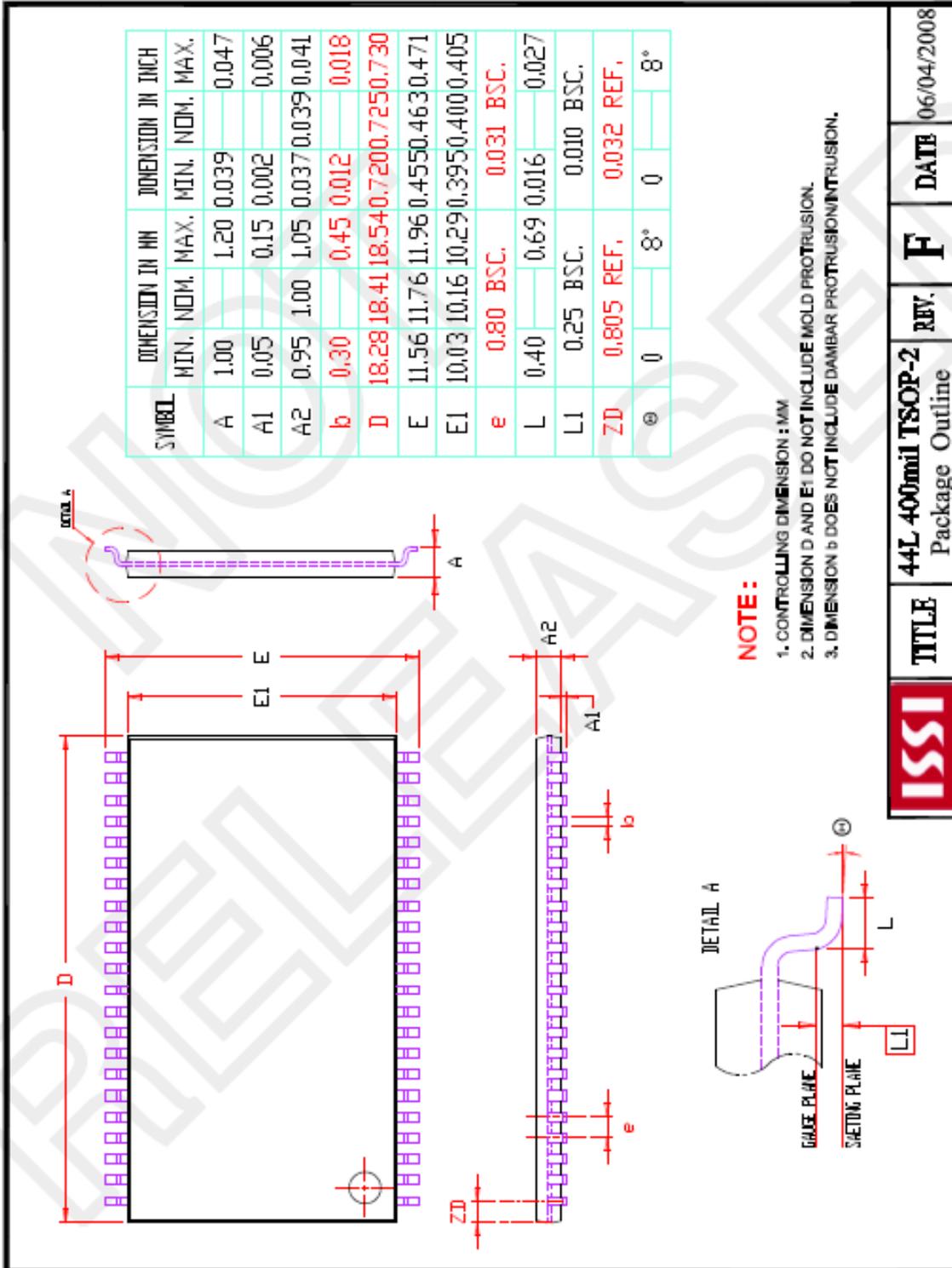
### Industrial Range: -40°C to +85°C, Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No.          | Package                                      |
|------------|-------------------------|--|
| 8          | IS61WV51216EEBLL-8BI    | mini BGA (6mm x 8mm)                         |
| 8          | IS61WV51216EEBLL-8BLI   | mini BGA (6mm x 8mm), Lead-free              |
| 8          | IS61WV51216EEBLL-8B2I   | mini BGA (6mm x 8mm), ERR1/2 Pins            |
| 8          | IS61WV51216EEBLL-8B2LI  | mini BGA (6mm x 8mm), ERR1/2 Pins, Lead-free |
| 8          | IS61WV51216EEBLL-8TLI   | 44 TSOP (Type II), Lead-free                 |
| 8          | IS61WV51216EEBLL-8T2LI  | 48 TSOP (Type I), ERR1/2 Pins, Lead-free     |
| 8          | IS61WV51216EEBLL-8T3LI  | 54 TSOP (Type II), Lead-free                 |
| 8          | IS61WV51216EEBLL-8T4LI  | 54 TSOP (Type II), ERR1/2 Pins, Lead-free    |
| 10         | IS61WV51216EEBLL-10BI   | mini BGA (6mm x 8mm)                         |
| 10         | IS61WV51216EEBLL-10BLI  | mini BGA (6mm x 8mm), Lead-free              |
| 10         | IS61WV51216EEBLL-10B2I  | mini BGA (6mm x 8mm), ERR1/2 Pins            |
| 10         | IS61WV51216EEBLL-10B2LI | mini BGA (6mm x 8mm), ERR1/2 Pins, Lead-free |
| 10         | IS61WV51216EEBLL-10TLI  | 44 TSOP (Type II), Lead-free                 |
| 10         | IS61WV51216EEBLL-10T2LI | 48 TSOP (Type I), ERR1/2 Pins, Lead-free     |
| 10         | IS61WV51216EEBLL-10T3LI | 54 TSOP (Type II), Lead-free                 |
| 10         | IS61WV51216EEBLL-10T4LI | 54 TSOP (Type II), ERR1/2 Pins, Lead-free    |

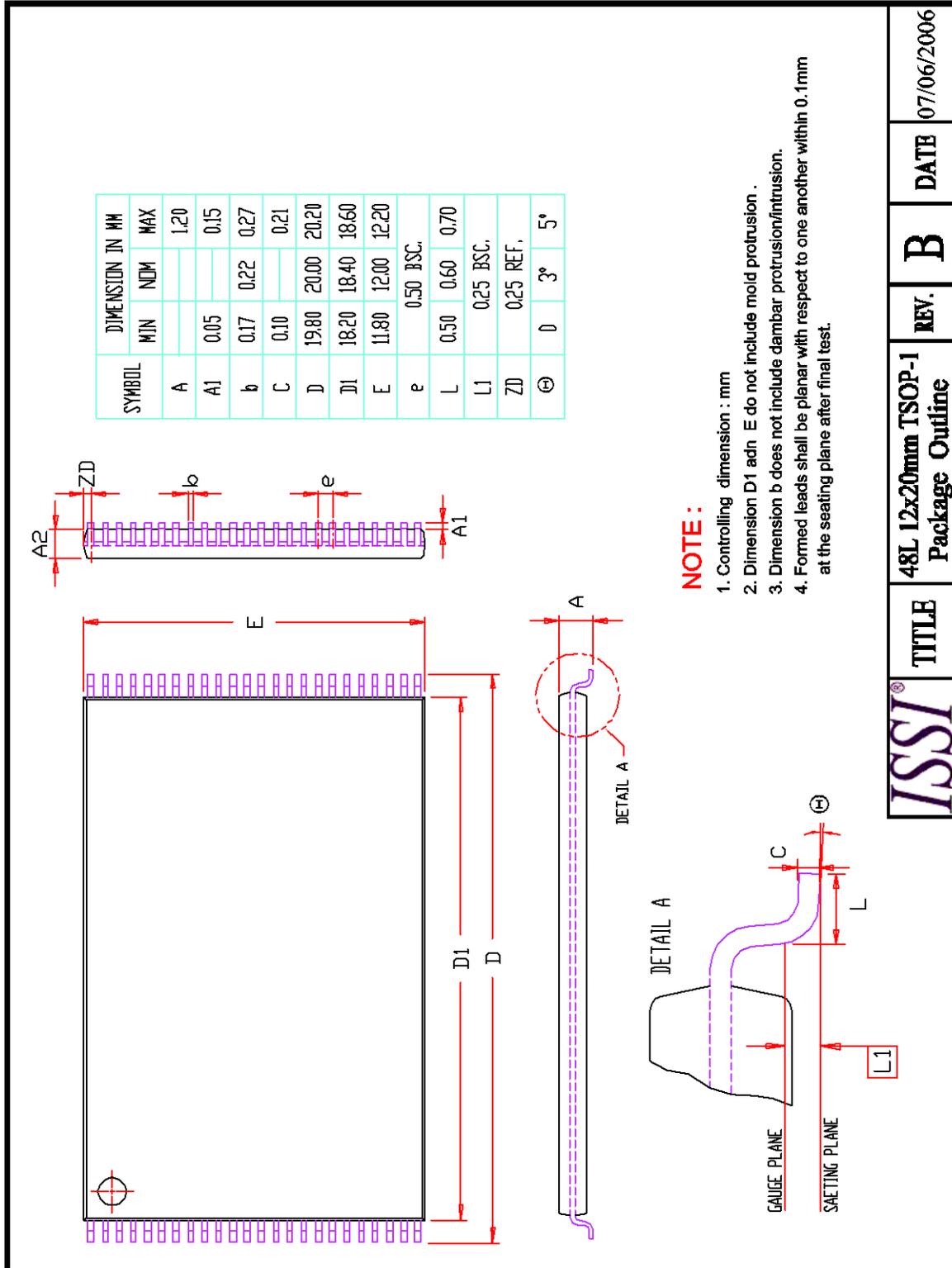
### Automotive Range (A3): -40°C to +125°C, Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No.            | Package   |
|------------|---------------------------|---|
| 10         | IS64WV51216EEBLL-10BA3    | mini BGA (6mm x 8mm)  |
| 10         | IS64WV51216EEBLL-10BLA3   | mini BGA (6mm x 8mm), Lead-free                             |
| 10         | IS64WV51216EEBLL-10B2A3   | mini BGA (6mm x 8mm), ERR1/ERR2 Pins                        |
| 10         | IS64WV51216EEBLL-10B2LA3  | mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free             |
| 10         | IS64WV51216EEBLL-10CTLA3  | 44 TSOP (Type II), Copper Leadframe, Lead-free              |
| 10         | IS64WV51216EEBLL-10CT2LA3 | 48 TSOP (Type I), Copper Leadframe, ERR1/2 Pins, Lead-free  |
| 10         | IS64WV51216EEBLL-10CT3LA3 | 54 TSOP (Type II), Copper Leadframe, Lead-free              |
| 10         | IS64WV51216EEBLL-10CT4LA3 | 54 TSOP (Type II), Copper Leadframe, ERR1/2 Pins, Lead-free |

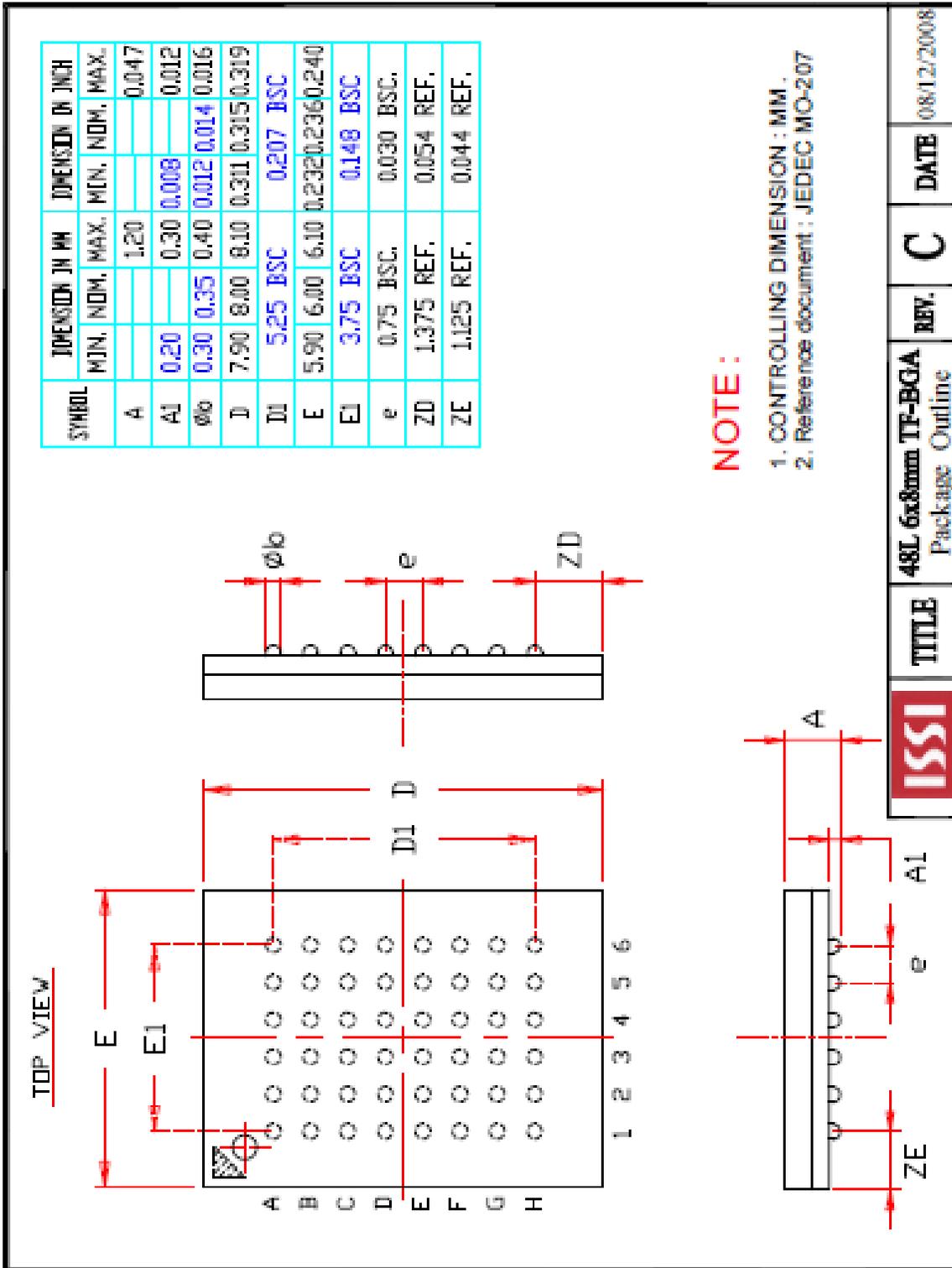
PACKAGE INFORMATION

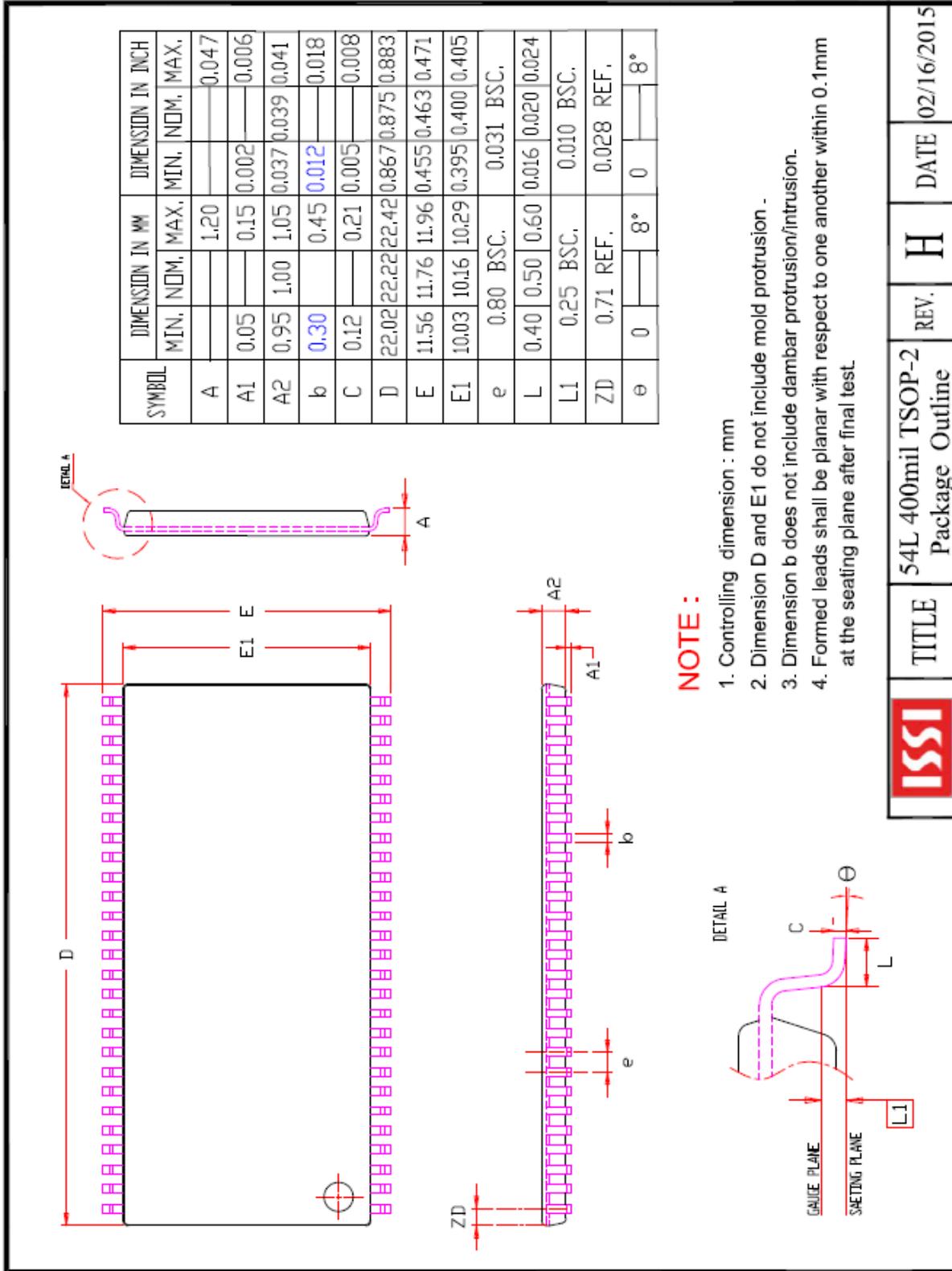


|             |                                      |             |             |
|-------------|--------------------------------------|-------------|-------------|
| <b>ISSI</b> | <b>TITLE</b>                         | <b>REV.</b> | <b>DATE</b> |
|             | 44L 400mil TSOP-2<br>Package Outline | F           | 06/04/2008  |



|       |                                    |      |            |
|-------|------------------------------------|------|------------|
| ISSI® | TITLE                              | REV. | DATE       |
|       | 48L 12x20mm TSOP-1 Package Outline | B    | 07/06/2006 |





|  |       |                                      |      |   |      |            |
|--|-------|--------------------------------------|------|---|------|------------|
|  | TITLE | 54L 400mil TSOP-2<br>Package Outline | REV. | H | DATE | 02/16/2015 |
|--|-------|--------------------------------------|------|---|------|------------|

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [SRAM](#) category:*

*Click to view products by [ISSI](#) manufacturer:*

Other Similar products are found below :

[CY6116A-35DMB](#) [CY7C1049GN-10VXI](#) [CY7C128A-45DMB](#) [GS8161Z36DD-200I](#) [GS88237CB-200I](#) [RMLV0408EGSB-4S2#AA0](#)  
[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)  
[CY7C1353S-100AXC](#) [AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#)  
[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [70V639S10BCG](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#)  
[IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#)  
[5962-8855206YA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-](#)  
[9161705MXA](#) [GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-8971202ZA](#) [5962-](#)  
[8872501LA](#) [5962-8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#) [5962-8751309VA](#)