

# IS31LT3948

## PFM MODE BOOST LED DRIVER WITH THE EXTERNAL NMOS

February 2015

### GENERAL DESCRIPTION

The IS31LT3948 is a PFM step-up DC-DC converter designed for driving the white LED arrays for large size LCD panel backlighting applications. It can deliver stable constant output current from a few milliamps up to 2A, programmed via an external resistor.

The IS31LT3948 utilizes a control scheme in which the output is automatically adjusted to the optimum output voltage for the system, maximizing the efficiency. Furthermore, the control scheme is inherently stable removing the need to provide additional loop compensation.

The device features external PWM dimming, which allows the flexible control of the back-lighting luminance.

The IS31LT3948 has a wide input voltage range from 5V to 100V (Note). An integrated OVP circuit protects the chip and the system even under no-load conditions.

The chip is assembled in SOP-8 package. It operates from 5V to 100V over two temperature ranges of -40°C to +85°C and -40°C to +125°C.

Note: The IS31LT3948 has an internal 5V shunt regulator connected to the VCC pin. A dropping resistor must be connected between the VCC pin and VIN to limit current flow. VIN voltages above 100V are allowed but care must be taken to ensure that the output voltage remains greater than VIN, and that the NMOS voltage rating is sufficiently large.

### FEATURES

- Wide input voltage range: 5V~100V
- Constant current output limited only by external component selection (Note)
- No loop compensation required
- Internal over-voltage protection
- Internal over-temperature protection
- Operating temperature range -40°C to +85°C (IS31LT3948-GRLS2-TR)
- Operating temperature range -40°C to +125°C (IS31LT3948-GRLS4-TR)
- SOP-8 package

Note: The maximum output current is determined by  $V_{OUT}/V_{IN}$  ratio as well as the external components. If output current and  $V_{OUT}/V_{IN}$  ratio is high, high current components of inductor and NMOS are needed.

### APPLICATIONS

- TV monitor backlighting
- Notebook
- Automotive
- Street lamp
- LED lighting

### TYPICAL APPLICATION CIRCUIT

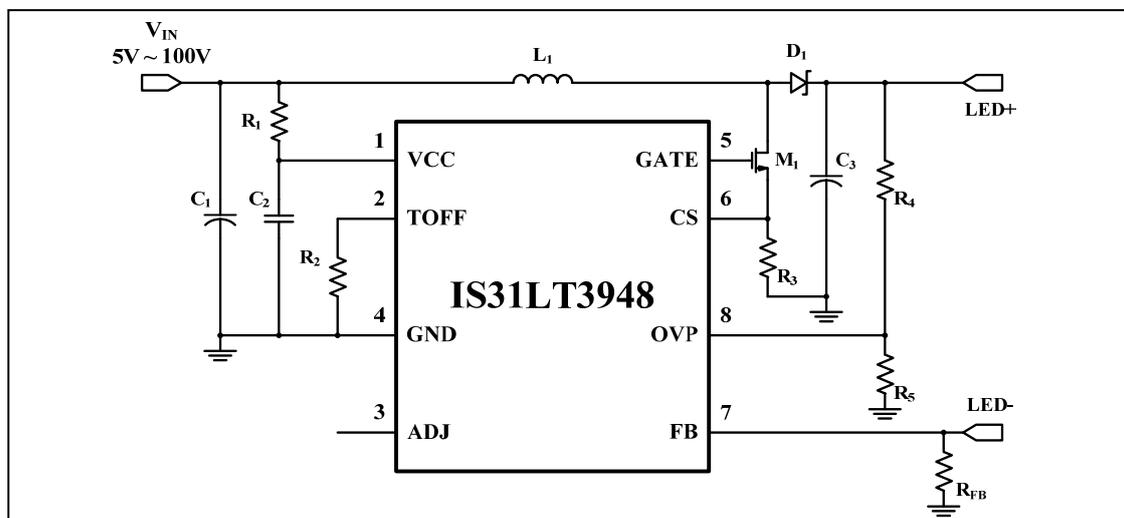
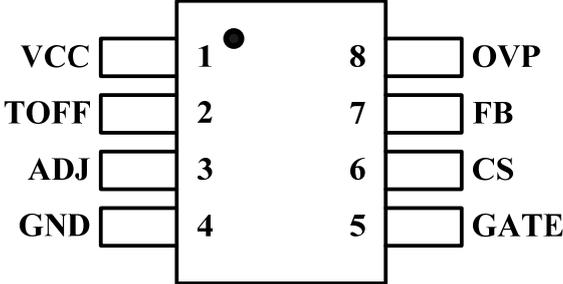


Figure 1 Typical Application Circuit

# IS31LT3948

## PIN CONFIGURATIONS

Package	Pin Configuration (Top View)
SOP-8	

## PIN DESCRIPTIONS

No.	Pin	Description
1	VCC	Positive power supply input pin. Internally clamped at 5V (Typ.).
2	TOFF	Off time setting pin. An external resistor connected to this pin forms an RC discharge path to generate a constant minimum off time of the NMOS.
3	ADJ	Enable and input peak current control pin. Pulled up to 4.5V internally to set $V_{CS\_TH}=0.24V$ when ADJ is floating. If $V_{ADJ}<0.5V$ , NMOS will always shutdown. If $0.5\leq V_{ADJ}\leq 2.4V$ , $V_{CS\_TH} = V_{ADJ}/10$ . If $V_{ADJ}>2.4V$ , $V_{CS\_TH}=0.24V$ . Note: During the start up ( $V_{CC}$ voltage is rising), ADJ must not be connected to low (recommended floating).
4	GND	Ground.
5	GATE	Driver's output for the gate of the external NMOS.
6	CS	Current sense input for the boost, peak current control loop.
7	FB	Feedback voltage input pin. Used to regulate the current of LEDs by keeping $V_{FB}=0.3V$ .
8	OVP	Overvoltage protection input pin, if the voltage of OVP exceed 1V, gate will always shutdown.

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## ORDERING INFORMATION

**Industrial Range: -40°C to +85°C**

Order Part No.	Package	QTY/Reel
IS31LT3948-GRLS2-TR	SOP-8, Lead-free	2500

### Part No. Rules

IS (ISSI Prefix)  
 31 (Product Family) - Analog and mix signal  
 LT (Product Type) - Lighting LED driver  
 3948 (Part Number) - 3948  
 GR (Package Code) - SOP  
 L (Solder Type) - Lead-free (RoHS compliant)  
 S2 (Temperature Grade) - Industrial temperature (-40°C ~ +85°C)  
 TR (Packing Option) - Tape & Reel

**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY/Reel
IS31LT3948-GRLS4-TR	SOP-8, Lead-free	2500

### Part No. Rules

IS (ISSI Prefix)  
 31 (Product Family) - Analog and mix signal  
 LT (Product Type) - Lighting LED driver  
 3948 (Part Number) - 3948  
 GR (Package Code) - SOP  
 L (Solder Type) - Lead-free (RoHS compliant)  
 S4 (Temperature Grade) - Industrial temperature (-40°C ~ +125°C)  
 TR (Packing Option) - Tape & Reel

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- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

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## ABSOLUTE MAXIMUM RATINGS

VCC to GND	-0.3V to 6.0V
CS, ADJ,GATE,TOFF,OVP,FB	-0.3V to 6.0V
VCC Max. input current	10mA
Maximum operating junction temperature, T <sub>JMAX</sub>	150°C
Storage temperature range, T <sub>STG</sub>	-65°C ~ +150°C
Operating temperature, T <sub>A</sub> = T <sub>J</sub>	-40°C ~ +85°C, IS31LT3948-GRLS2-TR -40°C ~ +125°C, IS31LT3948-GRLS4-TR
ESD (HBM)	±2kV
ESD (CDM)	±1kV

**Note:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V<sub>IN</sub>=10V, R<sub>IN</sub>=10kΩ, ADJ floating, T<sub>A</sub>= 25°C.

○ Parameter range based on T<sub>A</sub> = -40°C ~ +125°C (Note 1)

The symbol in the table means these parameters are only available in the above temperature range.

Symbol	Parameter	Conditions	Tem.	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Input voltage	Supply voltage connected to V <sub>CC</sub> via a appropriate resistor (Note 2)		5		100	V
V <sub>CC</sub>	V <sub>CC</sub> clamp voltage	R <sub>IN</sub> =10kΩ		4.3	5	5.6	V
			○	4.1	5	5.8	
V <sub>UVLO</sub>	Undervoltage threshold	V <sub>CC</sub> rising		2.2	2.7	3.0	V
			○	2.0	2.7	3.2	
V <sub>UVLO_HYS</sub>	Undervoltage threshold hysteresis				300		mV
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = V <sub>CC</sub> clamp voltage			400	500	μA
			○		400	700	
	Quiescent supply current when V <sub>CC</sub> undervoltage	V <sub>CC</sub> =2.5V			50	75	μA
			○		50	145	
V <sub>CS_TH</sub>	Peak current sense threshold	V <sub>ADJ</sub> =5V		215	240	265	mV
			○	202	240	275	
t <sub>BLANK</sub>	Peak current sense blank interval	V <sub>CS</sub> =V <sub>CS_TH</sub> +50mV			500		ns
t <sub>OFF</sub>	Fixed turn-off interval	R <sub>EXT</sub> =250kΩ			10		μs

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## ELECTRICAL CHARACTERISTICS (CONTINUE)

Unless otherwise specified,  $V_{IN}=10V$ ,  $R_{IN}=10k\Omega$ , ADJ floating,  $T_A=25^\circ C$ .

○ Parameter range based on  $T_A = -40^\circ C \sim +125^\circ C$  (Note 1)

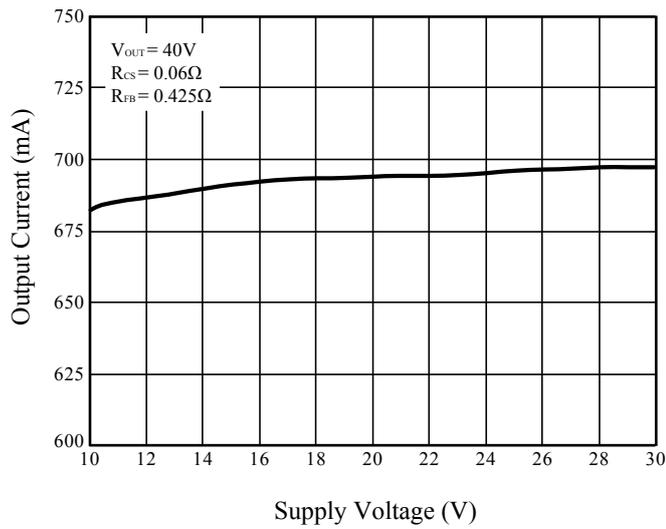
The symbol in the table means these parameters are only available in the above temperature range.

Symbol	Parameter	Conditions	Tem.	Min.	Typ.	Max.	Unit
$V_{ADJ}$	Peak current control low threshold				0.5		V
	Peak current control high threshold				2.4		V
$T_{SD}$	Thermal shutdown threshold				150		$^\circ C$
$T_{SD\_HYS}$	Thermal shutdown hysteresis				20		$^\circ C$
$V_{FB\_TH}$	Feedback voltage threshold	IS31LT3948-GRLS2-TR		290	300	310	mV
		IS31LT3948-GRLS4-TR		292	300	310	
			○	285	300	315	
$V_{OVP\_TH}$	Overvoltage input threshold			0.9	1.0	1.1	V

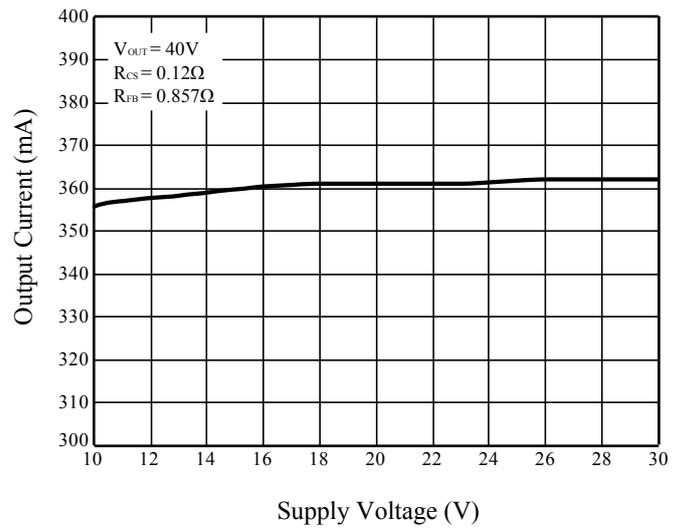
**Note 1:** Production testing of the device is performed at  $25^\circ C$ . Functional operation of the device and parameters specified over temperature range, are guaranteed by design, characterization and process control.

**Note 2:**  $V_{IN}$  is the input voltage. When  $V_{IN} \leq 5V$ , connect input voltage directly to  $V_{CC}$ . When  $V_{IN} > 5V$ , input voltage should be connected to  $V_{CC}$  pin via an appropriately valued resistor.

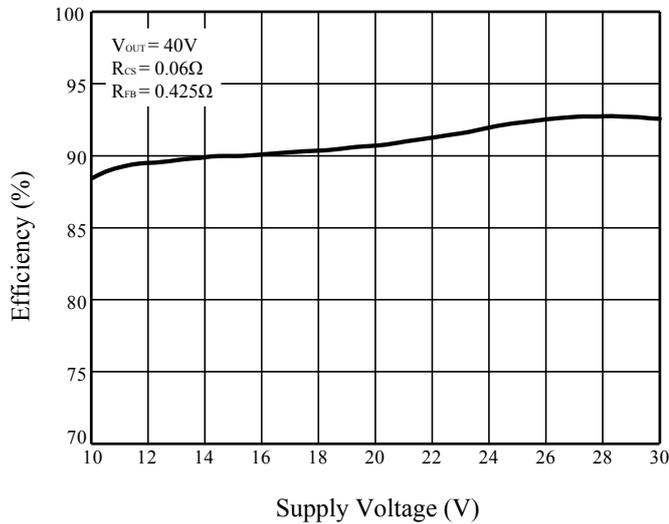
## TYPICAL PERFORMANCE CHARACTERISTICS



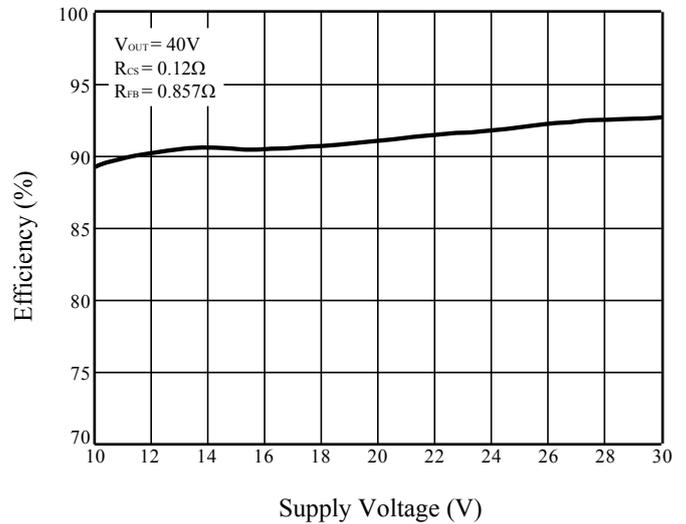
**Figure 2** Supply Voltage vs. Output Current



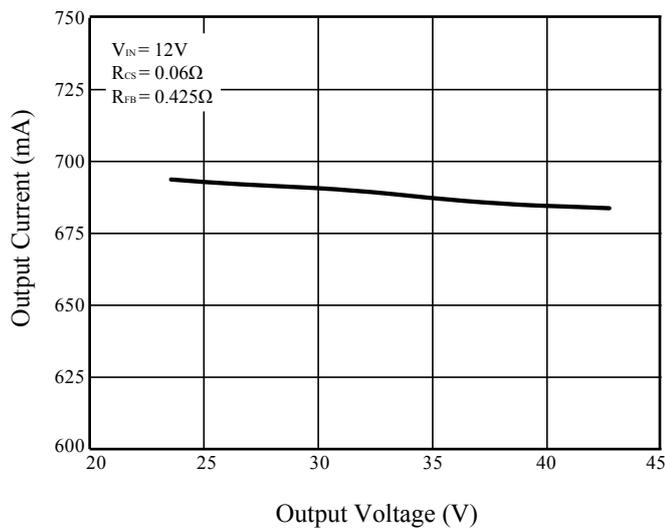
**Figure 3** Supply Voltage vs. Output Current



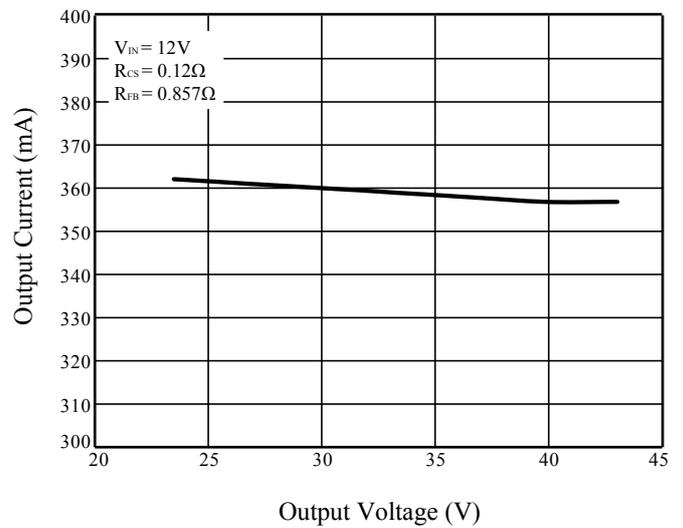
**Figure 4** Supply Voltage vs. Efficiency



**Figure 5** Supply Voltage vs. Efficiency

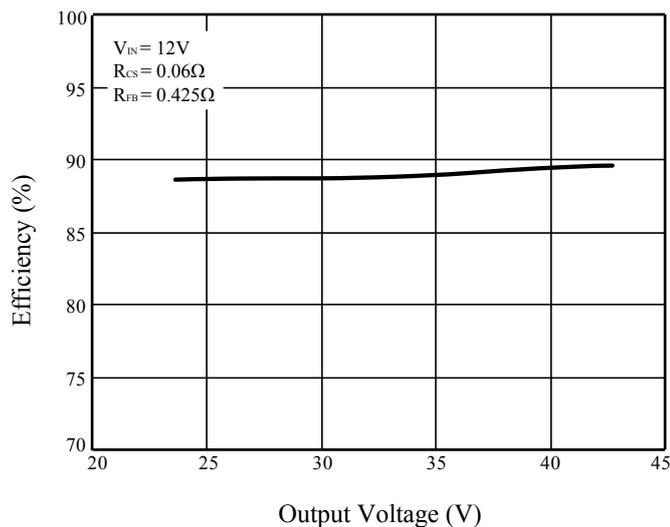


**Figure 6** Output Voltage vs. Output Current

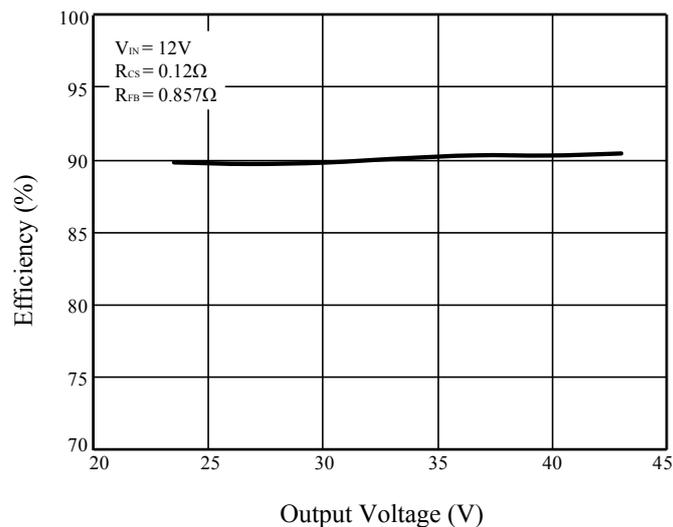


**Figure 7** Output Voltage vs. Output Current

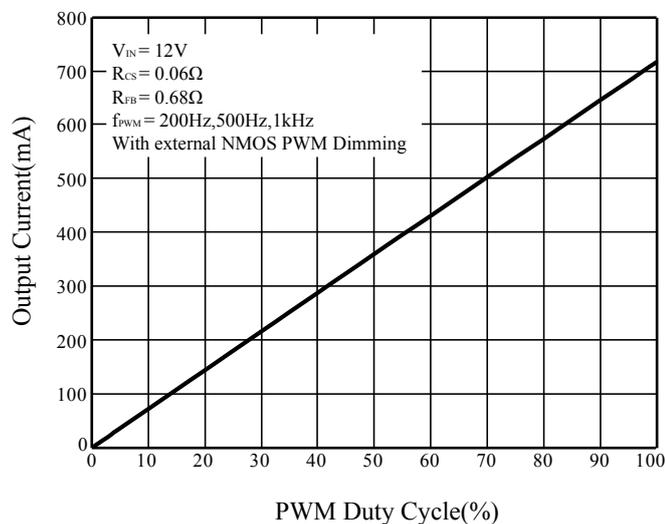
# IS31LT3948



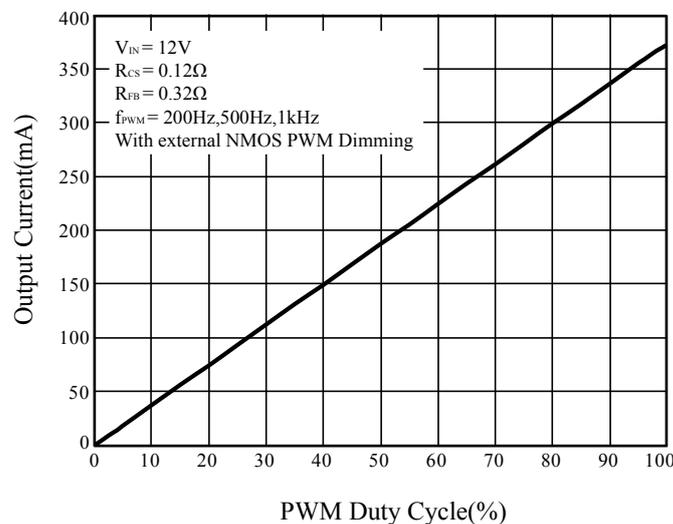
**Figure 8** Output Voltage vs. Efficiency



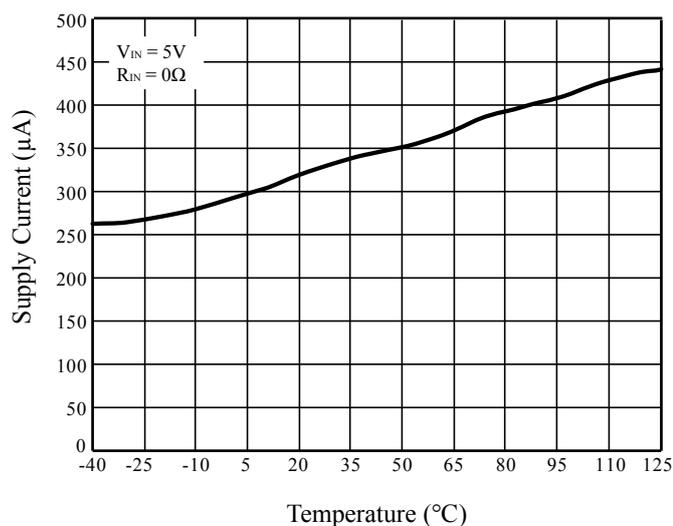
**Figure 9** Output Voltage vs. Efficiency



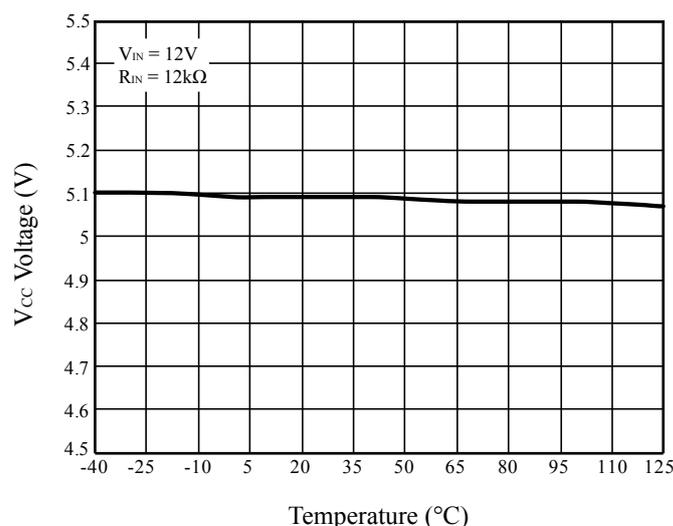
**Figure 10** PWM Duty Cycle vs. Output Current



**Figure 11** PWM Duty Cycle vs. Output Current

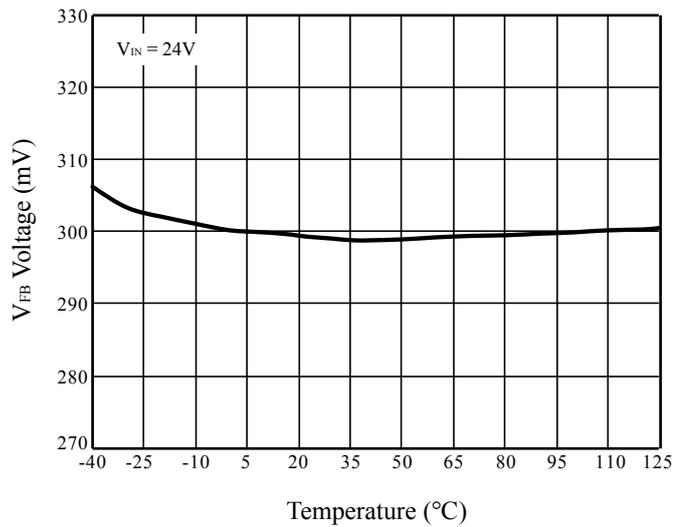


**Figure 12** Temperature vs. Supply Current

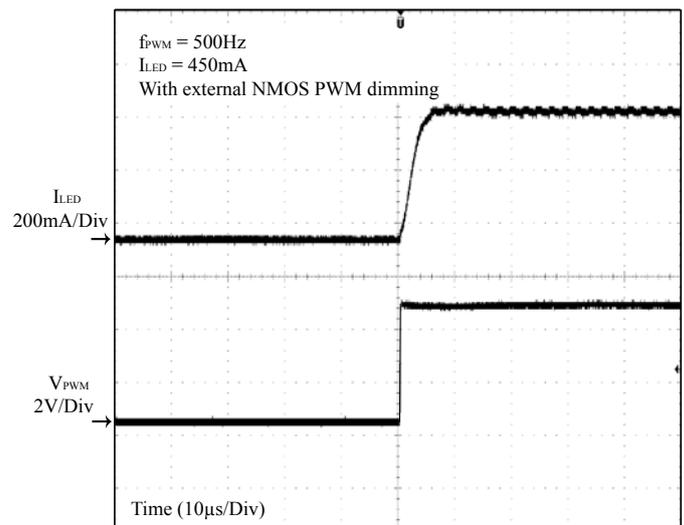


**Figure 13** Temperature vs. V<sub>CC</sub>

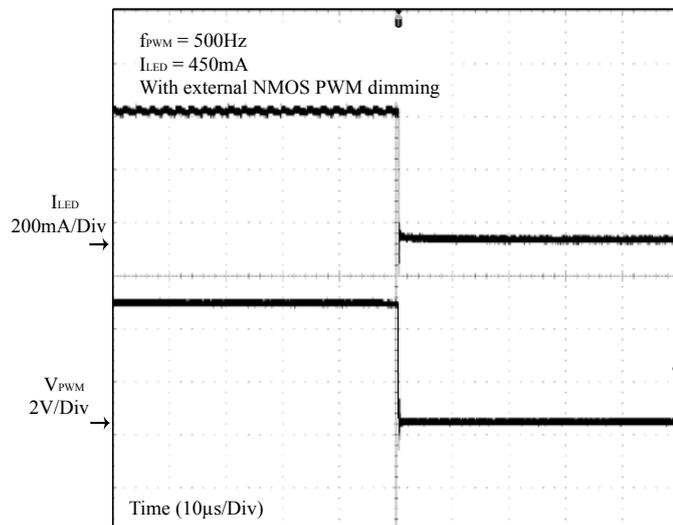
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**Figure 14** Temperature vs. V<sub>FB</sub>



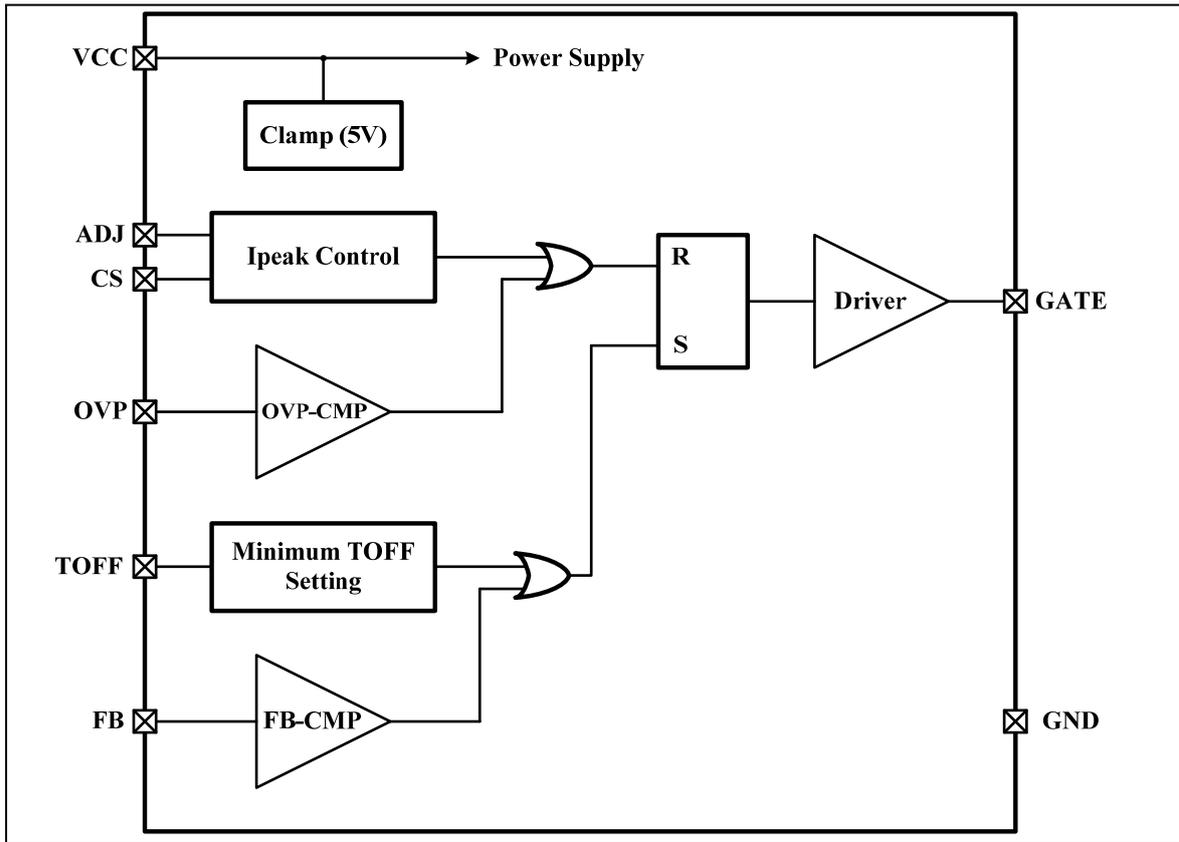
**Figure 15** Output Current vs. V<sub>PWM</sub> on Rising Time



**Figure 16** Output Current vs. V<sub>PWM</sub> on Falling Time

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## FUNCTIONAL BLOCK DIAGRAM



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## APPLICATION INFORMATION

### INTERNAL 5V REGULATOR

The IS31LT3948 includes an internal shunt regulator of 5V (Typ.) connected to the  $V_{CC}$  pin. When the input voltage is higher than 5V, connect  $V_{CC}$  to  $V_{IN}$  using an appropriately valued, current limiting resistor. The regulator maintains a 5V power supply for the internal NMOS switch gate driver and the internal control circuitry. In applications where the input voltage is 5V, connect the input voltage directly to  $V_{CC}$ . When  $V_{CC}$  is connected directly to  $V_{IN}$ ,  $V_{IN}$  may not exceed 5V. Bypass the  $V_{CC}$  pin using a low ESR capacitor (recommended 10 $\mu$ F ceramic capacitor) to provide a high frequency path to GND.

The current required by IS31LT3948 is 0.4mA (Typ.) plus the switching current of the external switch. The switching frequency of the external NMOS affects the amount of current required, as does the NMOS's gate charge requirement (found on the NMOS data sheet).

$$I_{IN} \approx 0.4mA + Q_G \times f_S \quad (1)$$

Where  $f_S$  is the switching frequency and  $Q_G$  is the external NMOS gate charge.

### UNDER VOLTAGE LOCKOUT

IS31LT3948 features an under voltage lockout threshold of 2.7V (Typ.) with a hysteresis of 300mV. The chip is disabled when  $V_{CC}$  is lower than 2.4V and enabled when  $V_{CC}$  exceeds 2.7V.

### STEP-UP CONVERTER

IS31LT3948's step-up converter uses a peak current mode topology wherein the CS pin voltage determines the peak current in the inductor of the converter and hence the duty cycle of the GATE switching waveform. The basic loop uses a pulse from an internal oscillator to set an RS flip-flop and turn on the external power NMOS. After the blanking time, the inductor current is sensed during the GATE on period by a sense resistor,  $R_{CS}$ , in the source of the external power NMOS. The current increases in the NMOS and inductor until the voltage across the sense resistor reaches the CS threshold, at which time NMOS is turned off. Once the NMOS is turned off, the inductor reverses polarity, providing the voltage boost, and the current of inductor will decrease until the FB pin voltage drops below internal reference voltage and the NMOS is then turned on again. This operation repeats each cycle.

Note, in the case where the FB pin voltage does not exceed the FB reference voltage of 0.3V, such as at start-up, the NMOS will remain off for the programmed minimum  $t_{OFF}$  time, then the NMOS is switched on again.

### LED CURRENT CONTROL

IS31LT3948 regulates the LED current by sensing the voltage across an external sense resistor in series with the LEDs. The voltage is sensed via the FB pin where the internal feedback reference voltage is 0.3V (Typ.). The LED current can be set from following equation easily.

$$I_{OUT} = \frac{0.3}{R_{FB}} \quad (2)$$

In order to have an accurate LED current, precision resistors are required (1% is recommended).

### SETTING THE OVER VOLTAGE PROTECTION

The open string protection is achieved through the over voltage protection (OVP). In some cases, an LED string failure results in a feedback voltage that is always zero. If this happens, the part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection will be triggered and stop the switching action. To make sure that the circuit functions properly, the OVP setting resistor divider must be set with an appropriate value. The recommended  $V_{OVP}$  point is about 1.2 times or 5V (choose the larger one) higher than the output voltage for normal operation.

$$V_{OVP} = V_{OVP\_TH} \times \frac{R_4 + R_5}{R_5} \quad (3)$$

Where,  $V_{OVP\_TH}$  is 1V, and  $V_{OVP}$  is the output voltage OVP level.

### DIMMING CONTROL

There are two methods for dimming.

- 1) External NMOS PWM dimming:

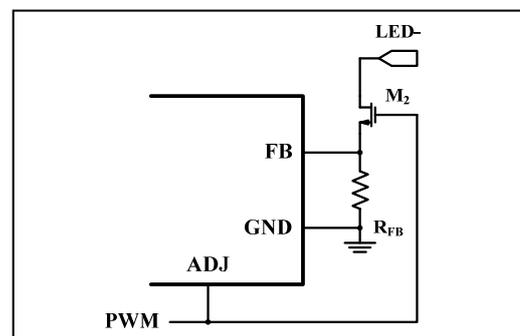


Figure 17 External PWM Dimming

When the PWM input is high ( $V_H > 2.4V$ ), M2 is on and IS31LT3948 operates normally to regulate the output current. When PWM is low logic ( $V_L < 0.5V$ ), M2 is off and IS31LT3948 is shutdown. Using a fixed frequency PWM signal and changing the duty cycle adjusts the average output current. The

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recommended 5V PWM frequency is between 200Hz and 1kHz. M2 is recommended to use AP2306. The rising time depends on external component. The minimum on time of PWM signal is recommended to be over the rising time to achieve better dimming rate.

## 2) RC filter PWM dimming:

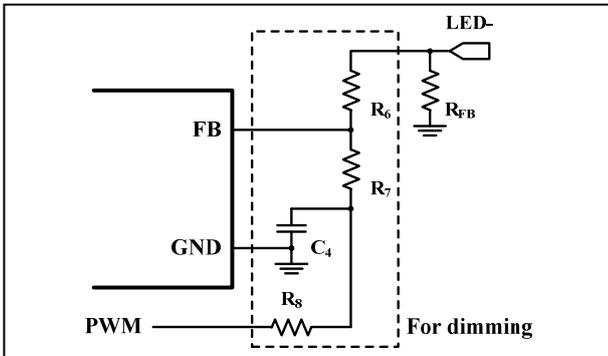


Figure 18 RC PWM Dimming

A filtered PWM signal can be used as an adjustable DC voltage for LED dimming control. The filtered PWM signal becomes DC voltage which is summed together with the FB voltage to regulate the output current. Fix the frequency of the PWM signal and change the duty cycle to adjust the LED current. The LED current can be calculated by the following equation:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH})}{R_7 + R_8} \quad (4)$$

The PWM duty cycle is inversely proportional to the LED current. That is, when the PWM signal is 100% duty cycle, the output current is minimum, ideally zero, and when the PWM signal is 0% duty cycle, the output current is maximum.

See details value in the Example section.

Note: When the  $V_{OUT}/V_{IN}$  ratio is less than 2, careful consideration must be given to ensure that  $V_{OUT}$  remains greater than  $V_{IN}$  at the minimum dimming level.

## INPUT PEAK CURRENT CONTROL

IS31LT3948 limits the peak inductor current, and thus peak input current through the feedback of  $R_3$  connected from source of NMOS to ground. The required average input current is based on the boost ratio,  $V_{OUT}/V_{IN}$ , and the designed value for average LED current. The required average input current can be calculated as:

$$I_{AVG\_IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (5)$$

$\eta$ : assumed power conversion efficiency (the recommended value is 0.9)

Generally, setting the peak inductor current to 1.5 times the average input current is sufficient to maintain a good regulation of the output current.

$$I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN} = \frac{V_{CS\_TH}}{R_{CS}} \quad (6)$$

$V_{CS\_TH}$ : If  $0.5 < V_{ADJ} < 2.4V$ ,  $V_{CS\_TH} = V_{ADJ}/10$ . If  $V_{ADJ} > 2.4V$ ,  $V_{CS\_TH} = 0.24V$ . ADJ floating,  $V_{CS\_TH} = 0.24V$ .

## INPUT CAPACITOR

The input capacitor of the IS31LT3948 will supply the transient input current of the power inductor. Value of 100 $\mu$ F or higher is recommended to prevent excessive input voltage ripple.

## SETTING $t_{OFF\_MIN}$

IS31LT3948 operates in a pulsed frequency modulation mode. The boost control loop is a constant off-time architecture. The off time is programmable and set by an external resistor connected between the  $t_{OFF}$  pin and GND. In most application, the recommended  $t_{OFF\_MIN}$  is 1 $\mu$ s. The governing equation for the off time is:

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{EXT} \quad (7)$$

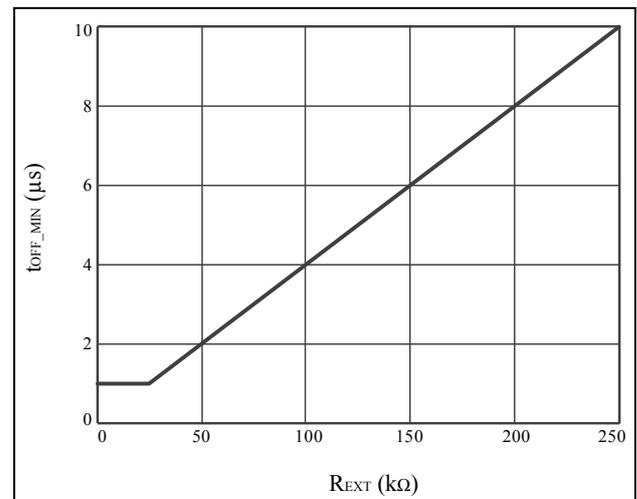


Figure 19  $R_{EXT}$  vs.  $t_{OFF\_MIN}$

Note, the minimum  $t_{OFF\_MIN}$  is 1 $\mu$ s.

## INDUCTOR SELECTION

Inductor value directly determines the switching frequency of the converter. To the fixed condition and the larger inductor value the lower switching frequency. The higher frequency will reduce the value of inductor, but will increase the switching loss on NMOS.

The switching frequency can be calculated blow.

Switching frequency:

$$f = 1/(t_{ON} + t_{OFF}) \quad (8)$$

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The current ripple in the inductor:

$$I_{RIPPLE} = 2 \times (I_{PEAK\_IN} - I_{AVG\_IN}) \quad (9)$$

NMOS on time:

$$t_{ON} = \frac{I_{RIPPLE} \times L}{V_{IN} - I_{AVG\_IN} \times (R_L + R_{DS\_ON} + R_{CS})} \quad (10)$$

NMOS off time:

$$t_{OFF} = \frac{I_{RIPPLE} \times L}{V_{OUT} + V_D - V_{IN} - I_{AVG\_IN} \times R_L} \quad (11)$$

Note, the selection of inductor must ensure that the  $t_{OFF}$  larger than the  $t_{OFF\_MIN}$ , or else the converter can not output the required current.

Where:

$V_{IN}$ : Input voltage (V)

$V_{OUT}$ : Output voltage (V)

$I_{RIPPLE}$ : Current ripple in the inductor (A)

L: inductor value (H)

$I_{PEAK\_IN}$ : Input peak current (A)

$I_{AVG\_IN}$ : Input average current (A)

$R_L$ : Inductor DCR ( $\Omega$ )

$R_{DS\_ON}$ : NMOS on resistance ( $\Omega$ )

$V_D$ : diode forward voltage at the required load current (V)

The recommended switching frequency:  $20\text{kHz} < f < 200\text{kHz}$  (Lower than 20kHz will cause audio noise of the inductor and too high frequency will increase the switching loss on NMOS).

To the fixed  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{AVG\_IN}$ ,  $I_{PEAK\_IN}$  and the switching frequency is inversely proportional to the inductor value.

Select an inductor with a rating current over input average current and the saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Also ensure that the inductor has a low DCR (copper wire resistance) to minimize  $I^2R$  power loss.

## OUTPUT CAPACITOR

The output capacitor holds the output current during NMOS on. The capacitor directly impacts the line regulation and the loading regulation.

Low ESR capacitors using at the IS31LT3948 converter output can minimize output ripple voltage and improve output current regulation. For most applications, a 220 $\mu\text{F}$  low ESR capacitor will be

sufficient. Proportionally lower ripple can be achieved with higher capacitor values.

## SCHOTTKY RECTIFIER

The external diode for the IS31LT3948 must be a Schottky diode, with low forward voltage drop and fast switching speed. The diode's average current rating must exceed the application's average output current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application. For PWM dimming applications, be aware of the reverse leakage of the Schottky diode. Lower leakage current will drain the output capacitor less during PWM low periods, allowing for higher PWM dimming ratios.

## Power NMOS Selection

The power NMOS selected should have a  $V_{DS}$  rating which exceeds the maximum over voltage protection (OVP) level programmed for the application. The  $V_{GS\_TH}$  of NMOS should be not higher than 4V. The  $R_{DS\_ON}$  of the NMOS will determine DC power loss. The DC power loss can be calculated by:

$$P_{loss} = I_{M1}^2 \times R_{DS\_ON} = \left( \frac{V_{OUT} \times I_{OUT} \times Duty}{V_{IN} \times \eta} \right)^2 \times R_{DS\_ON} \quad (12)$$

The recommended NMOS rating current is 5 times (or higher) to the input peak current ( $I_{PEAK\_IN}$ ). Be aware of the power dissipation within the NMOS and deciding if the thermal resistance of the NMOS package causes the junction temperature to exceed maximum ratings.

## PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems.

- Wide traces should be used for connection of the high current loop to minimize the EMI and unnecessary loss.
- The external components ground should be connected to IS31LT3948 ground as short as possible. Especially the  $R_{FB}$  ground to IS31LT3948 ground connection should be as short and wide as possible to have an accurate LED current.
- The capacitor  $C_1$ ,  $C_2$ ,  $C_3$  should be placed as close as possible to IS31LT3948 for good filtering. Especially the output capacitor  $C_3$  connection should be as short and wide as possible.
- NMOS drain is a fast switching node. The inductor and Schottky diode should be placed as close as possible to the drain and the connection

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should be kept as short and wide as possible. Avoid other traces crossing and routing too long in parallel with this node to minimize the noise coupling into these traces. The feedback pin (e.g. CS, FB, OVP) should be as short as possible and routed away from the inductor, the Schottky diode and NMOS. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

- The thermal pad on the back of NMOS package must be soldered to the large ground plane for ideal power dissipation.

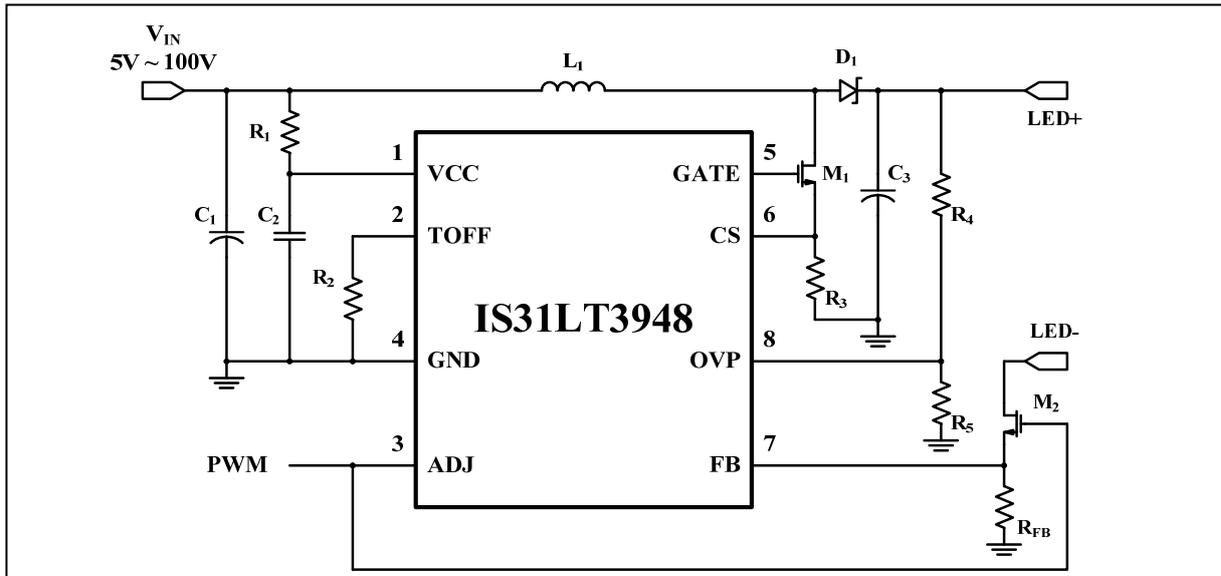


Figure 20 External NMOS PWM Dimming

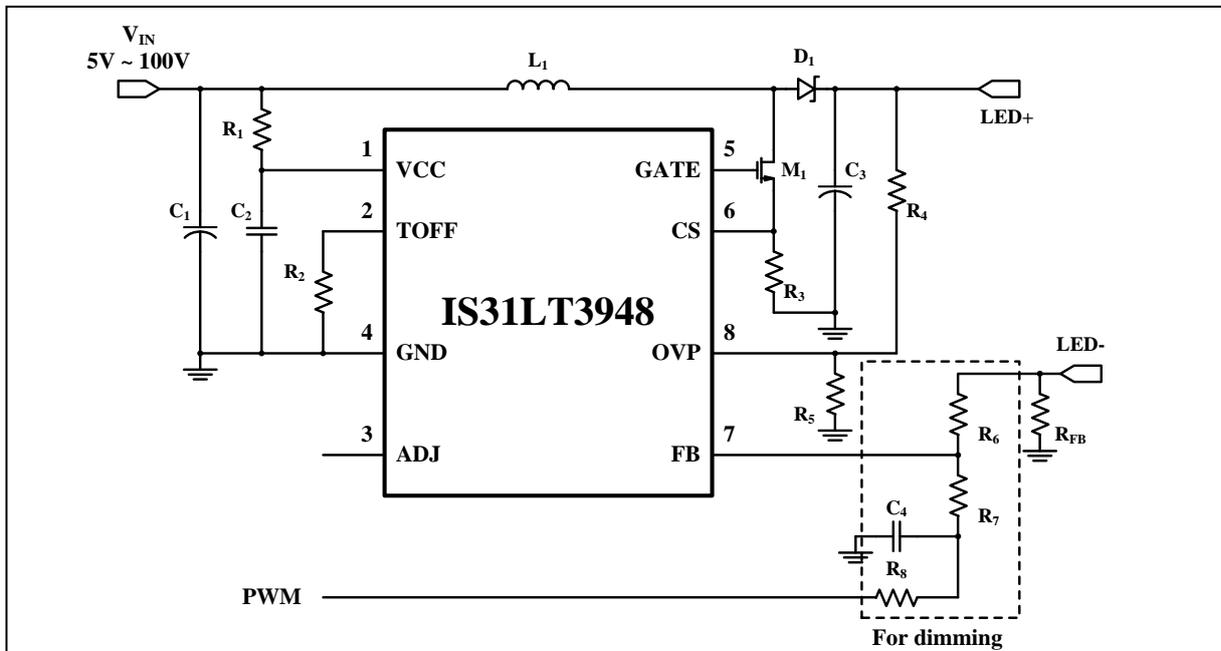


Figure 21 RC Filter PWM Dimming

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## EXAMPLE:

Input:  $V_{IN}=12V\sim 24V$

Output:  $I_{OUT}=350mA$ ,  $V_{OUT}\approx 30V\sim 40V$  (9~12LEDs,  $V_{FB}=3.3V$ )

To calculate the worst case parameter, use the minimum input voltage, the maximum output voltage, and maximum output current. So choose:  $V_{IN}=12V$ ,  $I_{OUT}=350mA$ ,  $V_{OUT}\approx 40V$  (12LEDs,  $V_{FB}=3.3V$ )

### 1. $R_1$ , $C_1$ and $C_2$

Assume  $I_{IN} = 2.5mA$ ,

$$R_1 = \frac{V_{IN\_MIN} - V_{CC}}{I_{IN}} = \frac{12 - 5}{2.5} = 2.8k\Omega \approx 3k\Omega$$

Note: The maximum VCC input current at highest input voltage must not exceed 10mA.

$$I_{IN} = (V_{IN\_MAX} - V_{CC})/R_1 < 10mA$$

Choose  $C_1$  as 220 $\mu$ F/35V,  $C_2$  as 10 $\mu$ F/16V.

### 2. $R_2$ to Set $t_{OFF\_MIN}$

The recommended value is 1 $\mu$ s,

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{EXT} = 1\mu s$$

Choose  $R_2=24k\Omega$ .

### 3. $R_{FB}$ to Set Output Current and $C_3$

$$R_{FB} = \frac{V_{FB\_TH}}{I_{OUT}} \approx 0.86\Omega$$

Choose  $C_3$  as 220 $\mu$ F/63V (Low ESR electrolytic capacitor).

### 4. $R_6$ , $R_7$ , $R_8$ and $C_4$

$R_6$ ,  $R_7$  and  $R_8$  can be calculated by:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH}) / (R_7 + R_8)}{R_{FB}}$$

Take Duty=100%,  $V_{PWM}=5V$  and  $I_{OUT}=0A$  into the equation, then we have:

$$0 = \frac{0.3 - R_6 \times (5 \times 100\% - 0.3) / (R_7 + R_8)}{0.86}$$

Which simplifies to:  $15.66 \times R_6 = R_7 + R_8$

The low-pass filter formed by  $R_8$  and  $C_4$  must have a corner frequency much lower than the PWM frequency. As the corner frequency of the filter decreases, the response time of the LED current to changes in PWM increases. Choose a corner frequency 50 times lower than  $f_{PWM}$ .

$$R_8 \times C_4 \geq \frac{50}{2\pi \times f_{PWM}}$$

Assuming  $f_{PWM}$  is 200Hz (or higher), and choosing  $C_4=0.1\mu$ F, we find  $R_8 \geq 400k\Omega$ .

Choose  $C_4=0.1\mu$ F,  $R_8=400k\Omega$ .

Choose a nominal value for  $R_7$ , then compute  $R_6$ .

Choose  $R_7=10k\Omega$ , then  $R_6=26.2k\Omega$

Take Duty=0,  $V_{PWM} = 5V$  and  $I_{OUT}=350mA$  into the equation, then we have:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH}) / (R_7 + R_8)}{R_{FB}} = \frac{0.3 - 26.2 \times (5 \times 0\% - 0.3) / (400 + 10)}{0.86} = 0.35A$$

So  $R_{FB}=0.91\Omega$  (With the RC filter PWM dimming, the  $R_{FB}$  will be different from the no dimming application.)

### 4. $R_3$ to Set Input Peak Current

Assume  $I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN}$

$$I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN} = 1.5 \times \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = 1.5 \times \frac{40 \times 0.35}{12 \times 0.9} \approx 1.95A$$

$\eta$ : assumed power conversion efficiency (the recommended value is 0.9).

$$R_{CS} = \frac{V_{CS\_TH}}{I_{PEAK\_IN}} = 0.123\Omega$$

Choose  $R_3=0.123\Omega$ ,  $I_{PEAK}=1.95A$

### 5. $L_1$ to Set Frequency

Input average current is

$$I_{AVG\_IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = 1.3A$$

The current ripple in the inductor:

$$I_{RIPPLE} = 2 \times (I_{PEAK\_IN} - I_{AVG\_IN}) = 1.3A$$

According to  $t_{OFF} > t_{OFF\_MIN}$ :

$$t_{OFF} = \frac{I_{RIPPLE} \times L}{V_{OUT} + V_D - V_{IN} - I_{AVG\_IN} \times R_L} > 1\mu s$$

This gives  $L > 22\mu H$ .

Assuming  $L=22\mu H$  and

$$R_L + R_{DS\_ON} + R_{CS} = 0.4\Omega.$$

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$$t_{ON} = \frac{I_{RIPPLE} \times L}{V_{IN} - I_{AVG\_IN} \times (R_L + R_{DS\_ON} + R_{CS})} \approx 2.5 \mu s$$

Then the assumed switching frequency:

$$f' = 1 / (t_{ON} + t_{OFF}) \approx 285 kHz$$

The recommended switching frequency:

20kHz < f < 200kHz, according to the switching frequency is inversely proportional to the inductor value, choose L=100μH. Therefore:

$$f = f' \times \frac{22}{100} \approx 63 kHz$$

The saturation current of the inductor must exceed the input peak current (I<sub>PEAK\_IN</sub>).

## 6. R<sub>4</sub>, R<sub>5</sub> to Set OVP

$$\text{Set } V_{OVP} = V_{OUT} + 5V = 45V$$

$$V_{OVP} = V_{OVP\_TH} \times \frac{R_4 + R_5}{R_5}$$

Choose R<sub>5</sub>=10kΩ, then R<sub>4</sub> = 470kΩ.

## 7. NMOS M<sub>1</sub> and Diode D<sub>1</sub>

$$I_{1(NMOS)} > I_{PEAK\_IN}$$

$$V_{1(NMOS)} > V_{OVP}$$

Lower R<sub>DS\_ON</sub> NMOS can improve the converter efficiency. The recommended NMOS rating current is 5 times (or higher) to the input peak current (I<sub>PEAK\_IN</sub>).

Choose 13N10L as M<sub>1</sub>.

The average and peak current of diode must exceed the output average current and input peak current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application.

Choose SS310 as D<sub>1</sub>.

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## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min (T <sub>smin</sub> ) Temperature max (T <sub>smax</sub> ) Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	150°C 200°C 60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> ) Time at liquidous (t <sub>L</sub> )	217°C 60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

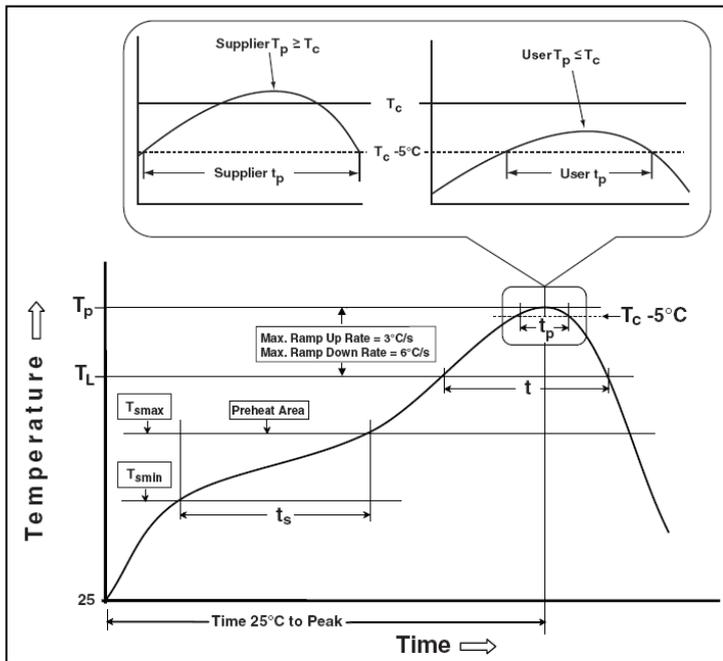
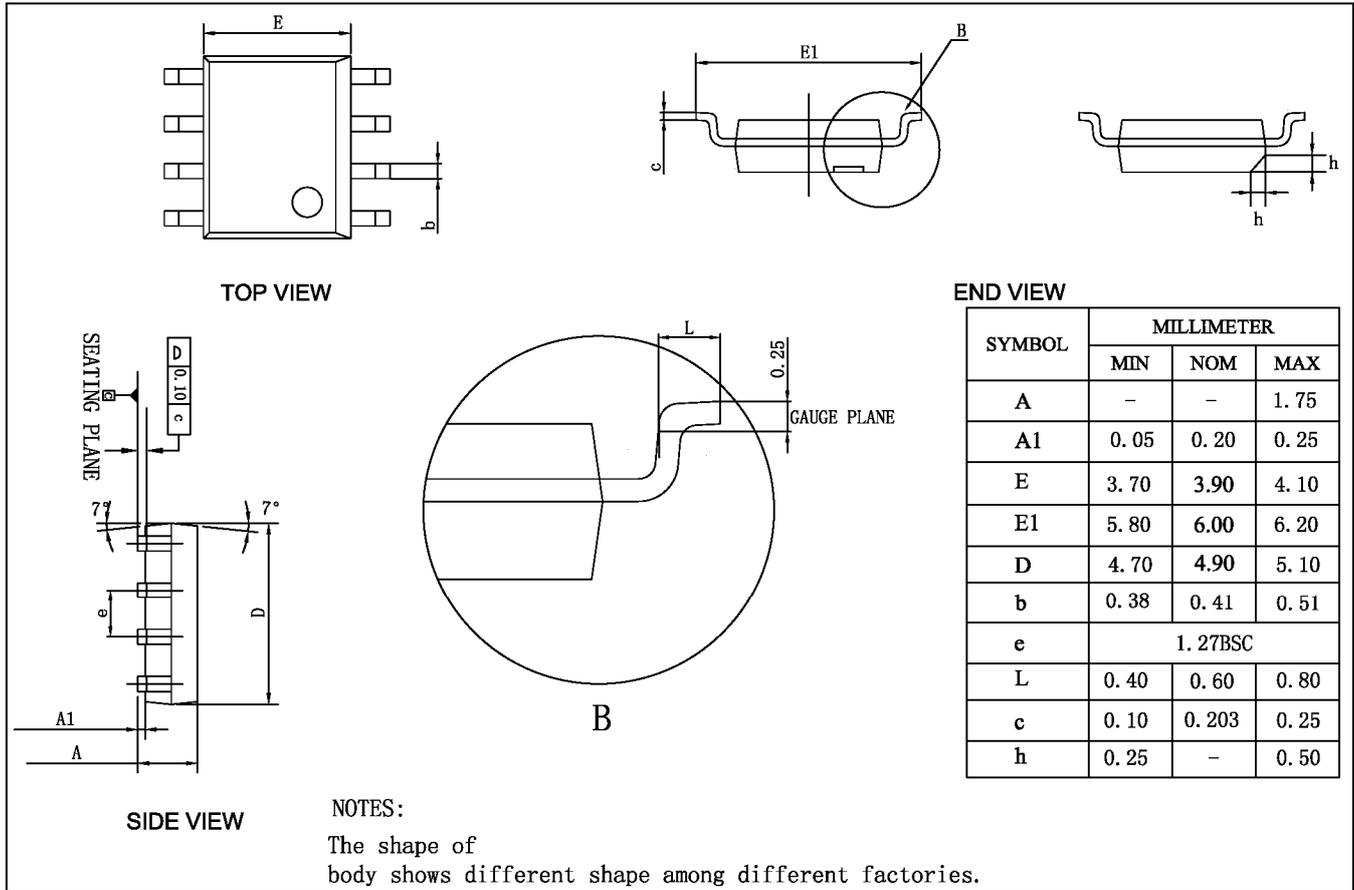


Figure 22 Classification Profile

# IS31LT3948

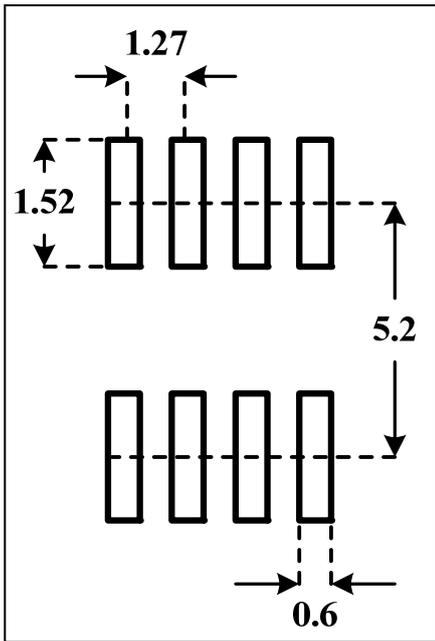
## PACKAGE INFORMATION

### SOP-8



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## LAND PATTERN



**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.

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