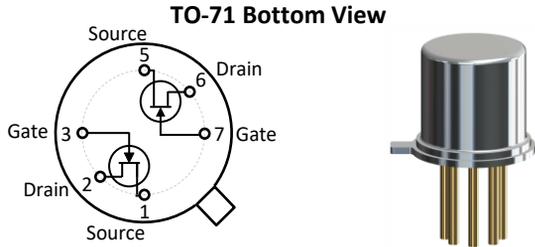


# IFNU231, IFNU232, IFNU233 Dual Matched N-Channel JFET

## Features

- InterFET [N0016H Geometry](#)
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 3.5 pF Typical
- High Input Impedance
- Replacement for U231, U232, U233
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

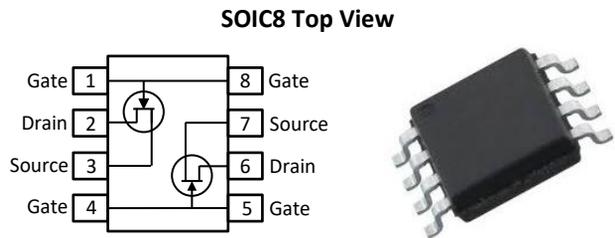


## Applications

- Low Noise Differential Amplifier
- Differential Amplifier
- Wide-Band Amplifier

## Description

The -50V InterFET IFNU231, IFNU232, and IFNU233 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



## Product Summary

Parameters	IFNU231 Min	IFNU232 Min	IFNU233 Min	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	-50	-50	-50	V
$I_{DSS}$ Drain to Source Saturation Current	0.5	0.5	0.5	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
$G_{FS}$ Forward Transconductance	0.6	0.6	0.6	mS

## Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU231; IFNU232; IFNU233	Through-Hole	TO-71	Bulk
SMPU231; SMPU232; SMPU233	Surface Mount	SOIC8	Bulk
SMPU231TR; SMPU232TR; SMPU233TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU231COT; IFNU232COT; IFNU233COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU231CFT; IFNU232CFT; IFNU233CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

\* Bare die packaged options are designed for matched specifications but not 100% tested



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V <sub>RGS</sub> Reverse Gate Source and Gate Drain Voltage	-50	V
I <sub>FG</sub> Continuous Forward Gate Current	50	mA
P <sub>D</sub> Continuous Device Power Dissipation	300	mW
P Power Derating	4.3	mW/°C
T <sub>J</sub> Operating Junction Temperature	-55 to 125	°C
T <sub>STG</sub> Storage Temperature	-65 to 150	°C

### Static Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

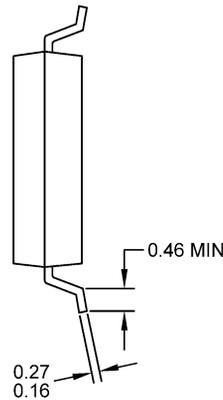
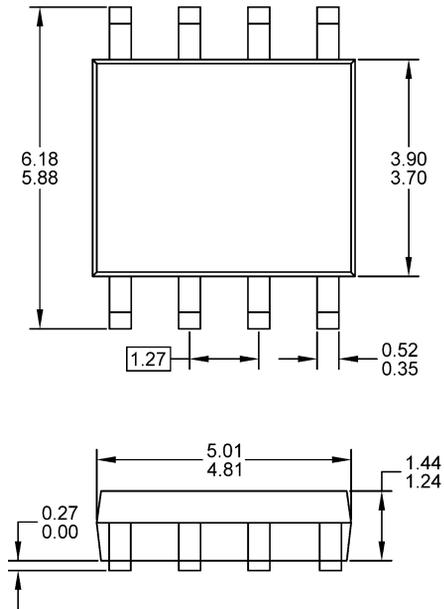
Parameters	Conditions	IFNU231, IFNU232, IFNU233		Unit
		Min	Max	
V <sub>(BR)GSS</sub> Gate to Source Breakdown Voltage	V <sub>DS</sub> = 0V, I <sub>G</sub> = -1μA	-50		V
I <sub>GSS</sub> Gate to Source Reverse Current	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 25°C V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 150°C		-100 -500	pA nA
V <sub>GS(OFF)</sub> Gate to Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-0.5	-4.5	V
V <sub>GS</sub> Gate to Source Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA	-0.3	-4	V
I <sub>DSS</sub> Drain to Source Saturation Current	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V (Pulsed)	0.5	5	mA
I <sub>G</sub> Gate Current	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA, T <sub>A</sub> = 25°C V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA, T <sub>A</sub> = 125°C		-50 -250	pA nA

### Dynamic Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Conditions	IFNU231, IFNU232, IFNU233		Unit
		Min	Max	
G <sub>FS</sub> Forward Transconductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA, f = 1kHz	0.6	1.6	mS
G <sub>OS</sub> Output Conductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA, f = 1kHz		10	μS
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz		6	pF
C <sub>rss</sub> Reverse Transfer Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz		2	pF
e <sub>n</sub> Equivalent Circuit Input Noise Voltage	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 100Hz		80	nV/√Hz
V <sub>GS1</sub> - V <sub>GS2</sub>   Differential Gate Source Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA	IFNU231	5	mV
		IFNU232	10	
		IFNU233	15	
$\frac{V_{GS1} - V_{GS2}}{\Delta T}$   Differential Gate Source Voltage with Temperature	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA, T <sub>A</sub> = -55°C, T <sub>B</sub> = 25°C, T <sub>C</sub> = 125°C	IFNU231	1	mV/°C
		IFNU232	2.5	
		IFNU233	4	

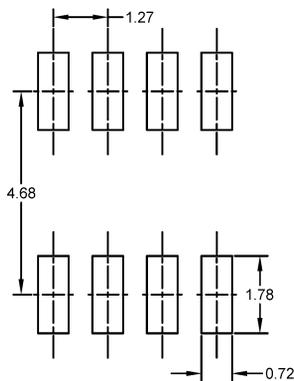
## SOIC8 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

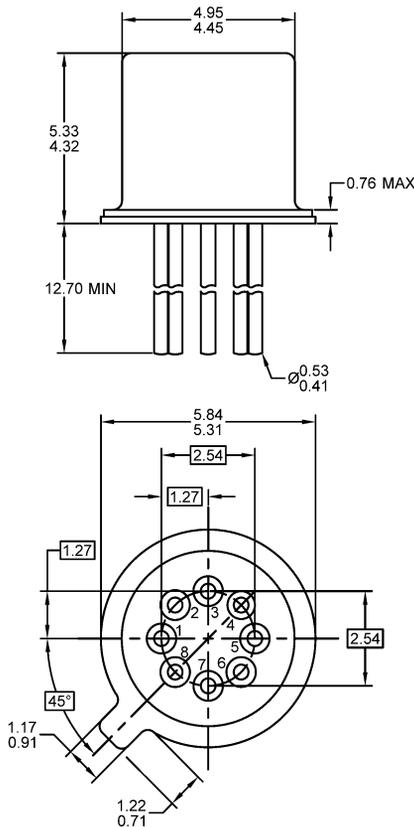
### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

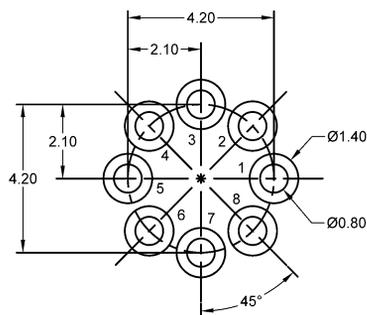
## TO-71 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

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