

XMC1400 AA-Step

Microcontroller Series for Industrial Applications

ARM® Cortex® -M0
32-bit processor core

About this Document

This datasheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1400 series devices.

The document describes the characteristics of a superset of the XMC1400 series devices. For simplicity, the various device types are referred to by the collective term XMC1400 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Datasheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Datasheets. Errata Sheets are provided for the superset of devices.

Attention: *Please consult all parts of the documentation set to attain consolidated knowledge about your device.*

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

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1 Summary of Features

1 Summary of Features

The XMC1400 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1400 series addresses the real-time control needs of motor control and digital power conversion. It also features peripherals for LED Lighting applications and Human-Machine Interface (HMI).

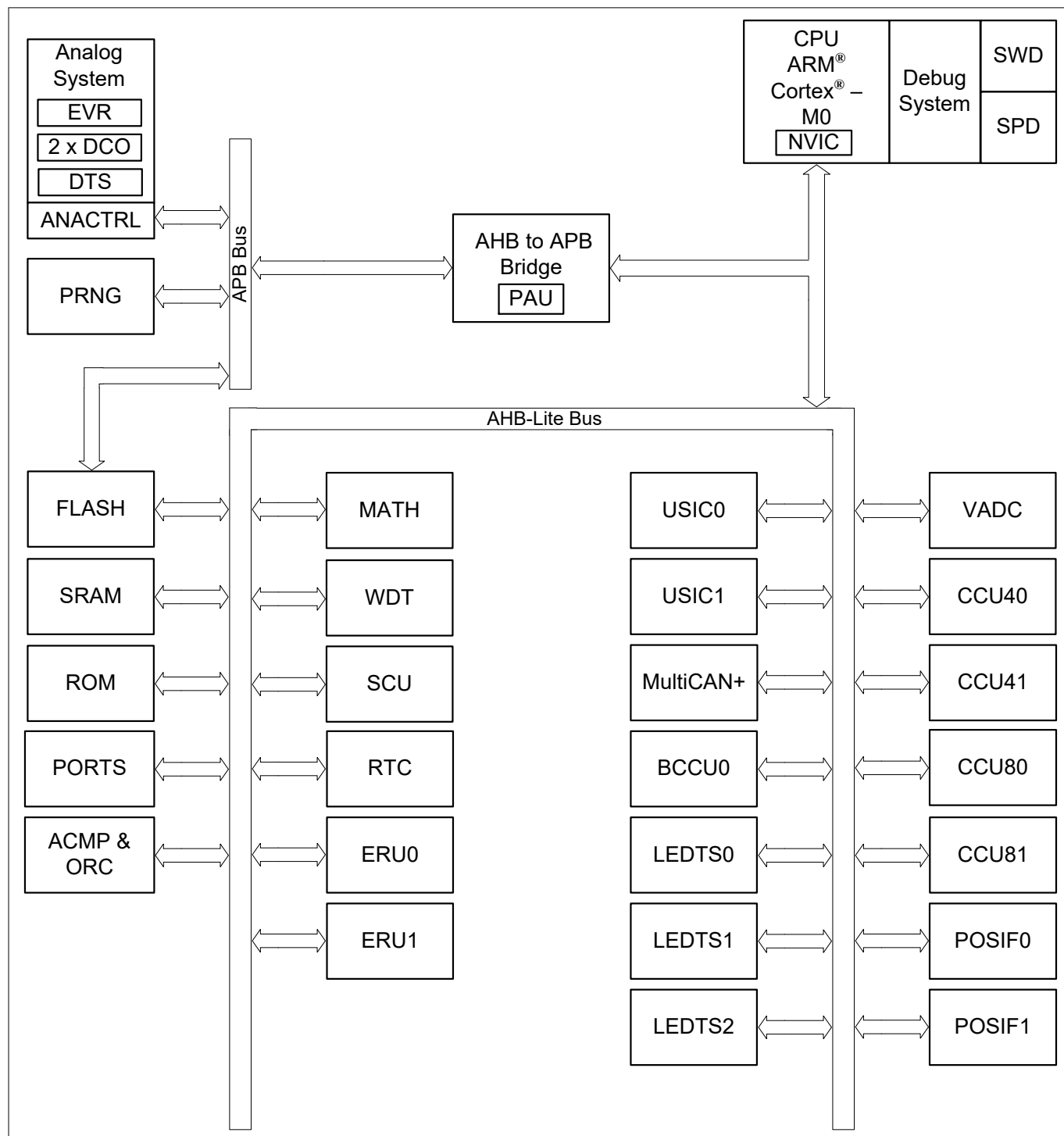


Figure 1 **Block Diagram**

1 Summary of Features

CPU Subsystem

- 32-bit ARM Cortex-M0 CPU Core
 - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller (NVIC)
- 64 interrupt nodes
- MATH coprocessor
 - 24-bit trigonometric calculation (CORDIC)
 - 32-bit divide operation
- 2x4 channels ERU for event interconnections

On-Chip Memories

- 8 kbytes ROM
- 16 kbytes SRAM (with parity)
- up to 200 kbytes Flash (with ECC)

Supply, Reset and Clock

- 1.8 V to 5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Internal slow and fast oscillators without the need of PLL

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
 - UART (up to 12 Mb/s)
 - single-SPI (up to 12 Mb/s)
 - double-SPI (up to 2×12 Mb/s)
 - quad-SPI (up to 4×12 Mb/s)
 - IIC (up to 400 kb/s)
 - IIS (up to 12 Mb/s)
 - LIN interfaces (20 kb/s)
- LEDTS in Human-Machine interface
 - up to 24 touch pads
 - drive up to 144 LEDs
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)

Analog Frontend Peripherals

- A/D Converters (up to 12 analog inputs)
 - 2 sample and hold stages
 - fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
 - 0 V to 5.5 V input range

1 Summary of Features

- Up to 8 channels out of range comparators
- Up to 4 fast analog comparators
- Temperature Sensor (TSE)

Industrial Control Peripherals

- 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and multi phase control
- 2x POSIF for hall and quadrature encoders, motor positioning
- 9 channel BCCU (brightness and color control) for LED lighting applications

Up to 56 Input/Output Ports

- 1.8 V to 5.5 V capable
- up to 8 high current pads (50 mA sink)

On-Chip Debug Support

- 4 breakpoints, 2 watchpoints
- ARM serial wire debug, single-pin debug interfaces

Programming Support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 ($9.7 \times 6.4 \text{ mm}^2$)
- VQFN-40/48/64 ($5 \times 5/7 \times 7/8 \times 8 \text{ mm}^2$)
- LQFP-48/64 ($7 \times 7/12 \times 12 \text{ mm}^2$)

Tools

- Free ModusToolbox™ toolchain with low-level drivers and apps

1.1 Device Overview

The following table lists the available features per device type for the XMCl400 series.

Table 1 Features of XMCl400 Device Types¹⁾

Features		XMC 1401 -T03 8	XMC 1401 -Q04 8	XMC 1401 -F04 8	XMC 1401 -F06 4	XMC 1402 -T03 8	XMC 1402 -Q04 0	XMC 1402 -Q04 8	XMC 1402 -Q06 4	XMC 1402 -F04 8	XMC 1402 -F06 4	XMC 1403 -Q04 0	XMC 1403 -Q04 8	XMC 1403 -Q06 4	XMC 1404 -Q04 0	XMC 1404 -Q04 8	XMC 1404 -Q06 4	XMC 1404 -F04 8	XMC 1404 -F06 4
CPU frequency		48 MHz																	
Operating temperature (ambient)		-40 to 105° C	-40 to 85° C	-40 to 105° C	-40 to 85° C	-40 to 105°C													
Operating voltage		1.8 V to 5.5 V																	
Flash options (Kbytes)		64, 128, 200	64, 128, 64, 128	32, 64, 128, 200	64, 128, 64, 128	32, 64, 128, 200			64, 128, 200	32, 64, 128, 200	64, 128, 200								
SRAM (Kbytes)		16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
MATH		–	–	-	–	1	1	1	1	1	1	–	–	–	1	1	1	1	1
Industrial Control	CCU4	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	CCU8	–	–	-	–	2	2	2	2	2	2	–	–	–	2	2	2	2	2
	POSIF	–	–	-	–	1	1	2	2	2	2	–	–	–	1	2	2	2	2
	BCCU	–	–	-	–	1	1	1	1	1	1	–	–	–	1	1	1	1	1

(table continues...)

Table 1 (continued) Features of XMC1400 Device Types¹⁾

Features		XMC 1401 -T03 8	XMC 1401 -Q04 8	XMC 1401 -F04 8	XMC 1401 -F06 4	XMC 1402 -T03 8	XMC 1402 -Q04 0	XMC 1402 -Q04 8	XMC 1402 -Q06 4	XMC 1402 -F04 8	XMC 1402 -F06 4	XMC 1403 -Q04 0	XMC 1403 -Q04 8	XMC 1403 -Q06 4	XMC 1404 -Q04 0	XMC 1404 -Q04 8	XMC 1404 -Q06 4	XMC 1404 -F04 8	XMC 1404 -F06 4
Communication	USIC (modules/channels)	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4
	LEDTS	3	3	3	3	–	–	–	–	–	–	–	–	–	2	3	3	3	3
	MultiCAN+ (nodes/MOs)	–	–	–	–	–	–	–	–	–	–	2/32	2/32	2/32	2/32	2/32	2/32	2/32	2/32
Analog	ADC (kernels/analog inputs)	2/12	2/12	2/14	2/12	2/12	2/12	2/12	2/12	2/14	2/12	2/12	2/12	2/12	2/12	2/12	2/12	2/14	2/12
	ACMP	–	–	–	–	3	3	4	4	4	4	–	–	–	3	4	4	4	4
GPIOs		26	34	35	48	26	27	34	48	35	48	27	34	48	27	34	48	35	48
GPIs		8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
Packages		TSSOP-38	VQFN-48	LQFP-48	LQFP-64	TSSOP-38	VQFN-40	VQFN-48	VQFN-64	LQFP-48	LQFP-64	VQFN-40	VQFN-48	VQFN-64	VQFN-40	VQFN-48	VQFN-64	LQFP-48	LQFP-64

1) Features that are not included in this table are available in all the derivatives.

1 Summary of Features

1.2 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
 - F: LQFP
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size in Kbytes

For ordering codes for the XMC1400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1400 series, some descriptions may not apply to a specific product. Please see [Table 2](#).

For simplicity the term **XMC1400** is used for all derivatives throughout this document.

1.3 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 2 Synopsis of XMC1400 Device Types

Derivative	Package	Flash Kbytes
XMC1401-T038X0064	PG-TSSOP-38	64
XMC1401-T038X0128	PG-TSSOP-38	128
XMC1401-T038X0200	PG-TSSOP-38	200
XMC1401-Q048F0064	PG-VQFN-48	64
XMC1401-Q048F0128	PG-VQFN-48	128
XMC1401-F048X0032	PG-LQFP-48	32
XMC1401-F048X0064	PG-LQFP-48	64
XMC1401-F048X0128	PG-LQFP-48	128
XMC1401-F048X0200	PG-LQFP-48	200
XMC1401-F064F0064	PG-LQFP-64	64
XMC1401-F064F0128	PG-LQFP-64	128
XMC1402-T038X0032	PG-TSSOP-38	32
XMC1402-T038X0064	PG-TSSOP-38	64
XMC1402-T038X0128	PG-TSSOP-38	128
XMC1402-T038X0200	PG-TSSOP-38	200
XMC1402-Q040X0032	PG-VQFN-40	32

(table continues...)

1 Summary of Features

Table 2 (continued) Synopsis of XMC1400 Device Types

Derivative	Package	Flash Kbytes
XMC1402-Q040X0064	PG-VQFN-40	64
XMC1402-Q040X0128	PG-VQFN-40	128
XMC1402-Q040X0200	PG-VQFN-40	200
XMC1402-Q048X0032	PG-VQFN-48	32
XMC1402-Q048X0064	PG-VQFN-48	64
XMC1402-Q048X0128	PG-VQFN-48	128
XMC1402-Q048X0200	PG-VQFN-48	200
XMC1402-Q064X0064	PG-VQFN-64	64
XMC1402-Q064X0128	PG-VQFN-64	128
XMC1402-Q064X0200	PG-VQFN-64	200
XMC1402-F048X0032	PG-LQFP-48	32
XMC1402-F048X0064	PG-LQFP-48	64
XMC1402-F048X0128	PG-LQFP-48	128
XMC1402-F048X0200	PG-LQFP-48	200
XMC1402-F064X0064	PG-LQFP-64	64
XMC1402-F064X0128	PG-LQFP-64	128
XMC1402-F064X0200	PG-LQFP-64	200
XMC1403-Q040X0064	PG-VQFN-40	64
XMC1403-Q040X0128	PG-VQFN-40	128
XMC1403-Q040X0200	PG-VQFN-40	200
XMC1403-Q048X0064	PG-VQFN-48	64
XMC1403-Q048X0128	PG-VQFN-48	128
XMC1403-Q048X0200	PG-VQFN-48	200
XMC1403-Q064X0064	PG-VQFN-64	64
XMC1403-Q064X0128	PG-VQFN-64	128
XMC1403-Q064X0200	PG-VQFN-64	200
XMC1404-Q040X0064	PG-VQFN-40	64
XMC1404-Q040X0128	PG-VQFN-40	128
XMC1404-Q040X0200	PG-VQFN-40	200
XMC1404-Q048X0064	PG-VQFN-48	64
XMC1404-Q048X0128	PG-VQFN-48	128
XMC1404-Q048X0200	PG-VQFN-48	200
XMC1404-Q064X0064	PG-VQFN-64	64

(table continues...)

1 Summary of Features

Table 2 (continued) **Synopsis of XMC1400 Device Types**

Derivative	Package	Flash Kbytes
XMC1404-Q064X0128	PG-VQFN-64	128
XMC1404-Q064X0200	PG-VQFN-64	200
XMC1404-F048X0064	PG-LQFP-48	64
XMC1404-F048X0128	PG-LQFP-48	128
XMC1404-F048X0200	PG-LQFP-48	200
XMC1404-F064X0064	PG-LQFP-64	64
XMC1404-F064X0128	PG-LQFP-64	128
XMC1404-F064X0200	PG-LQFP-64	200

1 Summary of Features

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location: 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-T038X0064	00014013 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 FFFFFFFF _H	AA
XMC1401-T038X0128	00014013 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 FFFFFFFF _H	AA
XMC1401-T038X0200	00014013 07CF00FF 1E071FF7 20006000 00000D00 00001000 00033000 FFFFFFFF _H	AA
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1401-F048X0032	000140B3 07CF00FF 1E071FF7 20006000 00000D00 00001000 00009000 CODE1705 _H	AA
XMC1401-F048X0064	000140B3 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 CODE1705 _H	AA
XMC1401-F048X0128	000140B3 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 CODE1705 _H	AA
XMC1401-F048X0200	000140B3 07CF00FF 1E071FF7 20006000 00000D00 00001000 00033000 CODE1705 _H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083 _H	AA

(table continues...)

1 Summary of Features

Table 3 (continued) XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-Q048X0064	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q048X0128	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q048X0200	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q064X0064	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q064X0128	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q064X0200	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-F048X0032	000140B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 CODE1705 _H	AA
XMC1402-F048X0064	000140B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 CODE1705 _H	AA
XMC1402-F048X0128	000140B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 CODE1705 _H	AA
XMC1402-F048X0200	000140B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 CODE1705 _H	AA
XMC1402-F064X0064	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-F064X0128	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-F064X0200	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q040X0064	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA

(table continues...)

1 Summary of Features

Table 3 (continued) XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1403-Q040X0128	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA
XMC1403-Q040X0200	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q048X0064	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA
XMC1403-Q048X0128	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA
XMC1403-Q048X0200	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q064X0064	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA
XMC1403-Q064X0128	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA
XMC1403-Q064X0200	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q040X0064	00014043 07FF00FF 1E071FF7 00BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q040X0128	00014043 07FF00FF 1E071FF7 00BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q040X0200	00014043 07FF00FF 1E071FF7 00BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q048X0064	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q048X0128	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q048X0200	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q064X0064	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q064X0128	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q064X0200	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-F048X0064	000140B3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 CODE1705 _H	AA

(table continues...)

1 Summary of Features

Table 3 (continued) XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1404-F048X0128	000140B3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 CODE1705 _H	AA
XMC1404-F048X0200	000140B3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 CODE1705 _H	AA
XMC1404-F064X0064	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-F064X0128	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-F064X0200	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

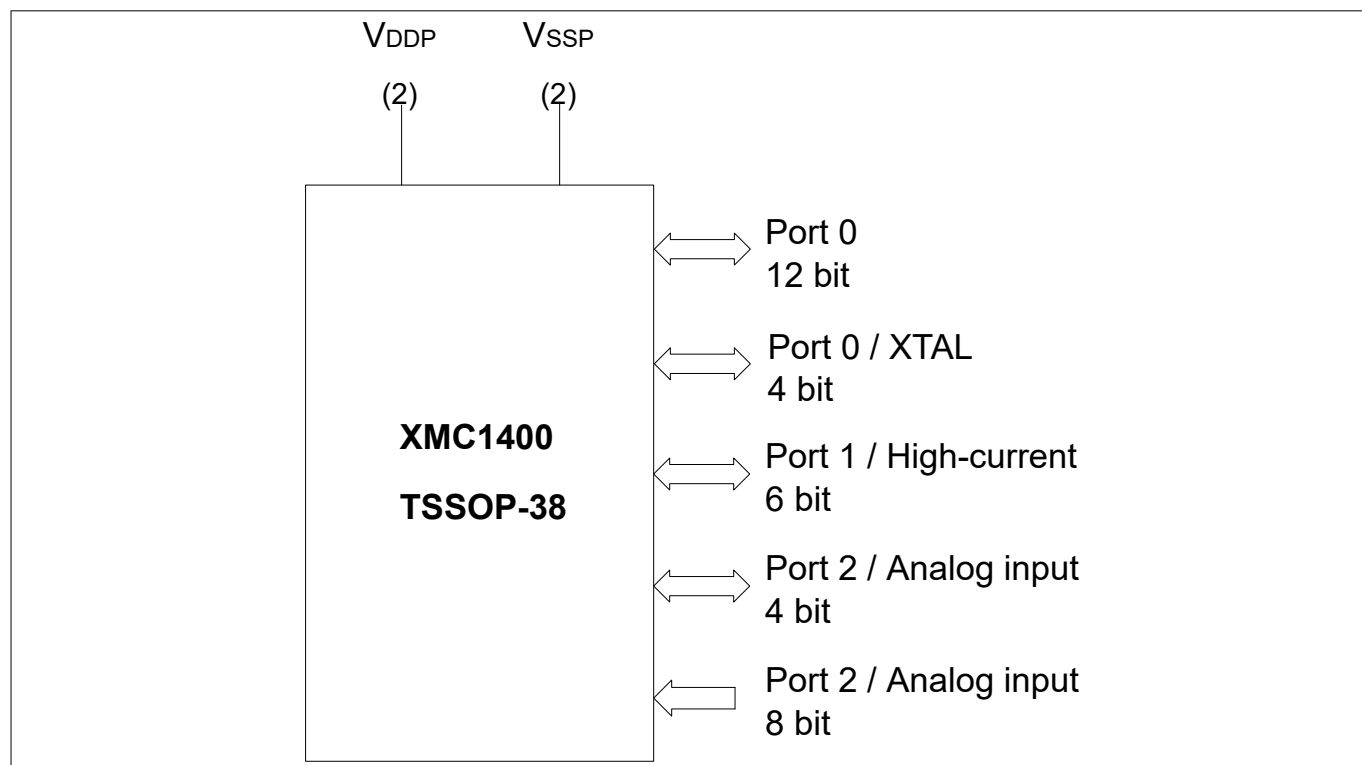


Figure 2 XMC1400 Logic Symbol for TSSOP-38-9

2 General Device Information

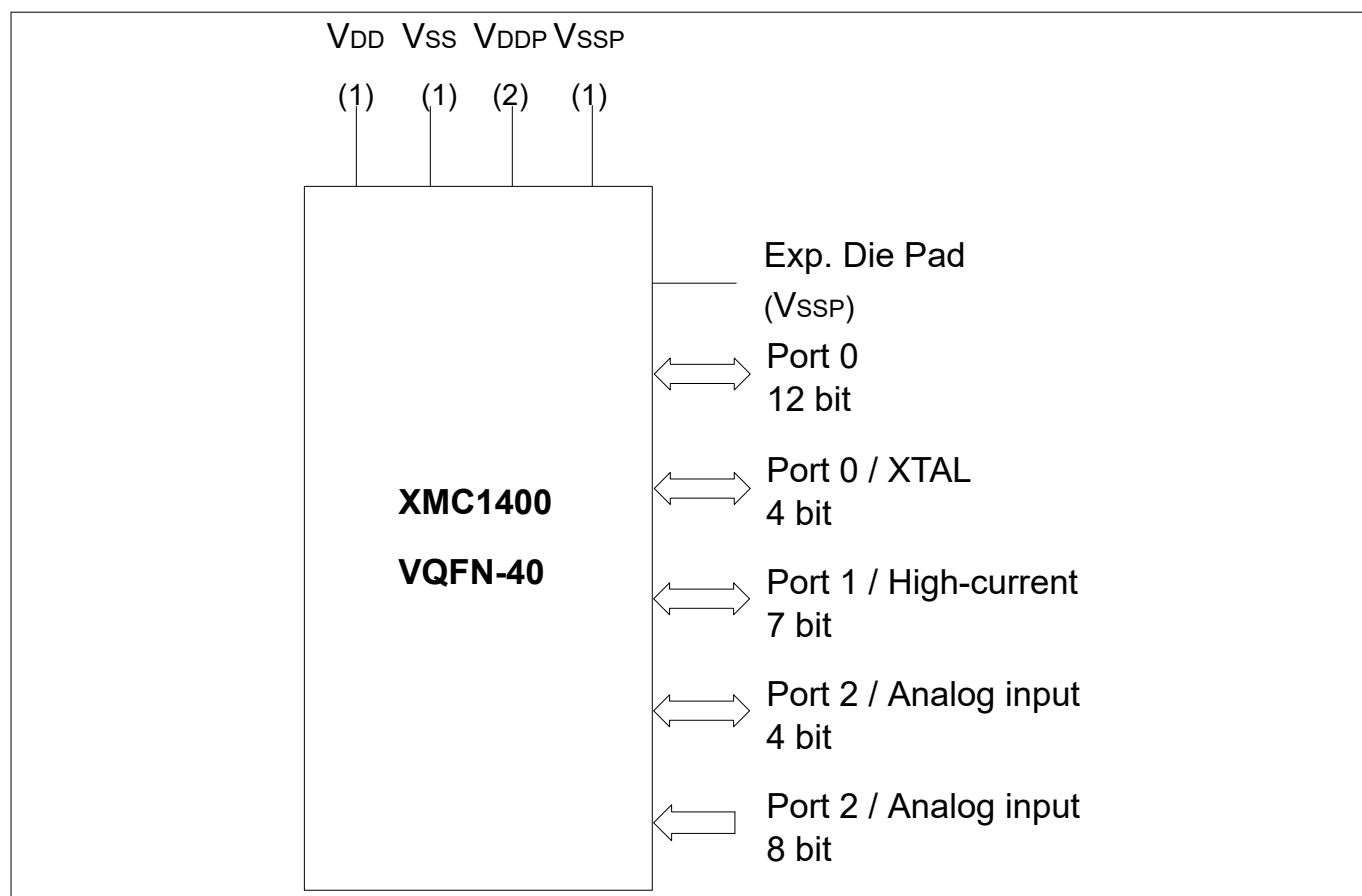


Figure 3 XMC1400 Logic Symbol for PG-VQFN-40-17

2 General Device Information

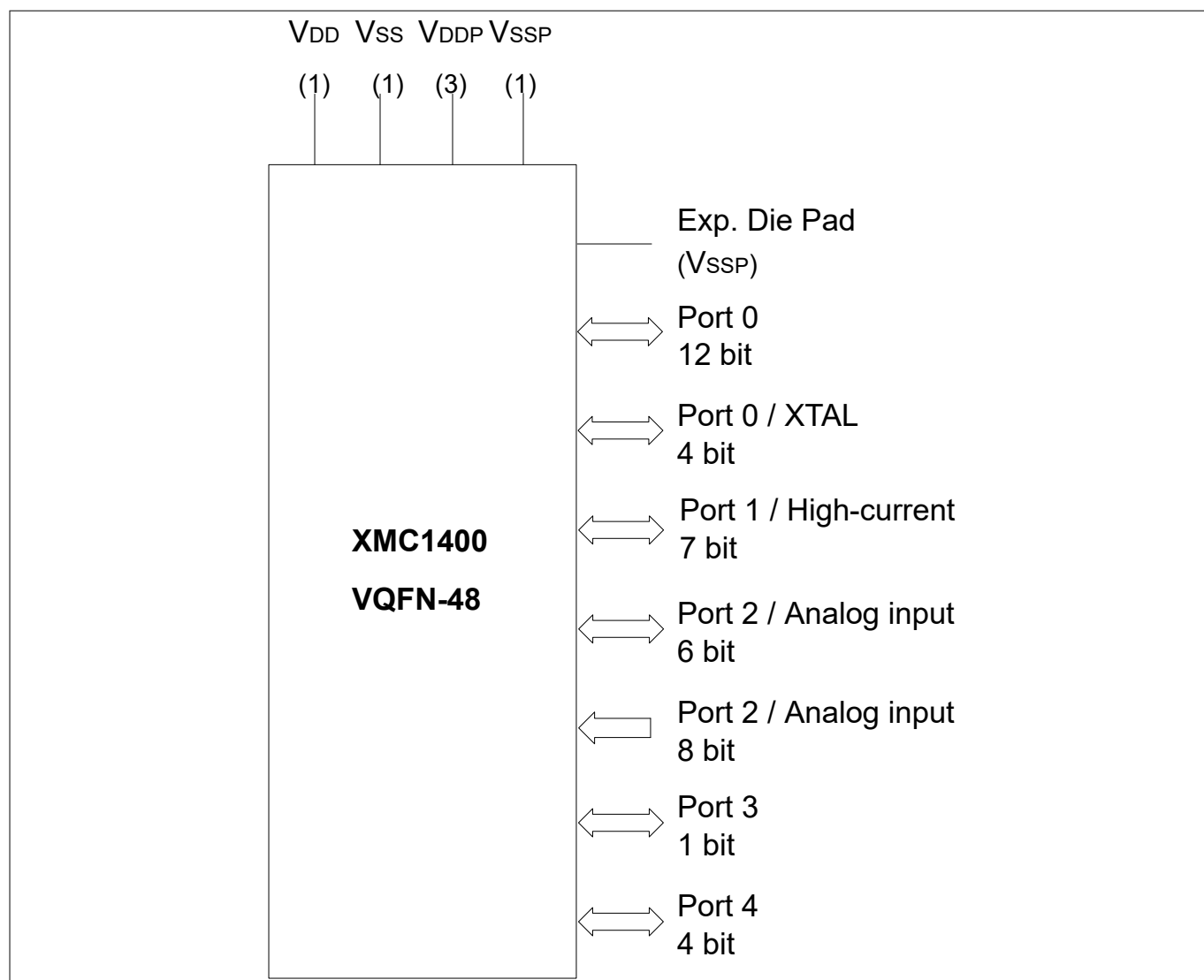


Figure 4 **XMC1400 Logic Symbol for PG-VQFN-48-73**

2 General Device Information

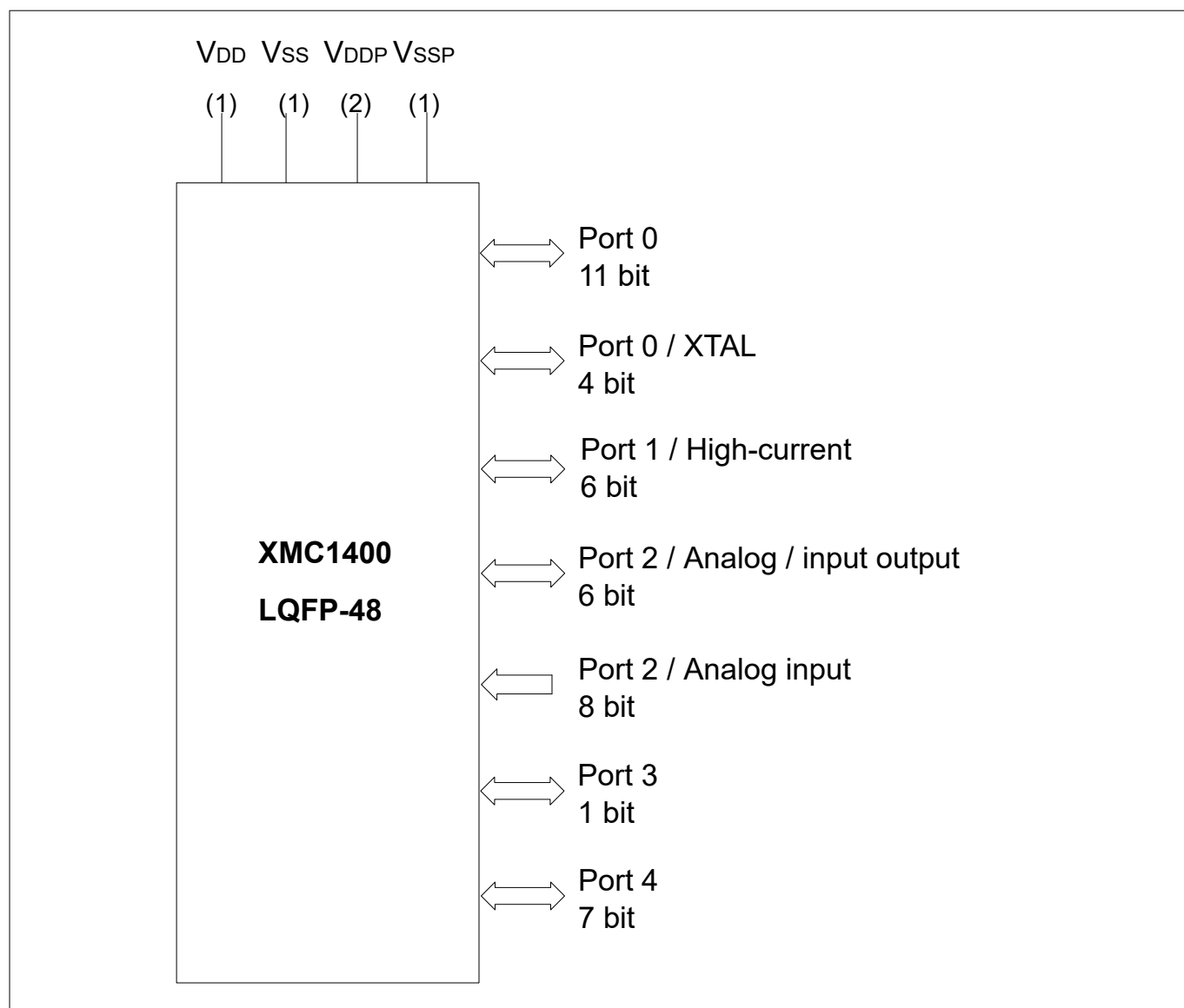


Figure 5 XMC1400 Logic Symbol for PG-LQFP-48-10

2 General Device Information

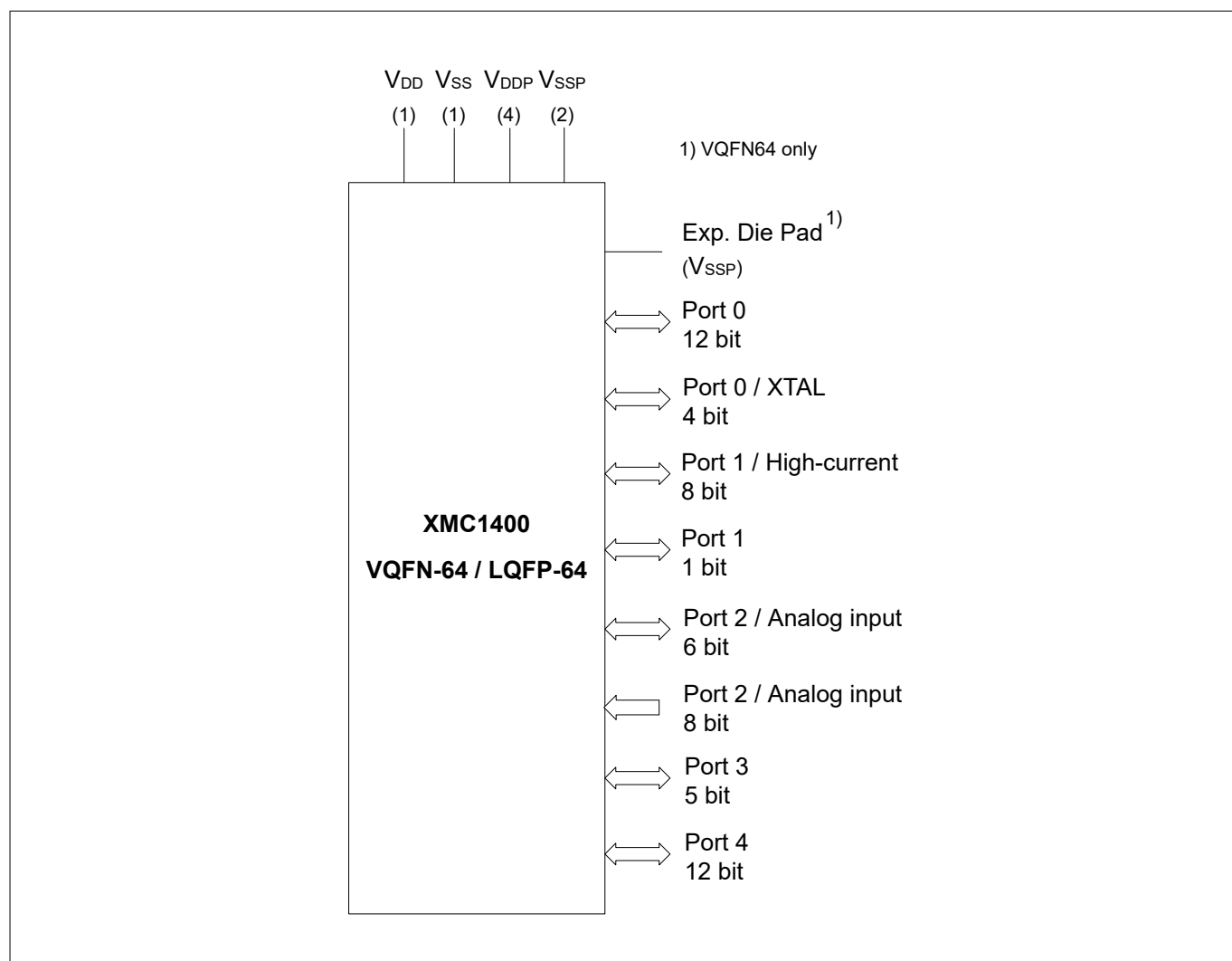


Figure 6 XMC1400 Logic Symbol for PG-LQFP-64-26/PG-VQFN-64-6

2 General Device Information

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

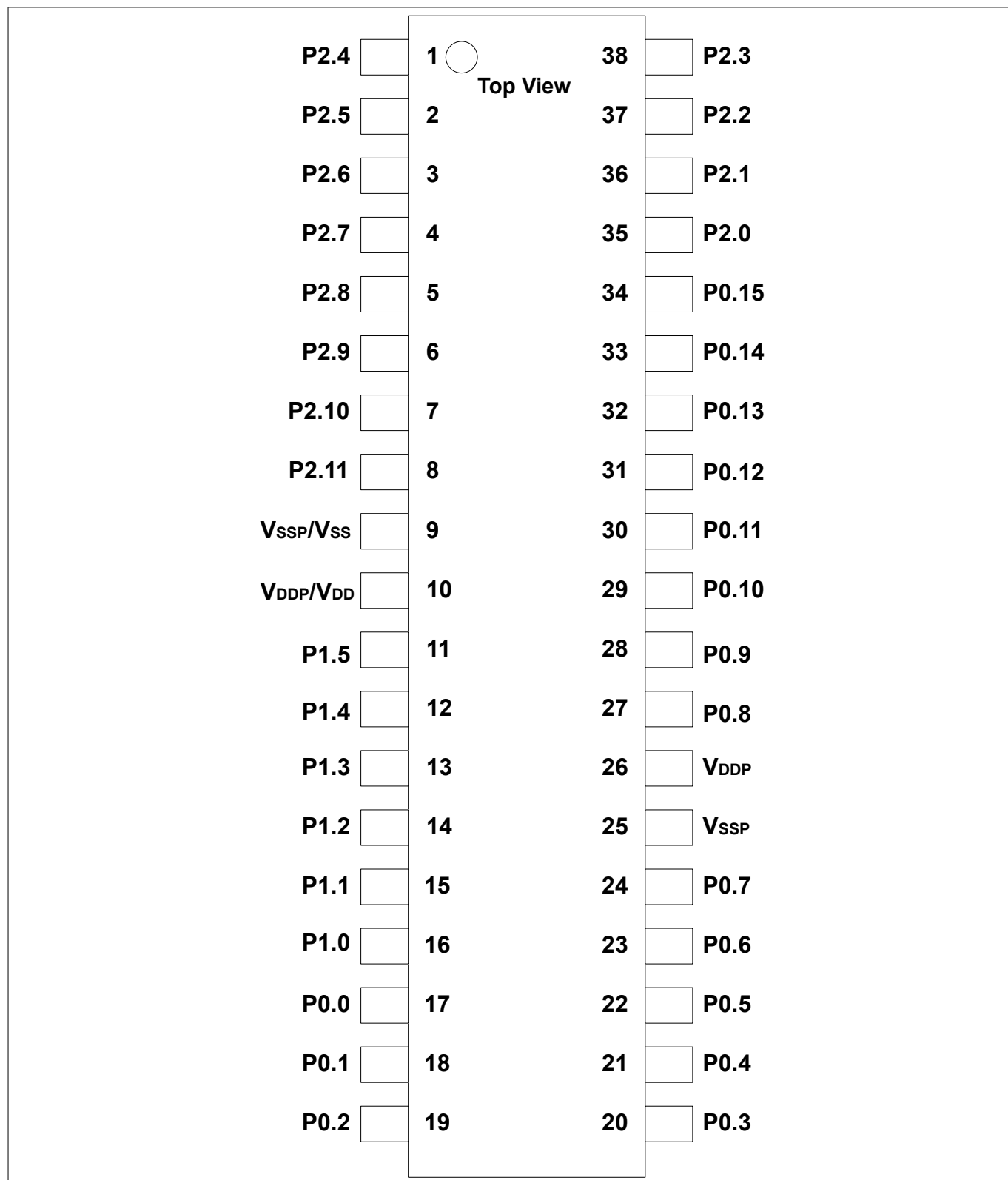


Figure 7 XMC1400 PG-TSSOP-38-9 Pin Configuration (top view)

2 General Device Information

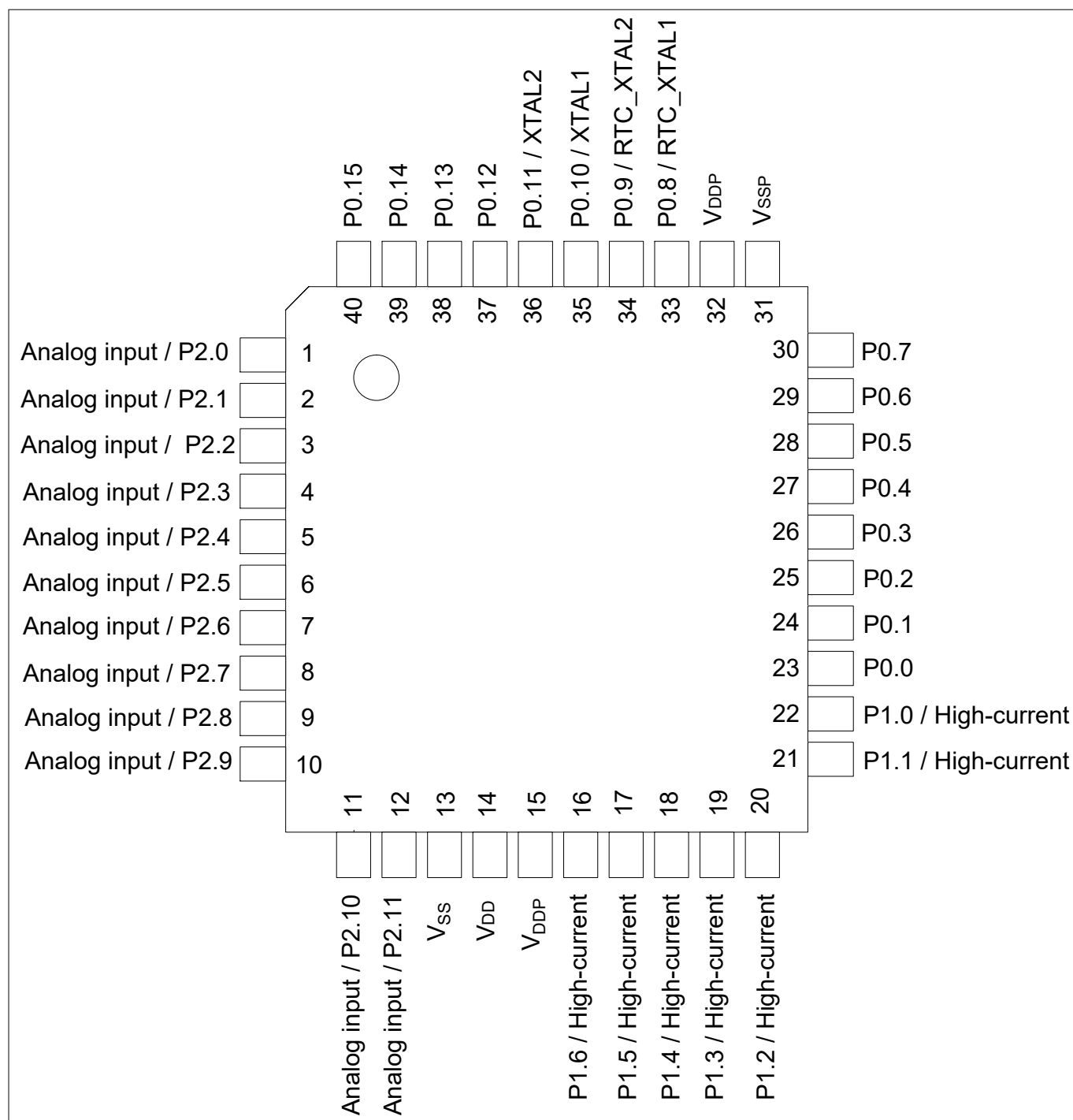


Figure 8 XMC1400 PG-VQFN-40-17 Pin Configuration (top view)

2 General Device Information

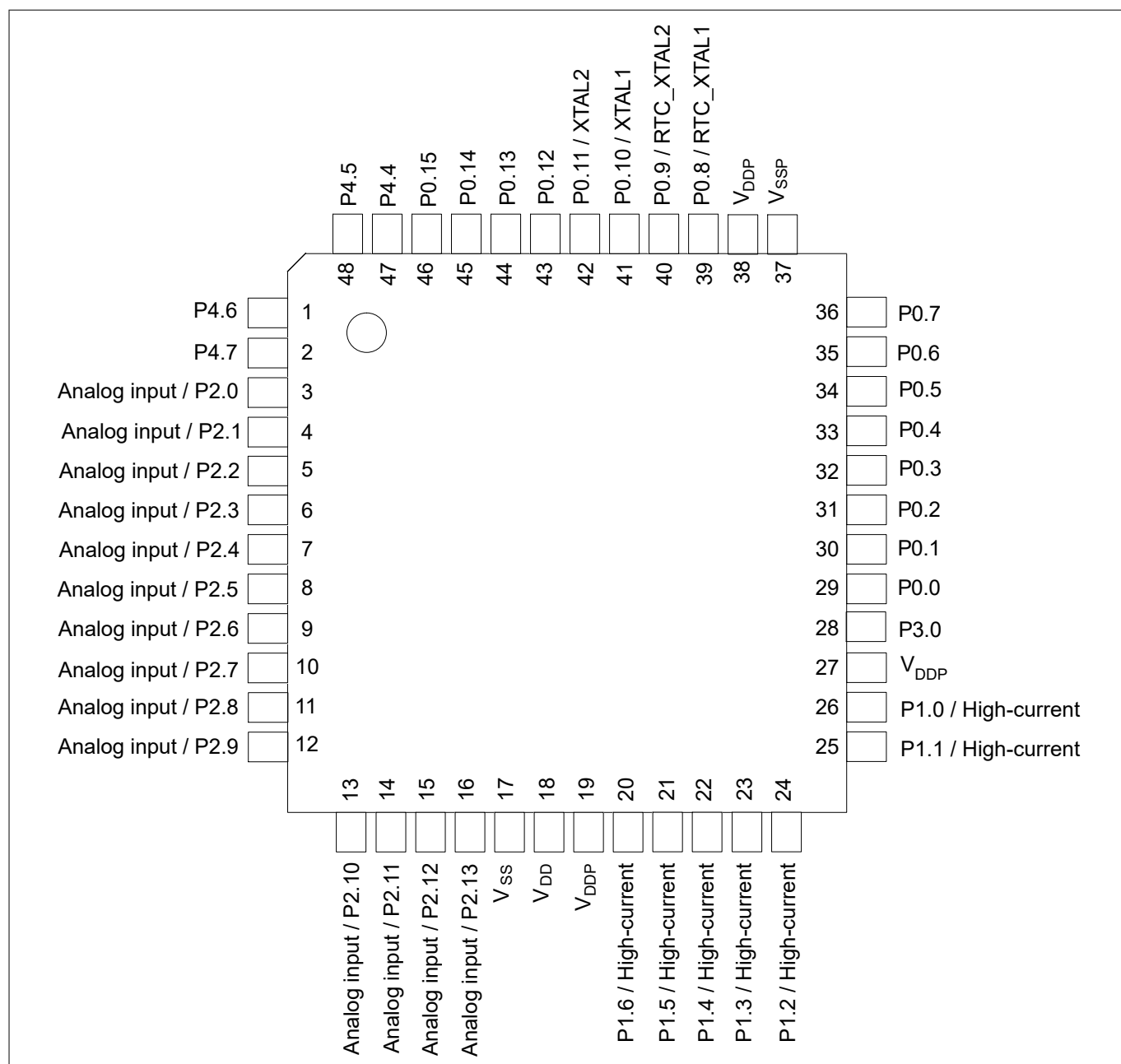


Figure 9 XMC1400 PG-VQFN-48-73 Pin Configuration (top view)

2 General Device Information

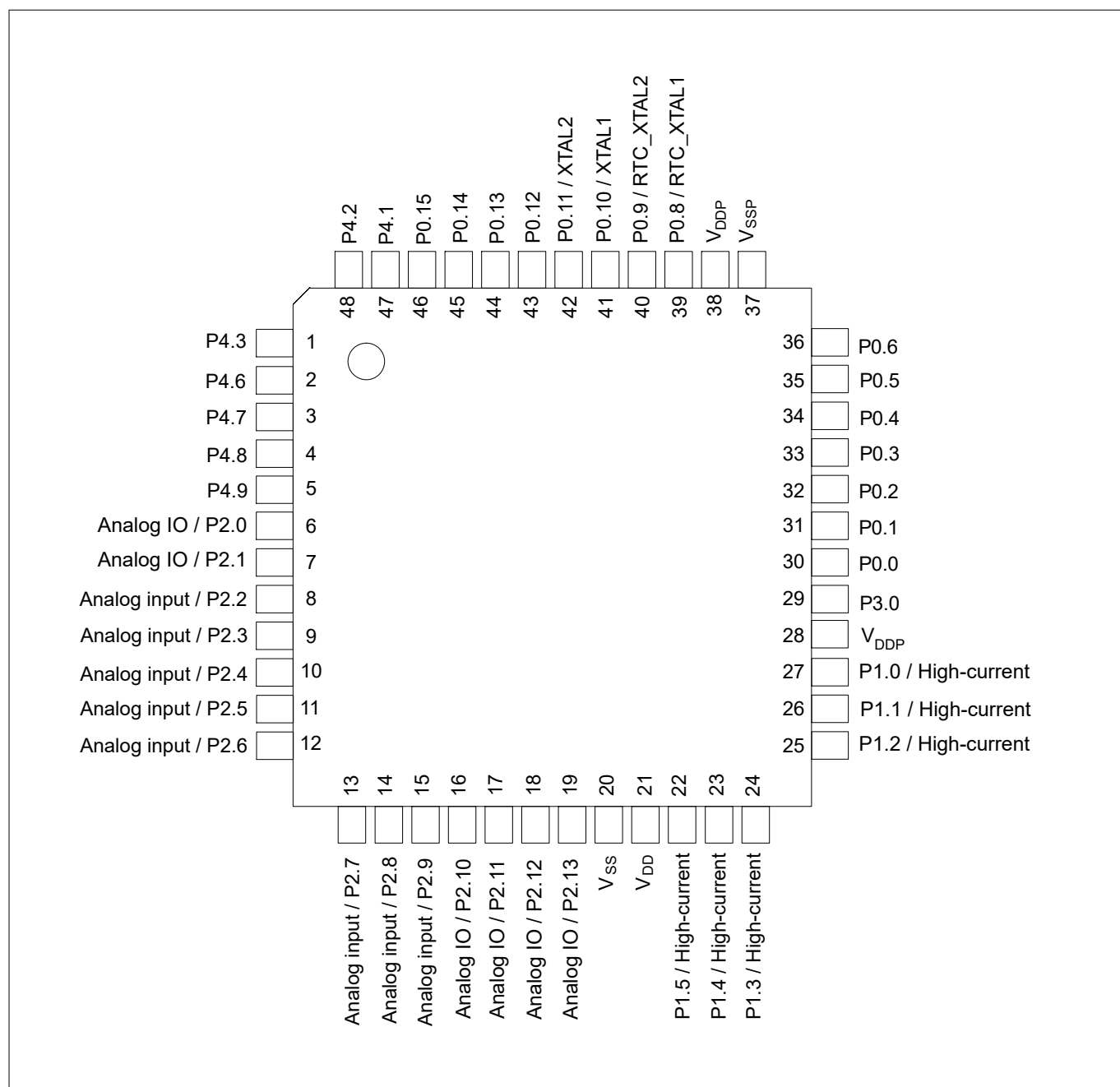


Figure 10 XMC1400 PG-LQFP-48-10 Pin Configuration (top view)

2 General Device Information

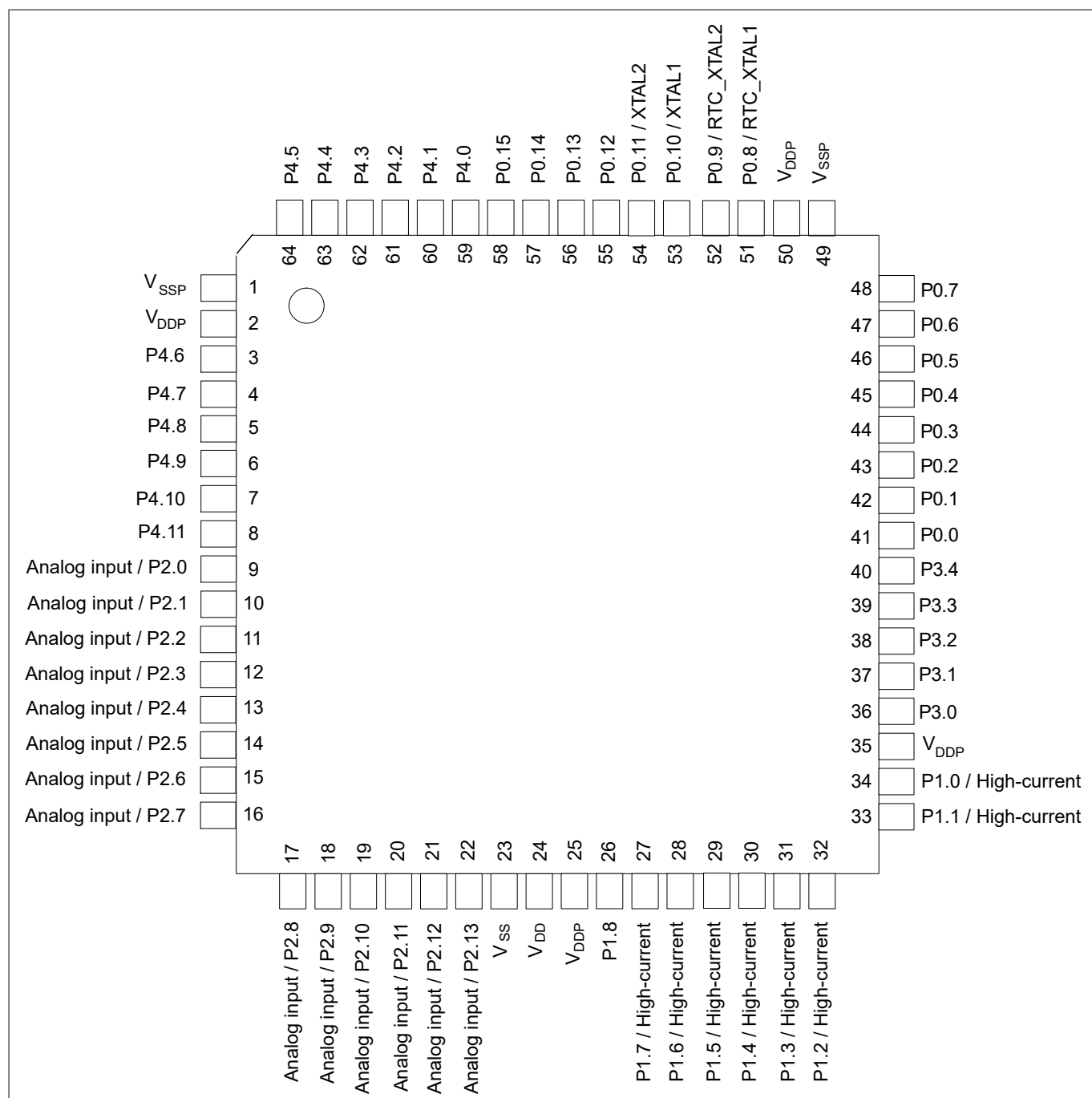


Figure 11 XMC1400 PG-LQFP-64-26/PG-VQFN-64-6 Pin Configuration (top view)

2 General Device Information

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters chapter.

Table 5 Package Pin Mapping

Function	LQFP 64, VQFN 64	LQFP 48	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.0	41	30	29	23	17	STD_INOUT	
P0.1	42	31	30	24	18	STD_INOUT	
P0.2	43	32	31	25	19	STD_INOUT	
P0.3	44	33	32	26	20	STD_INOUT	
P0.4	45	34	33	27	21	STD_INOUT	
P0.5	46	35	34	28	22	STD_INOUT	
P0.6	47	36	35	29	23	STD_INOUT	
P0.7	48	-	36	30	24	STD_INOUT	
P0.8/ RTC_ XTAL1	51	39	39	33	27	STD_INOUT/clock_IN	

(table continues...)

2 General Device Information

Table 5 (continued) Package Pin Mapping

Function	LQFP 64, VQFN 64	LQFP 48	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.9/ RTC_ XTAL2	52	40	40	34	28	STD_INOU T/clock_O	
P0.10/ XTAL1	53	41	41	35	29	STD_INOU T/clock_IN	
P0.11/ XTAL2	54	42	42	36	30	STD_INOU T/clock_O	
P0.12	55	43	43	37	31	STD_INOU T	
P0.13	56	44	44	38	32	STD_INOU T	
P0.14	57	45	45	39	33	STD_INOU T	
P0.15	58	46	46	40	34	STD_INOU T	
P1.0	34	27	26	22	16	High Current	
P1.1	33	26	25	21	15	High Current	
P1.2	32	25	24	20	14	High Current	
P1.3	31	24	23	19	13	High Current	
P1.4	30	23	22	18	12	High Current	
P1.5	29	22	21	17	11	High Current	
P1.6	28	-	20	16	-	High Current	
P1.7	27	-	-	-	-	High Current	
P1.8	26	-	-	-	-	STD_INOU T	
P2.0	9	6	3	1	35	STD_INOU T/AN	
P2.1	10	7	4	2	36	STD_INOU T/AN	
P2.2	11	8	5	3	37	STD_IN/AN	

(table continues...)

2 General Device Information

Table 5 (continued) Package Pin Mapping

Function	LQFP 64, VQFN 64	LQFP 48	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P2.3	12	9	6	4	38	STD_IN/AN	
P2.4	13	10	7	5	1	STD_IN/AN	
P2.5	14	11	8	6	2	STD_IN/AN	
P2.6	15	12	9	7	3	STD_IN/AN	
P2.7	16	13	10	8	4	STD_IN/AN	
P2.8	17	14	11	9	5	STD_IN/AN	
P2.9	18	15	12	10	6	STD_IN/AN	
P2.10	19	16	13	11	7	STD_INOU T/AN	
P2.11	20	17	14	12	8	STD_INOU T/AN	
P2.12	21	18	15	–	–	STD_INOU T/AN	
P2.13	22	19	16	–	–	STD_INOU T/AN	
P3.0	36	29	28	–	–	STD_INOU T	
P3.1	37	–	–	–	–	STD_INOU T	
P3.2	38	–	–	–	–	STD_INOU T	
P3.3	39	–	–	–	–	STD_INOU T	
P3.4	40	–	–	–	–	STD_INOU T	
P4.0	59	–	–	–	–	STD_INOU T	
P4.1	60	47	–	–	–	STD_INOU T	
P4.2	61	48	–	–	–	STD_INOU T	
P4.3	62	1	–	–	–	STD_INOU T	
P4.4	63	–	47	–	–	STD_INOU T	
P4.5	64	–	48	–	–	STD_INOU T	

(table continues...)

2 General Device Information

Table 5 (continued) Package Pin Mapping

Function	LQFP 64, VQFN 64	LQFP 48	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P4.6	3	2	1	–	–	STD_INOUT	
P4.7	4	3	2	–	–	STD_INOUT	
P4.8	5	4	–	–	–	STD_INOUT	
P4.9	6	5	–	–	–	STD_INOUT	
P4.10	7	–	–	–	–	STD_INOUT	
P4.11	8	–	–	–	–	STD_INOUT	
VSS	23	20	17	13	9	Power	Supply GND, ADC reference GND
VDD	24	21	18	14	10	Power	Supply VDD, ADC reference voltage/ORC reference voltage
VDDP	25	28	19	15	10	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VDDP	2	–	–	–	–	Power	I/O port supply
VDDP	35	–	27	–	–	Power	I/O port supply
VDDP	50	38	38	32	26	Power	I/O port supply
VSSP	1	–	–	–	–	Power	I/O port ground
VSSP	49	37	37	31	25	Power	I/O port ground
VSSP	Exp. Pad (in VQFN 64 only)	–	Exp. Pad	Exp. Pad	–	Power	Exposed Die Pad The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2 General Device Information

2.2.2 Port Pin for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. [Table 6](#) shows the port pins used for the various boot modes.

Table 6 Port Pin for Boot Modes

Pin	Boot	Boot Description
P0.13	CS(O)	SSC BSL mode
P0.14	SWDIO_0	Debug mode (SWD)
	SPD_0	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
	SCLK(O)	SSC BSL mode
P0.15	SWDCLK_0	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
	DATA(I/O)	SSC BSL mode
P1.2	SWDCLK_1	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
P1.3	SWDIO_1	Debug mode (SWD)
	SPD_1	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
P4.6	HWCON0	Boot Pins (Boot from pins mode must be selected)
P4.7	HWCON1	

2.2.3 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

2 General Device Information

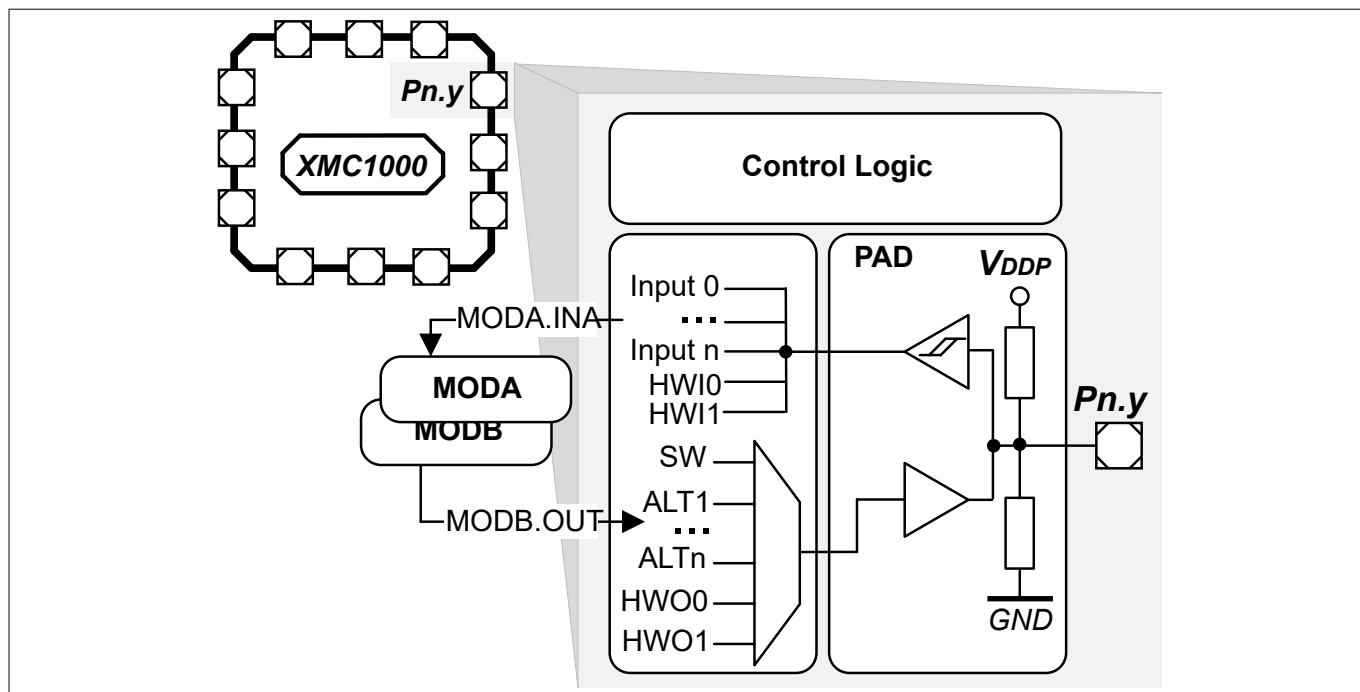


Figure 12 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to [Table 9](#) for the complete Port I/O function mapping.

2.2.4 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HWO_PD	HWO_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrides settings in the respective port pin registers. Additional hardware signals HWO_PD/HWI_PD and HWO_PU/HWI_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to [Table 10](#) for the complete hardware I/O and pull control function mapping.

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU 0.P DO UT0	LED TS0 .LIN E7	ERU 0.G OUT 0	CCU 40. OUT 0	CCU 80. OUT 00	USI C0_ CH0 .SE LO0	USI C0_ CH1 .SE LO0	CCU 81. OUT 00	USI C1_ CH1 .DO UT0	BCC U0. TRAP IN B	CCU4 0.I N0AC					USIC 1_ CH1. DX 0A	USIC 0_ CH0. D X2A		USIC 0_ CH1. DX 2A		
P0.1	ERU 0.P DO UT1	LED TS0 .LIN E6	ERU 0.G OUT 1	CCU 40. OUT 1	CCU 80. OUT 01	BCC U0. OUT 8	SCU .VD ROP	USI C1_ CH1 .SC LKO UT	USI C1_ CH1 .DO UT0		CCU4 0.I N1AC					USIC 1_ CH1. DX 0B	USIC 1_ CH1. D X1A				
P0.2	ERU 0.P DO UT2	LED TS0 .LIN E5	ERU 0.G OUT 2	CCU 40. OUT 2	CCU 80. OUT 02	VAD C0. EM UX0 2	CCU 80. OUT 10	USI C1_ CH0 .SC LKO UT	USI C1_ CH0 .DO UT0		CCU4 0.I N2AC					USIC 1_ CH0. DX 0A	USIC 1_ CH0. D X1A				
P0.3	ERU 0.P DO UT3	LED TS0 .LIN E4	ERU 0.G OUT 3	CCU 40. OUT 3	CCU 80. OUT 03	VAD C0. EM UX0 1	CCU 80. OUT 11	USI C1_ CH1 .SC LKO UT	USI C1_ CH0 .DO UT0		CCU4 0.I N3AC					USIC 1_ CH0. DX 0B					

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.4	BCC U0. OUT 0	LED TS0 .LIN E3	LED TS0 .CO L3	CCU 40. OUT 1	CCU 80. OUT 13	VAD C0. EM UX0 0	WW DT. SER VIC E_O UT	USI C1_ CH1 .SE LOO	CAN .N0 _TX D			CCU4 1.I N0AB	CCU8 0.I N0AB							CAN. N0 _RXD A	
P0.5	BCC U0. OUT 1	LED TS0 .LIN E2	LED TS0 .CO L2	CCU 40. OUT 0	CCU 80. OUT 12	ACM P2. OUT	CCU 80. OUT 01	VAD C0. EM UX1 0_T XD	CAN .N0			CCU4 1.I N1AB	CCU8 0.I N1AB							CAN. N0 _RXD B	
P0.6	BCC U0. OUT 2	LED TS0 .LIN E1	LED TS0 .CO L1	CCU 40. OUT 0	CCU 80. OUT 11	USI C0_ CH1 .MC LKO UT	USI C0_ CH1 .DO UT0	VAD C0. EM UX1 1	CCU 41. OUT 0		CCU4 0.I N0AB	CCU4 1.I N2AB						USIC 0_ CH1. DX 0C			
P0.7	BCC U0. OUT 3	LED TS0 .LIN E0	LED TS0 .CO L0	CCU 40. OUT 1	CCU 80. OUT 10	USI C0_ CH0 .SC LKO UT	USI C0_ CH1 .DO UT0	VAD C0. EM UX1 2	CCU 41. OUT 1		CCU4 0.I N1AB	CCU4 1.I N3AB					USIC 0_ CH0. D X1C	USIC 0_ CH1. DX 0D	USIC 0_ CH1. DX 1C		

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.8 / RTC_XTAL1	BCC U0. OUT 4	LED TS1 .LIN E0	LED TS0 .CO LA	CCU 40. OUT 2	CCU 80. OUT 20	USI CO_ CH0 .SC LKO UT	USI CO_ CH1 .SC LKO UT	CCU 81. OUT 20	CCU 41. OUT 2		CCU4 0.I N2AB						USIC 0_ CH0. D X1B		USIC 0_ CH1. DX 1B		
P0.9 / RTC_XTAL2	BCC U0. OUT 5	LED TS1 .LIN E1	LED TS0 .CO L6	CCU 40. OUT 3	CCU 80. OUT 21	USI CO_ CH0 .SE LO0	USI CO_ CH1 .SE LO0	CCU 81. OUT 21	CCU 41. OUT 3		CCU4 0.I N3AB						USIC 0_ CH0. D X2B		USIC 0_ CH1. DX 2B		
P0.1 0/ XTAL 1	BCC U0. OUT 6	LED TS1 .LIN E2	LED TS0 .CO L5	ACM P0. OUT	CCU 80. OUT 22	USI CO_ CH0 .SE LO1	USI CO_ CH1 .SE LO1	CCU 81. OUT 22					CCU8 0.I N2AB	CCU8 1.I N2AB			USIC 0_ CH0. D X2C		USIC 0_ CH1. DX 2C		
P0.1 1/ XTAL 2	BCC U0. OUT 7	LED TS1 .LIN E3	LED TS0 .CO L4	USI CO_ CH0 .MC LKO UT	CCU 80. OUT 23	USI CO_ CH0 .SE LO2	USI CO_ CH1 .SE LO2	CCU 81. OUT 23									USIC 0_ CH0. D X2D		USIC 0_ CH1. DX 2D		
P0.1 2	BCC U0. OUT 6	LED TS1 .LIN E4	LED TS0 .CO L3	LED TS1 .CO L3	CCU 80. OUT 33	USI CO_ CH0 .SE LO3	CCU 80. OUT 20		CAN .N1 _TX D	BCC U0. TRAP IN A	CCU4 0.I N0AA	CCU4 0.I N1AA	CCU4 0.I N2AA	CCU8 1.I N0AU	CCU4 0.I N3AA	CCU8 0.I N0AA	USIC 0_ CH0. D X2E	CCU8 0.I N1AA	CCU8 0.I N2AA	CAN. N1 _RXD A	CCU8 0.I N3AA

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.1 3	WW DT. SER VIC E_O UT	LED TS1 .LIN E5	LED TS0 .CO L2	LED TS1 .CO L2	CCU 80. OUT 32	USI CO_ CH0 .SE LO4	CCU 80. OUT 21		CAN .N1 _TX D				CCU8 0.I N3AB	CCU8 1.I N1AU	POSI F0. IN0B		USIC 0_ CH0. D X2F			CAN. N1 _RXD B	
P0.1 4	BCC U0. OUT 7	LED TS1 .LIN E6	LED TS0 .CO L1	LED TS1 .CO L1	CCU 80. OUT 31	USI CO_ CH0 .DO UT0	USI CO_ CH0 .SC LKO UT		CAN .NO _TX D					CCU8 1.I N2AU	POSI F0. IN1B	USIC 0_ CH0. DX 0A	USIC 0_ CH0. D X1A	USIC 1_ CH1. DX 5B		CAN. NO _RXD C	
P0.1 5	BCC U0. OUT 8	LED TS1 .LIN E7	LED TS0 .CO L0	LED TS1 .CO L0	CCU 80. OUT 30	USI CO_ CH0 .DO UT0	USI CO_ CH1 .MC LKO UT		CAN .NO _TX D					CCU8 1.I N3AU	POSI F0. IN2B	USIC 0_ CH0. DX 0B		USIC 1_ CH1. DX 3B	USIC 1_ CH1. DX 4B	CAN. NO _RXD D	
P1.0	BCC U0. OUT 0	CCU 40. OUT 0	LED TS0 .CO L0	LED TS1 .CO LA	CCU 80. OUT 00	ACM P1. OUT	USI CO_ CH0 .DO UT0	CCU 81. OUT 00	CAN .NO _TX D						POSI F0. IN2A	USIC 0_ CH0. DX 0C				CAN. NO _RXD G	

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P1.1	ERU 1.P DO UT1	CCU 40. OUT 1	LED TS0 .CO L1	LED TS1 .CO L0	CCU 80. OUT 01	USI CO_ CH0 .DO UT0	USI CO_ CH1 .SE LO0	CCU 81. OUT 01	CAN .N0 _TX D						POSI F0. IN1A	USIC 0_ CH0. DX 0D	USIC 0_ CH0. D X1D		USIC 0_ CH1. DX 2E	CAN. N0 _RXD H	
P1.2	ERU 1.P DO UT2	CCU 40. OUT 2	LED TS0 .CO L2	LED TS1 .CO L1	CCU 80. OUT 10	ACM P2. OUT	USI CO_ CH1 .DO UT0	CCU 81. OUT 10	CAN .N1 _TX D						POSI F0. IN0A			USIC 0_ CH1. DX 0B		CAN. N1 _RXD G	
P1.3	ERU 1.P DO UT3	CCU 40. OUT 3	LED TS0 .CO L3	LED TS1 .CO L2	CCU 80. OUT 11	USI CO_ CH1 .SC LKO UT	USI CO_ CH1 .DO UT0	CCU 81. OUT 11	CAN .N1 _TX D									USIC 0_ CH1. DX 0A	USIC 0_ CH1. DX 1A	CAN. N1 _RXD H	
P1.4	ERU 1.P DO UT0	USI CO_ CH1 .SC LKO UT	LED TS0 .CO L4	LED TS1 .CO L3	CCU 80. OUT 20	USI CO_ CH0 .SE LO0	USI CO_ CH1 .SE LO1	CCU 81. OUT 20	CCU 41. OUT 0							USIC 0_ CH0. DX 5E		USIC 0_ CH1. DX 5E			
P1.5	ERU 1.P DO UT1	USI CO_ CH0 .DO UT0	LED TS0 .CO LA	BCC U0. OUT 1	CCU 80. OUT 21	USI CO_ CH0 .SE LO1	USI CO_ CH1 .SE LO2	CCU 81. OUT 21	CCU 41. OUT 1									USIC 0_ CH1. DX 5F			

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	ERU 1.P DO UT2	USI CO_ CH1 .DO UT0	LED TS0 .CO L5	USI CO_ CH0 .SC LKO UT	BCC U0. OUT 2	USI CO_ CH0 .SE LO2	USI CO_ CH1 .SE LO3	CCU 81. OUT 30	CCU 41. OUT 2						POSI F1. IN2A	USIC 0_ CH0. DX 5F					
P1.7	BCC U0. OUT 8	CCU 40. OUT 3	LED TS0 .CO L6	LED TS1 .CO L4		ACM P3. OUT	ERU 1.P DO UT3	CCU 81. OUT 31	CCU 41. OUT 3						POSI F1. IN1A	USIC 1_ CH0. DX 5B			USIC 1_ CH1. DX 2C		
P1.8	BCC U0. OUT 0	CCU 40. OUT 0	USI C1_ CH1 .SC LKO UT	VAD C0. EM UX0 2		ACM P1. OUT	ERU 1.P DO UT0	CCU 81. OUT 32							POSI F1. IN0A	USIC 1_ CH0. DX 3B	USIC 1_ CH0. D X4B		USIC 1_ CH1. DX 1C		
P2.0	ERU 0.P DO UT3	CCU 40. OUT 0	ERU 0.G OUT 3	LED TS1 .CO L5	CCU 80. OUT 20	USI CO_ CH0 .DO UT0	USI CO_ CH0 .SC LKO UT	CCU 81. OUT 20	CAN .NO _TX D		VADC 0. G0C H5					USIC 0_ CH0. DX 0E	USIC 0_ CH0. D X1E		USIC 0_ CH1. DX 2F	CAN. NO _RXD E	ERU0 .0 B0

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.1	ERU 0.P DO UT2	CCU 40. OUT 1	ERU 0.G OUT 2	LED TS1 .CO L6	CCU 80. OUT 21	USI CO_ CH0 .DO UT0	USI CO_ CH1 .SC LKO UT	CCU 81. OUT 21	CAN .NO _TX D	ACM P2.I NP	VADC 0. G0C H6					USIC 0_ CH0. DX 0F		USIC 0_ CH1. DX 3A	USIC 0_ CH1. DX 4A	CAN. NO _RXD F	ERU0 .1 B0
P2.2										ACM P2.I NN	VADC 0. G0C H7		ORC0 .AI N	USIC 1_ CH0. DX 5E		USIC 0_ CH0. DX 3A	USIC 0_ CH0. D X4A	USIC 0_ CH1. DX 5A			ERU0 .0 B1
P2.3												VADC 0. G1C H5	ORC1 .AI N	USIC 1_ CH0. DX 3E	USIC 1_ CH0. DX 4E	USIC 1_ CH1. DX 5C	USIC 0_ CH0. D X5B	USIC 0_ CH1. DX 3C	USIC 0_ CH1. DX 4C		ERU0 .1 B1
P2.4												VADC 0. G1C H6	ORC2 .AI N	USIC 1_ CH1. DX 3C	USIC 1_ CH1. DX 4C	USIC 0_ CH0. DX 3B	USIC 0_ CH0. D X4B	USIC 1_ CH0. DX 5F	USIC 0_ CH1. DX 5B		ERU0 .0 A1
P2.5												VADC 0. G1C H7	ORC3 .AI N	USIC 1_ CH1. DX 5D		USIC 0_ CH0. DX 5D		USIC 0_ CH1. DX 3E	USIC 0_ CH1. DX 4E		ERU0 .1 A1

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.6										ACM P1.I NN	VADC 0. G0C H0		ORC4 .AI N	USIC 1_ CH1. DX 3E	USIC 1_ CH1. DX 4E	USIC 0_ CH0. DX 3E	USIC 0_ CH0. D X4E	USIC 0_ CH1. DX 5D			ERU0 .2 A1
P2.7										ACM P1.I NP		VADC 0. G1C H1	ORC5 .AI N	USIC 1_ CH1. DX 5E		USIC 0_ CH0. DX 5C		USIC 0_ CH1. DX 3D	USIC 0_ CH1. DX 4D		ERU0 .3 A1
P2.8										ACM P0.I NN	VADC 0. G0C H1	VADC 0. G1C H0	ORC6 .AI N			USIC 0_ CH0. DX 3D	USIC 0_ CH0. D X4D	USIC 0_ CH1. DX 5C			ERU0 .3 B1
P2.9										ACM P0.I NP	VADC 0. G0C H2	VADC 0. G1C H4	ORC7 .AI N			USIC 0_ CH0. DX 5A		USIC 0_ CH1. DX 3B	USIC 0_ CH1. DX 4B		ERU0 .3 B0
P2.10	ERU 0.P DO UT1	CCU 40. OUT 2	ERU 0.G OUT 1	LED TS1 .CO L4	CCU 80. OUT 30	ACM P0. OUT	USI C0_ CH1 .DO UT0		CAN .N1 _TX D		VADC 0. G0C H3	VADC 0. G1C H2				USIC 0_ CH0. DX 3C	USIC 0_ CH0. D X4C	USIC 0_ CH1. DX 0F		CAN. N1 _RXD E	ERU0 .2 B0

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.1 1	ERU 0.P DO UT0	CCU 40. OUT 3	ERU 0.G OUT 0	LED TS1 .CO L3	CCU 80. OUT 31	USI CO_ CH1 .SC LKO UT	USI CO_ CH1 .DO UT0		CAN .N1 _TX D	ACM P.R EF	VADC 0. G0C H4	VADC 0. G1C H3						USIC 0_ CH1. DX 0E	USIC 0_ CH1. DX 1E	CAN. N1 _RXD F	ERU0 .2 B1
P2.1 2	BCC U0. OUT 3	VAD C0. EM UX0 0CH 0.S C	USI C1_ LKO UT	USI C1_ CH1 .SC LKO UT		ACM P2. OUT	USI C1_ CH1 .DO UT0	LED TS2 .CO L6		ACM P3.I NN						USIC 1_ CH0. DX 3A	USIC 1_ CH0. D X4A	USIC 1_ CH1. DX 0C	USIC 1_ CH1. DX 1B		ERU1 .3 A2
P2.1 3	BCC U0. OUT 4	CCU 40. OUT 3	USI C1_ CH0 .MC LKO UT	CCU 81. OUT 31		VAD C0. EM UX0 1	USI C1_ CH1 .DO UT0	CCU 81. OUT 33	CCU 41. OUT 3	ACM P3.I NP						USIC 1_ CH0. DX 5A		USIC 1_ CH1. DX 0D			ERU1 .3 A3
P3.0	BCC U0. OUT 0	USI C1_ CH1 .DO UT0	USI C1_ CH1 .SC LKO UT	LED TS2 .CO LA	CCU 80. OUT 21	ACM P1. OUT	USI C1_ CH0 .SE LO1	CCU 81. OUT 21	CCU 41. OUT 0	BCC U0. TRAP IN C	CCU4 1.I N0AA	CCU4 1.I N1AA	CCU4 1.I N2AA	CCU4 1.I N3AA	CCU8 1.I N0AA	CCU8 1.I N1AA	CCU8 1. IN2A A	USIC 1_ CH1. DX 0E	USIC 1_ CH1. DX 1D	CCU8 1.I N3AA	ERU1 .0 A1

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P3.1	BCC U0. OUT 1	USI C1_ CH1 .DO UT0		LED TS2 .CO L0	CCU 80. OUT 20	ACM P3. OUT	USI C1_ CH0 .SE LO0	CCU 81. OUT 20	CCU 41. OUT 1								USIC 1_ CH0. D X2F	USIC 1_ CH1. DX 0F		ERU1 .1 A1
P3.2	BCC U0. OUT 2	USI C1_ CH1 .SC LKO UT		LED TS2 .CO L1	CCU 80. OUT 11	ACM P2. OUT	USI C1_ CH0 .SC LKO UT	CCU 81. OUT 11	CCU 41. OUT 2							USIC 1_ CH0. DX 3C	USIC 1_ CH0. D X4C	USIC 1_ CH1. DX 3D	USIC 1_ CH1. DX 4D	ERU1 .2 A1
P3.3	BCC U0. OUT 5	USI C1_ CH0 .DO UT0		LED TS2 .CO L2	CCU 80. OUT 10	ACM P0. OUT	USI C1_ CH1 .SE LO0	CCU 81. OUT 10	CCU 41. OUT 3							USIC 1_ CH0. DX 0E			USIC 1_ CH1. DX 2A	ERU1 .1 A3
P3.4	BCC U0. OUT 6	USI C1_ CH0 .DO UT0	USI C1_ CH0 .SC LKO UT	LED TS2 .CO L3	CCU 80. OUT 01	USI C1_ CH1 .MC LKO UT	USI C1_ CH1 .SE LO1	CCU 81. OUT 01								USIC 1_ CH0. DX 0F	USIC 1_ CH0. D X1E		USIC 1_ CH1. DX 2B	ERU1 .2 A3
P4.0	BCC U0. OUT 0	ERU 1.P DO UT0	LED TS2 .CO L5	ERU 1.G OUT 0	CCU 40. OUT 0	ACM P1. OUT	USI C1_ CH1 .SE LO1	CCU 81. OUT 10	CCU 41. OUT 0		CCU4 0.I N0BA	CCU4 1.I N0AC	CCU8 0.I N0AU			USIC 1_ CH0. DX 3D	USIC 1_ CH0. D X4D			

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P4.1	BCC U0. OUT 8	ERU 1.P DO UT1	LED TS2 .CO L4	ERU 1.G OUT 1	CCU 40. OUT 1	ACM P3. OUT	USI C1_ CH1 .SE LO2	CCU 81. OUT 11	CCU 41. OUT 1		CCU4 0.I N1BA	CCU4 1.I N1AC	CCU8 0.I N1AU		POSI F1. IN0B	USIC 1_ CH0. DX 5C					
P4.2	BCC U0. OUT 4	ERU 1.P DO UT2	CCU 81. OUT 20	ERU 1.G OUT 2	CCU 40. OUT 2	ACM P2. OUT	USI C1_ CH1 .SE LO3	CCU 81. OUT 12	CCU 41. OUT 2		CCU4 0.I N2BA	CCU4 1.I N2AC	CCU8 0.I N2AU	CCU8 1.I N1AB	POSI F1. IN1B	USIC 1_ CH0. DX 5D					
P4.3	BCC U0. OUT 5	ERU 1.P DO UT3	CCU 81. OUT 21	ERU 1.G OUT 3	CCU 40. OUT 3	ACM P0. OUT	USI C1_ CH0 .SC LKO UT	CCU 81. OUT 13	CCU 41. OUT 3		CCU4 0.I N3BA	CCU4 1.I N3AC	CCU8 0.I N3AU		POSI F1. IN2B		USIC 1_ CH0. D X1B				
P4.4	BCC U0. OUT 0	LED TS2 .LIN E0		LED TS1 .CO LA	CCU 80. OUT 00	USI C1_ CH0 .DO UT0		CCU 81. OUT 00	CCU 41. OUT 0			CCU4 1.I N0AV				USIC 1_ CH0. DX 0C		USIC 1_ CH1. DX 5F			ERU1 .0 A2
P4.5	BCC U0. OUT 8	LED TS2 .LIN E1		LED TS1 .CO L6	CCU 80. OUT 01	USI C1_ CH0 .DO UT0	USI C1_ CH0 .SC LKO UT	CCU 81. OUT 01	CCU 41. OUT 1			CCU4 1.I N1AV				USIC 1_ CH0. DX 0D	USIC 1_ CH0. D X1C				ERU1 .1 A2

(table continues...)

Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P4.6	BCC U0. OUT 2	LED TS2 .LIN E2	CCU 81. OUT 10	LED TS1 .CO L5	CCU 80. OUT 10		USI C1_ CH0 .SC LKO UT	CCU 81. OUT 02	CCU 41. OUT 2			CCU4 1.I N2AV		CCU8 1.I N0AB			USIC 1_ CH0. D X1D			ERU1 .2 A2
P4.7	BCC U0. OUT 5	LED TS2 .LIN E3	CCU 81. OUT 11	LED TS1 .CO L4	CCU 80. OUT 11		USI C1_ CH0 .SE LO0	CCU 81. OUT 03	CCU 41. OUT 3			CCU4 1.I N3AV					USIC 1_ CH0. D X2A			ERU1 .0 A3
P4.8	BCC U0. OUT 7	LED TS2 .LIN E4	LED TS2 .CO L3	LED TS1 .CO L3	CCU 80. OUT 30	CCU 40. OUT 0	USI C1_ CH0 .SE LO1	CCU 81. OUT 30	CAN .N1 _TX D		CCU4 0.I N0AV	CCU4 1.I N0BA					USIC 1_ CH0. D X2B		CAN. N1 _RXD C	
P4.9	BCC U0. OUT 3	LED TS2 .LIN E5	LED TS2 .CO L2	LED TS1 .CO L2	CCU 80. OUT 31	CCU 40. OUT 1	USI C1_ CH0 .SE LO2	CCU 81. OUT 31	CAN .N1 _TX D		CCU4 0.I N1AV	CCU4 1.I N1BA					USIC 1_ CH0. D X2C		CAN. N1 _RXD D	
P4.1 0		LED TS2 .LIN E6	LED TS2 .CO L1	LED TS1 .CO L1	CCU 80. OUT 00	CCU 40. OUT 2	USI C1_ CH0 .SE LO3	CCU 81. OUT 32	CCU 81. OUT 00	BCC U0. TRAP IN D	CCU4 0.I N2AV	CCU4 1.I N2BA		CCU8 1.I N3AB			USIC 1_ CH0. D X2D	USIC 1_ CH1. DX 5A		

(table continues...)



Table 9 (continued) Port I/O Functions

Function	Outputs									Inputs												
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	
P4.1 1		LED TS2 .LIN E7	LED TS2 .CO L0	LED TS1 .CO L0	CCU 80. OUT 01	CCU 40. OUT 3	USI C1_ CH0 .SE LO4	CCU 81. OUT 33	CCU 81. OUT 01		CCU4 0.I N3AV	CCU4 1.I N3BA						USIC 1_ CH0. D X2E	USIC 1_ CH1. DX 3A	USIC 1_ CH1. DX 4A		

Table 10 **Hardware I/O Controlled Functions**

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0.EXTENDED 7		LEDTS0.TSI N7	LEDTS0.TSI N7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0.EXTENDED 6		LEDTS0.TSI N6	LEDTS0.TSI N6				
P0.2	LEDTS0.EXTENDED 5		LEDTS0.TSI N5	LEDTS0.TSI N5				
P0.3	LEDTS0.EXTENDED 4		LEDTS0.TSI N4	LEDTS0.TSI N4				
P0.4	LEDTS0.EXTENDED 3		LEDTS0.TSI N3	LEDTS0.TSI N3				
P0.5	LEDTS0.EXTENDED 2		LEDTS0.TSI N2	LEDTS0.TSI N2				
P0.6	LEDTS0.EXTENDED 1		LEDTS0.TSI N1	LEDTS0.TSI N1				
P0.7	LEDTS0.EXTENDED 0		LEDTS0.TSI N0	LEDTS0.TSI N0				
P0.8	LEDTS1.EXTENDED 0		LEDTS1.TSI N0	LEDTS1.TSI N0				

(table continues...)

Table 10 (continued) Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.9	LEDTS1. EXTENDED 1		LEDTS1.TSI N1	LEDTS1.TSI N1				
P0.10	LEDTS1. EXTENDED 2		LEDTS1.TSI N2	LEDTS1.TSI N2				
P0.11	LEDTS1. EXTENDED 3		LEDTS1.TSI N3	LEDTS1.TSI N3				
P0.12	LEDTS1. EXTENDED 4		LEDTS1.TSI N4	LEDTS1.TSI N4				
P0.13	LEDTS1. EXTENDED 5		LEDTS1.TSI N5	LEDTS1.TSI N5				
P0.14	LEDTS1. EXTENDED 6		LEDTS1.TSI N6	LEDTS1.TSI N6				
P0.15	LEDTS1. EXTENDED 7		LEDTS1.TSI N7	LEDTS1.TSI N7				
P1.0		USIC0_CH0 .DOUT0		USIC0_CH0 .HWIN0	$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2		
P1.1		USIC0_CH0 .DOUT1		USIC0_CH0 .HWIN1	$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3		
P1.2		USIC0_CH0 .DOUT2		USIC0_CH0 .HWIN2	$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		

(table continues...)

Table 10 (continued) Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.3		USIC0_CH0 .DOUT3		USIC0_CH0 .HWIN3	$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		
P1.4					$\overline{\text{BCCU0.OUT6}}$	BCCU0.OUT6		
P1.5					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7		
P1.6					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8		
P1.7								
P1.8								
P2.0					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1		
P2.1					$\overline{\text{BCCU0.OUT6}}$	BCCU0.OUT6		
P2.2					$\overline{\text{BCCU0.OUT0}}$	BCCU0.OUT0	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.3					$\overline{\text{ACMP2.OUT}}$	ACMP2.OUT		
P2.4					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8		
P2.5					$\overline{\text{ACMP1.OUT}}$	ACMP1.OUT		
P2.6					$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		
P2.11					$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		
P2.12					$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3	$\overline{\text{CCU41.OUT0}}$	CCU41.OUT0
P2.13					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4	$\overline{\text{CCU41.OUT2}}$	CCU41.OUT2

(table continues...)

Table 10 (continued) Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P3.0								
P3.1		USIC1_CH0 .DOUT3		USIC1_CH0 .HWIN3				
P3.2		USIC1_CH0 .DOUT2		USIC1_CH0 .HWIN2				
P3.3		USIC1_CH0 .DOUT1		USIC1_CH0 .HWIN1				
P3.4		USIC1_CH0 .DOUT0		USIC1_CH0 .HWIN0				
P4.0								
P4.1								
P4.2								
P4.3								
P4.4	LEDTS2. EXTENDED 0		LEDTS2.TSI N0	LEDTS2.TSI N0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2. EXTENDED 1		LEDTS2.TSI N1	LEDTS2.TSI N1				
P4.6	LEDTS2. EXTENDED 2		LEDTS2.TSI N2	LEDTS2.TSI N2				
P4.7	LEDTS2. EXTENDED 3		LEDTS2.TSI N3	LEDTS2.TSI N3				

(table continues...)

Table 10 (continued) Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HW00	HW01	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P4.8	LEDTS2. EXTENDED 4		LEDTS2.TSI N4	LEDTS2.TSI N4				
P4.9	LEDTS2. EXTENDED 5		LEDTS2.TSI N5	LEDTS2.TSI N5				
P4.10	LEDTS2. EXTENDED 6		LEDTS2.TSI N6	LEDTS2.TSI N6				
P4.11	LEDTS2. EXTENDED 7		LEDTS2.TSI N7	LEDTS2.TSI N7				

3 Electrical Parameters

3 Electrical Parameters

This section provides the electrical parameters which are implementation-specific for the XMC1400.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1400 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
 Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1400 and must be regarded for a system design.
- **SR**
 Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1400 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Junction temperature	T_J SR	-40	–	115	°C	–
Storage temperature	T_{ST} SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP} SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} ¹⁾	V_{IN} SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on P2 pins with respect to V_{SSP} ²⁾	V_{INP2} SR	-0.3	–	$V_{DDP} + 0.3$	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF} SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN} SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN} SR	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].

2) Applicable to port pins P2.[1,2,6,7,8,9,11].

3 Electrical Parameters

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for:
 - pad supply levels (V_{DDP})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 13 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

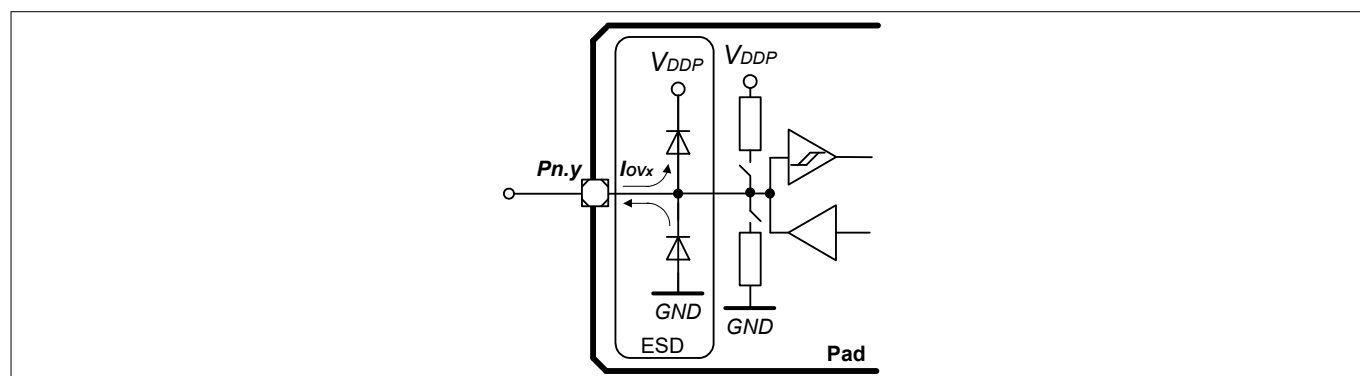


Figure 13 Input Overload Current via ESD structures

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Table 13 and Table 14 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the [Absolute Maximum Ratings](#) must not be exceeded during overload.

Table 13 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5 \text{ V}$ $V_{AIN} = V_{DDP} + 0.5 \text{ V}$ $V_{AREF} = V_{DDP} + 0.5 \text{ V}$
P2.[1,2,6;9,11]	$V_{INP2} = V_{DDP} + 0.3 \text{ V}$

Table 14 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5 \text{ V}$ $V_{AIN} = V_{SS} - 0.5 \text{ V}$ $V_{AREF} = V_{SS} - 0.5 \text{ V}$
P2.[1,2,6;9,11]	$V_{INP2} = V_{SS} - 0.3 \text{ V}$

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1400. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage ¹⁾	V_{DDP} SR	1.8	–	5.5	V	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, [Chapter 3.3.2](#).

3 Electrical Parameters

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1400.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
Output low voltage on port pins (with standard pads)	$V_{OLP\ CC}$	–	1.0	V	$I_{OL} = 11\text{ mA}$ (5 V) $I_{OL} = 7\text{ mA}$ (3.3 V)
		–	0.4	V	$I_{OL} = 5\text{ mA}$ (5 V) $I_{OL} = 3.5\text{ mA}$ (3.3 V)
Output low voltage on high current pads	$V_{OLP1\ CC}$	–	1.0	V	$I_{OL} = 50\text{ mA}$ (5 V) $I_{OL} = 25\text{ mA}$ (3.3 V)
		–	0.32	V	$I_{OL} = 10\text{ mA}$ (5 V)
		–	0.4	V	$I_{OL} = 5\text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	$V_{OHP\ CC}$	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10\text{ mA}$ (5 V) $I_{OH} = -7\text{ mA}$ (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5\text{ mA}$ (5 V) $I_{OH} = -2.5\text{ mA}$ (3.3 V)
Output high voltage on high current pads	$V_{OHP1\ CC}$	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6\text{ mA}$ (5 V)
		$V_{DDP} - 1.0$	–	V	$I_{OH} = -8\text{ mA}$ (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4\text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	$V_{ILPS\ SR}$	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	$V_{IHPS\ SR}$	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	$V_{ILPL\ SR}$	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Large Hysteresis)	$V_{IHPL\ SR}$	$0.85 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Rise/fall time on High Current Pad ¹⁾	$t_{HCPR}, t_{HCPF\ CC}$	–	9	ns	50 pF @ 5 V ²⁾
		–	12	ns	50 pF @ 3.3 V ³⁾

(table continues...)

3 Electrical Parameters

Table 16 (continued) **Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
		–	25	ns	50 pF @ 1.8 V ⁴⁾
Rise/fall time on Standard Pad ¹⁾	t_R, t_F CC	–	12	ns	50 pF @ 5 V ⁵⁾
		–	15	ns	50 pF @ 3.3 V ⁶⁾
		–	31	ns	50 pF @ 1.8 V ⁷⁾
Input Hysteresis on port pin except P2.3 - P2.9 ⁸⁾	HYS CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
		$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
		$0.02 \times V_{DDP}$	–	V	CMOS Mode (2.2 V), Standard Hysteresis
		$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode (5 V), Large Hysteresis
		$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode (3.3 V), Large Hysteresis
		$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode (2.2 V), Large Hysteresis
Input Hysteresis on port pin P2.3 - P2.9 ⁸⁾	HYS_P2 CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
		$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
		$0.02 \times V_{DDP}$	–	V	CMOS Mode (2.2 V), Standard Hysteresis
		$0.35 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode (5 V), Large Hysteresis
		$0.25 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode (3.3 V), Large Hysteresis
		$0.15 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode (2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-up current on port pins	I_{PUP} CC	–	-80	μA	$V_{IH,min}$ (5 V)
		-95	–	μA	$V_{IL,max}$ (5 V)
		–	-50	μA	$V_{IH,min}$ (3.3 V)
		-65	–	μA	$V_{IL,max}$ (3.3 V)
Pull-down current on port pins	I_{PDP} CC	–	40	μA	$V_{IL,max}$ (5 V)
		95	–	μA	$V_{IH,min}$ (5 V)

(table continues...)

3 Electrical Parameters

Table 16 (continued) **Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
		–	30	μA	$V_{IL,max}$ (3.3 V)
		60	–	μA	$V_{IH,min}$ (3.3 V)
Input leakage current except P0.11 ⁹⁾	I_{OZP} CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ\text{C}$
Input leakage current for P0.11 ⁹⁾	I_{OZP1} CC	-10	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ\text{C}$
Voltage on any pin during V_{DDP} power off	V_{PO} SR	–	0.3	V	¹⁰⁾
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP} SR	-10	11	mA	–
Maximum current per high current pins	I_{MP1A} SR	-10	50	mA	–
Maximum current into V_{DDP} (VQFN64, LQFP64)	I_{MVDD1} SR	–	520	mA	
Maximum current into V_{DDP} (VQFN48)	I_{MVDD2} SR	–	390	mA	
Maximum current into V_{DDP} (VQFN40)	I_{MVDD3} SR	–	260	mA	
Maximum current out of V_{SS} (VQFN64, LQFP64)	I_{MVSS1} SR	–	390	mA	
Maximum current out of V_{SS} (VQFN48)	I_{MVSS2} SR	–	260	mA	
Maximum current out of V_{SS} (VQFN40)	I_{MVSS3} SR	–	260	mA	

- 1) Rise/Fall time parameters are taken with 10% - 90% of supply.
- 2) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.150 ns/pF at 5 V supply voltage.
- 3) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.205 ns/pF at 3.3 V supply voltage.
- 4) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.445 ns/pF at 1.8 V supply voltage.
- 5) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.225 ns/pF at 5 V supply voltage.
- 6) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.288 ns/pF at 3.3 V supply voltage.
- 7) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.588 ns/pF at 1.8 V supply voltage.
- 8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
- 10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3 Electrical Parameters

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11 _B ; CALCTR.CALGNSTC = 0C _H for f_{SH} = 32 MHz, 12 _H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground ²⁾	V_{REFGND} SR	$V_{SSP} - 0.05$	–	1.0	V	G0CH0
		$V_{SSP} - 0.05$	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)

(table continues...)

3 Electrical Parameters

Table 17 (continued) ADC Characteristics (Operating Conditions apply)¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Sample Time	$t_{\text{sample CC}}$	5	–	–	$1/f_{\text{ADC}}$	$V_{\text{DD}} = 5.0 \text{ V}$, $f_{\text{ADCI}} = 48 \text{ MHz}$
		3	–	–	$1/f_{\text{ADC}}$	$V_{\text{DD}} = 5.0 \text{ V}$, $f_{\text{ADCI}} = 32 \text{ MHz}$
		3	–	–	$1/f_{\text{ADC}}$	$V_{\text{DD}} = 3.3 \text{ V}$, $f_{\text{ADCI}} = 32 \text{ MHz}$
		30	–	–	$1/f_{\text{ADC}}$	$V_{\text{DD}} = 2.0 \text{ V}$, $f_{\text{ADCI}} = 32 \text{ MHz}$
Conversion time in fast compare mode	$t_{\text{CF CC}}$	9			$1/f_{\text{ADC}}$	³⁾
Conversion time in 12-bit mode	$t_{\text{C12 CC}}$	20			$1/f_{\text{ADC}}$	³⁾
Maximum sample rate in 12-bit mode ⁴⁾	$f_{\text{C12 CC}}$	–	–	$f_{\text{ADC}}/42.5$	–	1 sample pending
		–	–	$f_{\text{ADC}}/62.5$	–	2 samples pending
Conversion time in 10-bit mode	$t_{\text{C10 CC}}$	18			$1/f_{\text{ADC}}$	³⁾
Maximum sample rate in 10-bit mode ⁴⁾	$f_{\text{C10 CC}}$	–	–	$f_{\text{ADC}}/40.5$	–	1 sample pending
		–	–	$f_{\text{ADC}}/58.5$	–	2 samples pending
Conversion time in 8-bit mode	$t_{\text{C8 CC}}$	16			$1/f_{\text{ADC}}$	³⁾
Maximum sample rate in 8-bit mode ⁴⁾	$f_{\text{C8 CC}}$	–	–	$f_{\text{ADC}}/38.5$	–	1 sample pending
		–	–	$f_{\text{ADC}}/54.5$	–	2 samples pending
RMS noise ⁵⁾	$EN_{\text{RMS CC}}$	–	1.5	–	LSB12	DC input, SHSCFG.AREF = 00 _B , GNCTRxz.GAINy = 00 _B (unity gain), $V_{\text{DD}} = 5.0 \text{ V}$, $V_{\text{AIN}} = 2.5 \text{ V}$, 25°C
DNL error	$EA_{\text{DNL CC}}$	–	±2.0	–	LSB12	
INL error	$EA_{\text{INL CC}}$	–	±4.0	–	LSB12	
Gain error with external reference	$EA_{\text{GAIN CC}}$	–	±0.5	–	%	SHSCFG.AREF = 00 _B (calibrated)
Gain error with internal reference ⁶⁾	$EA_{\text{GAIN CC}}$	–	±3.6	–	%	SHSCFG.AREF = 1X _B (calibrated), -40°C - 110°C
		–	±2.0	–	%	SHSCFG.AREF = 1X _B (calibrated), 0°C - 85°C
Offset error	$EA_{\text{OFF CC}}$	–	±8.0	–	mV	Calibrated, $V_{\text{DD}} = 5.0 \text{ V}$

3 Electrical Parameters

- 1) The parameters are defined for ADC clock frequencies $f_{SH} = 32$ MHz for the full supply range, and $f_{SH} = 48$ MHz at V_{DD_int} , $V_{DD_ext} = 5$ V. Usage of any other frequencies may affect the ADC performance.
- 2) The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.
- 3) No pending samples assumed, excluding sampling time and calibration.
- 4) Includes synchronization and calibration (average of gain and offset calibration).
- 5) This parameter can also be defined as an SNR value: $SNR[dB] = 20 \times \log(A_{MAXeff}/N_{RMS})$.
 With $A_{MAXeff} = 2^N/2$, $SNR[dB] = 20 \times \log(2048/N_{RMS})$ [$N = 12$].
 $N_{RMS} = 1.5$ LSB12, therefore, equals $SNR = 20 \times \log(2048/1.5) = 62.7$ dB.
- 6) Includes error from the reference voltage.

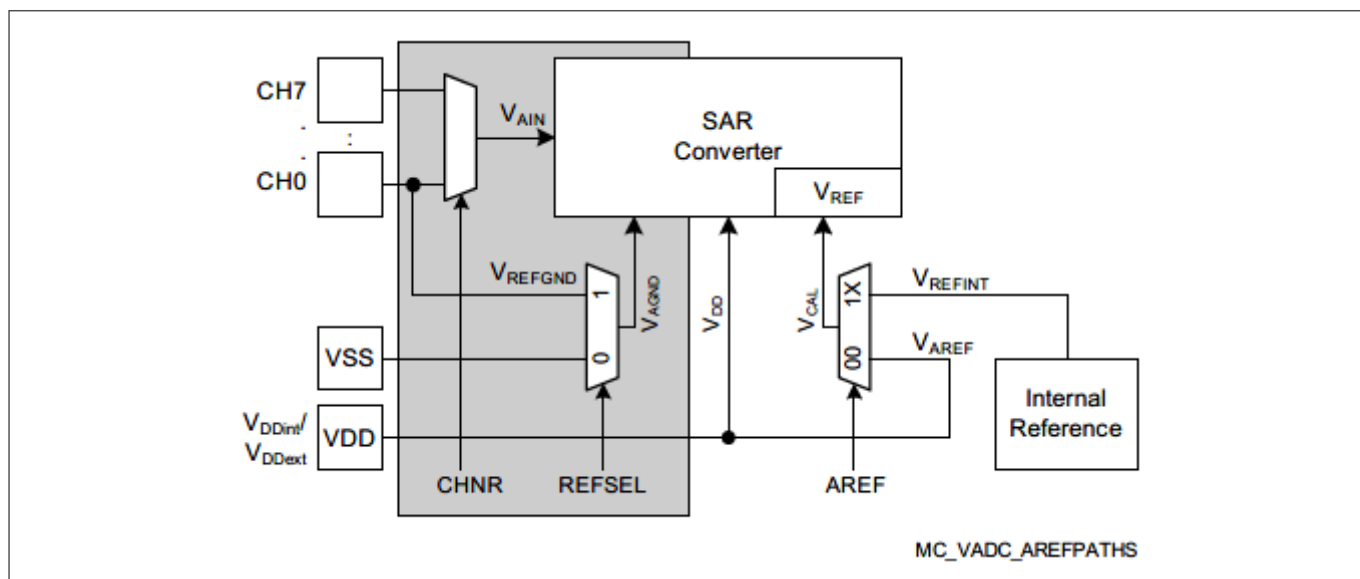


Figure 14 **ADC Voltage Supply**

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 18 **Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP} = 3.0$ V - 5.5 V; $C_L = 0.25$ pF)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DC Switching Level	V_{ODC} CC	–	–	180	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS} CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD} CC	103	–	–	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		88	–	–	ns	$V_{AIN} \geq V_{DDP} + 350$ mV
Never detected Overvoltage Pulse	t_{OPDN} CC	–	–	21	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		–	–	11	ns	$V_{AIN} \geq V_{DDP} + 350$ mV
Detection Delay	t_{ODD} CC	39	–	132	ns	$V_{AIN} \geq V_{DDP} + 150$ mV
		31	–	121	ns	$V_{AIN} \geq V_{DDP} + 350$ mV

(table continues...)

3 Electrical Parameters

Table 18 (continued) Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP} = 3.0\text{ V} - 5.5\text{ V}$; $C_L = 0.25\text{ pF}$)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Release Delay	$t_{ORD\ CC}$	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 5\text{ V}$
		57	–	340	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 3.3\text{ V}$
Enable Delay	$t_{OED\ CC}$	–	–	300	ns	ORCTRL.ENORCx = 1

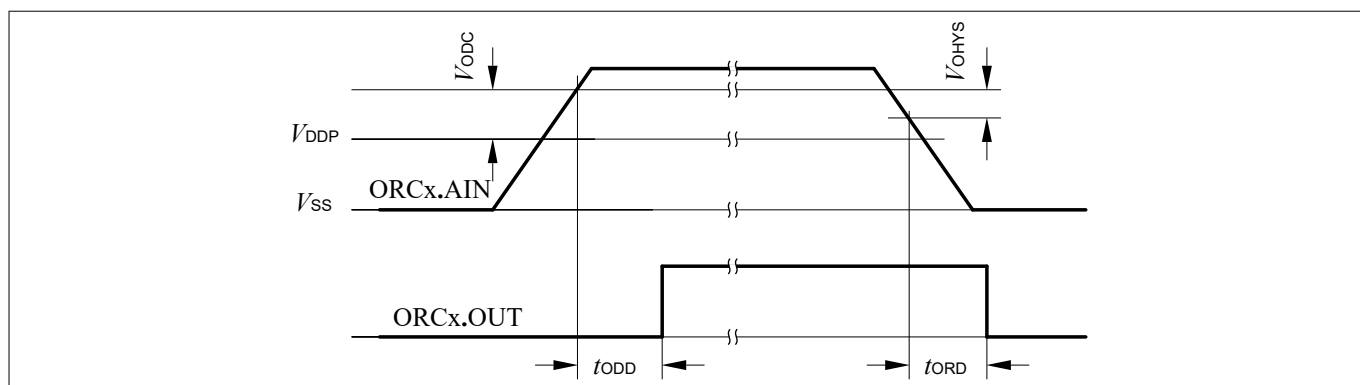


Figure 15 ORCx.OUT Trigger Generation

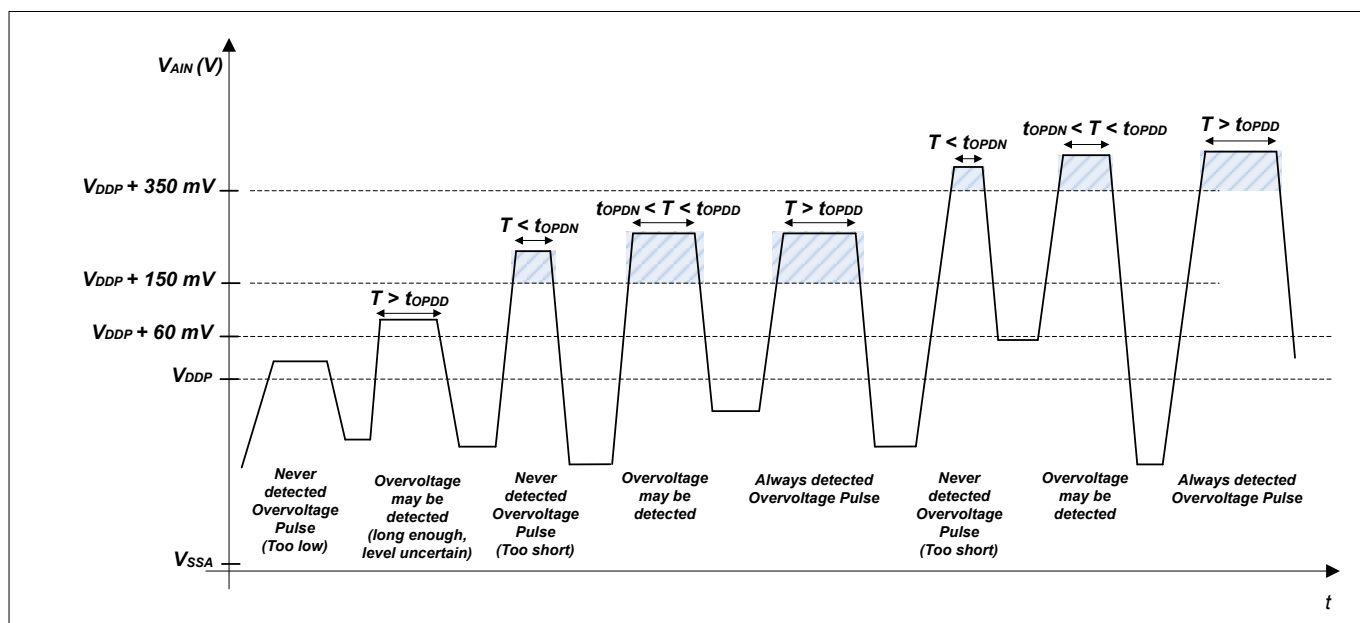


Figure 16 ORC Detection Ranges

3 Electrical Parameters

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Voltage	$V_{\text{CMP SR}}$	-0.05	–	$V_{\text{DDP}} + 0.05$	V	
Input Offset	$V_{\text{CMPOFF CC}}$	–	+/-3	–	mV	High power mode $\Delta V_{\text{CMP}} < 200 \text{ mV}$
Propagation Delay ¹⁾	$t_{\text{PDELAY CC}}$	–	25	–	ns	High power mode, $\Delta V_{\text{CMP}} = 100 \text{ mV}$
		–	80	–	ns	High power mode, $\Delta V_{\text{CMP}} = 25 \text{ mV}$
		–	250	–	ns	Low power mode, $\Delta V_{\text{CMP}} = 100 \text{ mV}$
		–	700	–	ns	Low power mode, $\Delta V_{\text{CMP}} = 25 \text{ mV}$
Current Consumption	$I_{\text{ACMP CC}}$	–	100	–	μA	First active ACMP in high power mode, $\Delta V_{\text{CMP}} > 30 \text{ mV}$
		–	66	–	μA	Each additional ACMP in high power mode, $\Delta V_{\text{CMP}} > 30 \text{ mV}$
		–	10	–	μA	First active ACMP in low power mode
		–	6	–	μA	Each additional ACMP in low power mode
Input Hysteresis	$V_{\text{HYS CC}}$	–	+/-15	–	mV	
Filter Delay ¹⁾	$t_{\text{FDELAY CC}}$	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

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3.2.5 Temperature Sensor Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy ¹⁾	T_{TSAL} CC	-6	–	6	°C	$T_J > 20^\circ\text{C}$
		-10	–	10	°C	$0^\circ\text{C} \leq T_J \leq 20^\circ\text{C}$
		–	-/+8	–	°C	$T_J < 0^\circ\text{C}$
Start-up time	t_{TSST} SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

3.2.6 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal/resonator (see Figure 17) or in direct input mode (see Figure 18).

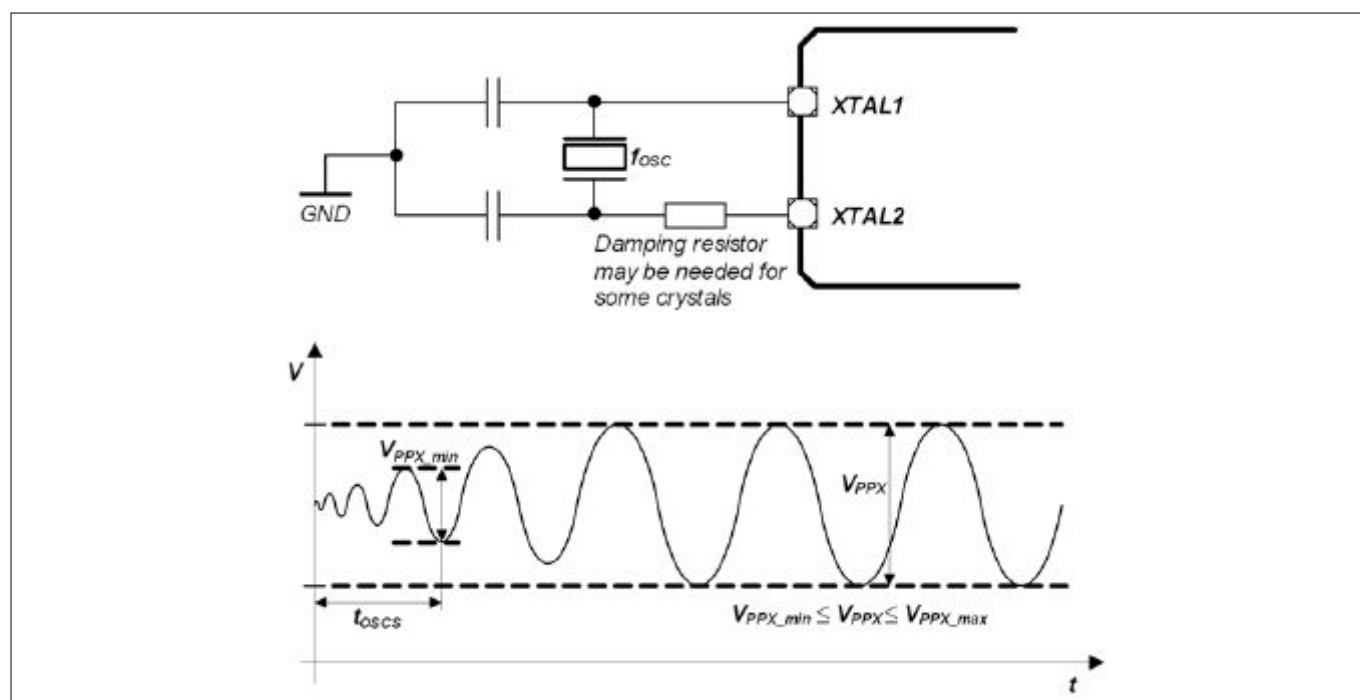


Figure 17 Oscillator in Crystal Mode

3 Electrical Parameters

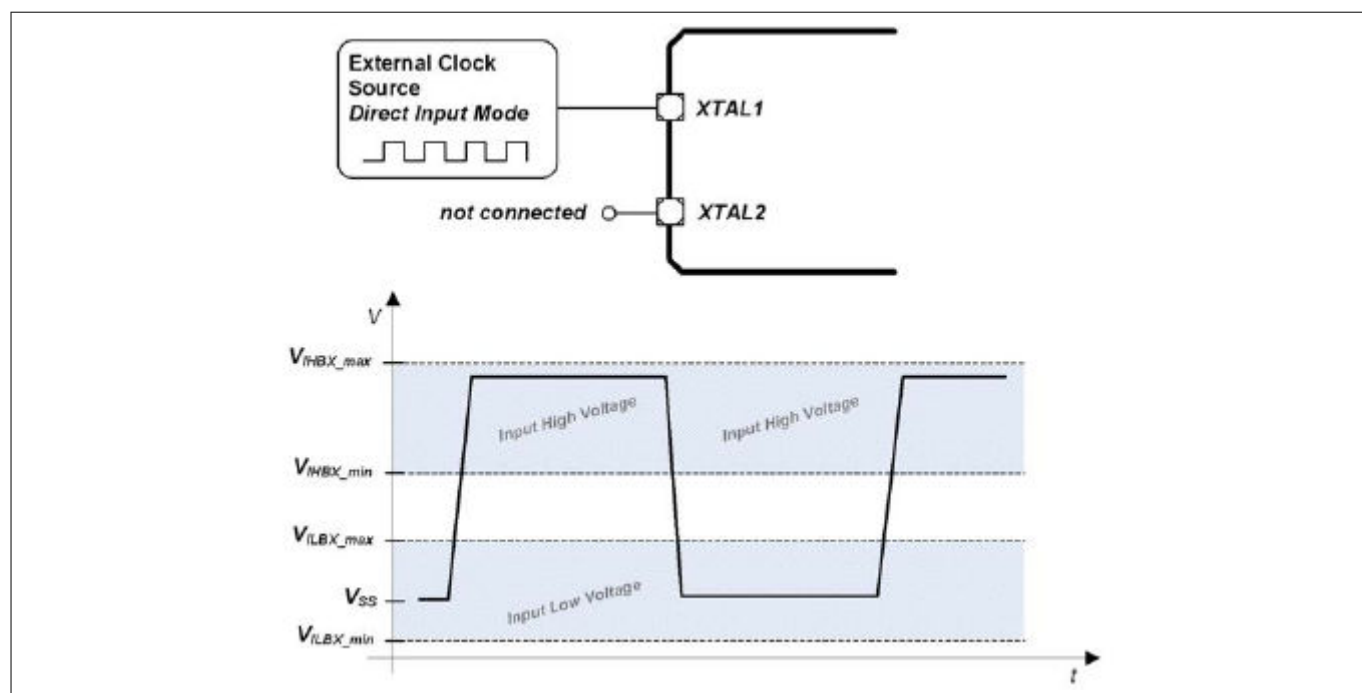


Figure 18 Oscillator in Direct Input Mode

Table 21 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	48	MHz	Direct Input Mode
		4	–	20	MHz	External Crystal Mode
Oscillator start-up time ^{1) 2)}	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.3	–	1.5	V	External Crystal Mode
		-0.3	–	5.5	V	Direct Input Mode
Input amplitude (peak-to-peak) at XTAL1 ^{2) 3)}	V_{PPX} SR	0.6	–	1.7	V	External Crystal Mode

- 1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_ANAOSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.9 \cdot V_{\text{PPX}}$.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) If the shaper unit is enabled and not bypassed.

Table 22 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time ^{1) 2)}	t_{OSCS} CC	–	–	5	s	

(table continues...)

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Table 22 (continued) RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	1.5	V	
Input amplitude (peak- to-peak) at RTC_XTAL1 ^{2) 3)}	V_{PPX} SR	0.2	–	1.2	V	

- 1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of $0.9 \cdot V_{PPX}$.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) If the shaper unit is enabled and not bypassed.

3.2.7 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Power Supply parameter table; $V_{DDP} = 5\text{ V}$

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ. ¹⁾	Max.		
Active mode current Peripherals enabled f_{MCLK}/f_{PCLK} in MHz ²⁾	I_{DDPAE} CC	–	14.1	20	mA	48/96
		–	9.8	–	mA	24/48
		–	7.8	–	mA	16/32
		–	6.4	–	mA	8/16
		–	4.4	–	mA	1/1
Active mode current Peripherals disabled f_{MCLK}/f_{PCLK} in MHz ³⁾	I_{DDPAD} CC	–	6.2	–	mA	48/96
		–	4.6	–	mA	24/48
		–	3.6	–	mA	16/32
		–	3.1	–	mA	8/16
		–	1.8	–	mA	1/1
Active mode current Code execution from RAM Flash is powered down f_{MCLK}/f_{PCLK} in MHz	I_{DDPAR} CC	–	9.6	–	mA	48/96
Sleep mode current Peripherals clock enabled f_{MCLK}/f_{PCLK} in MHz ⁴⁾	I_{DDPSE} CC	–	11.0	–	mA	48/96
		–	7.6	–	mA	24/48
		–	6.4	–	mA	16/32

(table continues...)

3 Electrical Parameters

Table 23 (continued) Power Supply parameter table; $V_{DDP} = 5\text{ V}$

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ. ¹⁾	Max.		
		–	5.3	–	mA	8/16
		–	4.2	–	mA	1/1
Sleep mode current Peripherals clock disabled Flash active f_{MCLK}/f_{PCLK} in MHz ⁵⁾	$I_{DDPSD}\text{ CC}$	–	2.8	–	mA	48/96
		–	2.2	–	mA	24/48
		–	2.0	–	mA	16/32
		–	1.9	–	mA	8/16
		–	1.7	–	mA	1/1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK}/f_{PCLK} in MHz ⁶⁾	$I_{DDPSR}\text{ CC}$	–	2.2	–	mA	48/96
		–	1.7	–	mA	24/48
		–	1.4	–	mA	16/32
		–	1.2	–	mA	8/16
		–	1.1	–	mA	1/1
Deep Sleep mode current ⁷⁾	$I_{DDPDS}\text{ CC}$	–	0.27	–	mA	
Wake-up time from Sleep to Active mode ⁸⁾	$t_{SSA}\text{ CC}$	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode ⁹⁾	$t_{DSA}\text{ CC}$	–	290	–	μsec	

- 1) The typical values are measured at $T_A = +25^\circ\text{C}$ and $V_{DDP} = 5\text{ V}$.
- 2) CPU and all peripherals clock enabled, Flash is in active mode.
- 3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
- 4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
- 5) CPU in sleep, Flash is in active mode.
- 6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
- 7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
- 8) CPU in sleep, Flash is in active mode during sleep mode.
- 9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 19 shows typical graphs for active mode supply current for $V_{DDP} = 5\text{ V}$, $V_{DDP} = 3.3\text{ V}$, $V_{DDP} = 1.8\text{ V}$ across different clock frequencies.

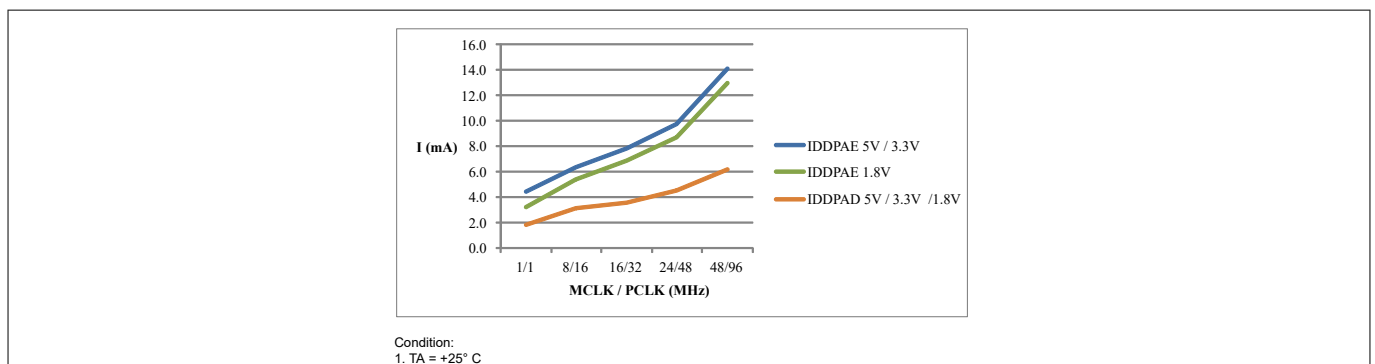


Figure 19 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

3 Electrical Parameters

Figure 20 shows typical graphs for sleep mode current for $V_{DDP} = 5\text{ V}$, $V_{DDP} = 3.3\text{ V}$, $V_{DDP} = 1.8\text{ V}$ across different clock frequencies.

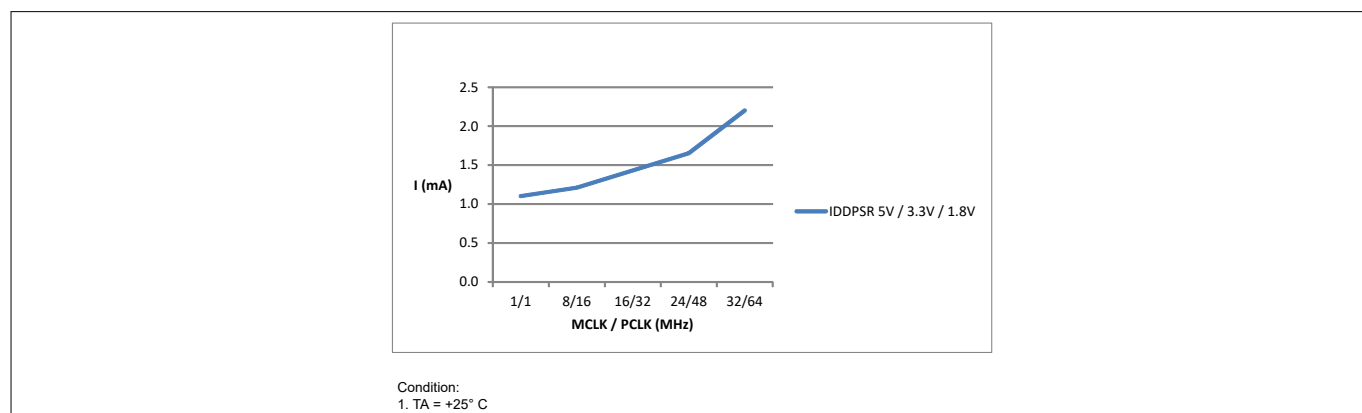


Figure 20 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSD} over supply voltage V_{DDP} for different clock frequencies

Table 24 provides the active current consumption of some modules operating at 5 V power supply at 25°C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 24 Typical Active Current parameter table

Active Current Consumption	Symbol	Limit Values	Unit	Note/Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	4.14	mA	Modules including Core, SCU, PORT, memories, ANATOP ¹⁾
VADC and SHS	I_{ADCDDC}	3.73	mA	Set CGATCLR0.VADC to 1 ²⁾
USICx	$I_{USIC0DDC}$	1.35	mA	Set CGATCLR0.USIC0 to 1 ³⁾
CCU4x	$I_{CCU40DDC}$	0.99	mA	Set CGATCLR0.CCU40 to 1 ⁴⁾
CCU8x	$I_{CCU80DDC}$	1.00	mA	Set CGATCLR0.CCU80 to 1 ⁵⁾
POSIFx	$I_{PIF0DDC}$	1.05	mA	Set CGATCLR0.POSIF0 to 1 ⁶⁾
LEDTSx	$I_{LTSxDDC}$	1.14	mA	Set CGATCLR0.LEDTSx to 1 ⁷⁾
BCCU0	$I_{BCCU0DDC}$	0.29	mA	Set CGATCLR0.BCCU0 to 1 ⁸⁾
MATH	$I_{MATHDDC}$	0.50	mA	Set CGATCLR0.MATH to 1 ⁹⁾
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1 ¹⁰⁾
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1 ¹¹⁾
MultiCAN	$I_{MCANDDC}$	1.38	mA	Set CGATCLR0.MCAN0 to 1 ¹²⁾

- 1) Baseload current is measured with device running in user mode, MCLK=PCLK=48 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
- 2) Active current is measured with: module enabled, MCLK=48 MHz, running in auto-scan conversion mode.
- 3) Active current is measured with: module enabled, each of the 2 USIC channels sending alternate messages at 57.6 kbaud every 200 ms.
- 4) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 1 CCU4 slice for PWM switching at 20 kHz with duty cycle varying at 10%-90%, 1 CCU4 slice in capture mode for reading period and duty cycle.
- 5) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 3 CCU8 slices with PWM frequency at 20 kHz and a period match interrupt used to toggle duty cycle between 10% and 90%.
- 6) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, hall sensor mode.

3 Electrical Parameters

- 7) Active current is measured with: module enabled, MCLK=48 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms.
- 8) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, FCLK=0.8 MHz, Normal mode (BCCU clock = FCLK/4), 4 BCCU Channels with packers enabled and 1 Dimming Engine, change color or dim every 1 s.
- 9) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11.
- 10) Active current is measured with: module enabled, MCLK=48 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s.
- 11) Active current is measured with: module enabled, MCLK=48 MHz, Periodic interrupt enabled.
- 12) Active current is measured with: module enabled, MCLK=48 MHz, running at 20 MHz baudrate generator, 1 node activated, 1 transmit and 1 receive object active.

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Erase time per page/sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase/program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	2	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
		2	2	3		$f_{\text{MCLK}} = 48 \text{ MHz}$
Erase Cycles	$N_{\text{ECCY CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECCY CC}}$	–	–	$2 \cdot 10^6$	cycles	

- 1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3 Electrical Parameters

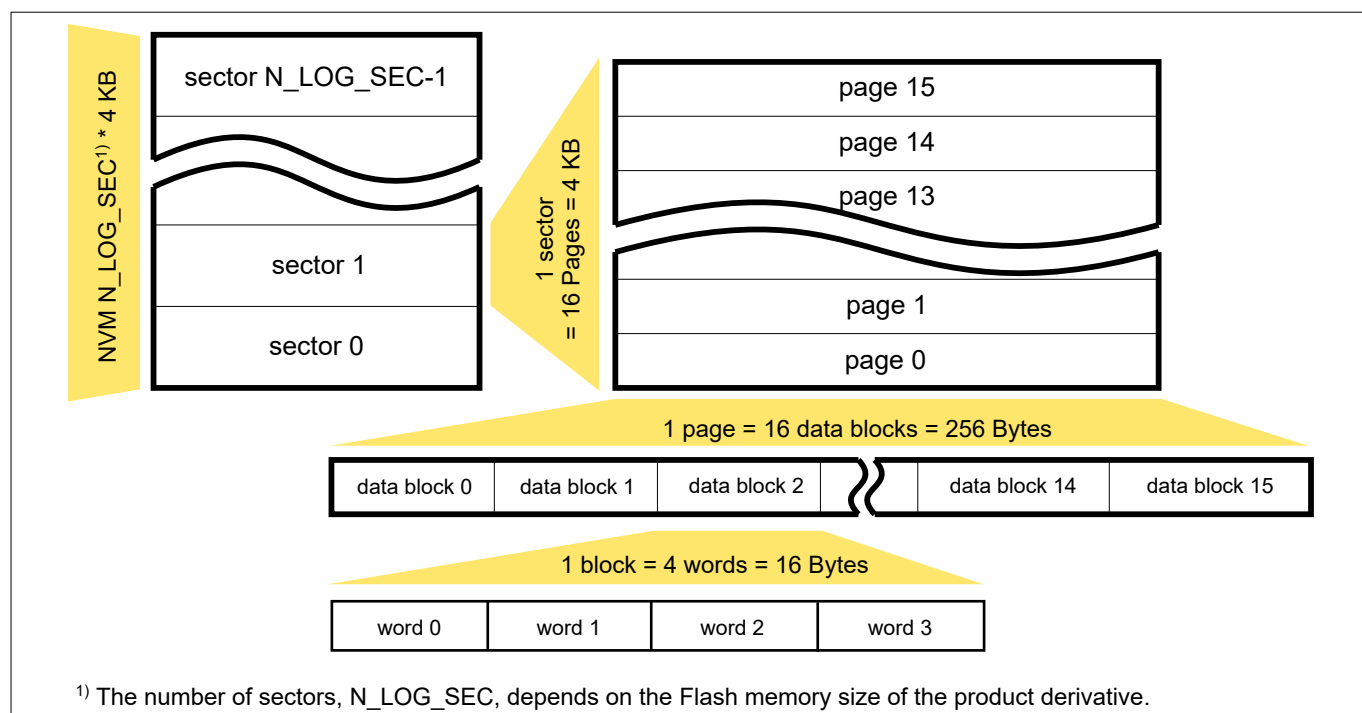


Figure 21 **Logical Structure of the Flash**

3.3 AC Parameters

3.3.1 Testing Waveforms

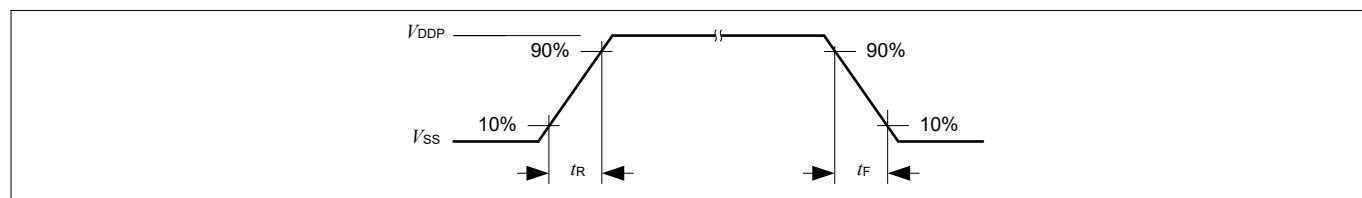


Figure 22 **Rise/Fall Time Parameters**

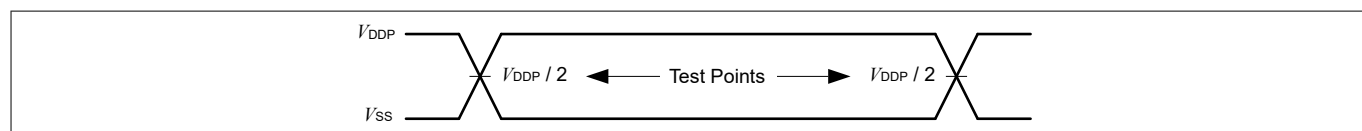


Figure 23 **Testing Waveform, Output Delay**

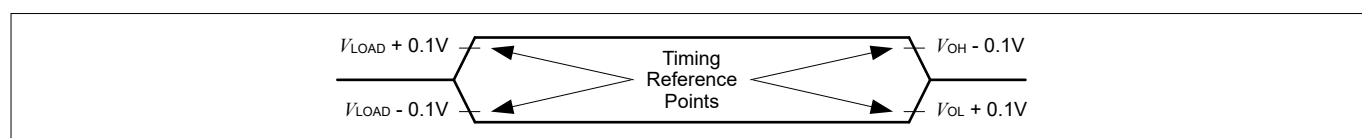


Figure 24 **Testing Waveform, Output High Impedance**

3 Electrical Parameters

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/S_{VDDPrise}$	–	10^7	μs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/ μs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/ μs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/ μs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}^{1)}$ SR	0	–	0.25	V/ μs	Slope during supply falling out of the +/-10% limits ²⁾
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 _B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 _B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 _B
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	260	–	μs	Time to the first user code instruction ³⁾
BMI program time	t_{BMI} SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is requested

1) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

3 Electrical Parameters

- 3) This values does not include the ramp-up time. During start-up firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.



Figure 25 Supply Threshold Parameters

3.3.3 On-Chip Oscillator Characteristics

Table 27 provides the characteristics of the 96 MHz digital controlled oscillator DCO1.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 96 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{NOM\ CC}$	–	96	–	MHz	under nominal conditions ¹⁾ after trimming
Accuracy with adjustment based on XTAL as reference	$\Delta f_{LTX\ CC}$	-0.3	–	0.3	%	with respect to $f_{NOM}(typ)$, over temperature (-40°C to 105°C)
Accuracy	$\Delta f_{LT\ CC}$	-1.7	–	3.4	%	with respect to $f_{NOM}(typ)$, over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to $f_{NOM}(typ)$, over temperature (-40°C to 105°C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_A = +25^\circ\text{C}$.

Table 28 provides the characteristics of the 32 kHz digital controlled oscillator DCO2.

Table 28 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{NOM\ CC}$	–	32.75	–	kHz	under nominal conditions ¹⁾ after trimming
Accuracy	$\Delta f_{LT\ CC}$	-1.7	–	3.4	%	with respect to $f_{NOM}(typ)$, over temperature (0°C to 85°C)
		-3.9	–	4.0	%	with respect to $f_{NOM}(typ)$, over temperature (-40°C to 105°C) ¹⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_A = +25^\circ\text{C}$.

3 Electrical Parameters

3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	$C_L = 50$ pF
		–	–	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

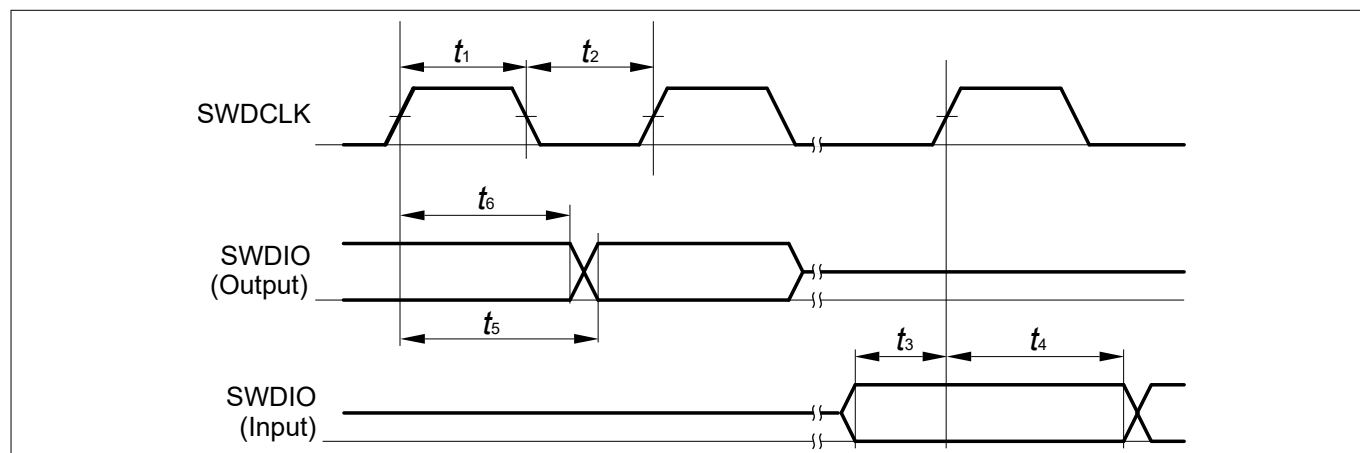


Figure 26 SWD Timing

3 Electrical Parameters

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is $0.75 \mu s$. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles ($0.69 \mu s$).

Table 30 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time ¹⁾	Remark
8 MHz	4	1 to 5	6 to 12	$0.69 \mu s$	The other closest option ($0.81 \mu s$) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with $0.5 + (\text{max. number of } 0_B \text{ sample clocks})$.

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is $\pm 5\%$
- Effective decision time is between $0.69 \mu s$ and $0.75 \mu s$ (calculated with nominal sample frequency)

3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 31 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	$t_{CLK} CC$	$4/MCLK$	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	$t_1 CC$	$t_{CLK}/2 - 28$	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	$t_2 CC$	0	–	–	ns	
Data output DOUT[3:0] valid time	$t_3 CC$	-28	–	28	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	$t_4 SR$	75	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	$t_5 SR$	0	–	–	ns	

3 Electrical Parameters

Table 32 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK} SR	4/ <i>MCLK</i>	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	16	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	21	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	–	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

3 Electrical Parameters

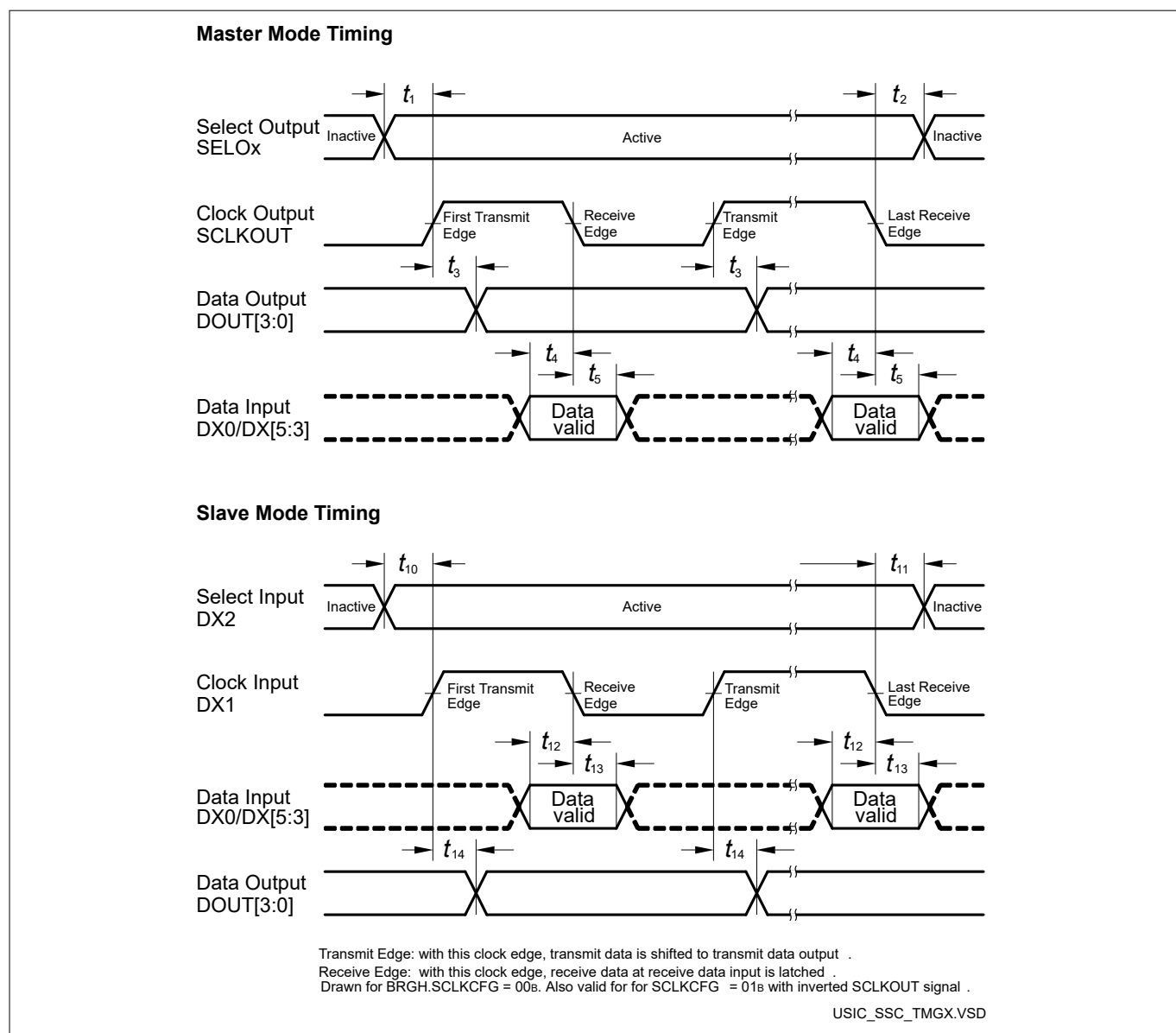


Figure 27 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3 Electrical Parameters

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 33 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	–	–	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	–	–	1000	ns	
Data hold time	t_3 CC/SR	0	–	–	μs	
Data set-up time	t_4 CC/SR	250	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	–	–	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	–	–	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	–	–	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	–	–	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	–	–	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	–	–	μs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 34 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	$20 + 0.1 \cdot C_b^{2)}$	–	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	$20 + 0.1 \cdot C_b$	–	300	ns	
Data hold time	t_3 CC/SR	0	–	–	μs	
Data set-up time	t_4 CC/SR	100	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	–	–	μs	
HIGH period of SCL clock	t_6 CC/SR	0.6	–	–	μs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	–	–	μs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	–	–	μs	
Set-up time for STOP condition	t_9 CC/SR	0.6	–	–	μs	

(table continues...)

3 Electrical Parameters

Table 34 (continued) **USIC IIC Fast Mode Timing¹⁾**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	–	–	μs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

- 1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.
- 2) C_b refers to the total capacitance of one bus line in pF.

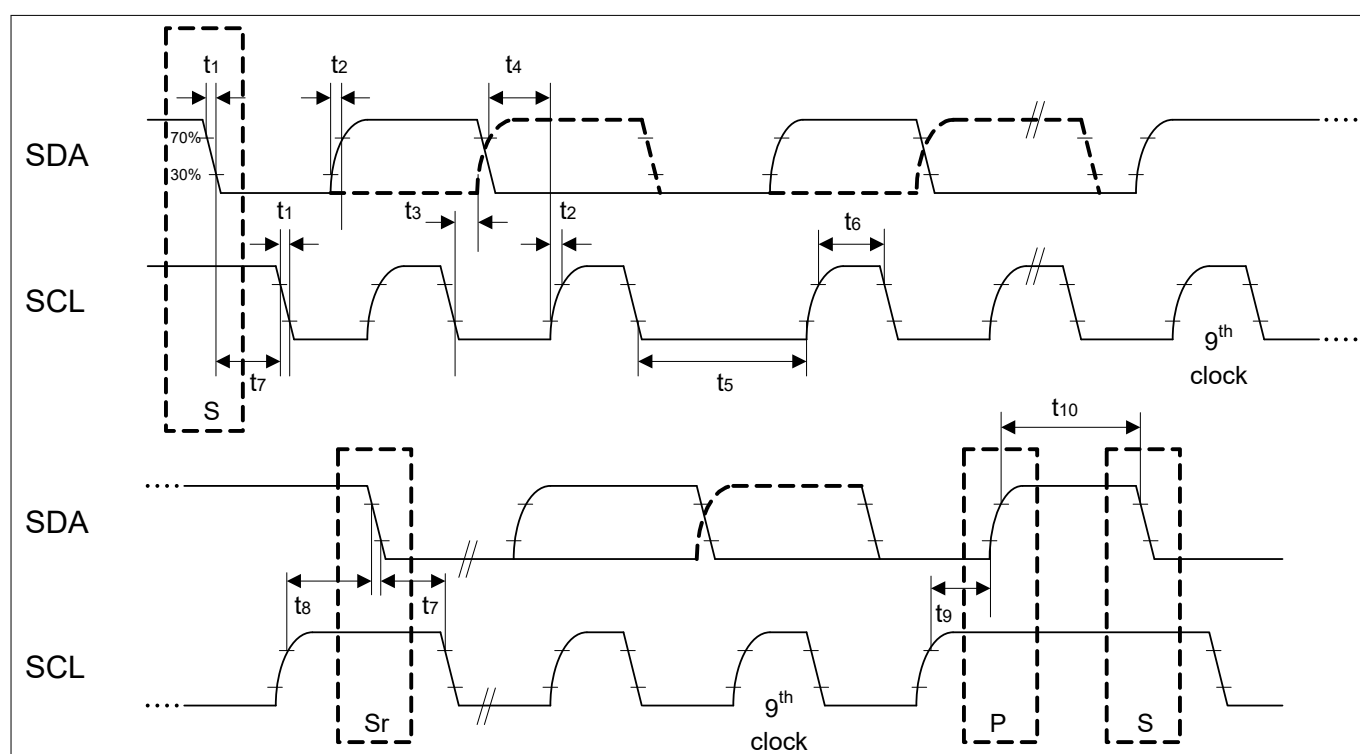


Figure 28 **USIC IIC Timing**

3 Electrical Parameters

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: *Operating Conditions apply.*

Table 35 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$4/f_{MCLK}$	–	–	ns	
Clock HIGH	t_2 CC	$0.35 \times t_{1min}$	–	–	ns	
Clock Low	t_3 CC	$0.35 \times t_{1min}$	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	$0.15 \times t_{1min}$	ns	

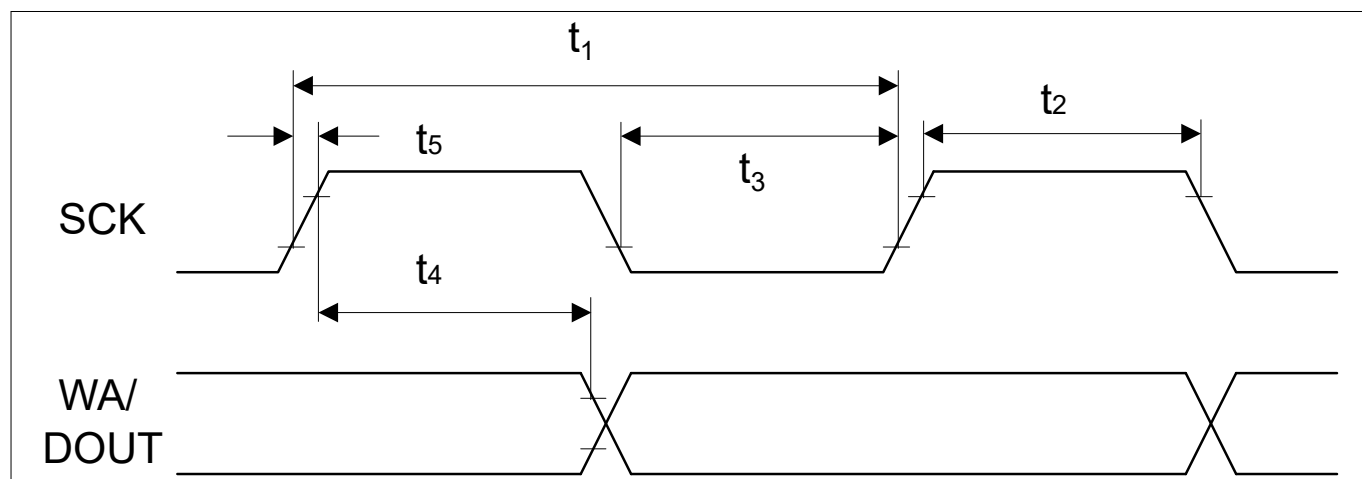


Figure 29 USIC IIS Master Transmitter Timing

3 Electrical Parameters

Table 36 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{\text{MCLK}}$	–	–	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6\text{min}}$	–	–	ns	
Clock Low	t_8 SR	$0.35 \times t_{6\text{min}}$	–	–	ns	
Set-up time	t_9 SR	$0.3 \times t_{6\text{min}}$	–	–	ns	
Hold time	t_{10} SR	15	–	–	ns	

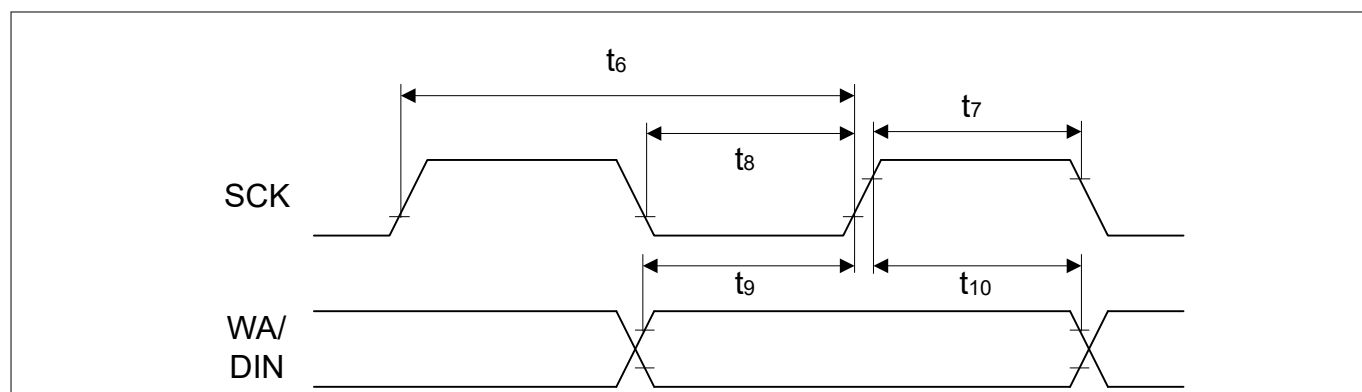


Figure 30 USIC IIS Slave Receiver Timing

4 Package and Reliability

4 Package and Reliability

The XMC1400 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 37 provides the thermal characteristics of the packages used in XMC1400.

Table 37 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	–	3.7 × 3.7	mm	PG-VQFN-40-17
		–	4.2 × 4.2	mm	PG-VQFN-48-73
		–	4.6 × 4.6	mm	PG-VQFN-64-6
Thermal resistance Junction-Ambient	R _{ΘJA} CC	–	86.0	K/W	PG-TSSOP-38-9 ¹⁾
		–	45.3	K/W	PG-VQFN-40-17 ¹⁾
		–	44.9	K/W	PG-VQFN-48-73 ¹⁾
		–	66.7	K/W	PG-LQFP-64-26 ¹⁾
		–	44.7	K/W	PG-VQFN-64-6 ¹⁾
		–	TBD	K/W	PG-LQFP-48-10

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP} , independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115°C.

The difference between junction temperature and ambient temperature is determined by

$$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

4 Package and Reliability

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

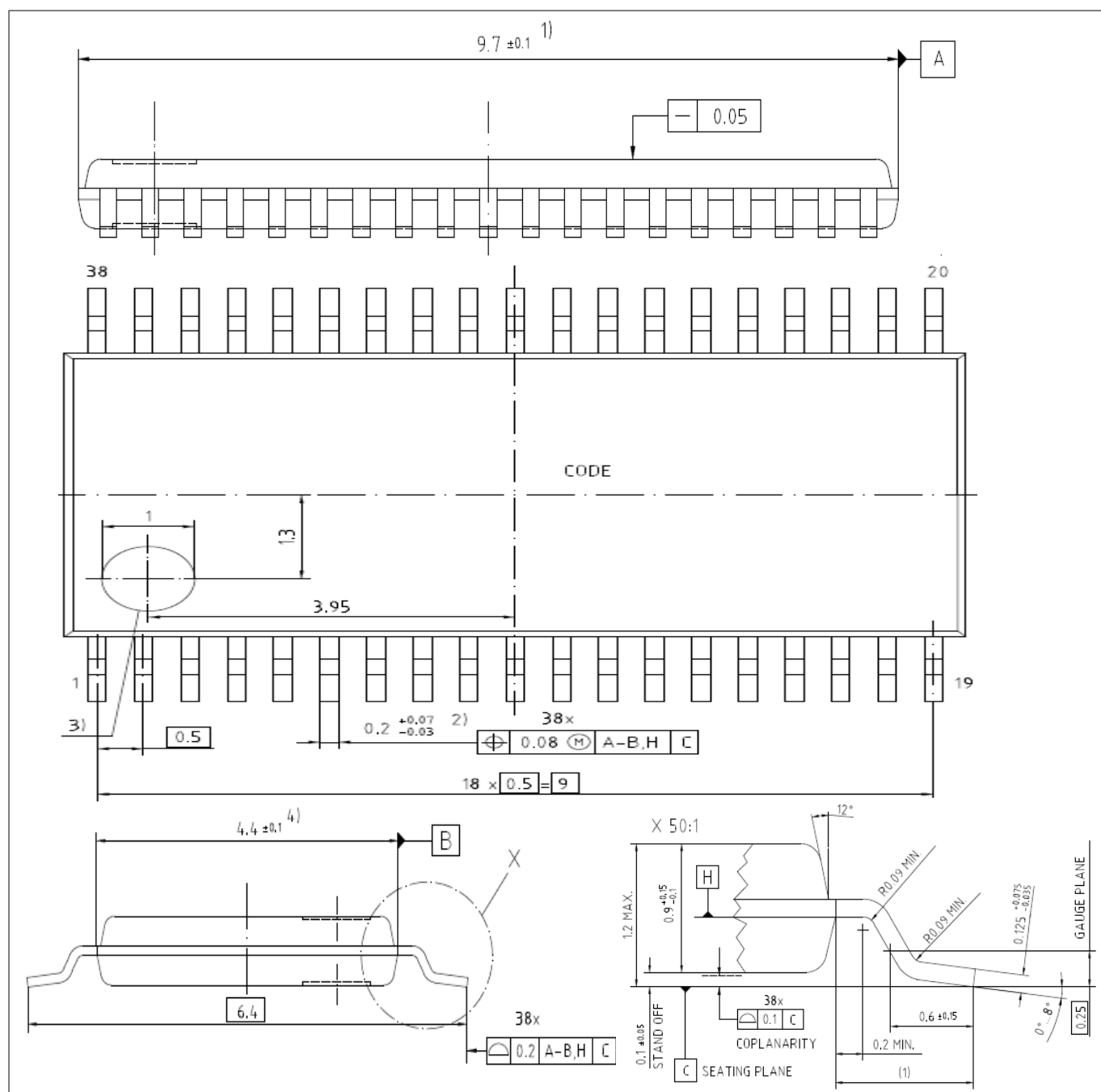


Figure 31 PG-TSSOP-38-9

4 Package and Reliability

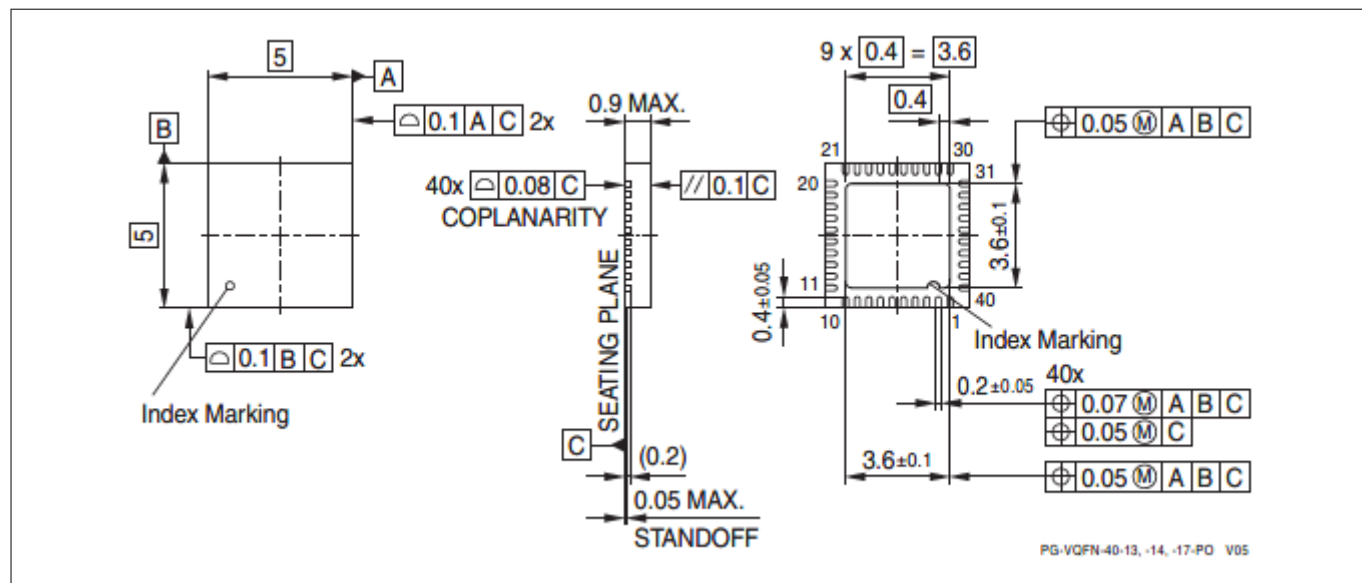


Figure 32 PG-VQFN-40-17

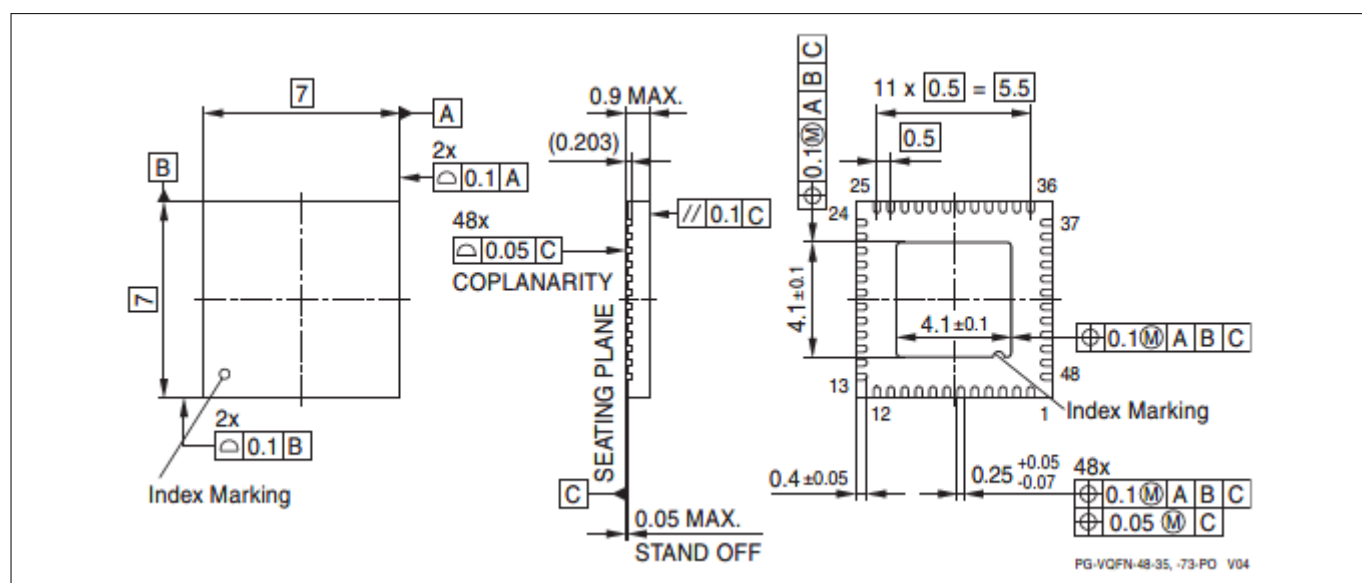


Figure 33 PG-VQFN-48-73

XMC1400 AA-Step Microcontroller Series for Industrial Applications

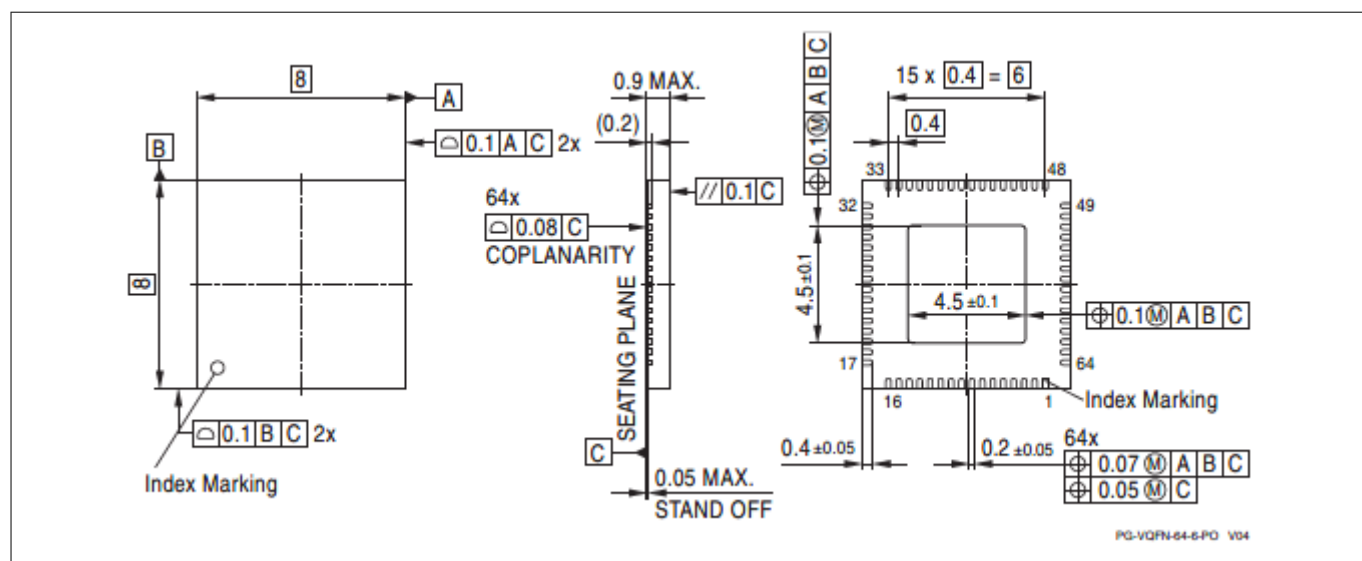


Figure 34 **PG-VQFN-64-6**

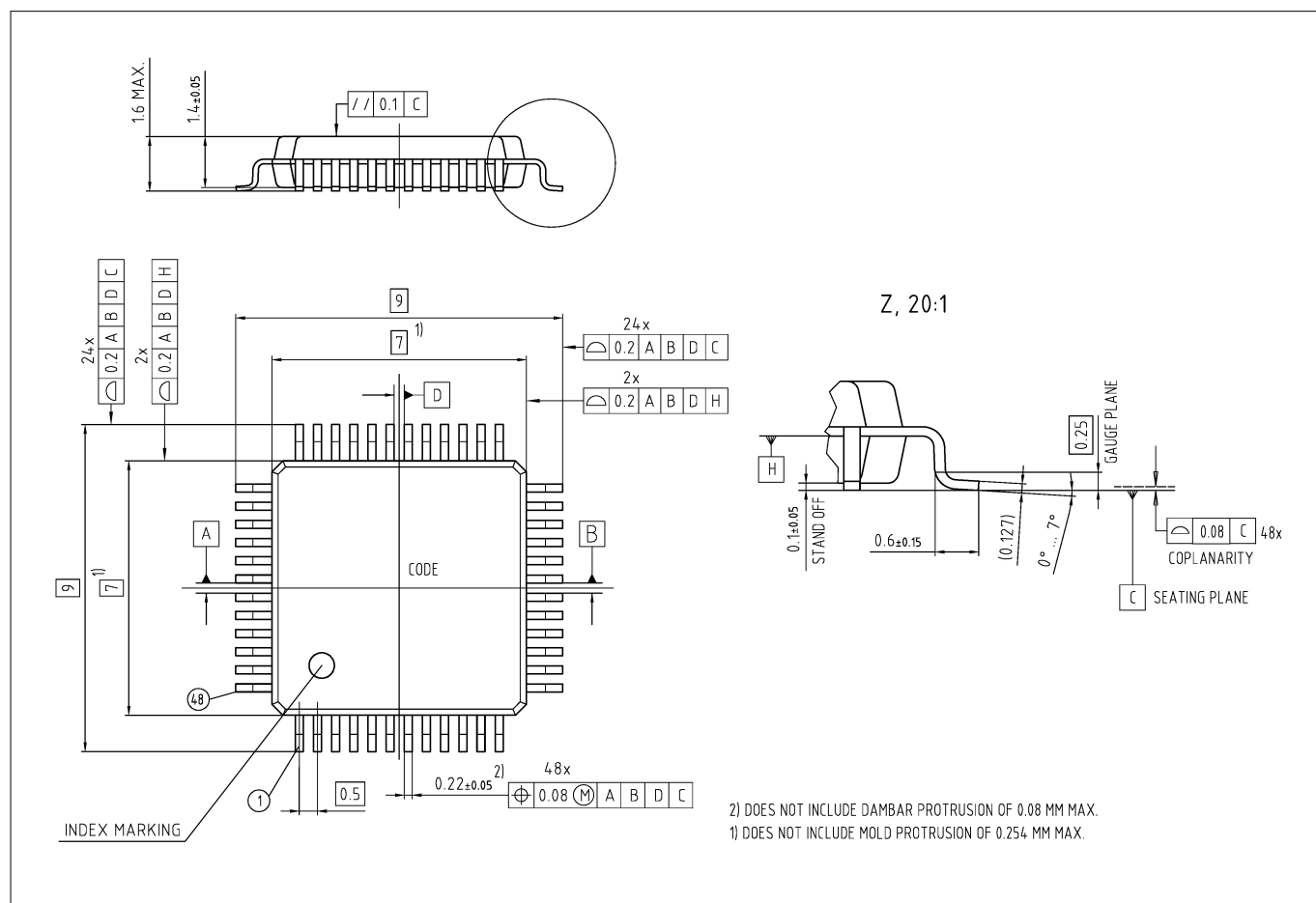


Figure 35 **PG-LQFP-48-10**

4 Package and Reliability

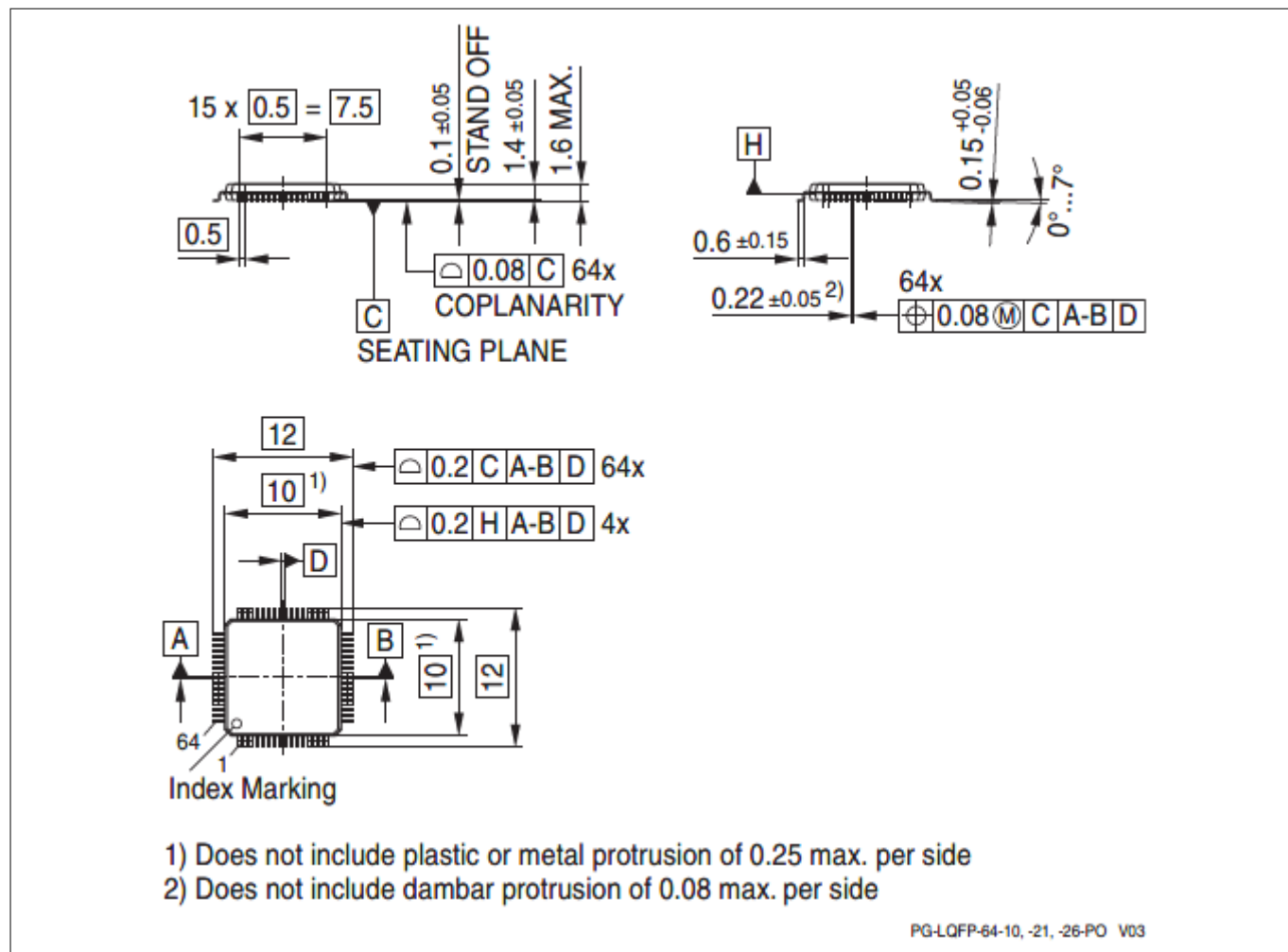


Figure 36 **PG-LQFP-64-26**

All dimensions in mm.

5 Quality Declaration

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMC1400.

Table 38 **Quality Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	4000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	–	1000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	–	JEDEC J-STD-020D
• TSSOP-38, LQFP-64			3		
• VQFN-40, VQFN-48, VQFN-64			1		
• LQFP-48			3		
Soldering temperature	T_{SDR} SR	–	260	°C	Profile according to JEDEC J-STD-020D

Revision history

Revision history

Document revision	Date	Description of changes
V1.0	2016-02	The device provides four USIC channels. XMC1401 devices available for max. ambient temperature of 85°C. Reformatted pinout table. Updated footnote to the definition of the start-up times of OSC_XTAL and RTC_XTAL oscillators. Added Δf_{LT} parameter to on-chip oscillators DCO1 and DCO2. Updated package outline drawings.
V1.1	2016-06	Added TSSOP-38-9 package Added XMC1402-T038 marking variants in TSSOP-38 Added XMC1403-Q040 marking variants
V1.2	2016-08	Added XMC™ trademark Added XMC1402-T038X0200, XMC1402-Q040X0200 and XMC1402-Q048X0200 marking variants
V1.3	2016-10	In Absolute Maximum Ratings renamed parameter V_{CM} to V_{INP2} , as the limitation is related to most P2 pins, also if no ACMP is available. Clarified limit to pins P2.[1,2,6:9,11] in Overload specification. Corrected XMC1402-T038X0200 and XMC1402-Q048X0200 marking variants in Table 2 .
V1.4	2017-11	Added XMC1404-Q040 variants in Table 1 Added XMC1404-Q040 variants in Table 2 Added XMC1404-Q040 variants in Table 3
V1.5	2024-04	Updated CHIP ID - 1 bit from 0 to 1 in Table 3 Release to web
V1.6	2025-01-22	Updated template. Removed Tools from Features section. Updated Moisture sensitivity level in Quality Declaration section.
V1.7	2025-07-17	Added XMC1401, XMC1402, XMC1404 in LQFP-48 package (Table 1 , Table 2 , Table 3 , Table 5 , Figure 5 , Figure 10 , Figure 35). Added XMC1401 in TSSOP-38 package (Table 1 , Table 2 , Table 3). Updated ESD ratings in Table 38 .

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