

# TLE9563-3QX

## BLDC Motor System IC



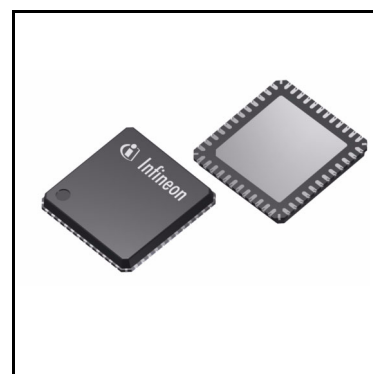
RoHS



## 1 Overview

### Features

- Low-drop voltage regulator 5 V, 250 mA for main supply
- Three half-bridge gate drivers for external N-channel MOSFETs
- Adaptive MOSFET gate control:
  - Regulation of the MOSFET switching time
  - Reduced switching losses in PWM mode
  - High efficient constant gate charge
- Control of reverse battery protection MOSFET
- One low-side capable current sense amplifier (CSA) with configurable gain for protection and diagnosis
- High-speed CAN transceiver supporting CAN FD communication up to 5 Mbit/s according to ISO11898-2:2016 including selective wake-up functionality via CAN partial networking and CAN FD tolerant mode
- Configurable wake-up sources
- Three high-side outputs 7  $\Omega$  typ.
- Six PWM inputs
  - High-side and low-side PWM capable
  - Active free-wheeling
  - Up to 25 kHz PWM frequency
- 32 bit serial peripheral interface (SPI) with cyclic redundancy check (CRC)
- Very low quiescent current consumption in Stop Mode and Sleep Mode
- Periodic cyclic sense and cyclic wake in Normal Mode, Stop Mode and Sleep Mode
- Reset and interrupt output
- Drain-source monitoring and open-load detection
- Configurable time-out and window watchdog
- Overtemperature and short circuit protection features
- Leadless power package with support of optical lead tip inspection
- Green Product (RoHS compliant)



## Overview

### Potential applications

- Auxiliary pumps (fuel, water, etc.)
- Blower motor
- Engine cooling fan
- Sunroof module
- Transfer case

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The TLE9563-3QX is a multifunctional system IC with integrated power supply, communication interfaces, multiple half-bridges and support features in an exposed pad PG-VQFN-48 power package. The device is designed for various motor control automotive applications.

To support these applications, the BLDC Motor System IC provides the main functions, such as a 5 V low-dropout voltage regulator one HS-CAN transceiver supporting CAN FD, CAN Partial Networking (incl. FD tolerant mode), three half-bridges for BDLC motor control, one current sense amplifier and one 32 bit serial peripheral interface (SPI).

The device includes diagnostic and supervision features, such as drain-source monitoring and open-load detection, short circuit protection, configurable time-out and window watchdog, as well as overtemperature protection.

Type	Package	Marking
TLE9563-3QX	PG-VQFN-48	TLE9563-3QX

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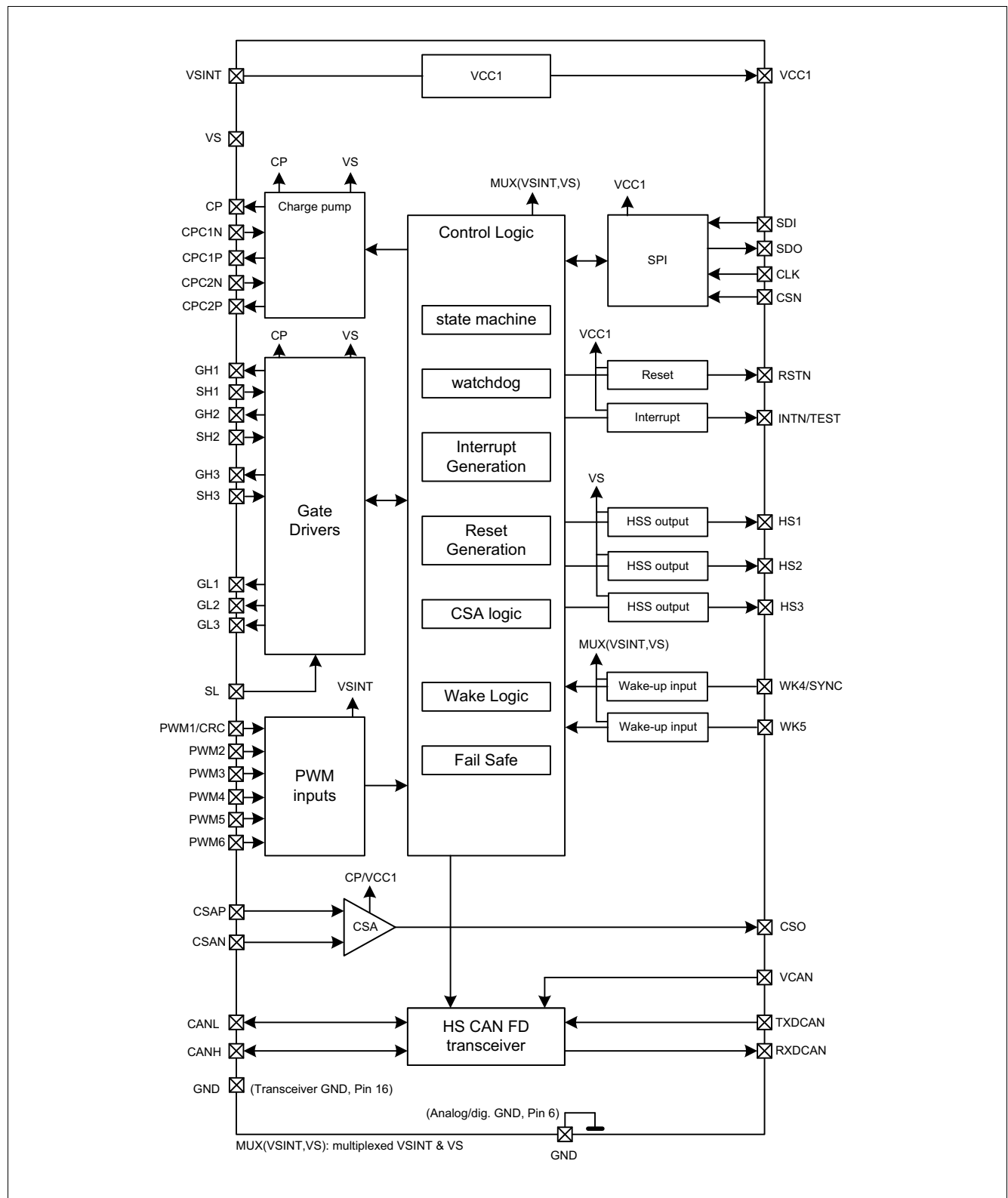
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## Block Diagram

### 2 Block Diagram



**Figure 1 Block Diagram**



## Pin Configuration

### 3 Pin Configuration

#### 3.1 Pin Assignment

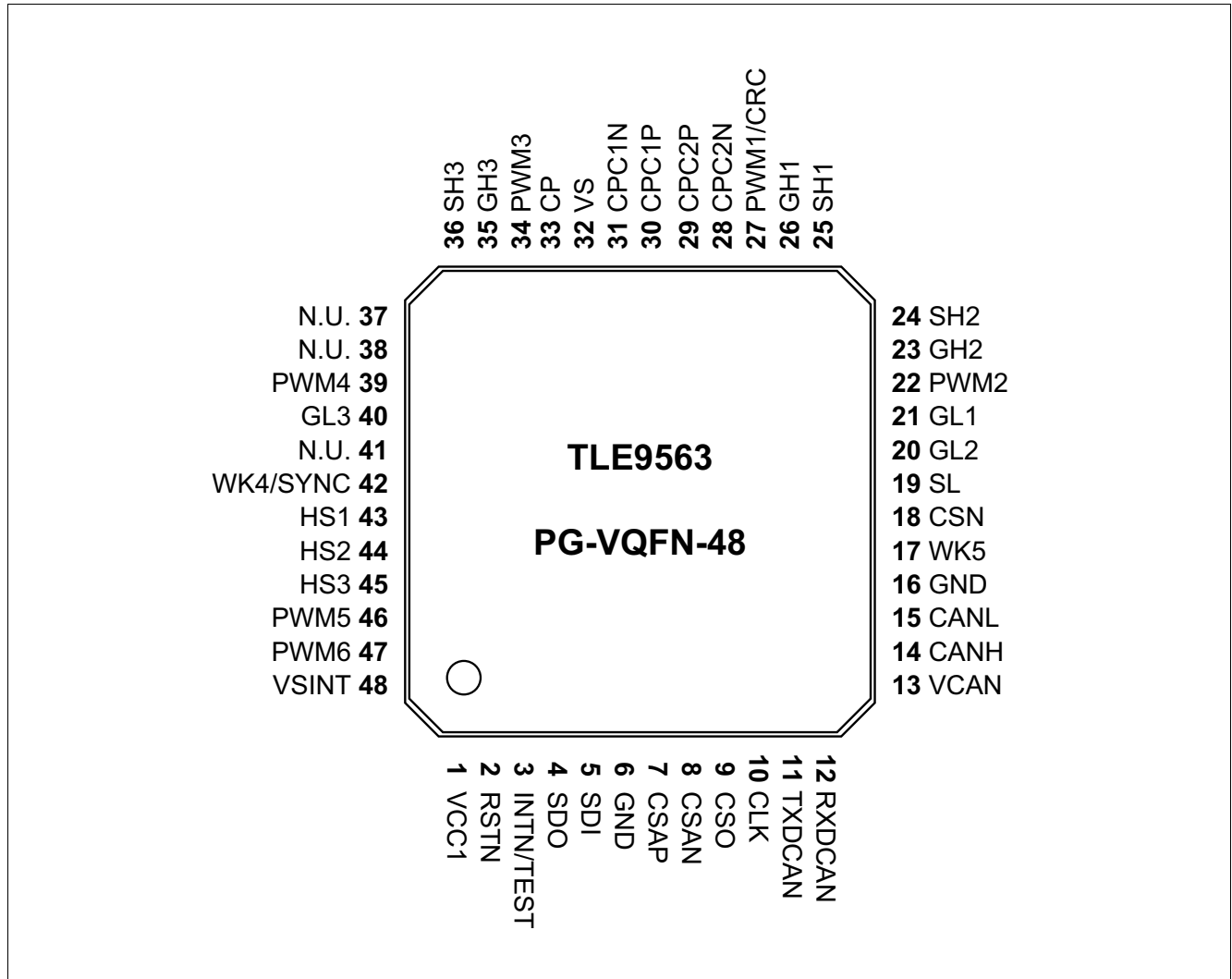


Figure 2 Pin Configuration

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	VCC1	<b>Voltage Regulator.</b> Output voltage 1
2	RSTN	<b>Reset Output.</b> Active LOW, internally passive pull-up with open-drain output
3	INTN/TEST	<b>Interrupt Output.</b> Active LOW output, push-pull structure <b>TEST.</b> Connect to GND (via pull-down) to activate Software Development Mode
4	SDO	<b>SPI Data Output to Microcontroller</b> (=MISO). Push-pull structure
5	SDI	<b>SPI Data Input from Microcontroller</b> (=MOSI). Internal pull-down
6	GND	<b>Ground.</b> Analog/digital ground
7	CSAP	<b>Not Inverting input of Current Sense Amplifier.</b>

**Pin Configuration**

Pin	Symbol	Function
8	CSAN	<b>Inverting input of Current Sense Amplifier.</b>
9	CSO	<b>Current Sense Amplifier Output.</b>
10	CLK	<b>SPI Clock Input.</b> Internal passive pull-down
11	TXDCAN	<b>Transmit CAN.</b> Internal passive pull-up
12	RXDCAN	<b>Receive CAN.</b> Push-pull structure
13	VCAN	<b>HS-CAN Supply Input.</b> For internal HS-CAN cell needed for CAN Normal Mode
14	CANH	<b>CAN High Bus.</b>
15	CANL	<b>CAN Low Bus.</b>
16	GND	<b>Ground.</b> Transceiver ground (CAN)
17	WK5	<b>Wake-up input 5.</b>
18	CSN	<b>SPI Chip Select Not input.</b> Internal passive pull-up
19	SL	<b>Source Low Side.</b>
20	GL2	<b>Gate Low Side 2.</b>
21	GL1	<b>Gate Low Side 1.</b>
22	PWM2	<b>PWM input 2.</b> Internal passive pull-up
23	GH2	<b>Gate High Side 2.</b>
24	SH2	<b>Source High Side 2.</b>
25	SH1	<b>Source High Side 1.</b>
26	GH1	<b>Gate High Side 1.</b>
27	PWM1/CRC	<b>PWM input 1.</b> Internal passive pull-down <b>CRC.</b> Connect to GND (via pull-down) to activate CRC functionality
28	CPC2N	<b>Negative connection to Charge Pump Capacitor 2.</b>
29	CPC2P	<b>Positive connection to Charge Pump Capacitor 2.</b>
30	CPC1P	<b>Positive connection to Charge Pump Capacitor 1.</b>
31	CPC1N	<b>Negative connection to Charge Pump Capacitor 1.</b>
32	VS	<b>Supply voltage for HSx, Bridge Drivers and Charge pump.</b> Connected to the battery voltage after reverse protection.
33	CP	<b>Charge Pump output voltage.</b>
34	PWM3	<b>PWM input 3.</b> Internal passive pull-down
35	GH3	<b>Gate High Side 3.</b>
36	SH3	<b>Source High Side 3.</b>
37	N.U.	<b>Not used.</b>
38	N.U.	<b>Not used.</b>
39	PWM4	<b>PWM input 4.</b> Internal passive pull-down
40	GL3	<b>Gate Low Side 3.</b>
41	N.U.	<b>Not used.</b>
42	WK4/SYNC	<b>Wake-up input 4/Sync.</b>
43	HS1	<b>High Side output 1.</b>
44	HS2	<b>High Side output 2.</b>

## Pin Configuration

Pin	Symbol	Function
45	HS3	<b>High Side output 3.</b>
46	PWM5	<b>PWM input 5.</b> Internal passive pull-down
47	PWM6	<b>PWM input 6.</b> Internal passive pull-down
48	VSINT	<b>Voltage regulator and main supply voltage.</b> Connected to the battery voltage after reverse protection
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground <sup>1)</sup>

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the device via the PCB. The exposed die pad is not connected to any active part of the IC. However, it should be connected to GND for the best EMC performance.

*Note: The GND pin as well as the Cooling Tab must be connected to one common GND potential.*

### 3.3 Hints for not functional pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI. Unused pins should be handled as follows:

- **N.U.:** not used; internally bonded for testing purpose; leave open.
- **RSVD:** must be connected to GND.

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage VS	$V_{S, \max}$	-0.3	–	28	V	–	P_4.1.1
Supply Voltage VS	$V_{S, \max}$	-0.3	–	40	V	Load Dump	P_4.1.2
Supply Voltage VSINT	$V_{SINT, \max}$	-0.3	–	28	V	–	P_4.1.3
Supply Voltage VSINT	$V_{SINT, \max}$	-0.3	–	40	V	Load Dump	P_4.1.4
Voltage Regulator 1	$V_{CC1, \max}$	-0.3	–	5.5	V		P_4.1.7
Charge Pump Output Pin (CP)	$V_{CP, \max}$	$V_S - 0.8$	–	$V_S + 17$	V	$I_{CP} > -200 \mu A$ if CP is disabled	P_4.1.8
CPC1P, CPC2P	$V_{CPCxP, \max}$	- 0.3	–	$V_S + 17$	V		P_4.1.38
CPC1N, CPC2N	$V_{CPCxN, \max}$	- 0.3	–	$V_S + 0.3$	V		P_4.1.39
Bridge Driver Gate High Side (GHx)	$V_{GHx, \max}$	-8.0	–	40	V	–	P_4.1.11
Bridge Driver Gate Low Side (GLx)	$V_{GLx, \max}$	-8.0	–	24	V	–	P_4.1.12
Voltage difference between GHx-SHx and between GLx-SLx	$V_{GS}$	-0.3	–	16	V	–	P_4.1.13
Bridge Driver Source High (SHx)	$V_{SHx, \max}$	-8.0	–	40	V	–	P_4.1.14
Bridge Driver Source Low Side SL	$V_{SL, \max}$	-8.0	–	6.0	V	–	P_4.1.15
Current Sense Amplifier inputs (CSAP, CSAN)	$V_{CSx, \max}$	-8.0	–	+8.0	V	–	P_4.1.16
Current Sense Amplifier Output CSO	$V_{CSx, \max}$	-0.3	–	$V_{CC1} + 0.3$	V	–	P_4.1.17
Differential input voltage range CSAPx - CSANx	$V_{CSA, Diff}$	-8.0	–	8.0	V	–	P_4.1.18
Wake Input WKx	$V_{WKx, \max}$	-0.3	–	40	V	–	P_4.1.19
High Side HSx	$V_{HSx, \max}$	-0.3	–	$V_{S, \max} + 0.3$	V	–	P_4.1.20
CANH, CANL	$V_{BUS, \max}$	-27	–	40	V	–	P_4.1.22

## General Product Characteristics

**Table 1 Absolute Maximum Ratings<sup>1)</sup>** (cont'd)

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWM1/CRC, PWM2, PWM3, PWM4, PWM 5, PWM6 Input Pins	$V_{\text{PWM1-2-3-4-5-6, max}}$	-0.3	–	40	V	–	P_4.1.25
Logic Input Pins (SDI, CLK, TXDCAN, TXDLIN)	$V_{\text{I, max}}$	-0.3	–	$V_{\text{CC1}} + 0.3$	V	–	P_4.1.28
CSN	$V_{\text{CSN}}$	-0.3	–	40	V	–	P_4.1.29
Logic Output Pins (SDO, RSTN, INTN, RXDCAN)	$V_{\text{O, max}}$	-0.3	–	$V_{\text{CC1}} + 0.3$	V	–	P_4.1.30
VCAN Input Voltage	$V_{\text{VCAN, max}}$	-0.3	–	5.5	V	–	P_4.1.31

### Temperatures

Junction Temperature	$T_j$	-40	–	150	$^{\circ}\text{C}$	–	P_4.1.32
Storage Temperature	$T_{\text{stg}}$	-55	–	150	$^{\circ}\text{C}$	–	P_4.1.33

### ESD Susceptibility

ESD Resistivity	$V_{\text{ESD,11}}$	-2	–	2	kV	HBM <sup>2)</sup>	P_4.1.34
ESD Resistivity to GND, CANH, CANL	$V_{\text{ESD,12}}$	-8	–	8	kV	HBM <sup>2)3)</sup>	P_4.1.35
ESD Resistivity to GND	$V_{\text{ESD,21}}$	-500	–	500	V	CDM <sup>4)</sup>	P_4.1.36
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND	$V_{\text{ESD,22}}$	-750	–	750	V	CDM <sup>4)</sup>	P_4.1.37

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

3) For ESD “GUN” Resistivity (according to IEC61000-4-2 “gun test” (150 pF, 330 Ω)), is shown in Application Information and test report will be provided from IBEE.

4) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1.

### Notes

- Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## General Product Characteristics

### 4.2 Functional Range

**Table 2 Functional Range<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	$V_{SINT,func}$	$V_{POR,f}$	–	28	V	<sup>2)</sup>	P_4.2.1
Bridge Supply Voltage	$V_{S,func}$	6.0	–	28	V	–	P_4.2.2
CAN Supply Voltage	$V_{CAN,func}$	4.75	–	5.25	V	–	P_4.2.4
Junction Temperature	$T_j$	-40	–	150	°C	–	P_4.2.6

1) Not subject to production test, specified by design.

2) Including Power-On Reset, Over- and Undervoltage Protection.

*Note:* Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

#### Device Behavior Outside of Specified Functional Range

- $28\text{ V} < V_{SINT,func} < 40\text{ V}$ : Device will still be functional including the state machine; the specified electrical characteristics might not be ensured anymore. The  $V_{CC1}$  is working properly, however, a thermal shutdown might occur due to high power dissipation. HSx switches might be turned OFF depending on HSx\_OV configurations. The specified SPI communication speed is ensured; the absolute maximum ratings are not violated, however the device is not intended for continuous operation of  $V_{SINT} > 28\text{ V}$  and a thermal shutdown might occur due to high power dissipation. The device operation at high junction temperatures for long periods might reduce the operating life time.

Note:  $V_{CAN} < 4.75\text{ V}$ : The undervoltage bit will be set in the SPI register and the transmitter will be disabled as long as the UV condition is present.

Note:  $5.25\text{ V} < V_{CAN} < 5.5\text{ V}$ : CAN transceiver still functional. However, the communication might fail due to out-of-spec operation.

- $V_{POR,f} < V_{SINT} < 5.5\text{ V}$  (given the fact that the device was powered up correctly before with  $V_{SINT} > 5.5\text{ V}$ ): Device will still be functional; the specified electrical characteristics might not be ensured anymore:
  - The voltage regulator will enter the low-drop operation mode.
  - A reset could be triggered depending on the Vrtlx settings.
  - HSx switch behavior will depend on the respective configuration:  
**HS\_UV\_SD\_DIS** = '0' (default): HSx will be turned OFF for  $V_S < V_{S,UVd}$  and will stay OFF.  
**HS\_UV\_SD\_DIS** = '1': HSx stays on as long as possible. An unwanted overcurrent shut down may occur. OC shut down bit set and the respective HSx switch will stay OFF.
  - The specified SPI communication speed is ensured.

*Note:*  $V_{S,UV} < V_S < 6.0\text{ V}$ : the charge pump might be deactivated due to a charge pump undervoltage detection, resulting in a turn-off of the external MOSFETs.

**General Product Characteristics**

### 4.3 Thermal Resistance

**Table 3 Thermal Resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	$R_{th(JSP)}$	–	7.2	–	K/W	Exposed Pad	P_4.3.1
Junction to Ambient	$R_{th(JA)}$	–	27	–	K/W	<sup>2)</sup>	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified  $R_{th(JA)}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for a power dissipation of 1.5 W; the product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm C); where applicable a thermal via array under the exposed pad contacted the first inner copper layer and 300 mm<sup>2</sup> cooling areas on the top layer and bottom layers (70 µm).

### 4.4 Current Consumption

**Table 4 Current Consumption**

Current consumption values are specified at  $T_j = 25^\circ\text{C}$ ,  $V_{SINT} = V_S = 13.5\text{ V}$ , all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Normal Mode							
Normal Mode current consumption	$I_{\text{Normal}}$	–	4.5	5.5	mA	<sup>1)</sup> $V_{\text{SINT}} = 5.5 \text{ V to } 28 \text{ V}$ ; $T_j = -40^{\circ}\text{C to } +150^{\circ}\text{C}$ ; CAN=CP=off	P_4.4.1
Stop Mode							
Stop Mode current consumption (low active peak threshold)	$I_{\text{Stop}_{1,25}}$	–	50	65	μA	<sup>1)2)</sup> CSA=CAN <sup>3)</sup> =off; WKx=HSx=CP=off; Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{\text{CC1}}$ ; <b>I_PEAK_TH</b> = 0 <sub>B</sub>	P_4.4.2
Stop Mode current consumption (low active peak threshold)	$I_{\text{Stop}_{1,85}}$	–	55	80	μA	<sup>1)2)4)</sup> $T_j = 85^{\circ}\text{C}$ ; CSA=CAN <sup>3)</sup> =off; WKx=HSx=CP=off; Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{\text{CC1}}$ ; <b>I_PEAK_TH</b> = 0 <sub>B</sub>	P_4.4.3
Stop Mode current consumption (high active peak threshold)	$I_{\text{Stop}_{2,25}}$	–	70	95	μA	<sup>1)2)</sup> CSA=CAN <sup>3)</sup> =off; WKx=HSx=CP=off; Cyclic Wak./Sen.=off Watchdog = off; no load on $V_{\text{CC1}}$ ; <b>I_PEAK_TH</b> = 1 <sub>B</sub>	P_4.4.4

**General Product Characteristics**

**Table 4 Current Consumption (cont'd)**

Current consumption values are specified at  $T_j = 25^\circ\text{C}$ ,  $V_{\text{SINT}} = V_S = 13.5\text{ V}$ , all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Stop Mode current consumption (high active peak threshold)	$I_{\text{Stop}_2,85}$	–	75	105	$\mu\text{A}$	<sup>1)2)4)</sup> $T_j = 85^\circ\text{C}$ ; CSA=CAN <sup>3)</sup> =off; Cyclic Wak./Sen.=off; Watchdog = off; no load on $V_{\text{CC1}}$ ; <b><math>I_{\text{PEAK\_TH}} = 1_B</math></b>	P_4.4.5

**Sleep Mode**

Sleep Mode current consumption	$I_{\text{Sleep},25}$	–	18	30	$\mu\text{A}$	<sup>1)</sup> CSA=CAN <sup>3)</sup> =off; WKx=HSx=CP=off; Cyclic Wak./Sen.= off	P_4.4.6
Sleep Mode current consumption	$I_{\text{Sleep},85}$	–	28	40	$\mu\text{A}$	<sup>1)4)</sup> $T_j = 85^\circ\text{C}$ ; CSA=CAN <sup>3)</sup> =off; WKx=HSx=CP=off; Cyclic Wak./Sen.=off	P_4.4.7

**Feature Incremental Current Consumption**

Current consumption for CAN module, recessive state	$I_{\text{CAN,rec}}$	–	2	3.5	$\text{mA}$	<sup>1)4)</sup> Normal/Stop Mode; CAN Normal Mode; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ ; $V_{\text{CC1}}$ connected to $V_{\text{CAN}}$ ; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no RL on CAN	P_4.4.13
Current consumption for CAN module, dominant state	$I_{\text{CAN,dom}}$	–	3	5.0	$\text{mA}$	<sup>1)4)</sup> Normal/Stop Mode; CAN Normal Mode; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ ; $V_{\text{CC1}}$ connected to $V_{\text{CAN}}$ ; $V_{\text{TXDCAN}} = \text{GND}$ ; no RL on CAN	P_4.4.14
Current consumption for CAN module, Receive Only Mode, Normal Mode	$I_{\text{CAN,Rec\_onlyN}}$	–	0.5	0.7	$\text{mA}$	<sup>1)4)5)</sup> Normal Mode; CAN Receive Only Mode; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ ; $V_{\text{CC1}}$ connected to $V_{\text{CAN}}$ ; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no RL on CAN	P_4.4.15



**General Product Characteristics**

**Table 4 Current Consumption (cont'd)**

Current consumption values are specified at  $T_j = 25^\circ\text{C}$ ,  $V_{\text{SINT}} = V_S = 13.5\text{ V}$ , all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for CAN module, Receive Only Mode, Stop Mode	$I_{\text{CAN,Rec\_only}}$	–	1.4	1.5	mA	<sup>1)4)5)</sup> Stop Mode; CAN Receive Only Mode; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ ; $V_{\text{CC1}}$ connected to $V_{\text{CAN}}$ ; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no RL on CAN	P_4.4.16
Current consumption for CAN wake capability (tsilence expired)	$I_{\text{CAN,wake,25}}$	–	4.5	7	$\mu\text{A}$	<sup>1)3)6)</sup> Sleep Mode; CAN wake capable;	P_4.4.17
Current consumption for CAN wake capability (tsilence expired)	$I_{\text{CAN,wake,85}}$	–	8	10	$\mu\text{A}$	<sup>1)3)4)6)</sup> Sleep Mode; $T_j = 85^\circ\text{C}$ ; CAN wake capable; WK = off;	P_4.4.18
Current consumption during CAN Partial Networking frame detect mode (RX_WK_SEL= '0')	$I_{\text{CAN,SWK,25}}$	–	475	550	$\mu\text{A}$	<sup>1)4)</sup> $T_j = 25^\circ\text{C}$ ; Stop Mode; WK, CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN;	P_4.4.19
Current consumption during CAN Partial Networking frame detect mode (RX_WK_SEL= '0')	$I_{\text{CAN,SWK,85}}$	–	500	575	$\mu\text{A}$	<sup>1)4)</sup> $T_j = 85^\circ\text{C}$ ; Stop Mode; WK, CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN;	P_4.4.20
Current consumption for each WK input	$I_{\text{WK,wake,25}}$	–	0.2	2	$\mu\text{A}$	<sup>1)6)7)8)</sup> Sleep Mode; WK wake capable; no activity on WK pin;	P_4.4.22
Current consumption for each WK input	$I_{\text{WK,wake,85}}$	–	0.5	3	$\mu\text{A}$	<sup>1)4)6)7)8)</sup> Sleep Mode; $T_j = 85^\circ\text{C}$ ; WK wake capable; no activity on WK pin;	P_4.4.23
Current consumption for first High-Side in Stop Mode	$I_{\text{Stop,HS,25}}$	–	250	375	$\mu\text{A}$	<sup>4)6)9)11)10)</sup> Stop Mode; HS with 100% duty cycle (no load);	P_4.4.24

**General Product Characteristics**

**Table 4 Current Consumption (cont'd)**

Current consumption values are specified at  $T_j = 25^\circ\text{C}$ ,  $V_{\text{SINT}} = V_S = 13.5\text{ V}$ , all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for first High-Side in Stop Mode	$I_{\text{Stop,HS,85}}$	–	250	375	$\mu\text{A}$	<sup>4)6)9)11)10)</sup> Stop Mode; $T_j = 85^\circ\text{C}$ ; HS with 100% duty cycle (no load);	P_4.4.25
Current consumption for cyclic sense function	$I_{\text{Stop,CS25}}$	–	20	26	$\mu\text{A}$	<sup>6)9)11)12)</sup> Stop Mode; WD = off;	P_4.4.26
Current consumption for cyclic sense function	$I_{\text{Stop,CS85}}$	–	24	32	$\mu\text{A}$	<sup>4)6)9)11)12)</sup> Stop Mode; $T_j = 85^\circ\text{C}$ ; WD = off;	P_4.4.27
Current consumption for watchdog active in Stop Mode	$I_{\text{Stop,WD25}}$	–	18	23	$\mu\text{A}$	<sup>4)13)</sup> Stop Mode; Watchdog running;	P_4.4.28
Current consumption for watchdog active in Stop Mode	$I_{\text{Stop,WD85}}$	–	19	25	$\mu\text{A}$	<sup>4)13)</sup> Stop Mode; $T_j = 85^\circ\text{C}$ ; Watchdog running;	P_4.4.29
Current Sense Amplifier	$I_{\text{CSA1}}$	–	–	4	mA	<sup>13)</sup> <b>CSA_OFF</b> = 0 <sub>B</sub> ; VCSP = VCSAP = VCSAN = 0 V; <b>CSO_CAP</b> = 0 <sub>B</sub> ; CCSO = 330 pF	P_4.4.31
Current Sense Amplifier	$I_{\text{CSA2}}$	–	–	10	mA	<sup>13)</sup> <b>CSA_OFF</b> = 0 <sub>B</sub> ; VCSP = VCSAP = VCSAN = 0 V; <b>CSO_CAP</b> = 1 <sub>B</sub> ; CCSO = 2.2 nF	P_4.4.36
Current consumption in parking braking mode (LSx ON)	$I_{\text{parking}}$	–	10	14	$\mu\text{A}$	<sup>4)13)</sup> Stop Mode or Sleep Mode; $T_j < 85^\circ\text{C}$ ; <b>PARK_BRK_EN</b> = 1 <sub>B</sub>	P_4.4.32
Current consumption Over voltage braking mode (LSx OFF)	$I_{\text{OV,LS\_OFF}}$	–	7	10	$\mu\text{A}$	<sup>4)13)</sup> Stop Mode or Sleep Mode; $T_j < 85^\circ\text{C}$ ; <b>OV_BRK_EN</b> = 1 <sub>B</sub>	P_4.4.34
Current consumption in VS for Charge Pump and Bridge Driver	$I_{\text{CP,BD}}$	–	30	40	mA	Normal Mode; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ ; <b>CPEN</b> = 1; All HB OFF	P_4.4.35

1) Measured at  $V_{\text{SINT}}$ .

2) If the load current on  $V_{\text{CC1}}$  will exceed the configured  $V_{\text{CC1}}$  active peak threshold, the current consumption will increase by typ. 2.9 mA to ensure optimum dynamic load behavior. See also [Chapter 6](#).

3) CAN not configured in Selective Wake Mode.

4) Not subject to production test, specified by design.

5) Current consumption adder also applies for during WUF detection (frame detect mode) when CAN Partial Networking is activated.

6) Current consumption adders of features defined for Stop Mode also apply for Sleep Mode and vice versa. Wake input signals are stable (i.e. not toggling), cyclic wake/sense & watchdog are OFF (unless otherwise specified).

7) No pull-up or pull-down configuration selected.

## General Product Characteristics

- 8) The specified WKx current consumption adder for wake capability applies regardless how many WK inputs are activated.
- 9) Additional current will be drawn from  $V_S$  and  $V_{SINT}$ .
- 10) Typical adder of additional high-side switch activation 200  $\mu$ A.
- 11) HSx used for cyclic sense, Timerx with 20ms period, 0.1 ms on-time, no load.  
In general the current consumption adder for cyclic sense in Stop Mode can be calculated with below equation:  
$$I_{Stop,CS\_typ} = 18 \mu A + (I_{Stop,HS,25} \times t_{on}/T_{Per})$$
  
where the 18  $\mu$ A is the base current consumption of the digital cyclic sense/wake functionality.
- 12) Also applies to cyclic wake but without adder from HS biasing contribution.
- 13) Additional current will be drawn from  $V_{SINT}$ .

## Notes

1. *There is no additional current consumption contribution in Normal Mode due to PWM generators or Timers.*
2. *The quiescent current consumption in Stop Mode and Sleep Mode will increase for  $V_{SINT} < 9$  V.*

## **5 System Features**

This chapter describes the system features and behavior of the TLE9563-3QX:

- State machine
- Device configuration
- State machine modes and mode transitions
- Wake-up features such as cyclic sense and cyclic wake

### **5.1 Short State Machine Description**

The BLDC Motor System IC offers six operating modes:

- Init Mode: Power-up of the device and after a soft reset.
- Normal Mode: The main operating mode of the device.
- Stop Mode: The first-level power saving mode with the main voltage regulator VCC1 enabled.
- Sleep Mode: The second-level power saving mode with VCC1 disabled.
- Restart Mode: An intermediate mode after a wake event from Sleep Mode or Fail-Safe Mode or after a failure (e.g. WD failure, VCC1 under voltage reset) to bring the microcontroller into a defined state via a reset.
- Fail-Safe Mode: A safe-state mode after critical failures (e.g. Temperature shutdown) to bring the system into a safe state and to ensure a proper restart of the system.

A special mode, called Software Development Mode, is available during software development or debugging of the system. All above mentioned operating modes can be accessed in this mode. However, the watchdog is still running, but no reset to the microcontroller is applied. Watchdog failures are indicated over INTN pin instead.

However, the watchdog reset signaling can be reactivated again in Software Development Mode. The Watchdog will start always with the Long Open Windows ( $t_{low}$ ).

The BLDC Motor System IC is controlled via a 32-bit SPI interface (refer to [Chapter 13](#) for detailed information). The configuration as well as the diagnosis is handled via the SPI.

The device offers various supervision features to support functional safety requirements. Refer to [Chapter 12](#) for more information.

## System Features

### 5.2 Device Configuration

Two features on the BLDC Motor System IC can be configured by hardware:

- The selection of the normal device operation or the Software Development Mode.
- Enabling/disabling the CRC on the SPI interface.

The configurations are done monitoring the follow pins:

- INTN/TEST
- PWM1/CRC

The hardware configuration can be done typically at device power-up, where the device is in Init Mode or (only in case of CRC setting) in Restart Mode.

#### Software development Mode configuration detail

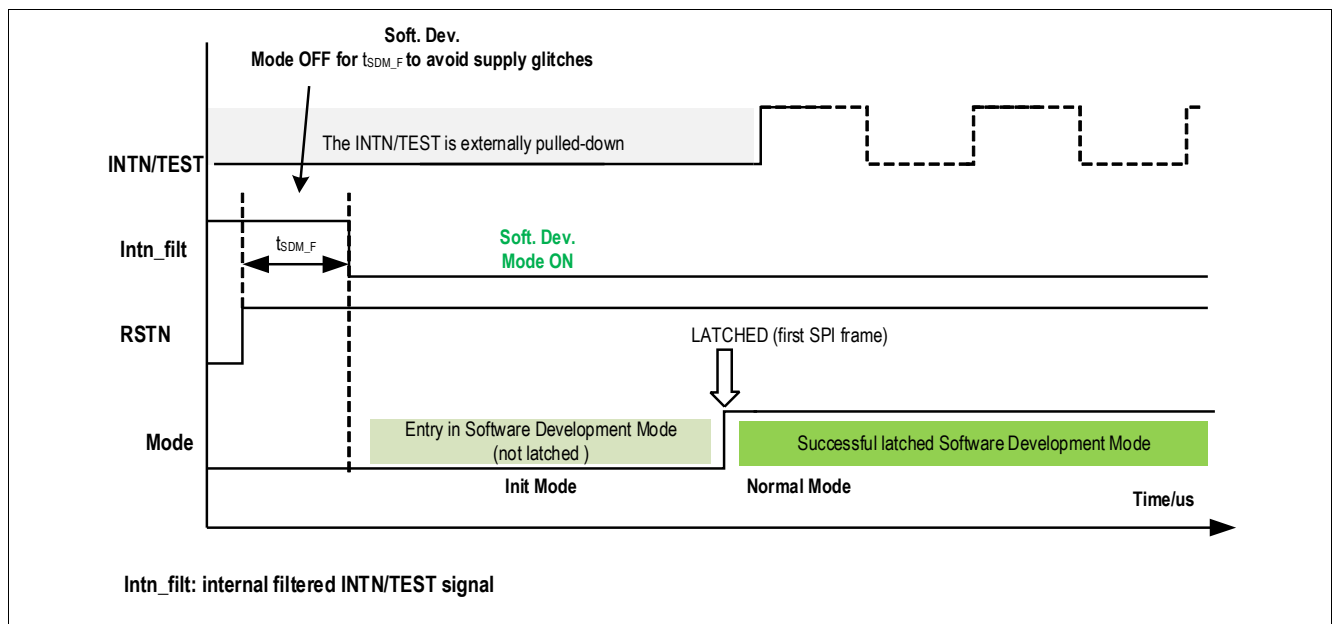
After the RSTN is released, the INTN/TEST pin is internally pulled HIGH with a weak pull-up resistor. Therefore the default configuration is the device in normal operation.

In order to configure the Software Development Mode, the following conditions have to be fulfilled:

- Init Mode from power-up
- $VCC1 > V_{rtx}$
- **POR**=1
- RSTN = HIGH

The Software Development Mode is configured using the following scheme:

- Only one external pull-down on INTN/TEST pin followed by an arbitrary SPI command, the device latches the Software Development Mode.
- External pull-up or no pull-down on INTN/TEST pin enable the device in normal operation.
- To enter Software Development Mode, a pull-down resistor to GND might be used.



**Figure 3 Software Development Mode Selection Timing**

Intn\_filt is a filtered signal from INTN/TEST, with the filter time  $t_{SDM\_F}$  (P\_11.2.7). Intn\_filt starts (at the rising edge if RSNT) with the value 1.

## System Features

*Note: If during monitoring the INTN/TEST pin for Software Development Mode entry, the device changes the mode without SPI command, the device will not enter/stay in Software Development Mode.*

### CRC configuration detail

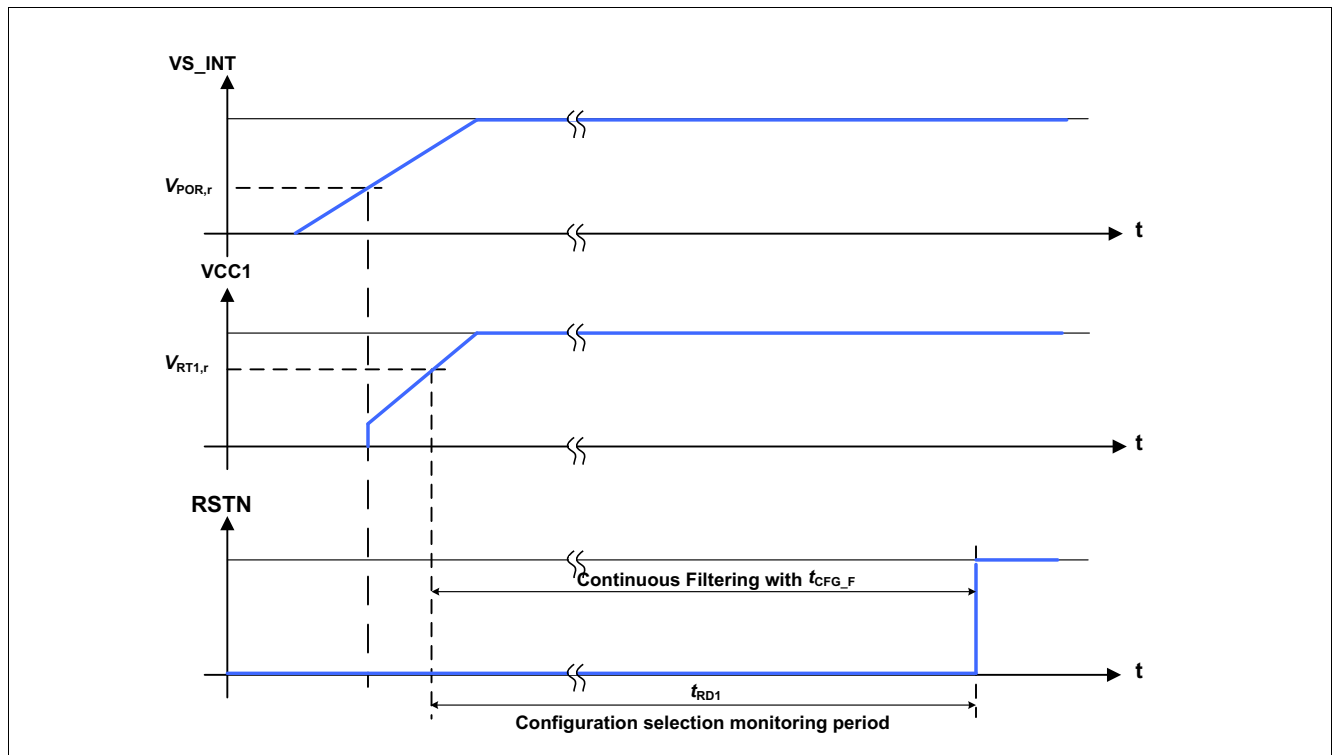
The CRC is configured using the following scheme:

- Pull-down on PWM1/CRC enable the CRC.
- No external components on PWM1/CRC disables the CRC.

In order to configure the CRC, the follow conditions have to be full filled:

- Init Mode (from power-up) or Restart Mode
- $V_{CC1} > V_{RTX}$
- **POR**=1
- $RSTN = LOW$

The configuration selection is done during the reset delay time  $t_{RD1}$  with a continuous filter time of  $t_{CFG\_F}$  and the configuration (depending on the voltage level at PWM1/CRC) is latched at the rising edge of RSTN.



**Figure 4 CRC configuration Selection Timing Diagram at the device power-up.**

In case of mismatch between CRC setting between the device and  $\mu C$  (**CRC\_STAT**), the device can accept two recovery SPI commands (static patterns).

The pattern 67AA AA0E<sub>H</sub> (addr + rw\_bit = 67 ; data = AAAA ; CRC = 0E ) enables the CRC.

The pattern E7AA AAC3<sub>H</sub> (addr + rw\_bit = E7 ; data = AAAA ; CRC = C3) disables the CRC.

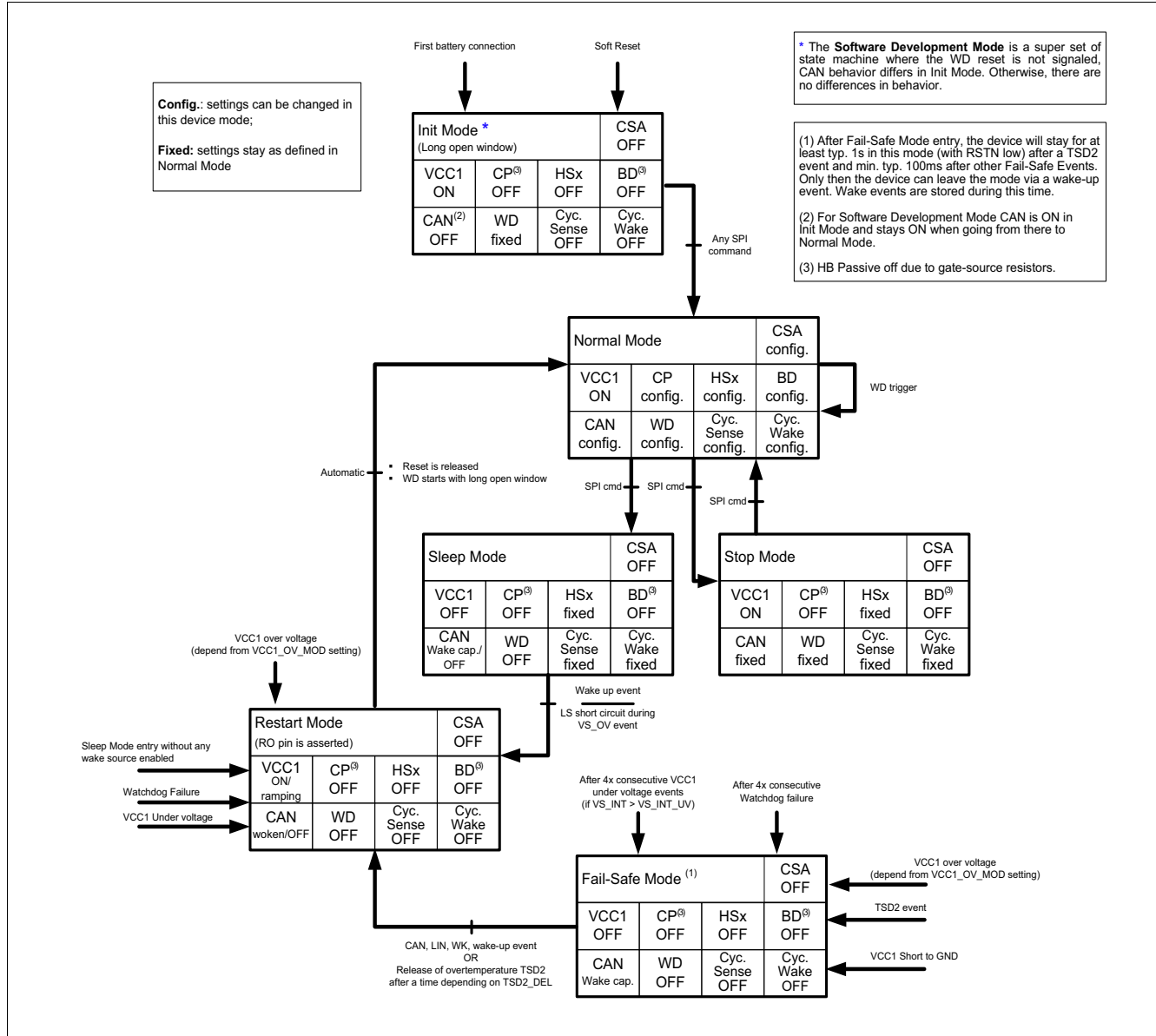
The patterns shall be send only in Normal Mode.

For additional details about the CRC setting and configuration, refer also to **Chapter 13.3.1**.

## System Features

### 5.3 Block Description of State Machine

The state machine describes the different states of operation, the device may get into. The following figure shows the state machine flow diagram.



**Figure 5 State Diagram showing the operating modes**

#### Description:

- ON /OFF:= Indicate if the module is enabled or disabled either via SPI or from the device itself
- config:= Settings can be changed in this mode
- fixed:= Settings stay as defined in Normal Mode or Init Mode
- active/inactive:= Indicate if the device activates/deactivates one specific feature
- Wake capable:= Transceiver that is capable to detect one wake-up events
- woken:= Transceiver that has detected one wake-up event

## System Features

### 5.4 State Machine Modes Description

#### 5.4.1 Init Mode

The device starts up in Init Mode after crossing the power-on reset  $V_{POR,r}$  threshold (see also [Chapter 12.3](#)) and the watchdog will start with a long open window ( $t_{LW}$ ) after RSTN is released (High level).

In Init Mode, the device waits for the microcontroller to finish its startup and initialization sequence.

Init Mode (Long open window)			CSA OFF
VCC1 ON	CP OFF	HSx OFF	BD OFF
CAN OFF	WD fixed	Cyc. Sense OFF	Cyc. Wake OFF

**Figure 6 Init Mode**

**Table 5 Init Mode Settings**

Part/Function	Value	Description
VCC1	ON	• The VCC1 is ON
WD	fixed	• Watchdog is fixed and set with a long open window ( $t_{LW}$ )
HSx	OFF	• All HSx are OFF
BD	OFF	• Bridge Drivers is OFF
CP	OFF	• Charge Pump is OFF
CSA	OFF	• Current Sense Amplifier is OFF
CAN	OFF	• CAN transceiver is OFF <sup>1)</sup>
Cyc Sense	OFF	• Cycle Sense is OFF
Cyc Wake	OFF	• Cycle Wake is OFF

1) Exception: The CAN transceiver is ON during Software Development Mode

#### 5.4.2 Normal Mode

The Normal Mode is the standard operating mode for the device. The VCC1 is active and all features are configurable. Supervision and monitoring features are enabled.



## System Features

Normal Mode			CSA config.
VCC1 ON	CP config.	HSx config.	BD config.
CAN config.	WD config.	Cyc. Sense config.	Cyc. Wake config.

**Figure 7 Normal Mode**

**Table 6 Normal Mode Settings**

Part/Function	Value	Description
VCC1	ON	<ul style="list-style-type: none"> <li>VCC1 is active</li> </ul>
WD	config	<ul style="list-style-type: none"> <li>Watchdog may be configured by SPI</li> </ul>
HSx	config	<ul style="list-style-type: none"> <li>The High Side Switches may be configured and switched ON or OFF by SPI</li> </ul>
BD/CP	config	<ul style="list-style-type: none"> <li>The Bridge Drivers and Charge Pump may be configured and switched ON or OFF by SPI</li> </ul>
CSA	config	<ul style="list-style-type: none"> <li>Current Sense Amplifier may be configurable and switched ON or OFF by SPI</li> </ul>
CAN	config	<ul style="list-style-type: none"> <li>CAN may be configurable and switched ON or OFF by SPI</li> </ul>
Cyc. Sense	config	<ul style="list-style-type: none"> <li>Cyclic sense may be configured with the HSx, WKx inputs and Timer1 or Timer2 or SYNC (WK4)</li> </ul>
Cyc. Wake	config	<ul style="list-style-type: none"> <li>Cyclic wake can be configured with the Timer1 or Timer 2</li> </ul>

### 5.4.3 Stop Mode

The Stop Mode is the first level technique to reduce the overall current consumption by setting the voltage regulator VCC1 into a low-power mode.

*Note: All settings have to be done before entering Stop Mode.*

In Stop Mode any kind of SPI WRITE commands are ignored and the **SPI\_FAIL** bit is set, except for changing to Normal Mode, triggering a device Soft Reset, refreshing the watchdog as well as for reading and clearing the SPI status registers.

*Note: A wake-up event on CAN, WKx, Low-Side short circuit detection in parking braking mode or overvoltage brake detection, could generate an interrupt on pin INTN (based on INTN masking configuration; refer to [Chapter 10](#)) however, no change of the device mode will occur.*

## System Features

Stop Mode			CSA OFF
VCC1 ON	CP OFF	HSx fixed	BD OFF
CAN fixed	WD fixed	Cyc. Sense fixed	Cyc. Wake fixed

**Figure 8 Stop Mode**

**Table 7 Stop Mode Settings**

Part/Function	Value	Description
VCC1	ON	• VCC1 is ON
WD	fixed	• Watchdog is fixed as configured in Normal Mode
HSx	fixed	• HSx are fixed as configured in Normal Mode
BD/CP	OFF	• The Bridge Drivers and Charge Pump are OFF
CSA	OFF	• Current Sense Amplifier is OFF
CAN	fixed	• CAN fixed as configured in Normal Mode
Cyc. Sense	fixed	• Cyclic sense fixed as configured in Normal Mode
Cyc. Wake	fixed	• Cyclic wake is fixed as configured in Normal Mode

*Note:* In Stop Mode, it is possible to activate the Low-Side of Bridge Drivers (e.g. in case of parking braking mode or overvoltage brake detection). Refer to [Chapter 12.11](#) for additional details.

### 5.4.4 Sleep Mode

The Sleep Mode is the second level technique to reduce the overall current consumption to a minimum needed to react on wake-up events or for the device to perform autonomous actions (e.g. cyclic sense).

*Note:* All settings have to be done before entering Sleep Mode.

Sleep Mode			CSA OFF
VCC1 OFF	CP OFF	HSx fixed	BD OFF
CAN Wake cap./ OFF	WD OFF	Cyc. Sense fixed	Cyc. Wake fixed

**Figure 9 Sleep Mode**

## System Features

**Table 8 Sleep Mode Settings**

Part/Function	Value	Description
VCC1	OFF	• VCC1 is OFF
WD	OFF	• Watchdog is OFF
HSx	fixed	• HSx are fixed as configured in Normal Mode
BD/CP	OFF	• The Bridge Drivers and Charge Pump are OFF
CSA	OFF	• Current Sense Amplifier is OFF
CAN	Wake Cap/ OFF	• CAN fixed as configured (Wake Capable or OFF)
Cyc. Sense	fixed	• Cyclic sense fixed as configured in Normal Mode
Cyc. Wake	fixed	• Cyclic wake is fixed

*Note:* In Sleep Mode, it is possible to activate the Low-Side's of Bridge Drivers (e.g. in case of parking braking mode or overvoltage braking). Refer to [Chapter 12.11](#) for additional details.

### 5.4.5 Restart Mode

The Restart Mode is a transition state where the RSNT pin is asserted.

Restart Mode (RO pin is asserted)				CSA OFF
VCC1 ON/ ramping	CP OFF	HSx OFF	BD OFF	
CAN woken/ OFF	WD OFF	Cyc. Sense OFF	Cyc. Wake OFF	

**Figure 10 Restart Mode**

**Table 9 Restart Mode Settings**

Part/Function	Value	Description
VCC1	ON/ ramping	• VCC1 is ON or ramping up
WD	OFF	• WD will be disabled if it was activated before
HSx	OFF	• HSx will be disabled if it was activated before
BD/CP	OFF	• The Bridge Drivers and Charge Pump are OFF
CSA	OFF	• Current Sense Amplifier is OFF
CAN	Woken/ wake capable/ OFF	• CAN may woken (in case of wake-up event on the Bus) or wake capable or OFF

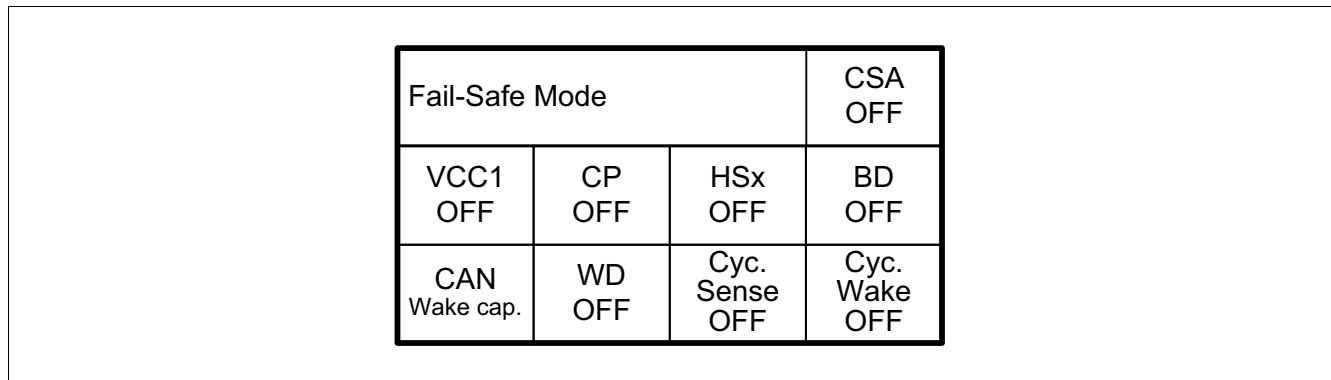
## System Features

**Table 9 Restart Mode Settings** (cont'd)

Part/Function	Value	Description
Cyc. Sense	OFF	• Cyclic sense will be disabled if it was activated before
Cyc. Wake	OFF	• Cyclic wake will be disabled if it was activated before

### 5.4.6 Fail-Safe Mode

The purpose of this mode is to bring the system in a safe status after a failure condition by turning OFF the VCC1 supply and powering off the microcontroller. After a wake event the system is then able to restart again.



**Figure 11 Fail-Safe Mode**

**Table 10 Fail-Safe Mode Settings**

Part/Function	Value	Description
VCC1	OFF	• VCC1 is switched OFF
WD	OFF	• WD is switched OFF
HSx	OFF	• HSx are switched OFF
BD/CP	OFF	• The Bridge Drivers and Charge Pump are OFF
CSA	OFF	• Current Sense Amplifier is OFF
CAN	Wake Cap	• CAN is forced to be Wake capable
Cyc. Sense	OFF	• Cyclic sense is switched OFF
Cyc. Wake	OFF	• Cyclic wake is switched OFF

#### Note

- In Fail-Safe Mode, the default wake sources CAN and WKx (if configured as wake inputs) are activated automatically and all wake event bits will be cleared.
- The Fail-Safe Mode will be maintained until a wake event on the default wake sources occurs. To avoid any fast toggling behavior a filter time of typ. 100ms ( $t_{FS,min}$ ) is implemented. Wake events during this time will be stored and will automatically lead to entering Restart Mode after the filter time.  
 In case of an VCC1 overtemperature shutdown (TSD2) the Restart Mode will be reached automatically after a filter time of typ. 1s ( $t_{TSD2}$ ) without the need of a wake event once the device temperature has fallen below the TSD2 threshold.
- The parking braking mode is automatically disabled in Fail-Safe Mode.

## System Features

### 5.4.7 Software Development Mode

The Software Development Mode is a dedicated device configuration especially useful for software development.

Compared to the default device user mode operation, this mode is a super set of the state machine. The device will start also in Init Mode and it is possible to use all the modes and functions with following differences:

- Restart Mode or Fail-Safe Mode (depending on the configuration) is not reached due to watchdog failure but the other reasons to enter these modes are still valid.
- CAN default value in Init Mode and entering Normal Mode from Init Mode is ON instead of OFF.

**Table 11 Normal Mode Settings (Software Development Mode active)**

Part/Function	Default State	Description
VCC1	ON	<ul style="list-style-type: none"> <li>• VCC1 is active</li> </ul>
WD	ON	<ul style="list-style-type: none"> <li>• WD is on, but will not trigger transition to Fail-Safe Mode or Restart Mode</li> </ul>
HSx	OFF	<ul style="list-style-type: none"> <li>• The High Side Switches may be configured and switched ON or OFF by SPI</li> </ul>
BD/CP	OFF	<ul style="list-style-type: none"> <li>• The Bridge Drivers and Charge Pump may be configured and switched ON or OFF by SPI</li> </ul>
CAN	ON	<ul style="list-style-type: none"> <li>• CAN may be configurable and switched ON or OFF by SPI</li> </ul>
Cyc. Sense	OFF	<ul style="list-style-type: none"> <li>• Can be configured</li> </ul>
Cyc. Wake	OFF	<ul style="list-style-type: none"> <li>• Can be configured</li> </ul>

### Software Development Mode entry

For timing and configuration details, refer to [Chapter 5.2](#).

#### Note

- After Init Mode, the pull-up is released as the INTN/TEST pin acts as output then to drive the INTN signal.
- If the device enters Fail-Safe Mode due to VCC1 short circuit to GND during the Init Mode, the Software Development Mode will not be entered and can only be reached at the next power-up of the device after the VCC1 short circuit is removed.
- The absolute maximum ratings of the pin INTN must be observed. To increase the robustness of this pin during debugging or programming a series resistor between INTN and the connector can be added.

### Watchdog in Software Development Mode

The Watchdog is enabled in Software Development Mode as default state. One INTN event is generated due to wrong watchdog trigger.

It is possible to deactivate the integrated Watchdog module using the [WD\\_SDM\\_DISABLE](#) bit. After disabling the Watchdog, no INTN events are generated and the [WD\\_FAIL](#) bit will also not be set anymore in case of a trigger failure. It is also possible only to mask / unmask the INTN event of the WD in Software Development Mode by using the bit [WD\\_SDM](#). In case of unmasking, a WD trigger fail will only lead to [WD\\_FAIL](#) bit set.

## 5.5 Transition Between States

This chapter describes the transition between the modes triggered by power-up, SPI commands or wake-up events.

## System Features

### 5.5.1 Transition into Init Mode

The device goes into Init Mode in case of a power-up or after sending a soft-reset in Normal or Stop Mode.

#### Prerequisites:

- Power OFF
- Device in Normal Mode or Stop Mode with follow conditions:
  - $VSINT > VPOR,r$
  - RSTN High

#### Triggering Events:

- A Soft Reset command (**MODE** = '11'). All SPI registers will be changed to their respective Soft Reset values.

#### Note

- In case of Soft Reset command, a hardware RSTN event can be generated depending on the configuration. An external Reset will be generated in case of **SOFT\_RESET\_RO** = 0<sub>B</sub>. In case of **SOFT\_RESET\_RO** = 1<sub>B</sub>, no RSTN hardware event is generated in case of Soft Reset.
- At power-up, the SPI bit **VCC1\_UV** will not be set as long as VCC1 is below the VRT,x threshold and if VSINT is below the VSINT,UV threshold. The RSTN pin will be kept LOW as long as VCC1 is below the selected VRT1,r threshold. The reset delay counter will start after VRT1,r threshold is reached. After the first threshold crossing of  $VCC1 > V_{RT1,R}$  and RSTN transition from low to high, all subsequent undervoltage events will lead to Restart Mode.
- Wake events are ignored during Init Mode and will be lost.
- The bit **VSINT\_UV** will only be updated in Init Mode once RSTN resumes a high level.

### 5.5.2 Init Mode -> Normal Mode

This transition moves the device in the mode where all configurations are accessible via SPI command.

#### Prerequisites:

- $VSINT > VPOR,r$
- Init Mode
- RSTN High

#### Triggering Events:

- Any valid SPI command (from SPI protocol point of view) will bring the device to Normal Mode (i.e. any register can be written, cleared and read) during the long open window where the watchdog has to be triggered (refer also [Chapter 13.2](#)). The CRC is not taken into account for this transition.
- For example:
  - A SPI Sleep Mode command will still bring the device into Normal Mode. However, as this is an invalid state transition, the SPI bit **SPI\_FAIL** is set.
  - Any invalid SPI command (from content point of view) will still bring the device into Normal Mode. The SPI bit **SPI\_FAIL** is set.

#### Note

- It is recommended to use the first SPI command to trigger and to configure the watchdog.

### 5.5.3 Normal Mode -> Stop Mode

This transition is intended as first measure to reduce the current consumption. All the device features needed in Stop Mode shall be configured in Normal Mode.

## System Features

### Prerequisites:

- VCC1>Vrtx
- Device in Normal Mode

### Triggering Events:

- State transition is only initiated by specific SPI command.

### Note

- An interrupt is triggered on the pin INTN when Stop Mode is entered and not all wake source signalization flags were cleared.
- If high-side switches are kept enabled during Stop Mode, then the device current consumption will increase.
- It is not possible to switch directly from Stop Mode to Sleep Mode. Doing so will also set the **SPI\_FAIL** flag and will bring the device into Restart Mode.

## 5.5.4 Normal Mode -> Sleep Mode

This transition is intended to reduce as much as possible the current consumption keeping active only wake-up sources. All wake-up sources configurations shall be done in Normal Mode.

### Prerequisites:

- VCC1>Vrtx
- Device in Normal Mode
- All wake source signalization flags were cleared (including the LSxDSOV\_BRK bit)
- At least one wake-up source activated

### Triggering Events:

- State transition is only initiated by specific SPI command.

### Note

- If the HSx outputs are kept enabled during Sleep Mode, then the device current consumption will increase (see [Chapter 4.4](#)).
- The Cyclic Sense function will not work properly anymore in case of a failure event (e.g. overcurrent, over temperature, reset) because the configured HSx and Timers will be disabled.
- If **VCC1\_UV** or **VCC1\_OV** (with Config to go to Restart Mode) occurs at the border of the Sleep Mode entry: The device will go immediately into Restart Mode.
- If **TS\_D2** or **VCC1\_OV** (with Config to go to Fail-Safe Mode) occurs at the border of the Sleep Mode entry: The device will enter immediately Fail-Safe Mode.
- As soon as the Sleep Mode command is sent, the Reset will go low.
- It is not possible to switch all wake sources off in Sleep Mode. Doing so will set the **SPI\_FAIL** flag and will bring the device into Restart Mode.

## 5.5.5 Stop Mode -> Normal Mode

This transition is intended to set the device in Normal Mode where all the device integrated features are available and configurable.

### Prerequisites:

- VCC1>Vrtx

## System Features

- Device in Stop Mode

### Triggering Events:

- State transition is only initiated by SPI command.

### Note

- None

## 5.5.6 Sleep Mode -> Restart Mode

This transition is the consequence of a detection of wake-up event by the device. This transition is used to ramp up VCC1 after a wake in a defined way.

### Prerequisites:

- Device in Sleep Mode
- At least one wake-up source active

### Triggering Events:

- A wake-up event on CAN, WKx, Cyclic Sense, Cyclic Wake.
- Bridge driver low-side short circuit detected during overvoltage braking or in parking braking mode.

### Note

- It is not possible to switch off all wake sources in Sleep Mode. Doing so will set the **SPI\_FAIL** flag and will bring the device into Restart Mode.
- RSTN is pulled low during Restart Mode.
- The Restart Mode entry is signalled in the SPI register **DEV\_STAT**.
- The wake-up events are flagged in **WK\_STAT** register or **DSOV** register.

## 5.5.7 Restart Mode -> Normal Mode

From Restart Mode, the device goes automatically to Normal Mode.

### Prerequisites:

- Device in Sleep Mode or Fail-Safe Mode

### Triggering Events:

- Automatic
- Reset is released

### Note

- The watchdog timer will start with a long open window starting from the moment of the rising edge of RSTN and the watchdog period setting in the register **WD\_CTRL** will be changed to the respective default value.

## 5.5.8 Fail-Safe Mode -> Restart Mode

This transition is similar to device from Sleep Mode to Restart Mode and consequence of a detection of wake-up event by the device. This transition is used to ramp up VCC1 after a wake in a defined way.

### Prerequisites:

- Device in Fail-Safe Mode

### Triggering Events:



## System Features

- A wake-up event on CAN, WKx, TSD2 (released over temperature TDS2 after  $t_{TSD2}$ ).
- Bridge Driver Low Side short circuit detected during VS/VSINT overvoltage braking mode or in parking braking mode.

*Note:* After leaving Fail-Safe Mode, the **FAILURE** bit in **DEV\_STAT** register is set.

## 5.6 Reaction on Detected Faults

The device can react at some critical events either signalling the specific failure or changing the device mode. The chapter describes actions taken from the device in case of critical events in particular related the device mode change.

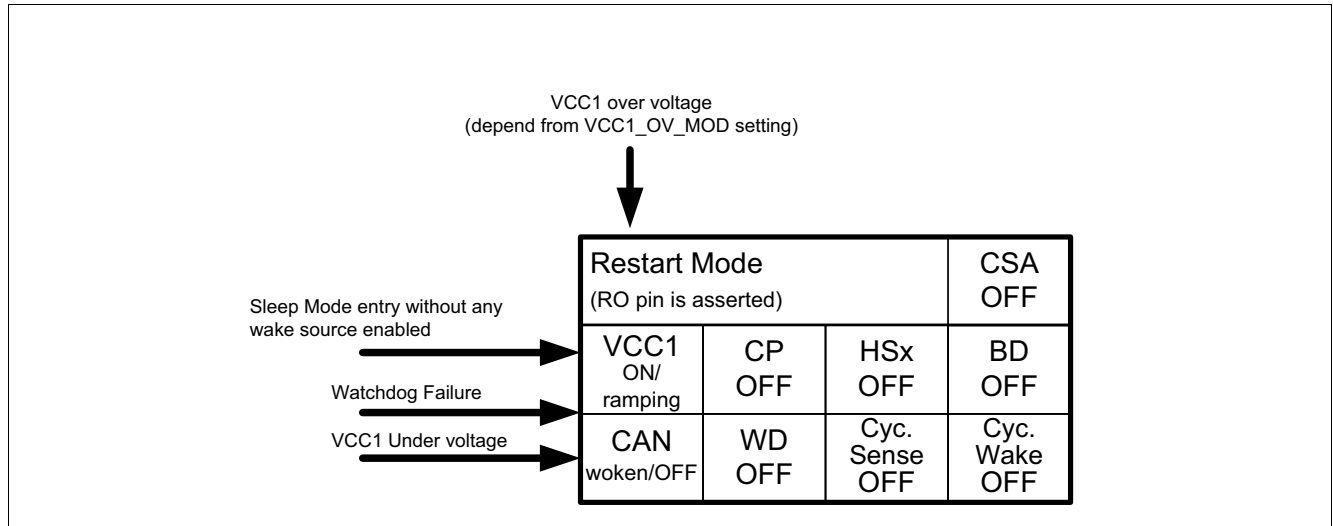
### 5.6.1 Stay in Current State

The following failures will not trigger any device mode changes, but will indicate the failures by an INTN event (depending from the Interrupt Masking) and in dedicated status registers:

- Failures on CAN
- Failures in Bridge Driver and/or Charge Pump
- Failures on HSx

### 5.6.2 Transition into Restart Mode

The Restart Mode can be entered in case of failure as shown in following figure.



**Figure 12 Move into Restart Mode**

### Prerequisites

- In case of wake-up event from Sleep Mode or Fail Safe Mode
- In case of Normal Mode
- In case of Stop Mode

### Trigger Events

- VCC1 Undervoltage in case of Normal Mode or Stop Mode.
- Watchdog trigger failure in case of Normal Mode or Stop Mode.
- VCC1 Overvoltage (based on **VCC1\_OV\_MOD**) in case of Normal Mode or Stop Mode.

### **System Features**

- Sleep Mode entry without any wake-up sources enabled in Normal Mode or Stop Mode.

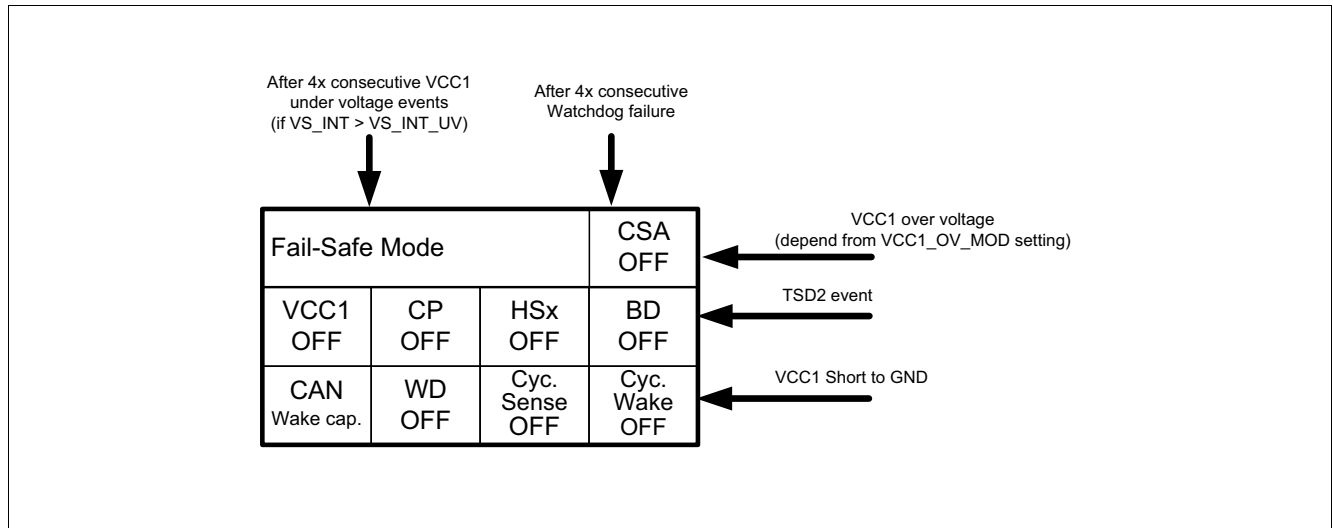
### **Note**

- None

## System Features

### 5.6.3 Transition into Fail-Safe Mode

The Fail-Safe Mode can be entered in case of critical event as shown in the following figure.



**Figure 13 Move into Fail-Safe Mode**

#### Prerequisites:

- Critical events on VCC1
- Watchdog trigger failures

#### Trigger Events:

- Device thermal shutdown (TSD2) (see also [Chapter 12.10.3](#)).
- VCC1 is shorted to GND (see also [Chapter 12.8](#)).
- VCC1 over voltage (based on [VCC1\\_OV\\_MOD](#)).
- 4 consecutive Watchdog trigger failure.
- 4 consecutive VCC1 under voltage events.

## 5.7 Wake Features

Following wake sources are implemented in the device:

- Static Sense: WKx inputs are permanently active as wake sources.
- Cyclic Sense: WKx inputs only active during on-time of cyclic sense period. Internal timers are activating HSx during on-time for sensing the WKx inputs.
- Cyclic Wake: wake controlled by internal timers, wake inputs are not used for cyclic wake.
- CAN wake: Wake-up via Bus pattern or frame (refer to [Chapter 8.2.4](#) and [Chapter 5.9](#)).

#### Note:

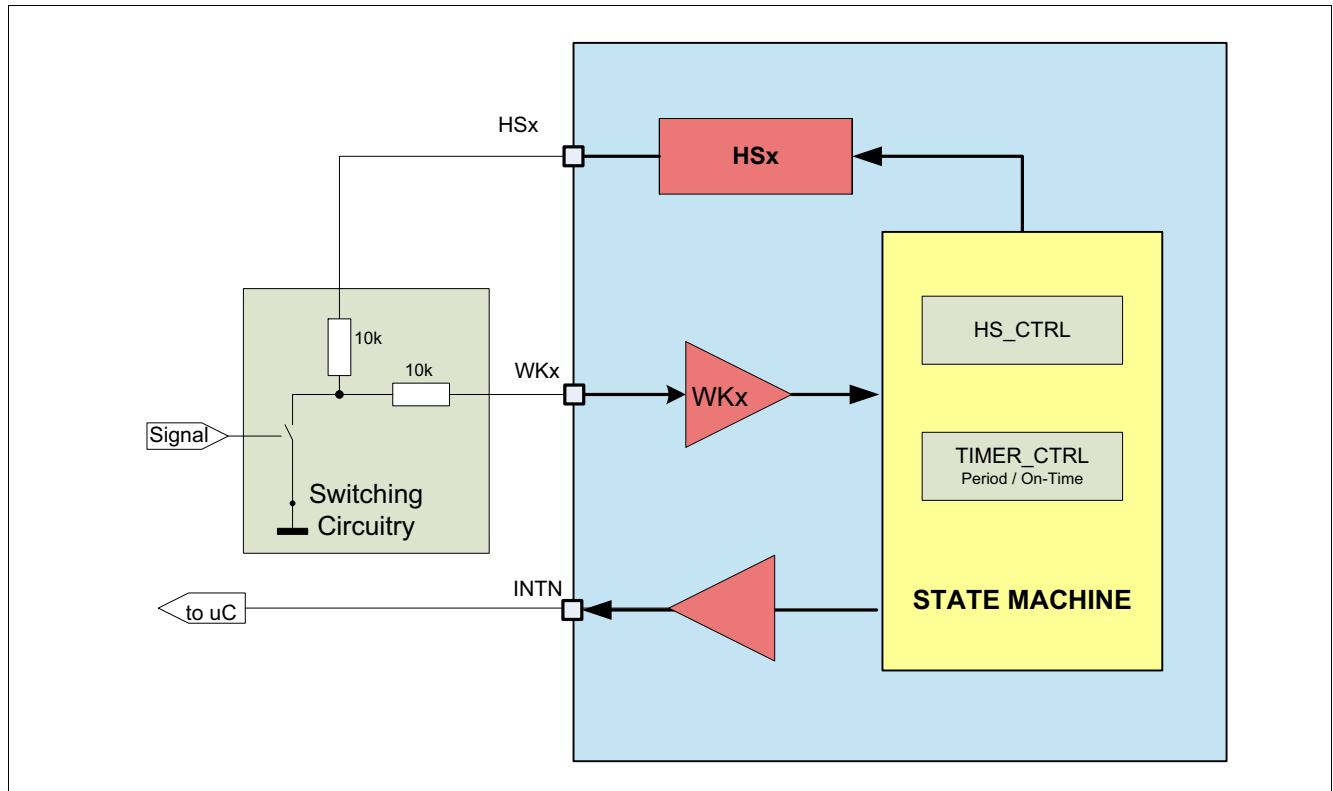
*Differences of 'cyclic sense' and 'cyclic wake':*

*In both cases a timer is active. With 'cyclic sense' one of the high-side drivers is switched on periodically and supplies some external circuits connected to the WK inputs. For the design, this means that the WK input states are only sampled at the end of the selected HS on-phase which is set by the corresponding SPI settings for GPIO HS and the timer. 'Cyclic wake' means that the timer is a wake source and thus generates periodic interrupts as long as it is enabled.*

## System Features

### 5.7.1 Cyclic Sense

The cyclic sense feature is intended to reduce the quiescent current of the device and the application. In the cyclic sense configuration, one high-side driver is switched on periodically controlled by **TIMER\_CTRL** or WK4/SYNC pin. One high-side driver supplies external circuitries e.g. switches and/or resistor arrays, which are connected to one wake input WKx (see **Figure 14**). Any edge change of the WKx input signal during the on-time of the cyclic sense period causes a wake event. Depending on the device mode, either the INTN is pulled low (Normal Mode and Stop Mode) or the device is woken enabling the VCC1 (after Sleep Mode).



**Figure 14 Cyclic Sense Working Principle**

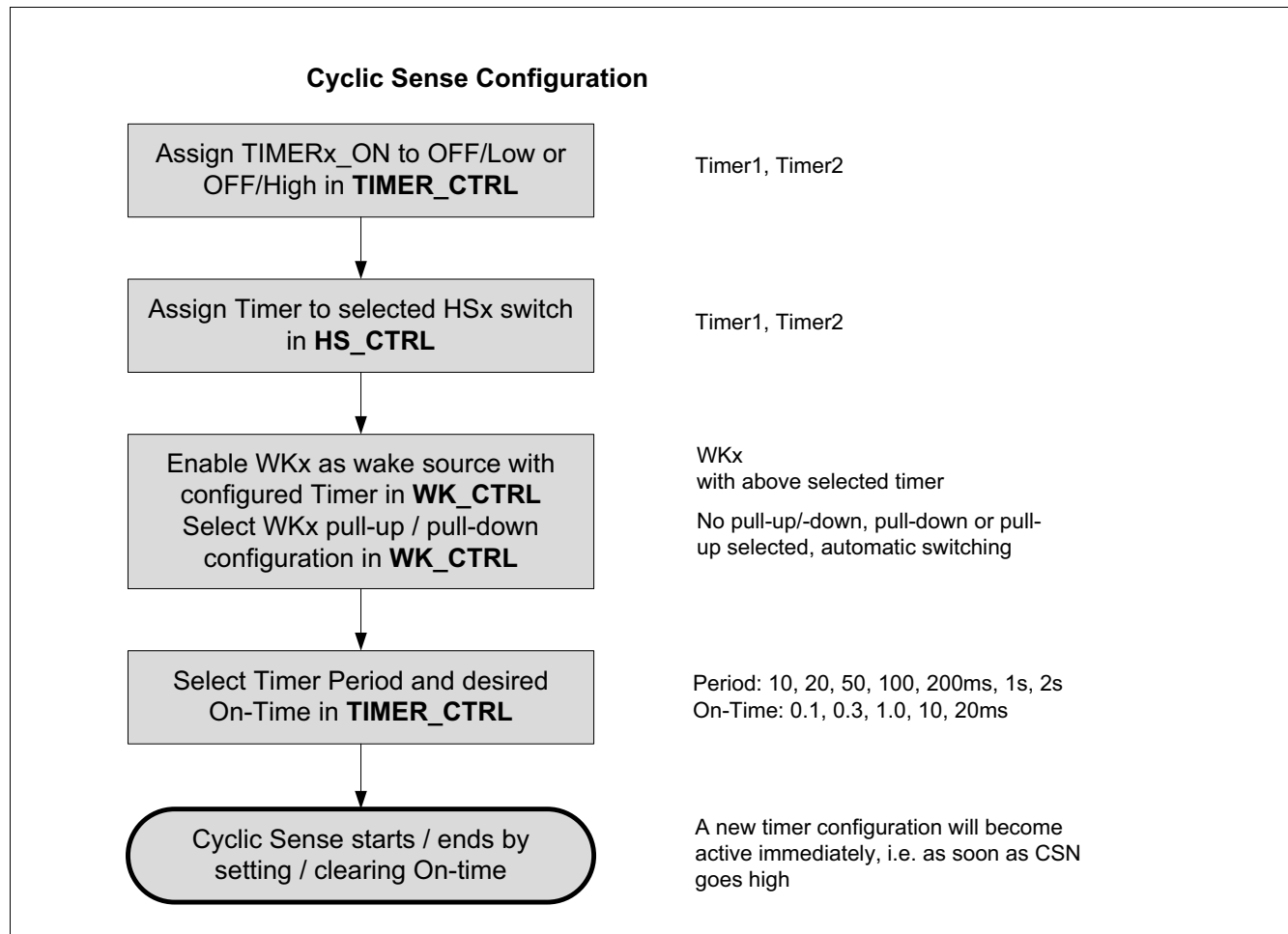
#### 5.7.1.1 Configuration and Operation of Cyclic Sense

The correct sequence to configure the cyclic sense is shown in **Figure 15**. All the configurations have to be performed before the on-time is set in the **TIMER\_CTRL** registers. The settings “OFF / LOW” and “OFF / HIGH” define the voltage level of the respective HS driver before the start of the cyclic sense. The intention of this selection is to avoid an unintentional wake due to a voltage level change at the start of the cyclic sense.

Cyclic Sense will start as soon as the respective on-time has been selected independently from the assignment of the HS and filter configuration. The correct configuration sequence is as follows:

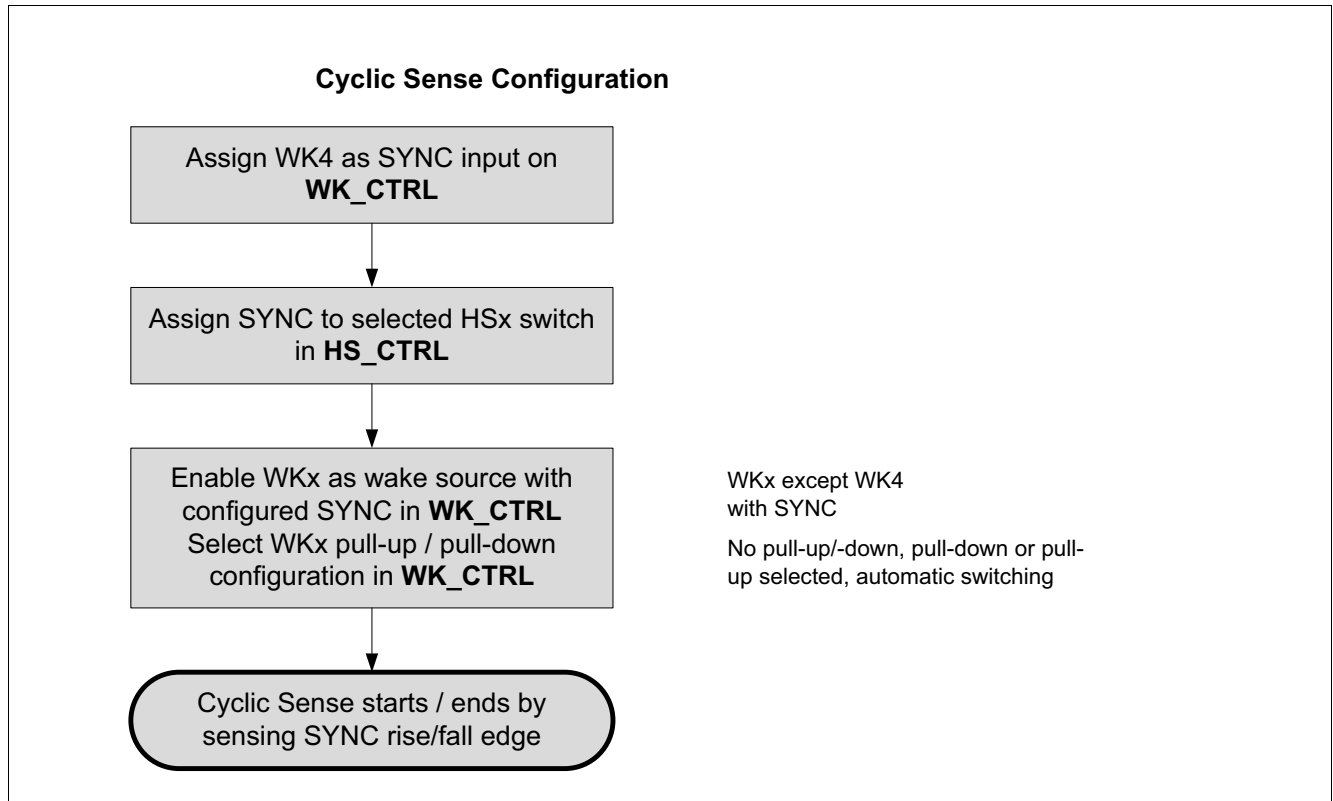
- Configure the initial level.
- Mapping of a Timer to the respective HSx outputs.
- Configuring the respective filter timing and WK pins.
- Configuring the timer period and on-time.

## System Features



**Figure 15 Cyclic Sense: Configuration and Sequence**

## System Features



**Figure 16 Cyclic Sense: Configuration and Sequence in case of SYNC usage**

### Note

- All configurations of period and on-time can be selected. However, recommended on-times for cyclic sense are 0.1ms, 0.3ms and 1ms for quiescent current saving reasons. The **SPI\_FAIL** will be set if the on-time is longer than the period.
- If the sequence is not ensured before entering Sleep Mode, then the cyclic sense function might not work properly, e.g. an interrupt could be missed or an unintentional interrupt could be triggered. However, if cyclic sense is the only wake source and it is not configured properly, then Restart Mode will be entered immediately because no valid wake source was set.
- During the HSx on phase in cyclic-sensing, the WKx level is sampled only once (one sample point). In case, a level change will appear during HSx on phase, but before the sampling, as the sampling will happen at the end of the on time, the level change will not be detected and has to wait for the next sensing-cycle.

A wake event caused by cyclic-sensing will also set the corresponding bit WKx\_WU.

During Cyclic Sense, **WK\_LVL\_STAT** is updated only with the sampled voltage levels of the WKx pin in Normal Mode or Stop Mode.

The functionality of the sampling and different scenarios are depicted in **Figure 17** to **Figure 19**. The behavior in Stop Mode and Sleep Mode is identical except that in Normal Mode and Stop Mode INTN will be triggered to signal a change of WKx input level and in Sleep Mode, VCC1 will power-up instead. A wake event will be triggered regardless if the bit WKx\_WU is already set.

System Features

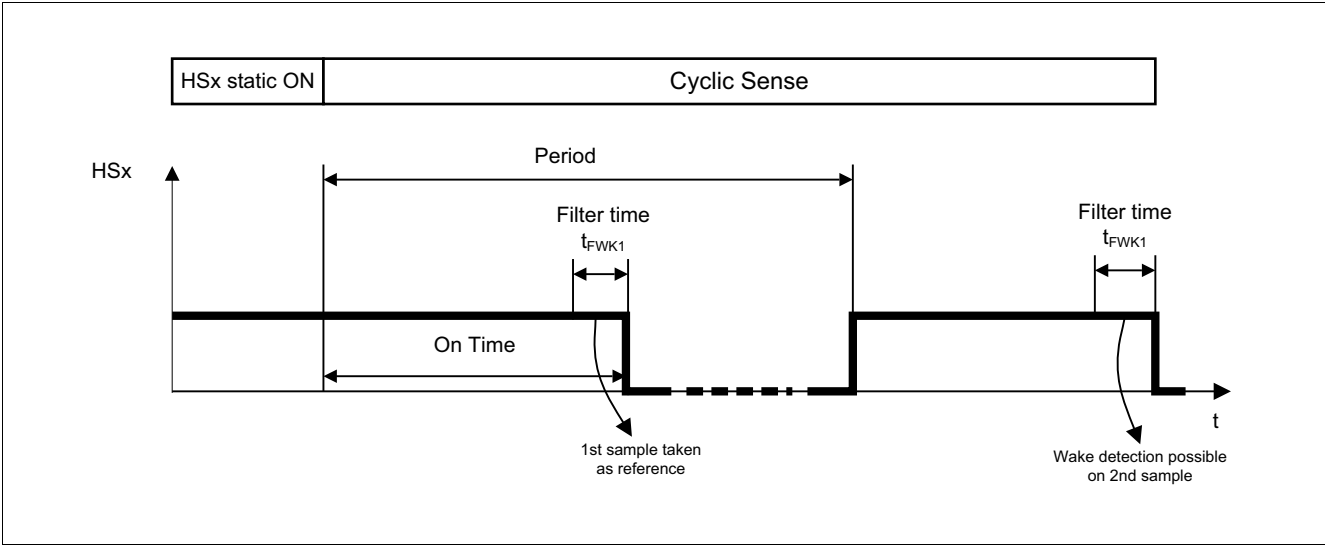


Figure 17 Cyclic Sense Timing

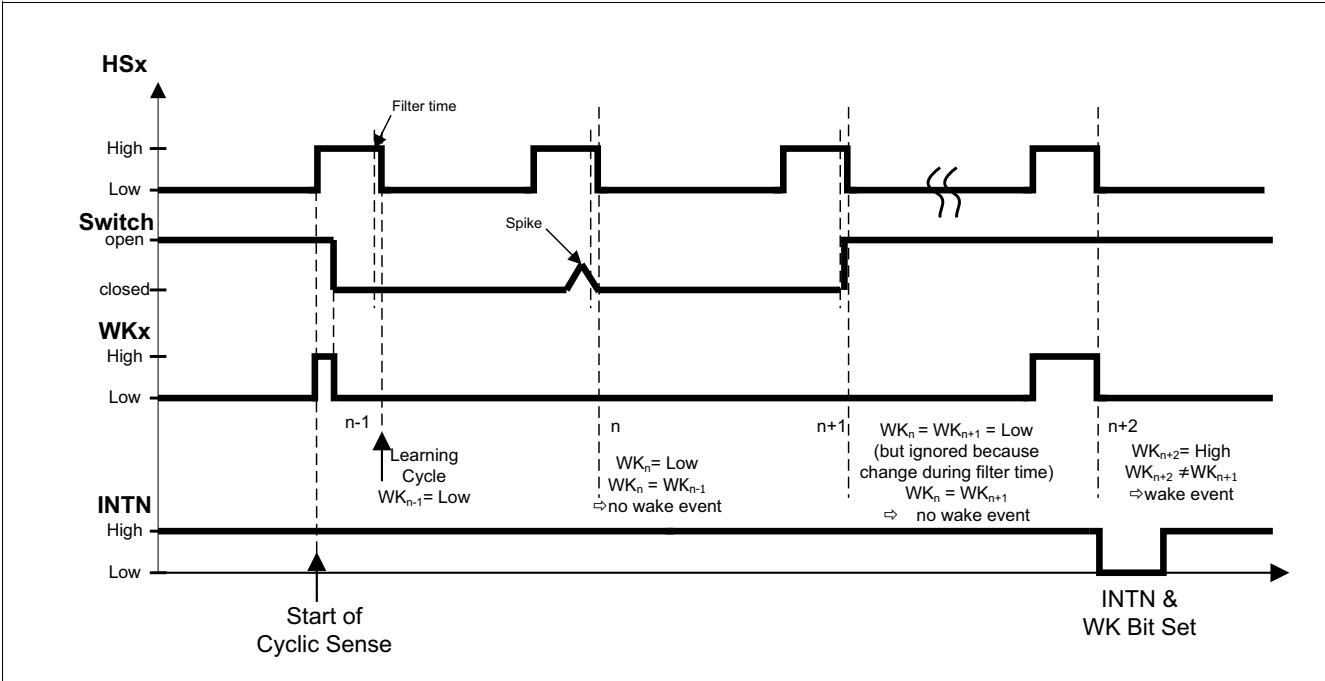
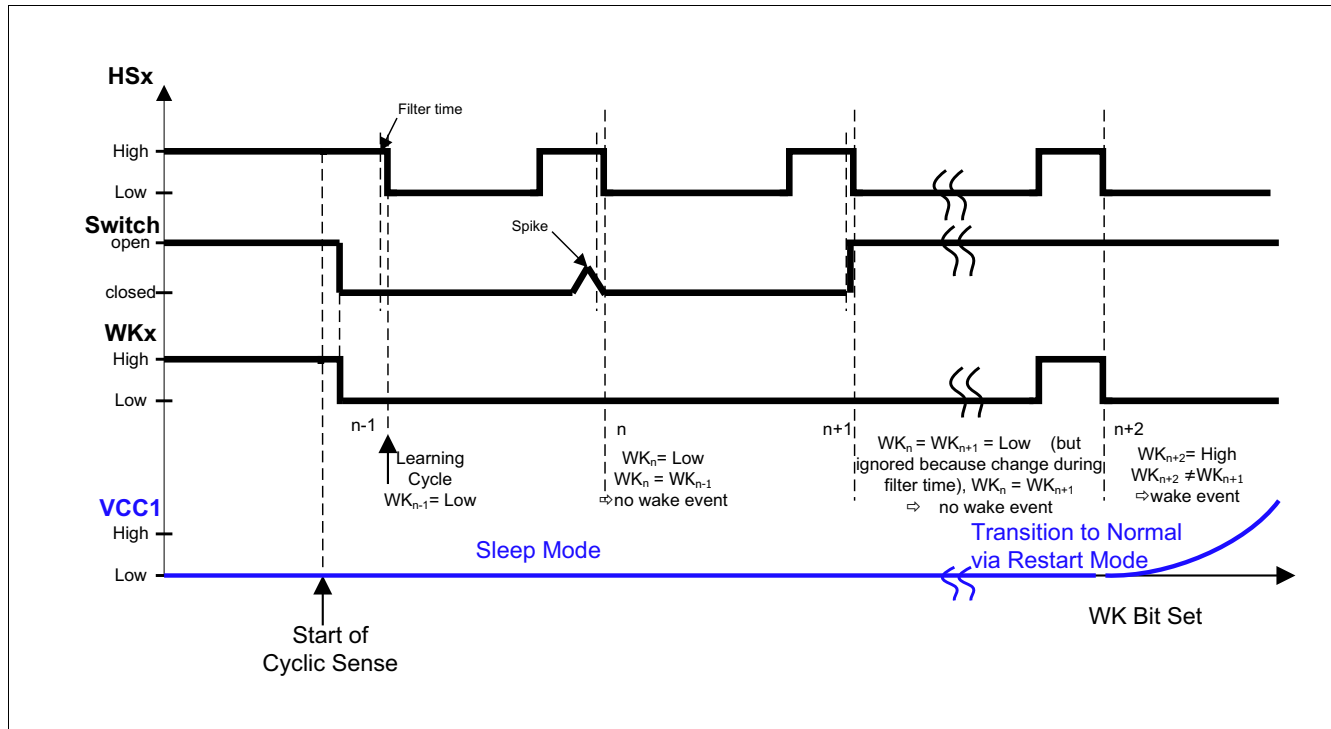


Figure 18 Cyclic Sense Example Timing for Stop Mode, HSx starts LOW, GND based WKx input

## System Features



**Figure 19 Cyclic Sense Example Timing for Sleep Mode, HSx starts with ON, GND based WKx input**

The cyclic sense function will be disabled in case of following conditions:

- in case Fail-Safe Mode is entered, the HSx switch will be disabled and the WKx pin will be changed to static sensing. An unintended wake-up event could be triggered when the WKx input is changed to static sensing.
- In Normal Mode, Stop Mode, or Sleep Mode in case of an overcurrent, or overtemperature, or under- or overvoltage event, the respective HS switch will be disabled.

### 5.7.1.2 Cyclic Sense in Low-power Mode

If cyclic sense is intended for Stop Mode or Sleep Mode, it is necessary to activate cyclic sense in Normal Mode before going to the low-power mode. A wake event due to cyclic sense will set the bit WKx\_WU. In Stop Mode a wake event will trigger an interrupt, in Sleep Mode the wake event will send the device via Restart Mode to Normal Mode.

Before returning to Sleep Mode, the wake status registers **WK\_STAT** and **DSOV** must be cleared. Trying to go to Sleep Mode with uncleared wake flags will lead to a direct wake-up from Sleep Mode by going via Restart Mode to Normal Mode and triggering of RSTN.

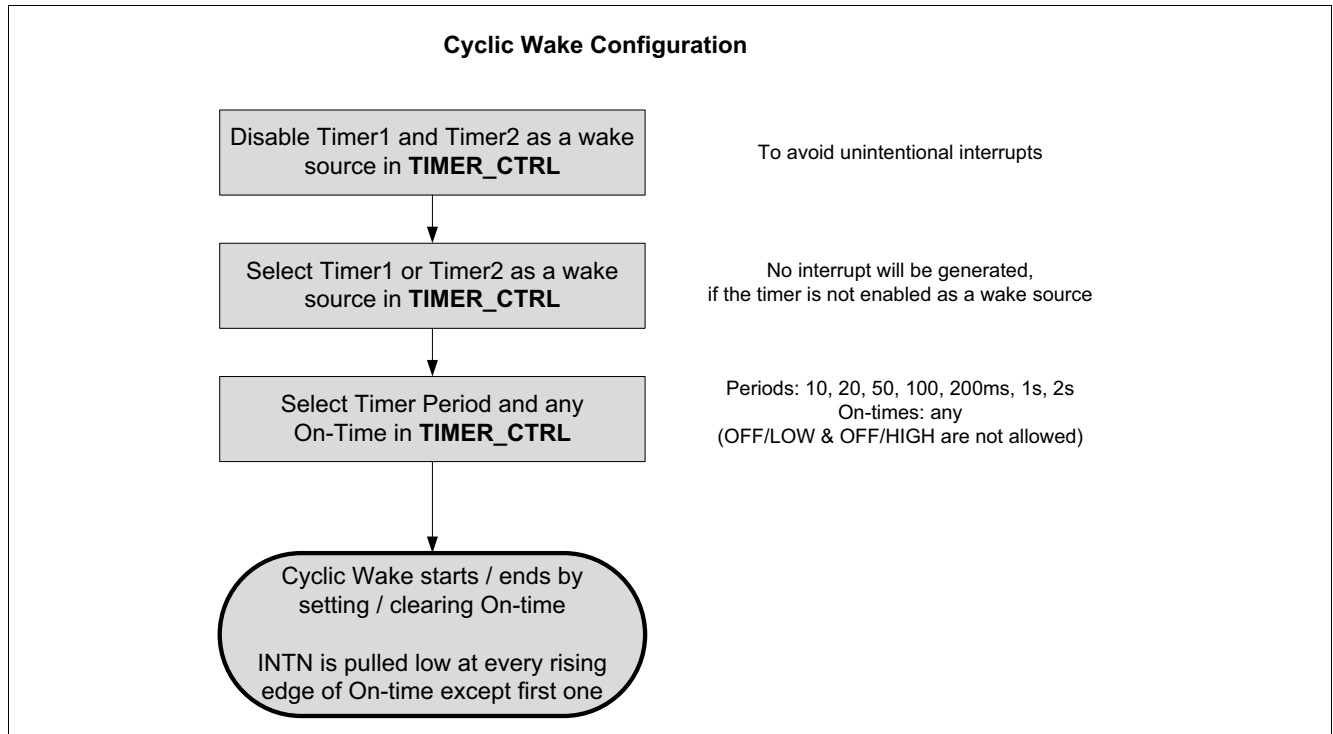
### 5.7.2 Cyclic Wake

For the cyclic wake feature one timer is configured as internal wake-up source and will periodically trigger an interrupt on INTN in Normal Mode and Stop Mode. During Sleep Mode, the timer triggers and wakes up the device again. The device enters via Restart Mode the Normal Mode.

The correct sequence to configure the cyclic wake is shown in **Figure 20**. The sequence is as follows:



## System Features



**Figure 20 Cyclic Wake: Configuration and Sequence**

*Note: The on-time is only used to enable the cyclic wake function regardless of the value of the on time, i.e. the on time value has no meaning to the cyclic wake function as long as it is not '000' or '110' or '111'.*

As in cyclic sense, the cyclic wake function will start as soon as the on-time is configured. An interrupt is generated for every start of the on-time except for the very first time when the timer is started.

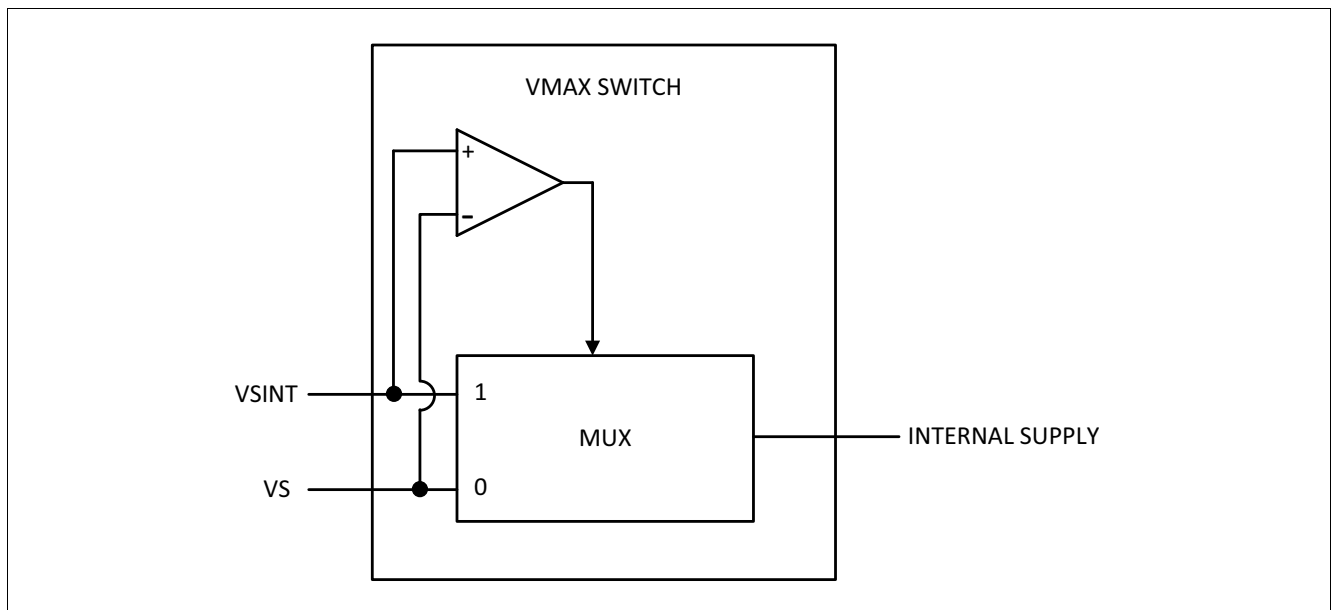
### 5.7.3 Internal Timers

Two integrated timers can be used to control the below features:

- Cyclic Wake, i.e. to wake up the microcontroller periodically in Normal Mode, Stop Mode and Sleep Mode.
- Cyclic Sense, i.e. to perform cyclic sensing using the wake input WKx and the HSx by mapping the timer accordingly via the **HS\_CTRL** register.

**System Features**

**5.8 VS Supply Multiplexing**



**Figure 21 VS Supply Multiplexing**

The internal supply voltage is multiplexed from VSINT and VS, choosing continuously the larger of both. In case of transient low VBAT, the buffered supply voltage takes over the internal supply, avoiding loss of power.

*Note: Only the internal digital logic of the device is supplied by the VMAX SWITCH. In case of a power loss of either VS or VSINT, the internal register values will not be lost.*

## **5.9 Partial Networking on CAN**

### **5.9.1 CAN Partial Networking - Selective Wake Feature**

The CAN partial networking feature can be activated for Normal Mode, in Sleep Mode and in Stop Mode. For Sleep Mode the partial networking has to be activated before sending the device to Sleep Mode. For Stop Mode the Partial Networking has to be activated before going to Stop Mode.

There are 2 detection mechanism available:

- WUP (Wake-Up Pattern) this is a CAN wake, that reacts on the CAN dominant time, with 2 dominant signals.
- WUF (Wake-Up frame) this is the wake-up on a CAN frame that matches the programmed message filter configured in the device via SPI.

The default baudrate is set to 500 kBaud. Besides the commonly used baudrates of 125 kBaud and 250 kBaud, other baudrates up to 1 MBaud can be selected (see [Chapter 13](#) for more details).

## 5.9.2 Partial Networking Function

The CAN partial networking modes are shown in the following figure.

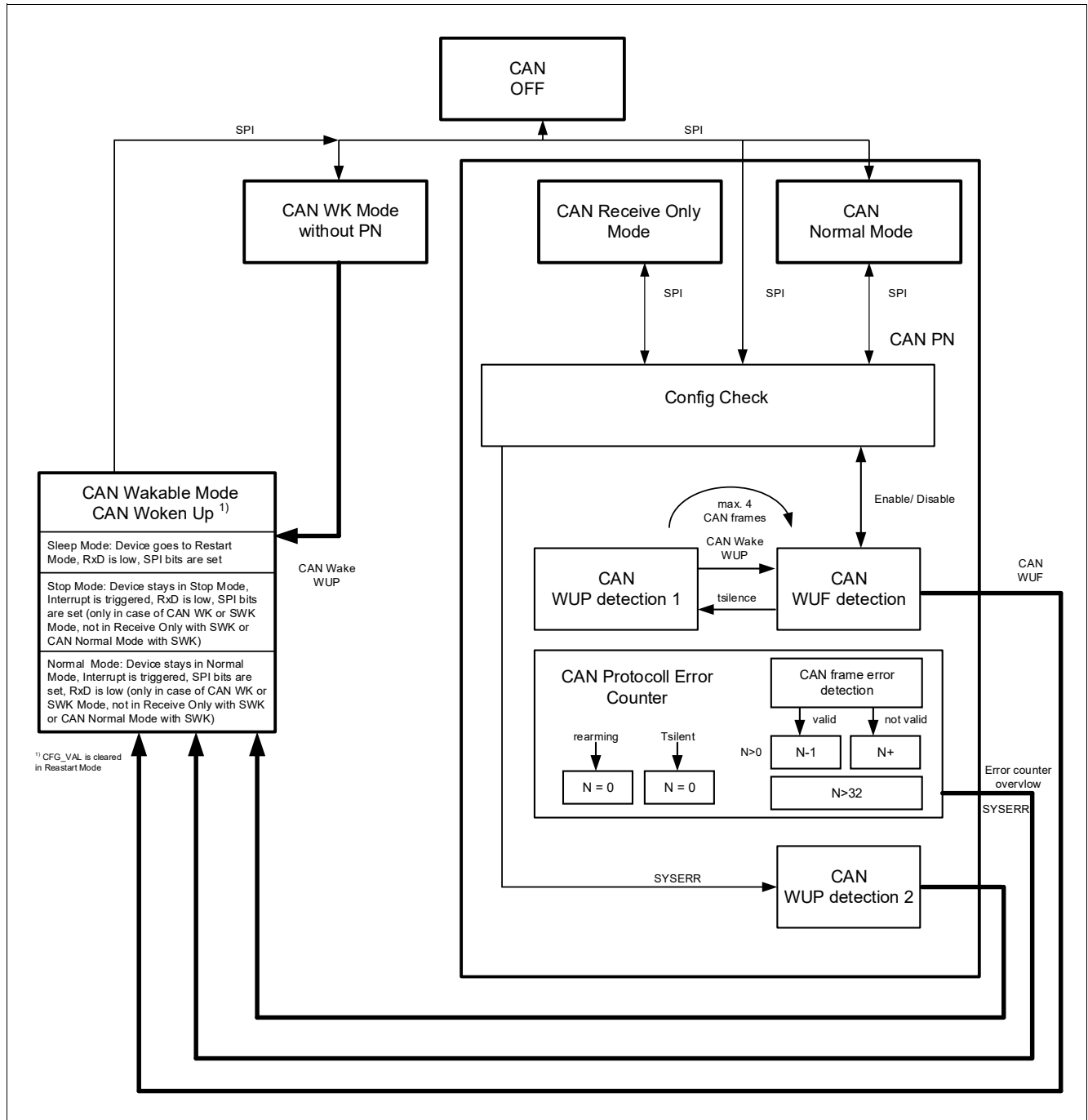


Figure 22 CAN Selective Wake State Diagram

### 5.9.2.1 Activation of SWK

The following figure shows the principal of the SWK activation.

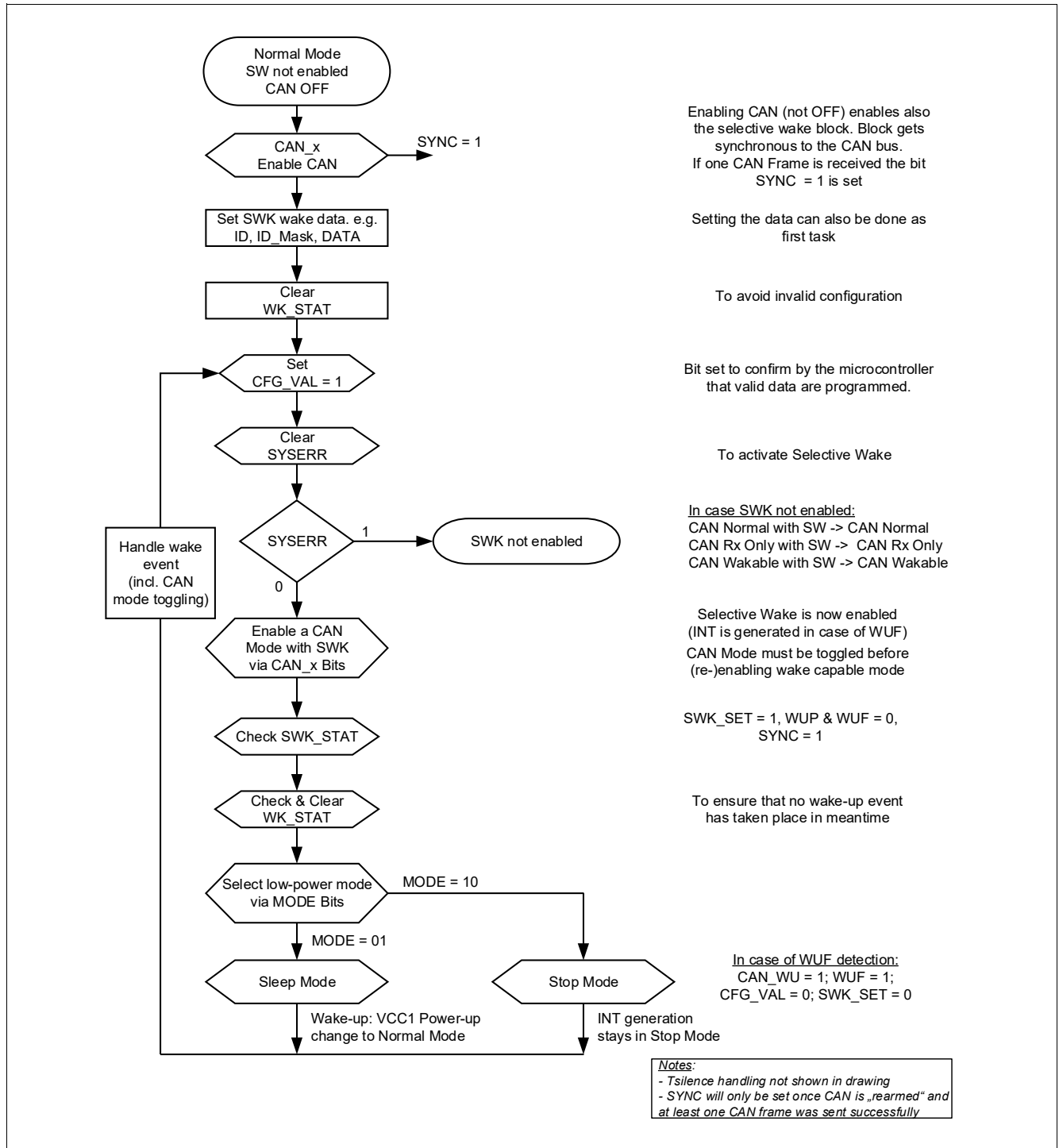


Figure 23 Flow for activation of SWK

### 5.9.2.2 Wake-up Pattern (WUP)

A WUP is signaled on the bus by two consecutive dominant bus levels for at least  $t_{Wake1}$ , each separated by a recessive bus level.

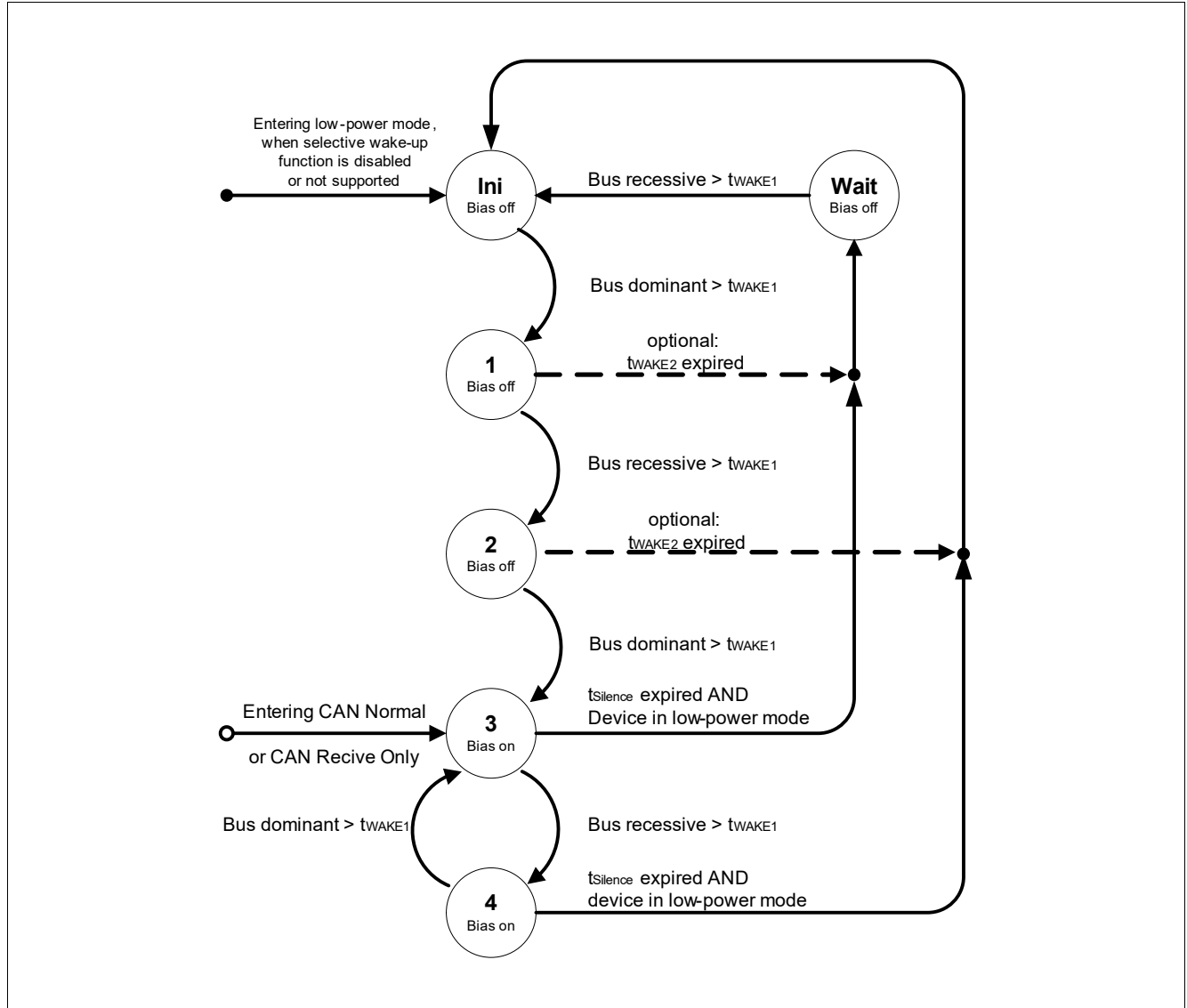


Figure 24 WUP detection following the definition in ISO11898-2:2016

### 5.9.2.3 Wake-up Frame (WUF)

The wake-up frame is defined in ISO11898-2:2016.

Only CAN frames according ISO11899-1 are considered as potential wake-up frames.

A bus wake-up shall be performed, if selective wake-up function is enabled and a "valid WUF" has been received. The transceiver may ignore up to four consecutive CAN data frames that start after switching on the bias.

A received frame is a "valid WUF" in case all of the following conditions are met:

- The ID of the received frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID mask. The ID and the ID mask might have either 11 bits or 29 bits.
- The DLC of the received frame is exactly matching the configured DLC.

- In case DLC is greater than 0, the data field of the received frame has at least one bit set in a bit position, where also in the configured data mask in the corresponding bit position the bit is set.
- No error exists according to ISO11898-2:2016 except errors which are signalled in the ACK field and EOF field.

#### **5.9.2.4 CAN Protocol Error Counter**

The counter is incremented, when a bit stuffing, CRC or form error according to ISO11898-2:2016 is detected. If a frame has been received that is valid up to the end of the CRC field and the counter is not zero, the counter is decremented.

If the counter has reached a value of 31, the following actions is performed on the next increment of this counter:

- The selective wake function is disabled.
- The CAN transceiver is woken.
- SYSERR is set and the error counter value = 32 can be read.

On each increment or decrement of the counter the decoder unit waits for at least 6 and most 10 recessive bits before considering a dominant bit as new start of frame.

The error counter is enabled:

- Whenever the CAN is in CAN Normal Mode, CAN Receive Only Mode or in WUF detection state.

The error counter is cleared under the following conditions:

- At the transition from WUF detection to WUP detection 1 (after  $t_{\text{SILENCE}}$  expiration, while SWK is correctly enabled).
- When WUF detection state is entered (in this way the counter will start from 0 when SWK is enabled).
- At CAN rearming (when exiting the woken state).
- When the CAN mode bits are selected '000', '100' (CAN off) or 0'01' (Wake capable without SWK function enabled).
- While CAN\_FD\_EN = '1' and DIS\_ERR\_CNT = '1'  
(the counter is cleared and stays cleared when these two bits are set in the SPI registers).

The Error Counter is frozen:

- After a wake-up being in woken state.

The counter value can be read out of the bits **ECNT**.

### 5.9.3 Diagnoses Flags

#### 5.9.3.1 PWRON/RESET-FLAG

The power-on reset can be detected and read by the **POR** bit in the Status register.  
The VS power on resets all register in the device to reset value. SWK is not configured.

#### 5.9.3.2 BUSERR-Flag

Bus Dominant Time-out detection is implemented and signaled by CAN\_Fail\_x in register **BUS\_STAT**.

#### 5.9.3.3 TXD Dominant Time-out flag

TXD Dominant timeout is shown in the SPI bit CAN\_FAIL\_x in register **BUS\_STAT**.

#### 5.9.3.4 WUP Flag

The WUP bit in the **SWK\_STAT** register shows that a Wake-Up Pattern (WUP) has caused a wake of the CAN transceiver. It can also indicate an internal mode change from WUP detection 1 state to WUF detection after a valid WUP.

In the following case the bit is set:

- SWK is activated: due to  $t_{\text{SILENCE}}$ , the CAN changes into the state WUP detection 1. If a WUP is detected in this state, then the **WUP** bit is set.
- SWK is deactivated: the **WUP** bit is set if a WUP wakes up the CAN. In addition, the **CAN\_WU** bit is set.
- In case WUP is detected during WUP detection 2 state (after a SYSERR) the bits **WUP** and **CAN\_WU** are set.

The **WUP** bit is cleared automatically by the device at the next rearming of the CAN transceiver.

*Note: It is possible that WUF and WUP bit are set at the same time if a WUF causes a wake out of SWK, by setting the interrupt or by restart out of Sleep Mode. The reason is because the CAN has been in WUP detection 1 state during the time of CAN SWK Mode (because of  $t_{\text{SILENCE}}$ ). See also **Figure 22**.*

#### 5.9.3.5 WUF Flag (WUF)

The WUF bit in the **SWK\_STAT** register shows that a Wake-Up frame (WUF) has caused a wake of the CAN block. In Sleep Mode this wake causes a transition to Restart Mode, in Normal Mode and in Stop Mode it causes an interrupt. Also in case of this wake the bit **CAN\_WU** in the register **WK\_STAT** is set.

The **WUF** bit is cleared automatically by the device at the next rearming of the CAN SWK function.

#### 5.9.3.6 SYSERR Flag (SYSERR)

The bit **SYSERR** is set in case of an configuration error and in case of an error counter overflow. The bit is only updated (set to '1') if a CAN mode with SWK is enabled via CAN\_x. An interrupt is triggered on INTN every time SYSERR is set if the **BUS\_STAT** is not masked.

When programming selective wake via CAN\_x, SYSERR = '0' signals that the SWK function has been enabled. The bit can be cleared via SPI. The bit is '0' after Power on Reset of the device.



### 5.9.3.7 Configuration Error

A configuration error sets the SYSERR bit to '1'. A configuration check is performed when enabling SWK via the bits CAN\_x. If the check is successful SWK is enabled, the bit SYSERR is set to '0'. In Normal Mode it is also possible to detect a Configuration Error while SWK is enabled. This will occur if the **CFG\_VAL** bit is cleared, e.g. by changing the SWK registers (from address 011 0001 to address 011 1010). In Stop Mode and Sleep Mode this is not possible as the SWK registers can not be changed.

Configuration Check:

In Restart Mode, the **CFG\_VAL** bit is cleared by the device. If the Restart Mode was not triggered by a WUF wake up from Sleep Mode and the CAN was with SWK enabled, then the **SYSERR** bit will be set.

The SYSERR bit has to be cleared by the microcontroller.

The SYSERR bit cannot be cleared when CAN\_2 is '1' and below conditions occur:

- Data valid bit not set by microcontroller, i.e. **CFG\_VAL** is not set to '1'. The **CFG\_VAL** bit is reset after SWK wake and needs to be set by the microcontroller before activation SWK again.
- **CFG\_VAL** bit reset by the device when data are changed via SPI programming. (Only possible in Normal Mode)

*Note: The SWK configuration is still valid if only the **SWK\_CTRL** register is modified.*

### 5.9.3.8 CAN Bus Timeout-Flag (**CANTO**)

In CAN WUF detection and CAN WUP detection 2 state the bit CANTO is set to '1' if the time  $t_{\text{SILENCE}}$  expires.

The bit can be cleared by the microcontroller. If the interrupt function for CANTO is enabled then an interrupt is generated in Stop Mode or Normal Mode when the CANTO set to '1'. The interrupt is enabled by setting the bit **CANTO\_MASK** to '1'. Each CANTO event will trigger a interrupt even if the CANTO bit is not cleared.

There is no wake out of Sleep Mode because of CAN time-out.

### 5.9.3.9 CAN Bus Silence-Flag (**CANSIL**)

In CAN WUF detection and CAN WUP detection 2 state the bit CANSIL is set to '1' if the time  $t_{\text{SILENCE}}$  expires.

The CANSIL bit is set back to '0' with a WUP. With this bit the microcontroller can monitor if there is activity on the CAN bus while being in CAN SWK Mode. The bit can be read in Stop Mode and Normal Mode.

### 5.9.3.10 SYNC-FLAG (**SYNC**)

The bit SYNC shows that SWK is working and synchronous to the CAN bus. To get a SYNC bit set it is required to enable the CAN to CAN Normal Mode or in CAN Receive Only Mode or in WUF detection. However - for WUF detection, the CAN SWK Mode must be enabled.

The bit is set to '1' if a valid CAN frame has been received (no CRC error and no stuffing error). It is set back to '0' if a CAN protocol error is detected. When switching into CAN SWK Mode the SYNC bit indicates to the microcontroller that the frame detection is running and the next CAN frame can be detected as a WUF, CAN wake-up can now be handled by the device. It is possible to enter a low-power mode with SWK even if the bit is not set to '1', as this is necessary in case of a silent bus.

### 5.9.3.11 SWK\_SET FLAG (**SWK\_SET**)

The SWK\_SET bit is set to signalize the following states (see also **Figure 22**):

- When SWK was correctly enabled in WUF Detection state.
- When SWK was correctly enabled when in WUP Detection 1 state.
- After a SYSERR before a wake event in WUP Detection 2 state.

The bit is cleared under following conditions:

- After a wake-up (ECNT overflow, WUP in WUP detection 2, WUF in WUF detection).
- If CAN\_2 is cleared.

#### 5.9.4 Modes for Selective Wake (SWK)

The device mode is selected via the **MODE** bits as described in [Chapter 5.3](#).

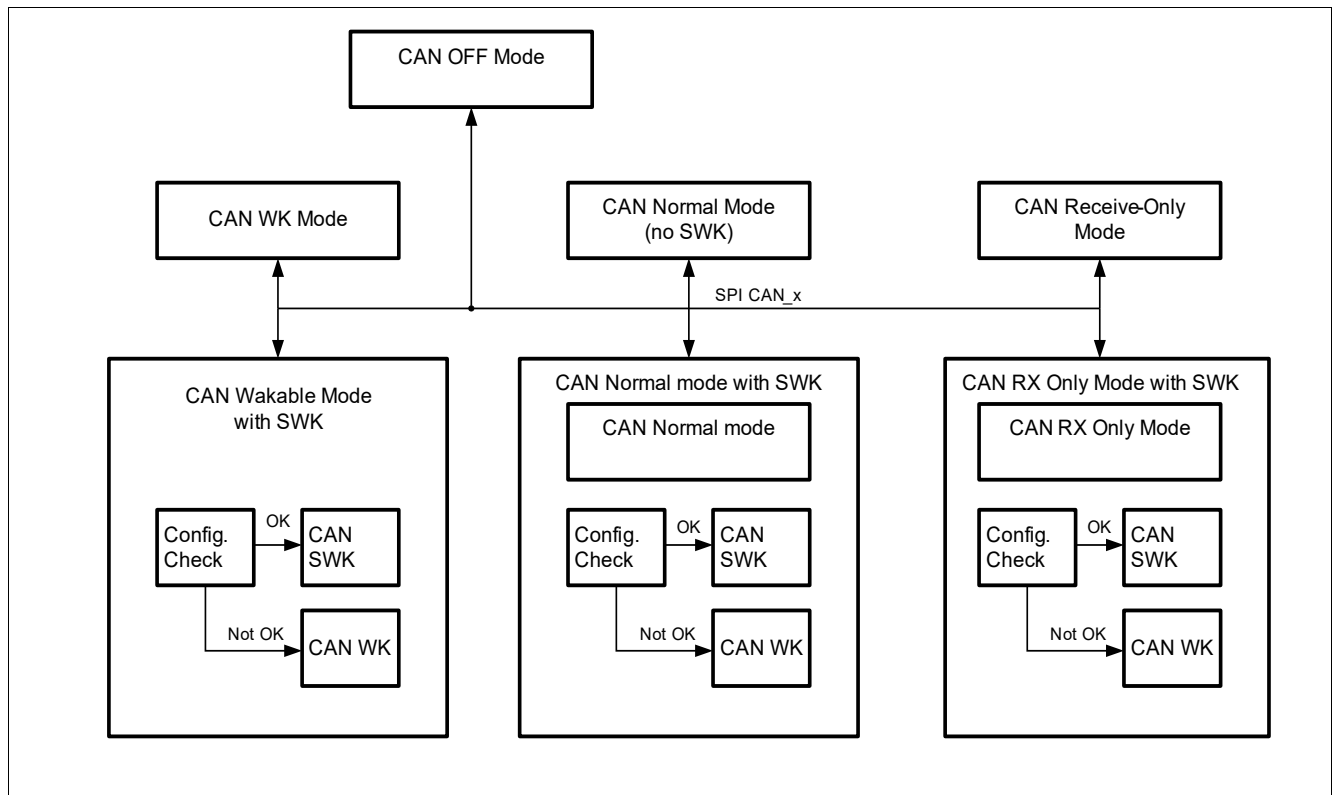
The mode of the CAN transceiver needs to be selected in Normal Mode. The CAN mode is programmed the bits CAN\_0, CAN\_1 and CAN\_2. In the low-power modes (Stop, Sleep) the CAN mode can not be changed via SPI.

The detailed state machine diagram including the CAN selective wake feature is shown in [Figure 5](#).

The application must now distinguish between the normal CAN operation and the selective wake function:

- CAN WK Mode: This is the normal CAN wake capable mode without the selective wake function.
- CAN SWK Mode: This is the CAN wake capable mode with the selective wake function enabled.

[Figure 25](#) shows the possible CAN transceiver modes.



**Figure 25 CAN SWK State Diagram**

##### 5.9.4.1 Normal Mode with SWK

In Normal Mode the CAN Transceiver can be switched into the following CAN modes:

- CAN OFF Mode
- CAN WK Mode (without SWK)
- CAN SWK Mode
- CAN Receive Only Mode (No SWK activated)
- CAN Receive Only Mode with SWK

- CAN Normal Mode (No SWK activated)
- CAN Normal Mode with SWK

In the CAN Normal Mode with SWK the CAN Transceiver works as in Normal Mode, so bus data is received through RXD, data is transmitted through TXD and sent to the bus. In addition the SWK block is active. It monitors the data on the CAN bus, updates the error counter and sets the **CANSIL** flag if there is no communication on the bus.

It will generate an CAN Wake interrupt in case a WUF is detected (RXD is not pulled to low in this configuration).

In CAN Receive Only Mode with SWK, CAN data can be received on RXD and SWK is active, no data can be sent to the bus.

The bit **SYSERR** = '0' indicates that the SWK function is enabled, and no frame error counter overflow is detected.

**Table 12 CAN modes selected via SPI in Normal Mode**

CAN mode	CAN_2	CAN_1	CAN_0
CAN OFF Mode	0	0	0
CAN WK Mode (no SWK)	0	0	1
CAN Receive Only Mode (no SWK)	0	1	0
CAN Normal Mode (no SWK)	0	1	1
CAN OFF Mode	1	0	0
CAN SWK Mode	1	0	1
CAN Receive Only Mode with SWK	1	1	0
CAN Normal Mode with SWK	1	1	1

When reading back CAN\_x the programmed mode is shown in Normal Mode. To read the real CAN mode the bits **SYSERR**, **SWK\_SET** and **CAN** have to be evaluated. A change out of Normal Mode can change the CAN\_0 and CAN\_1 bits.

#### 5.9.4.2 Stop Mode with SWK

In Stop Mode the CAN transceiver can be operated with the following CAN modes:

- CAN OFF Mode
- CAN WK Mode (no SWK)
- CAN SWK Mode
- CAN Receive Only Mode (no SWK)
- CAN Receive Only Mode with SWK
- CAN Normal Mode (no SWK)
- CAN Normal Mode with SWK

To enable CAN SWK Mode the CAN has to be switched to "CAN Normal Mode with SWK", "CAN Receive Only Mode with SWK" or to "CAN SWK Mode" in Normal Mode before sending the device to Stop Mode. The bit **SYSERR** = '0' indicates that the SWK function is enabled. The table shows the change of CAN mode when switching from Normal Mode to Stop Mode.

*Note: CAN Receive Only Mode in Stop Mode is implemented to also enable pretended networking (Partial networking done in the microcontroller).*

**Table 13 CAN modes change when switching from Normal Mode to Stop Mode**

Programmed CAN mode in Normal Mode	CAN_x bits	SYSERR bit	CAN mode in Stop Mode	CAN_x bits
CAN OFF Mode	000	0	CAN OFF Mode	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only Mode (no SWK)	010	0	CAN Receive Only Mode (no SWK)	010
CAN Normal Mode (no SWK)	011	0	CAN Normal Mode (no SWK)	011
CAN OFF Mode	100	0	CAN OFF Mode	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only Mode with SWK	110	0	CAN Receive Only Mode with SWK	110
CAN Receive Only Mode with SWK	110	1	CAN Receive Only Mode (no SWK)	110
CAN Normal Mode with SWK	111	0	CAN Normal Mode with SWK	111
CAN Normal Mode with SWK	111	1	CAN Normal Mode (no SWK)	111

*Note: When SYSERR is set then WUF frames will not be detected, i.e. the selective wake function is not activated (no SWK), but the MSB of CAN mode is not changed in the register.*

#### 5.9.4.3 Sleep Mode with SWK

In Sleep Mode the CAN Transceiver can be switched into the following CAN modes:

- CAN OFF Mode
- CAN WK Mode (without SWK)
- CAN SWK Mode

To enable “CAN SWK Mode” the CAN has to be switched to “CAN Normal Mode with SWK”, “CAN Receive Only Mode with SWK” or to “CAN SWK Mode” in Normal Mode before sending the device to Sleep Mode. The table shows the change of CAN mode when switching from Normal Mode to Sleep Mode.

A wake from Sleep Mode with Selective Wake (Valid WUF) leads to Restart Mode. In Restart Mode the CFG\_VAL bit will be cleared by the device, the SYSERR bit is not set. In the register CAN\_x the programmed CAN SWK Mode (101) can be read.

To enable the CAN SWK Mode again and to enter Sleep Mode the following sequence can be used; Program a CAN mode different from CAN SWK Mode (101, 110, 111), set the CFG\_VAL, CLEAR SYSERR bit, Set CAN\_x bits to CAN SWK Mode (101), switch the device to Sleep Mode.

To enable the CAN WK Mode or CAN SWK Mode again after a wake on CAN a rearming is required for the CAN transceiver to be wake capable again. The rearming is done by programming the CAN into a different mode with the CAN\_x bit and back into the CAN WK Mode or CAN SWK Mode. To avoid lock-up when switching the device into Sleep Mode with an already woken CAN transceiver, the device does an automatic rearming of the CAN transceiver when switching into Sleep Mode. So after switching into Sleep Mode the CAN transceiver is either in CAN SWK Mode or CAN WK Mode depending on CAN\_x setting and SYSERR bit (If CAN is switched to off mode it is also off in Sleep Mode).

**Table 14 CAN modes change when switching to Sleep Mode**

Programmed CAN mode in Normal Mode	CAN_x bits	SYSERR bit	CAN mode in Sleep Mode	CAN_x bits
CAN OFF Mode	000	0	CAN OFF Mode	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only Mode (no SWK)	010	0	CAN WK Mode (no SWK)	001
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001
CAN OFF Mode	100	0	CAN OFF Mode	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only Mode with SWK	110	0	CAN SWK Mode	101
CAN Receive Only Mode with SWK	110	1	CAN WK Mode (no SWK)	101
CAN Normal Mode with SWK	111	0	CAN SWK Mode	101
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101

#### 5.9.4.4 Restart Mode with SWK

If Restart Mode is entered the transceiver can change the CAN mode. During Restart or after Restart the following modes are possible:

- CAN OFF Mode
- CAN WK Mode (either still wake cable or already woken up)
- CAN SWK Mode (WUF Wake from Sleep)

**Table 15 CAN modes change in case of Restart out of Normal Mode**

Programmed CAN mode in Normal Mode	CAN_x bits	SYSERR bit	CAN mode in and after Restart Mode	CAN_x bits	SYSERR bit
CAN OFF Mode	000	0	CAN OFF Mode	000	0
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001	0
CAN Receive Only Mode (no SWK)	010	0	CAN WK Mode (no SWK)	001	0
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001	0
CAN OFF Mode	100	0	CAN OFF Mode	100	0
CAN SWK Mode	101	0	CAN WK Mode (no SWK)	101	1
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101	1
CAN Receive Only Mode with SWK	110	0	CAN WK Mode (no SWK)	101	1
CAN Receive Only Mode with SWK	110	1	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	0	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101	1

The various reasons for entering Restart Mode and the respective status flag settings are shown in [Table 16](#).

**Table 16 CAN modes change in case of Restart out of Sleep Mode**

CAN mode in Sleep Mode	CAN mode in and after Restart Mode	CAN_x	SYS ERR	CAN_WU	WUP	WUF	ECNT_x	Reason for Restart
CAN OFF Mode	CAN off	000	0	0	0	0	0	Wake on other wake source
CAN WK Mode	CAN woken up	001	0	1	1	0	0	Wake (WUP) on CAN
CAN WK Mode	CAN WK Mode	001	0	0	0	0	0	Wake on other wake source
CAN SWK Mode	CAN woken up	101	0	1	0/1 <sup>1)</sup>	1	x	Wake (WUF) on CAN
CAN SWK Mode,	CAN woken up	101	1	1	0/1 <sup>2)</sup>	0	100000	Wake due to error counter overflow
CAN SWK selected, CAN WK active	CAN woken up.	101	1	1	1	0	0	Wake (WUP) on CAN, config check was not pass
CAN SWK Mode	CAN WK Mode	101	1	0	0/1	0	x	Wake on other wake source

- 1) In case there is a WUF detection within  $t_{SILENCE}$  then the WUP bit will not be set. Otherwise it will always be set together with the WUF bit.
- 2) In some cases the WUP bit might stay cleared even after  $t_{SILENCE}$ , e.g. when the error counter expires without detecting a wake-up pattern.

#### 5.9.4.5 Fail-Safe Mode with SWK

When Fail-Safe Mode is entered the CAN transceiver is automatically set into CAN WK Mode (wake capable) without the selective wake function.

#### 5.9.5 Wake-up

A wake-up via CAN leads to a restart out of Sleep Mode and to an interrupt in Normal Mode, and in Stop Mode. After the wake event the bit CAN\_WU is set, and the details about the wake can be read out of the bits WUP, WUF, SYSERR, and ECNT.

#### 5.9.6 Configuration for SWK

The CAN protocol handler settings can be configured in following registers:

- **SWK\_BTL1\_CTRL** defines the number of time quanta in a bit time. This number depends also on the internal clock settings performed in the register **SWK\_CDR\_CTRL**.
- **SWK\_BTL1\_CTRL** defines the sampling point position.
- The respective receiver during frame detection mode can be selected via the bit **RX\_WK\_SEL**.
- The clock and data recovery (see also **Chapter 5.9.8**) can be configured in the registers **SWK\_CDR\_CTRL** and **SWK\_CDR\_LIMIT**.

The actual configuration for selective wake is done via the Selective Wake Control Registers SWK\_IDx\_CTRL, SWK\_MASK\_IDx\_CTRL, SWK\_DLC\_CTRL, SWK\_DATAx\_CTRL.

The oscillator has the option to be trimmed by the microcontroller. To measure the oscillator, the SPI bit OSC\_CAL needs to be set to 1 and a defined pulse needs to be given to the TXDCAN pin by the microcontroller (e.g. 1µs pulse, CAN needs to be switched off before). The device measures the length of the pulse by counting the time with the integrated oscillator. The counter value can be read out of the register SWK\_OSC\_CAL\_H\_STATE and SWK\_OSC\_CAL\_L\_STATE. To change the oscillator the trimming function needs to be enabled by setting the bits TRIM\_EN\_x = 11 (and OSC\_CAL = 1). The oscillator can then be adjusted by writing into the register **SWK\_OSC\_TRIM\_CTRL**. To finish the trimming, the bits TRIM\_EN\_x need to be set back to “00”.

### 5.9.7 CAN Flexible Data Rate (CAN FD) Tolerant Mode

The CAN FD tolerant mode can be activated by setting the bit **CAN\_FD\_EN** = ‘1’ in the register **SWK\_CAN\_FD\_CTRL**.

With this mode the internal CAN frame decoding will be stopped for CAN FD frame formats:

- The high baudrate part of a CAN FD frame will be ignored.
- No Error Handling (Bit Stuffing, CRC checking, Form Errors) will be applied to remaining CAN frame fields (Data Field, CRC Field, ...).
- No wake up is done on CAN FD frames.

The internal CAN frame decoder will be ready for new CAN frame reception when the End of frame (EOF) of a CAN FD frame is detected. The identification for a CAN FD frame is based on the EDL Bit, which is sent in the Control Field of a CAN FD frame:

- EDL Bit = 1 identifies the current frame as an CAN FD frame and will stop further decoding on it.
- EDL Bit = 0 identifies the current frame as CAN 2.0 frame and processing of the frame will be continued.

In this way it is possible to send mixed CAN frame formats without affecting the selective wake functionality by error counter increment and subsequent misleading wake up. In addition to the **CAN\_FD\_EN** bit also a filter setting must be provided for the CAN FD tolerant mode. This filter setting defines the minimum dominant time for a CAN FD dominant bit which will be considered as a dominant bit from the CAN FD frame decoder. This value must be aligned with the selected high baudrate of the data field in the CAN network.

To support programming via CAN during CAN FD mode a dedicated SPI bit **DIS\_ERR\_CNT** is available to avoid an overflow of the implemented error counter (see also **Chapter 5.9.2.4**).

The behavior of the error counter depends on the setting of the bits **DIS\_ERR\_CNT** and **CAN\_FD\_EN** and is show in below table:

**Table 17 Error Counter Behavior**

<b>DIS_ERR_CNT</b> setting	<b>CAN_FD_EN</b> setting	<b>Error Counter Behavior</b>
0	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO11898-2:2016)
1	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO11898-2:2016)

**Table 17 Error Counter Behavior** (cont'd)

<b>DIS_ERR_CNT setting</b>	<b>CAN_FD_EN setting</b>	<b>Error Counter Behavior</b>
0	1	Error Counter counts up when an incorrect/corrupted CAN frame is received; counts down when correct, including CAN FD frame, is received
1	1	Error Counter is and stays cleared to avoid an overflow during programming via CAN

The **DIS\_ERR\_CNT** bit is automatically cleared at **t<sub>SILENCE</sub>** expiration.



### 5.9.8 Clock and Data Recovery

In order to compensate possible deviations on the CAN oscillator frequency caused by assembly and lifetime effects, the device features an integrated clock and data recovery (CDR).

It is recommended to always enable the CDR feature during SWK operation.

#### 5.9.8.1 Configuring the Clock Data Recovery for SWK

The Clock and Data Recovery can be optionally enabled or disabled with the **CDR\_EN** bit in the **SWK\_CDR\_CTRL** SPI register. In case the feature is enabled, the CAN bit stream will be measured and the internal clock used for the CAN frame decoding will be updated accordingly.

Before the Clock and Data Recovery can be used it must be configured properly related to the used baud rate and filtering characteristics (see [Chapter 5.9.8.2](#)).

It is strongly recommended not to enable/disable the Clock Recovery during a active CAN Communication.

To ensure this, it is recommended to enable/disable it during CAN off (**BUS\_CTRL**; CAN[2:0] = 000).

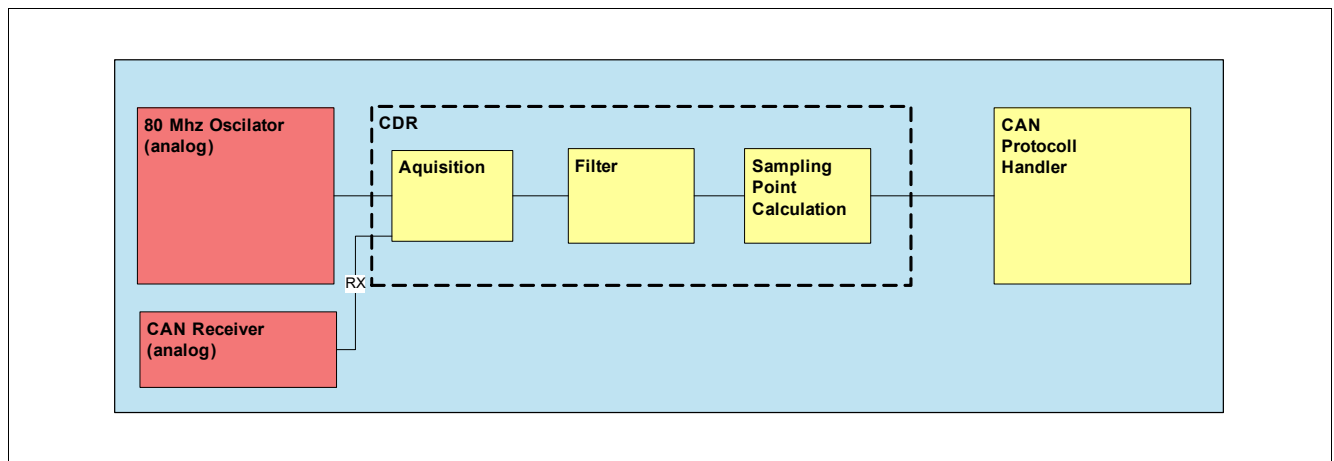


Figure 26 Clock and Data Recovery Block Diagram

### 5.9.8.2 Setup of Clock and Data Recovery

It is strongly recommended to enable the clock and data recovery feature only when the setup of the clock and data recovery is finished.

The following sequence should be followed for enabling the clock and data recovery feature:

- Step 1: Switch CAN to off and **CDR\_EN** to off  
Write SPI Register **BUS\_CTRL** (CAN[2:0] = 000).
- Step 2: Configure CDR Input clock frequency  
Write SPI Register **SWK\_CDR\_CTRL** (SEL\_OSC\_CLK[1:0]).
- Step 3: Configure Bit timing Logic  
Write SPI Register **SWK\_BTL1\_CTRL** and adjust **SWK\_CDR\_LIMIT** according to **Table 91**.
- Step 4: Enable Clock and Data Recovery  
Choose filter settings for Clock and Data recovery. Write SPI Register **SWK\_CDR\_CTRL** with **CDR\_EN** = 1.

Additional hints for the CDR configuration and operation:

- Even if the CDR is disabled, when the baud rate is changed, the settings of **SEL\_OSC\_CLK** in the register **SWK\_CDR\_CTRL** and **SWK\_BTL1\_CTRL** have to be updated accordingly.
- The **SWK\_CDR\_LIMIT** registers has to be also updated when the baud rate or clock frequency is changed (the CDR is discarding all the acquisitions and loses all acquired information, if the limits are reached - the **SWK\_BTL1\_CTRL** value is reloaded as starting point for the next acquisitions).
- When updating the CDR registers, it is recommended to disable the CDR and to enable it again only after the new settings are updated.
- The **SWK\_BTL1\_CTRL** register represents the sampling point position. It is recommended to be used at default value: 11 0011 (~80%).

## 5.9.9 Electrical Characteristics

**Table 18 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ;  $4.75 \text{ V} < V_{CAN} < 5.25 \text{ V}$ ;  $R_L = 60 \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Partial Network Timing							
Bus Bias reaction time	$t_{\text{bias}}$	–	–	250	μs	<sup>1)</sup> Load $R_{\text{L}} = 60 \, \Omega$ , $C_{\text{L}} = 100 \, \text{pF}$ , $C_{\text{GND}} = 100 \, \text{pF}$	P_5.10.2
Wake-up reaction time (WUP or WUF)	$t_{\text{WU\_WUP/WUF}}$	–	–	100	μs	<sup>1)2)3)</sup> Wake-up reaction time after a valid WUP or WUF;	P_5.10.3
Min. Bit Time	$t_{\text{Bit\_min}}$	1	–	–	μs	<sup>1)4)</sup>	P_5.10.4

**Table 18 Electrical Characteristics (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ;  $4.75 \text{ V} < V_{CAN} < 5.25 \text{ V}$ ;  $R_L = 60 \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN FD Tolerance <sup>5)</sup>							
SOF acceptance	$n_{\text{Bits\_idle}}$	6	–	10	bits	<sup>6)</sup> Number of recessive bits before a new SOF shall be accepted	P_5.10.5
Dominant signals which are ignored (up to 2MBit/s)	$t_{\text{FD\_Glitch\_4}}$	0	-	5	%	<sup>6)7)8)</sup> of arbitration bit time; to be configured via <b>FD_FILTER</b> ;	P_5.10.6
Dominant signals which are ignored (up to 5MBit/s)	$t_{\text{FD\_Glitch\_10}}$	0	-	2.5	%	<sup>6)8)9)</sup> ofarbitration bit time; to be configured via <b>FD_FILTER</b> ;	P_5.10.7
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 2MBit/s)	$t_{\text{FD\_DOM\_4}}$	17.5	-	-	%	<sup>6)7)8)</sup> ofarbitration bit time; to be configured via <b>FD_FILTER</b> ;	P_5.10.8
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 5MBit/s)	$t_{\text{FD\_DOM\_10}}$	8.75	-	-	%	<sup>6)8)9)</sup> ofarbitration bit time; to be configured via <b>FD_FILTER</b> ;	P_5.10.9

- 1) Not subject to production test, tolerance defined by internal oscillator tolerance.
- 2) Wake-up is signaled via INTN pin activation in Stop Mode and via VCC1 ramping up with wake from Sleep Mode.
- 3) For WUP: time starts with end of last dominant phase of WUP; for WUF: time starts with end of CRC delimiter of the WUF.
- 4) The minimum bit time corresponds to a maximum bit rate of 1 Mbit/s. The lower end of the bit rate depends on the protocol IC or the permanent dominant detection circuitry preventing a permanently dominant clamped bus.
- 5) Applies for an arbitration rate of up to 500 kbps until the FDF bit is detected.
- 6) Not subject to production test; specified by design.
- 7) A data phase bit rate less or equal to four times of the arbitration bit rate or 2 Mbit/s, whichever is lower.
- 8) Parameter applies only for the Normal Mode CAN receiver ( $RX\_WK\_sel = 1$ ).
- 9) A data phase bit rate less or equal to four times of the arbitration bit rate or 5 Mbit/s, whichever is lower.

## 6 Voltage Regulator 1

### 6.1 Block Description

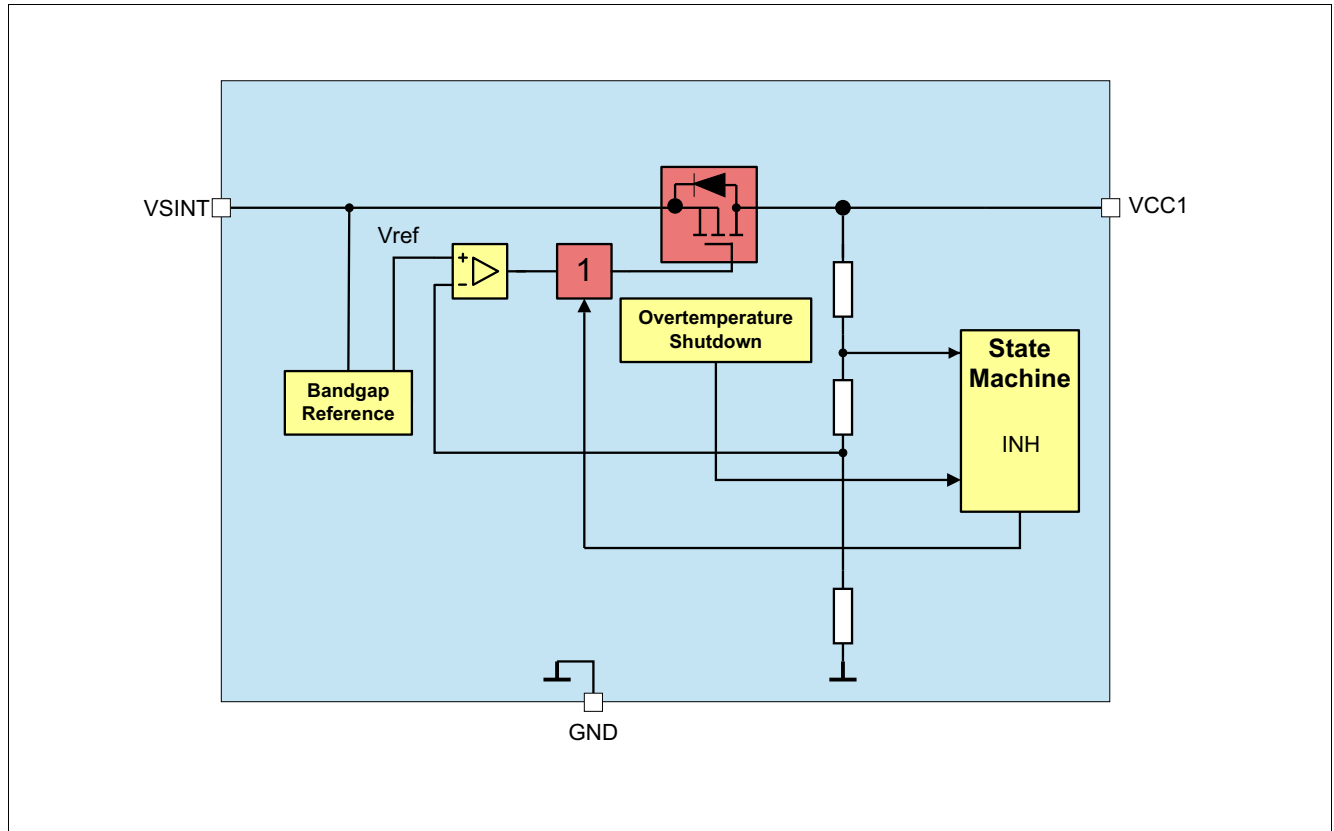


Figure 27 Module Block Diagram

#### Functional Features

- 5 V low-drop voltage regulator.
- Undervoltage monitoring with adjustable reset level and VCC1 undervoltage prewarning (refer to [Chapter 12.7](#) and [Chapter 12.8](#) for more information).
- Short circuit detection and switch off with undervoltage fail threshold, device enters Fail-Safe Mode.
- Effective capacitance must be  $\geq 1 \mu\text{F}$  at nominal voltage output for stability. A  $2.2 \mu\text{F}$  ceramic capacitor (MLCC) is recommended for best transient response.
- Output current capability up to  $I_{VCC1,lim}$ .

## Voltage Regulator 1

### 6.2 Functional Description

The Voltage Regulator 1 (=VCC1) is “ON” in Normal Mode and Stop Mode and is disabled in Sleep Mode and in Fail-Safe Mode. The regulator can provide an output current up to  $I_{VCC1,lim}$ .

For low-quiescent current reasons, the output voltage tolerance is decreased in Stop Mode because only the less accurate low-power mode regulator will be active for small loads. If the load current on VCC1 exceeds the selected threshold ( $I_{VCC1,peak1,r}$  or  $I_{VCC1,peak2,r}$ ) then the high-power mode regulator will be also activated to support an optimum dynamic load behavior. The current consumption will then increase (approx. 2.8 mA additional quiescent current). The device mode stays unchanged.

If the load current on VCC1 falls below the selected threshold ( $I_{VCC1,peak1,f}$  or  $I_{VCC1,peak2,f}$ ), then the low-quiescent current mode is resumed again by disabling the high-power mode regulator.

Both regulators (low-power mode and high-power mode) are active in Normal Mode.

Two different active peak thresholds can be selected via SPI:

- **I\_PEAK\_TH** = ‘0’ (default): the lower VCC1 active peak threshold 1 is selected with lowest quiescent current consumption in Stop Mode.
- **I\_PEAK\_TH** = ‘1’: the higher VCC1 active peak threshold 2 is selected with an increased quiescent current consumption in Stop Mode.

**Voltage Regulator 1**

**6.3 Electrical Characteristics**

**Table 19 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage including Line and Load Regulation	$V_{CC1,out1}$	4.9	5.0	5.1	V	<sup>1)</sup> Normal Mode; $10 \mu\text{A} < I_{VCC1} < 150 \text{ mA}$ ;	P_6.3.1
Output Voltage including Line and Load Regulation (Full Load Current Range)	$V_{CC1,out2}$	4.9	5.0	5.1	V	<sup>1)</sup> Normal Mode; $6 \text{ V} < V_{SINT} < 28 \text{ V}$ ; $10 \mu\text{A} < I_{VCC1} < 250 \text{ mA}$	P_6.3.2
Output Voltage including Line and Load Regulation (Higher Accuracy Range)	$V_{CC1,out3}$	4.95	–	5.05	V	<sup>2)</sup> Normal Mode; $20 \text{ mA} < I_{VCC1} < 80 \text{ mA}$ ; $8 \text{ V} < V_{SINT} < 18 \text{ V}$ ; $25^\circ\text{C} < T_j < 150^\circ\text{C}$	P_6.3.3
Output Voltage including Line and Load Regulation (low-power mode)	$V_{CC1,out4}$	4.9	5.05	5.2	V	Stop Mode; $10 \mu\text{A} < I_{VCC1} < I_{VCC1,peak}$	P_6.3.4
Output Drop Voltage	$V_{CC1,d1}$	–	200	400	mV	$I_{VCC1} = 50 \text{ mA}$ , $V_{SINT} = 5 \text{ V}$	P_6.3.9
Output Drop Voltage	$V_{CC1,d2}$	–	300	500	mV	$I_{VCC1} = 150 \text{ mA}$ , $V_{SINT} = 5 \text{ V}$	P_6.3.10
VCC1 Active Peak Threshold 1 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC1,lpeak1,r}$	–	3.25	5.0	mA	<sup>2)</sup> $I_{CC1}$ rising; $V_{SINT} = 13.5 \text{ V}$ ; <b>I_PEAK_TH</b> = '0'	P_6.3.17
VCC1 Active Peak Threshold 1 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC1,lpeak1,f}$	1.2	1.7	–	mA	<sup>2)</sup> $I_{CC1}$ falling; $V_{SINT} = 13.5 \text{ V}$ ; <b>I_PEAK_TH</b> = '0'	P_6.3.18
VCC1 Active Peak Threshold 2 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC1,lpeak2,r}$	6	–	20	mA	<sup>2)</sup> $I_{CC1}$ rising; $V_{SINT} = 13.5 \text{ V}$ ; <b>I_PEAK_TH</b> = '1'	P_6.3.19
VCC1 Active Peak Threshold 2 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC1,lpeak2,f}$	5	–	15	mA	<sup>2)</sup> $I_{CC1}$ falling; $V_{SINT} = 13.5 \text{ V}$ ; <b>I_PEAK_TH</b> = '1'	P_6.3.20
Overcurrent Limitation	$I_{VCC1,lim}$	260	360	500	mA	current following out of pin, $V_{CC1} = 0 \text{ V}$ <sup>2)</sup>	P_6.3.21

**Voltage Regulator 1**

**Table 19 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Minimum Output Capacitance for stability	$C_{VCC1,min}$	1 <sup>3)</sup>	–	–	$\mu\text{F}$	2)	P_6.3.22
Maximum Output Capacitance	$C_{VCC1,max}$	–	–	47	$\mu\text{F}$	2)	P_6.3.23

1) In Stop Mode, the specified output voltage tolerance applies when  $I_{VCC1}$  has exceeded the selected active peak threshold ( $I_{VCC1,peak1,r}$  or  $I_{VCC1,peak2,r}$ ) but with increased current consumption.

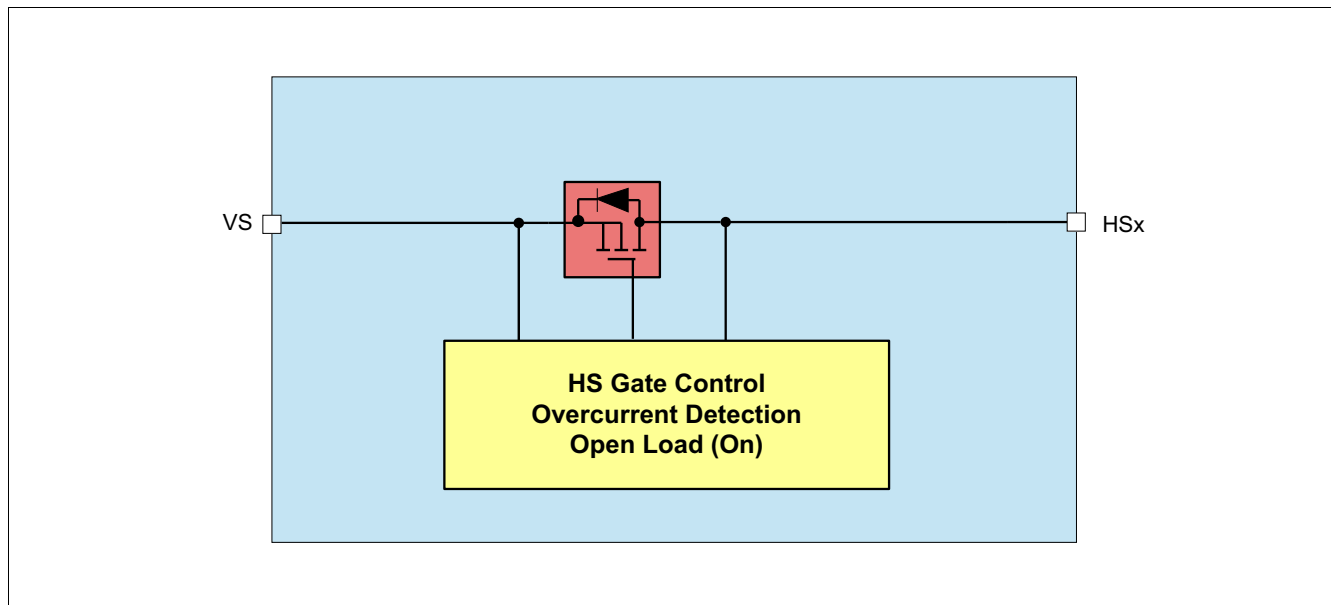
2) Not subject to production test, specified by design.

3) Value is meant to be an effective value at rated output voltage level.



## 7 High-Side Switch

### 7.1 Block Description



**Figure 28 High-Side Module Block Diagram**

#### Features

- All HSx supplied by VS
- Under voltage switch off configurable via SPI.
- Dedicated over voltage switch off per each HSx in Normal Mode- configurable via SPI.
- Overvoltage switch off in Stop Mode and Sleep Mode- configurable via SPI.
- Overcurrent detection and switch off.
- Open load detection in ON-state.
- PWM capability with internal or external timers configurable via SPI.
- Switch recovery after removal of OV or UV condition configurable via SPI.

### 7.2 Functional Description

The High-Side switches can be used for control of LEDs, as supply for the wake inputs and for other loads (except inductive load). The High-Side outputs can be controlled either directly via SPI by the integrated timers or by the integrated PWM generators or by external sync signal (using WK4/SYNC pin).

The high-side outputs are supplied by VS pin. The topology supports improved cranking condition behavior. The configuration of the High-Sides (Permanent On, PWM, cyclic sense, etc.) drivers must be done in Normal Mode. The configuration is taken over in Stop Mode or Sleep Mode and cannot be modified. When entering Restart Mode or Fail-Safe Mode the HSx outputs are disabled.

#### 7.2.1 Under Voltage Switch Off

All HS drivers in on-state are switched off in case of under voltage on VS. The feature can be disabled by setting the SPI bit **HS\_UV\_SD\_DIS**.

## High-Side Switch

After release of under voltage condition, the HSx switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the bit **HS\_UV\_REC** is set. Otherwise the switches will stay off and the respective SPI control bits are cleared.

The under voltage is signaled in the bit **HS\_UV**, no other error bits are set.

### 7.2.2 Over Voltage Switch Off

The HS drivers in on-state are switched off in case of over voltage on VS.. In Normal Mode the HSx can be kept in on-state above the VS overvoltage threshold if the HSx\_OV\_SDN\_DIS bit is set.

In Stop Mode or Sleep Modes all HS drivers can be kept in on-state if **HS\_OV\_SDS\_DIS** bit is set.

When the HSx are configured to switch off in case of over voltage condition, after release of over voltage condition, the HS switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the respective bit HSx\_OV\_REC is set. Otherwise the switch will stay off and the respective SPI control bits are cleared. This configuration is available for each HSx.

The over voltage is signaled in the bit **HS\_OV**, no other error bits are set.

### 7.2.3 Over Current Detection and Switch Off

If the load current exceeds the over current shutdown threshold for a time longer then the over current shutdown filter time the output is switched off.

The over current condition and the switch off is signaled with the respective HSx\_OC\_OT bit in the register **HS\_OL\_OC\_OT\_STAT**. The HSx configuration is then reset to 000 by the device. To activate the High-Side again the HSx configuration has to be set to ON (001) or be programmed to a timer function. It is recommended to clear the over current bit before activation the High-Side switch, as the bits are not cleared automatically by the device.

### 7.2.4 Open Load Detection

Open load detection on the High-Side outputs is done during on state of the output. If the current in the activated output falls below the open load detection current threshold, the open load is detected and signaled via the respective bit HS1\_OL, HS2\_OL, HS3\_OL, or HS4\_OL in the register **HS\_OL\_OC\_OT\_STAT**. The High-Side output stays activated.. If the open load condition disappears the Open Load bit in the SPI can be cleared. The bits are not cleared automatically by the device.

### 7.2.5 PWM, Timer and SYNC Function

Each integrated HSx can be configured in different ways, in particular:

- Static OFF
- Static ON
- Timer 1
- Timer 2
- Internal generator PWM1
- Internal generator PWM2
- Internal generator PWM3
- Internal generator PWM4
- SYNC (via WK4)

*Note: PWMx mentioned in this chapter refer to the internal PWM generators, which are configured by the registers **HS\_CTRL** and **PWM\_CTRL**. They can be used to control the internal high-side switches HSx.*

## High-Side Switch

*Note:* PWMx mentioned in this chapter **do not refer** to the PWMx pins. The PWMx pins are used for the PWM operation of the bridge drivers, to control the external MOSFETs.

### Static configuration (ON/OFF)

This configuration set the HSx permanently ON or OFF. This configuration is available in Normal Mode, Stop Mode and Sleep Mode.

The configuration shall be done via SPI.

### Timer configuration (TIMER1 or TIMER2)

Two Timers are dedicated to control the ON phase of dedicated HS outputs.

The Timers are mapped to the dedicated HS outputs. Period and the duty cycle can be independently configured with via SPI.

### PWM configuration (PWM1..PWM4)

Several internal PWM generators are dedicated to generate a PWM signal on the HSx output, e.g. for brightness adjustment or compensation of supply voltage fluctuation. The PWM generators are mapped to the dedicated HS outputs, and the duty cycle can be independently configured with a 10-bit resolution via SPI (**PWM\_CTRL**). Two different frequencies can be selected independently for every PWM generator in the register **PWM\_CTRL**.

In order to assign and configure the PWMx to specific HSx, the follow steps have to be followed:

- Configure duty cycle and frequency for respective PWM generator in **PWM\_CTRL**.
- Assign PWM generator to respective HS switch(es) in **HSx\_CTRL**.
- The PWM generation will start right after the HSx is assigned to the PWM generator (**HS\_CTRL**).

*Note:* The min. on-time during PWM is limited by the actual on- and off-time of the respective HS switch, e.g. the PWM setting '00 0000 0001' could not be realized.

### SYNC configuration (using WK4)

Another possible configuration is to use the WK4 (set as SYNC pin) and mapped to one dedicated HSx output.

The configuration of the WK4/SYNC bit is done using the **WK\_EN** bits. If the **WK\_EN**=10<sub>B</sub> (SYNC selected), all bits in WK4 bank are ignored and wake-up capability on WK4 is not available.

Only after the WK4/SYNC configuration, the HSx can be configured for SYNC usage (HSx = 1000<sub>B</sub>).

## High-Side Switch

### 7.3 Electrical Characteristics

**Table 20 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

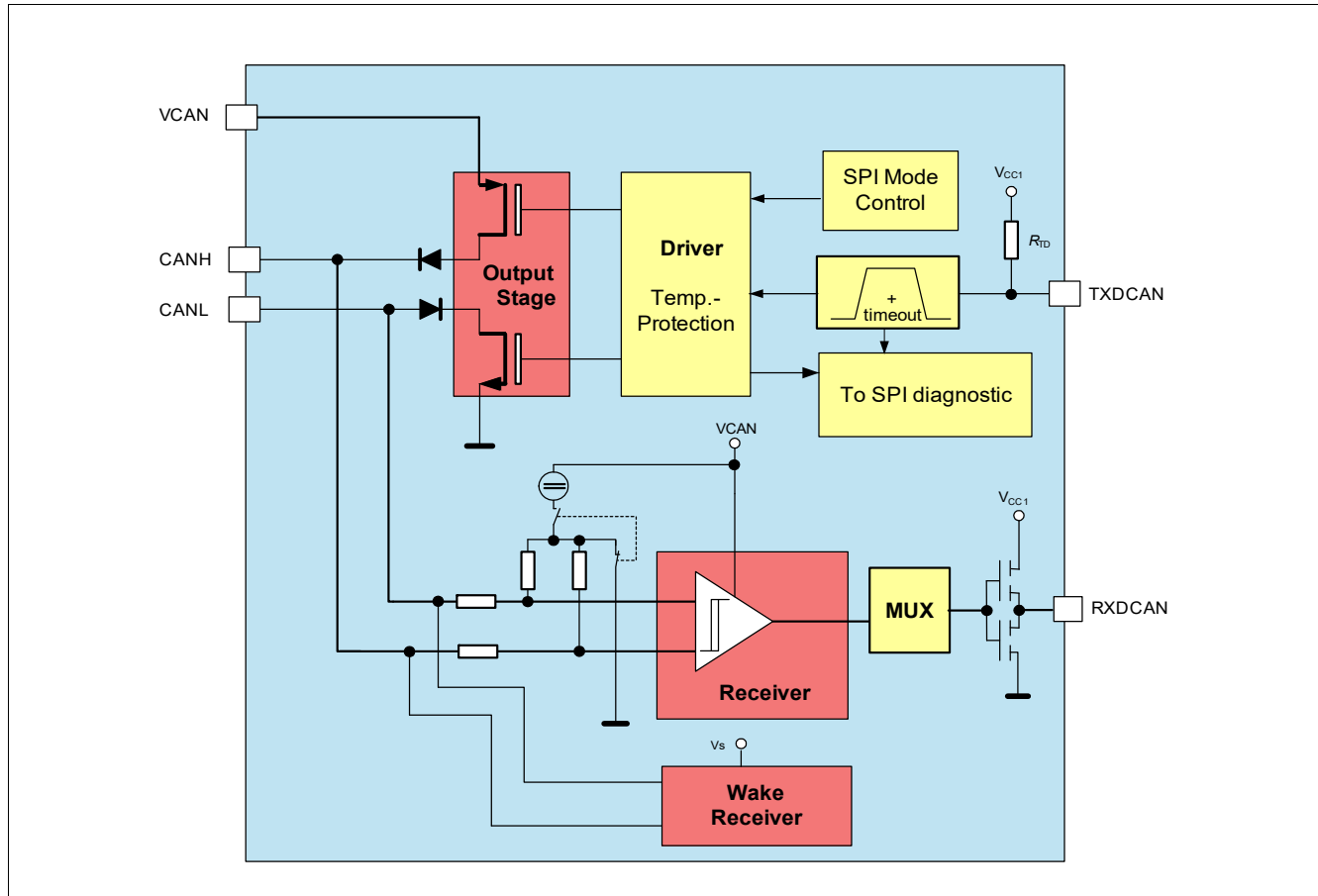
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output HS1, HS2, HS3, HS4							
Static Drain-Source ON Resistance HSx	$R_{\text{ON,HS25}}$	–	7	–	$\Omega$	$I_{\text{ds}} = 60 \text{ mA}$ , $T_{\text{j}} < 25^{\circ}\text{C}$	P_7.3.1
Static Drain-Source ON Resistance HSx	$R_{\text{ON,HS150}}$	–	11.5	16	$\Omega$	$I_{\text{ds}} = 60 \text{ mA}$ , $T_{\text{j}} < 150^{\circ}\text{C}$	P_7.3.2
Leakage Current HSx / per channel	$I_{\text{leak,HS}}$	–	–	2	$\mu\text{A}$	<sup>1)</sup> $0 \text{ V} < V_{\text{HSx}} < V_{\text{S\_HS}}$ ; $T_{\text{j}} < 85^{\circ}\text{C}$	P_7.3.3
Output Slew Rate (rising)	$SR_{\text{raise,HS}}$	0.8	–	2.5	$\text{V}/\mu\text{s}$	<sup>1)</sup> 20 to 80% $V_{\text{S}} = 6 \text{ to } 18 \text{ V}$ $R_{\text{L}} = 220 \Omega$	P_7.3.4
Output Slew Rate (falling)	$SR_{\text{fall,HS}}$	-2.5	–	-0.8	$\text{V}/\mu\text{s}$	<sup>1)</sup> 80 to 20% $V_{\text{S}} = 6 \text{ to } 18 \text{ V}$ $R_{\text{L}} = 220 \Omega$	P_7.3.5
Switch-on time HSx	$t_{\text{ON,HS}}$	3	–	30	$\mu\text{s}$	CSN = HIGH to $0.8 \times V_{\text{S}}$ ; $R_{\text{L}} = 220 \Omega$ ; $V_{\text{S}} = 6 \text{ to } 18 \text{ V}$	P_7.3.6
Switch-off time HSx	$t_{\text{OFF,HS}}$	3	–	30	$\mu\text{s}$	CSN = HIGH to $0.2 \times V_{\text{S}}$ ; $R_{\text{L}} = 220 \Omega$ ; $V_{\text{S}} = 6 \text{ to } 18 \text{ V}$	P_7.3.7
Short Circuit Shutdown Current	$I_{\text{SD,HS}}$	150	245	300	$\text{mA}$	$V_{\text{S}} = 6 \text{ to } 20 \text{ V}$	P_7.3.8
Short Circuit Shutdown Filter Time	$t_{\text{SD,HS}}$	12	16	22	$\mu\text{s}$	<sup>2)</sup>	P_7.3.9
Open Load Detection Current	$I_{\text{OL,HS}}$	0.4	–	2	$\text{mA}$	hysteresis included	P_7.3.10
Open Load Detection hysteresis	$I_{\text{OL,HS,hys}}$	–	0.45	–	$\text{mA}$	<sup>1)</sup>	P_7.3.11
Open Load Detection Filter Time	$t_{\text{OL,HS}}$	160	220	270	$\mu\text{s}$	<sup>2)</sup>	P_7.3.12

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

## 8 High Speed CAN Transceiver

### 8.1 Block Description



**Figure 29 Functional Block Diagram**

### 8.2 Functional Description

The Controller Area Network (CAN) transceiver part of the device provides High-Speed (HS) differential mode data transmission (up to 2 Mbaud/s) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO11898-2:2016 and SAE J2284.

The CAN FD transceiver offers low-power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive Only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp 15/30 applications).

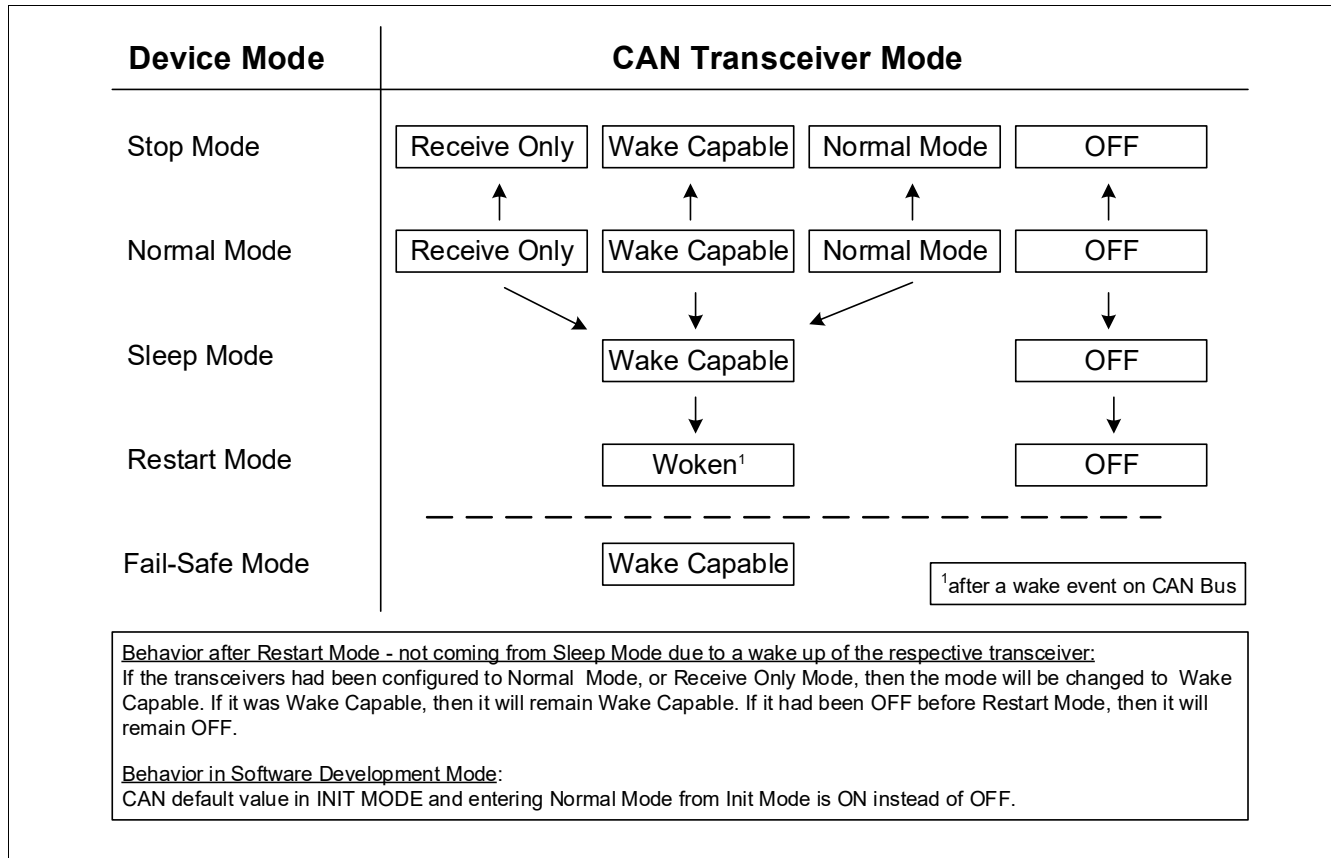
A wake-up from the CAN Wake Capable Mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and is woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

## High Speed CAN Transceiver

The transceiver can also be configured to Wake Capable in order to save current and to ensure a safe transition from Normal Mode to Sleep Mode (to avoid losing messages).

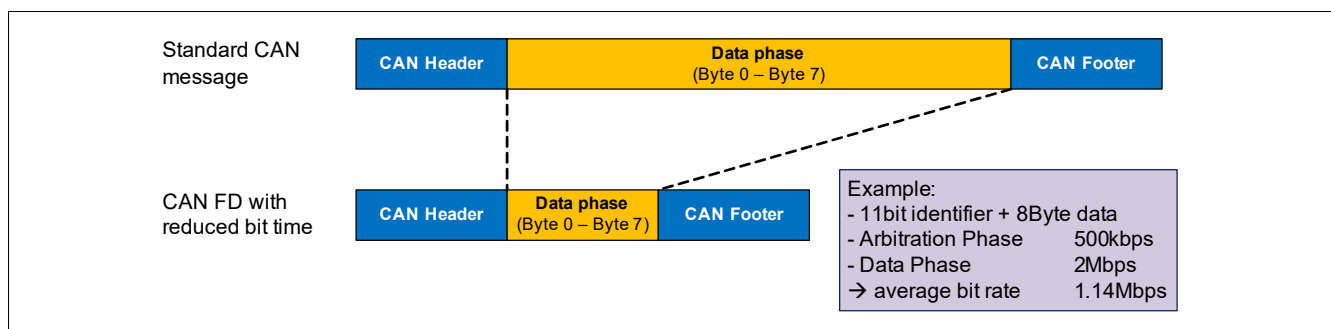
**Figure 30** shows the possible transceiver mode transition when changing the device mode.



**Figure 30 CAN Mode Control Diagram**

## CAN FD Support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO11898-2:2016. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then to return to the longer bit time at the CRC delimiter, before the receivers transmit their acknowledge bits. See also **Figure 31**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.



**Figure 31 Bit Rate Increase with CAN FD vs. Standard CAN**

## High Speed CAN Transceiver

Not only the physical layer must support CAN FD but also the CAN controller. In case the CAN controller is not able to support CAN FD then the respective CAN node must at least tolerate CAN FD communication. This CAN FD tolerant mode is realized in the physical layer.

### 8.2.1 CAN OFF Mode

The CAN OFF Mode is the default mode after power-up of the device. It is available in all device modes and is intended to completely stop CAN activities or when CAN communication is not needed. In CAN OFF Mode, a wake-up event on the bus will be ignored.

### 8.2.2 CAN Normal Mode

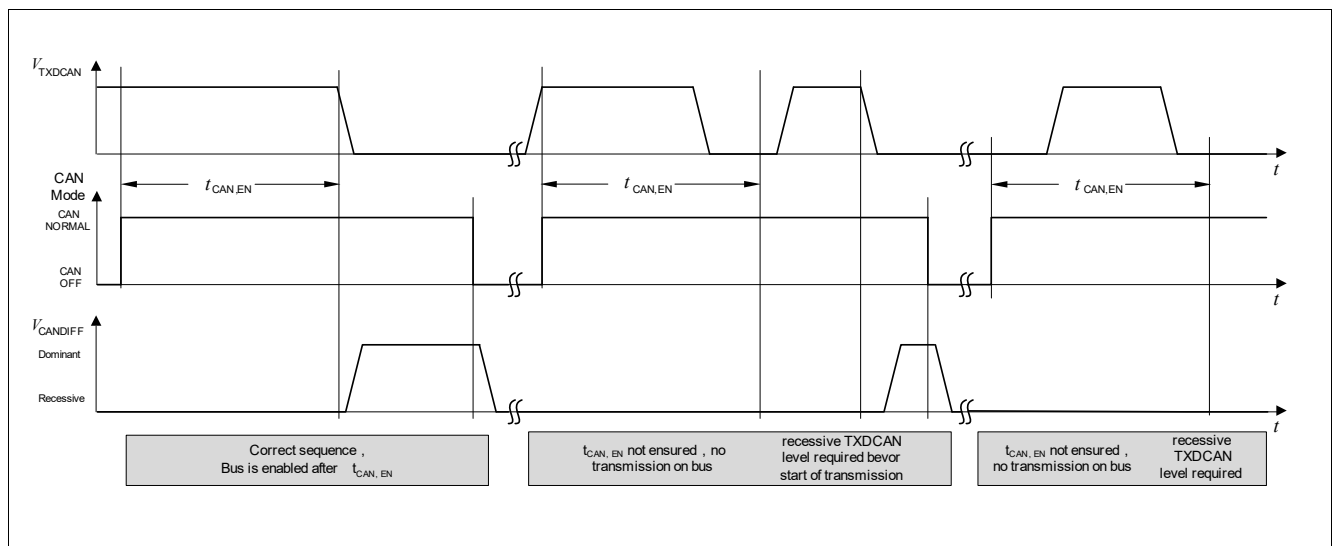
The CAN Transceiver is enabled via SPI in Normal Mode. CAN Normal Mode is designed for normal data transmission/reception within the HS-CAN network. The mode is available in Normal Mode and in Stop Mode. The bus biasing is set to  $V_{CAN}/2$ .

#### Transmission

The signal from the microcontroller is applied to the TXDCAN input of the device. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

#### Enabling sequence

The CAN transceiver requires an enabling time  $t_{CAN,EN}$  before a message can be sent on the bus. This means that the TXDCAN signal can only be pulled low after the enabling time. If this is not ensured, then the TXDCAN needs to be set back to high (=recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 32** shows different scenarios and explanations for CAN enabling.



**Figure 32 CAN Transceiver Enabling Sequence**

#### Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

#### Reception

Analog CAN bus signals are converted into digital signals at RXDCAN via the differential input receiver.

### 8.2.3 CAN Receive Only Mode

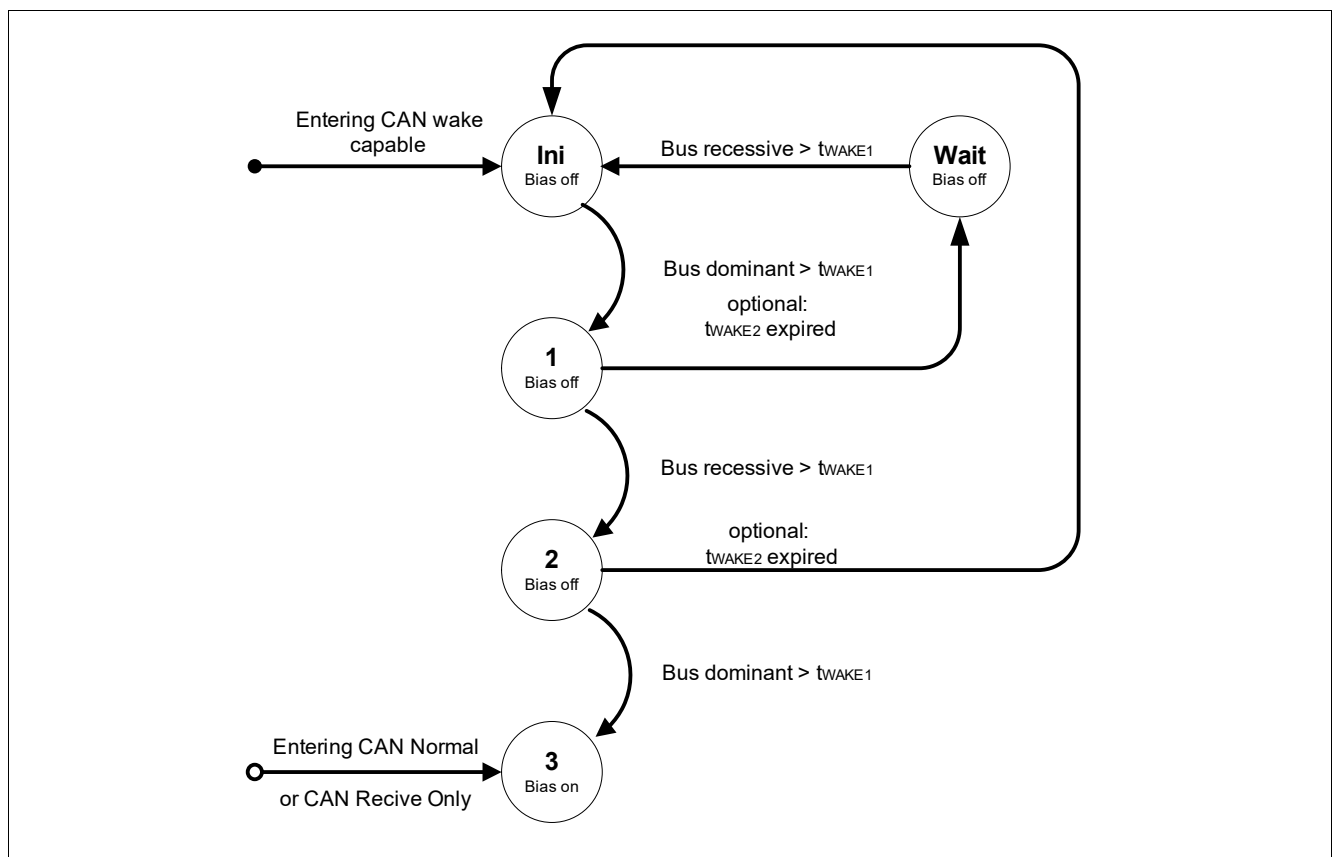
In CAN Receive Only Mode (RX only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command in Normal Mode and in Stop Mode.

*Note: The transceiver is still properly working in CAN Receive Only Mode even if VCAN is not available because of an independent receiver supply.*

### 8.2.4 CAN Wake Capable Mode

This mode can be used in Stop Mode, Sleep Mode, Restart Mode and Normal Mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in Fail-Safe Mode. A wake-up signal on the bus results in a change of behavior of the device, as described in [Table 21](#). As a signalization to the microcontroller, the RXDCAN pin is set low and will stay low until the CAN transceiver is changed to any other mode. After a wake-up event, the transceiver can be switched to CAN Normal Mode via SPI for bus communication.

As shown in [Figure 33](#), a wake-up pattern (WUP) is signaled on the bus by two consecutive dominant bus levels for at least  $t_{Wake1}$  (wake-up time) and less than  $t_{Wake2}$ , each separated by a recessive bus level of greater than  $t_{Wake1}$  and shorter than  $t_{Wake2}$ .



**Figure 33 CAN Wake-up Pattern Detection according to the Definition in ISO11898-2:2016**

#### Rearming the Transceiver for Wake Capability

After a BUS wake-up event, the transceiver is woken. However, the **CAN** transceiver mode bits will still show wake capable (=‘01’) so that the RXDCAN signal will be pulled low. There are two possibilities how the CAN transceiver’s wake capable mode is enabled again after a wake-up event:

- The CAN transceiver mode must be toggled, i.e. switched from CAN Wake Capable Mode to CAN Normal Mode, CAN Receive Only Mode or CAN OFF Mode, before switching to CAN Wake Capable Mode again.
- Rearming is done automatically when the device is changed to Stop Mode, Sleep Mode or Fail-Safe Mode to ensure wake-up capability.



## High Speed CAN Transceiver

### Wake-Up in Stop Mode and Normal Mode

In Stop Mode, if a wake-up is detected, it is always signaled by the INTN output and in the **WK\_STAT** SPI register. It is also signaled by RXDCAN pulled to low. The same applies for the Normal Mode. The microcontroller should set the device from Stop Mode to Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in Stop Mode after a bus wake-up event in case it was disabled before (if bit **WD\_EN\_WK\_BUS** was configured to high before).

### Wake-Up in Sleep Mode

Wake-up is possible via a CAN message. The wake-up automatically transfers the device into the Restart Mode and from there to Normal Mode the corresponding RXDCAN pin is set to low. The microcontroller is able to detect the low signal on RXDCAN and to read the wake source out of the **WK\_STAT** register via SPI. No interrupt is generated when coming out of Sleep Mode. The microcontroller can now for example switch the CAN transceiver into CAN Normal Mode via SPI to start communication.

**Table 21 Action due to CAN Bus Wake-Up**

Mode	Mode after Wake	VCC1	INTN	RXDCAN
Normal Mode	Normal Mode	On	Low	Low
Stop Mode	Stop Mode	On	Low	Low
Sleep Mode	Restart Mode	Ramping Up	High	Low
Restart Mode	Restart Mode	On	High	Low
Fail-Safe Mode	Restart Mode	Ramping Up	High	Low

## 8.2.5 CAN Bus termination

In accordance with the CAN configuration, four types of bus terminations are allowed:

- **CAN Normal Mode:** VCAN/2 termination.
- **CAN Receive Only Mode:** VCAN/2 termination in case that VCAN is nominal supply. when VCAN UV is detected, the termination is 2.5 V.
- **CAN Wake Capable Mode:** GND termination: after wake-up, the termination is 2.5 V.
- **CAN OFF Mode:** no termination necessary (bus floating).

When entering CAN Wake Capable Mode the termination is only connected to GND after the  $t_{\text{silence}}$  time has expired.

## 8.2.6 TXD Time-out Feature

If the TXDCAN signal is dominant for a time  $t > t_{\text{TXDCAN\_TO}}$ , in CAN Normal Mode, the TXDCAN time-out function deactivates the transmission of the signal at the bus setting the TXDCAN pin to recessive. This is implemented to prevent the bus from being blocked permanently due to an error. The transmitter is disabled and thus switched to recessive state. The CAN SPI control bits (**CAN** on **BUS\_CTRL**) remain unchanged and the failure is stored in the SPI flag **CAN\_FAIL**. The CAN transmitter stage is activated again after the dominant time-out condition is removed and the transceiver is automatically switched back to CAN Normal Mode.

## 8.2.7 Bus Dominant Clamping

If the CAN bus is dominant for a time  $t > t_{\text{BUS\_CAN\_TO}}$ , when CAN is configured as CAN Normal Mode or CAN Receive Only Mode, a bus dominant clamping is detected and the SPI bit **CAN\_FAIL** is set. The transceiver configuration stays unchanged. In order to avoid that a bus dominant clamping is detected due to a TXD time-out the bus dominant clamping filter time  $t_{\text{BUS\_CAN\_TO}} > t_{\text{TXDCAN\_TO}}$ .

### 8.2.8 Undervoltage Detection

The voltage at the CAN supply pin is monitored in CAN Normal Mode and CAN Receive Only Mode. In case of VCAN undervoltage a signalization via SPI bit **VCAN\_UV** is triggered and the TLE9563-3QX disables the transmitter stage. If the CAN supply reaches a higher level than the undervoltage detection threshold ( $V_{CAN} > V_{CAN\_UV}$ ), the transceiver is automatically switched back to CAN Normal Mode.

The undervoltage detection is enabled if the mode bit CAN\_1 = '1', i.e. in CAN Normal or CAN Receive Only Mode. .

## 8.3 Electrical Characteristics

**Table 22 Electrical Characteristics**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{SINT} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{CAN} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Bus Receiver							
Differential Receiver Threshold Voltage, recessive to dominant edge	$V_{\text{diff,rd\_N}}$	–	0.80	0.90	V	$V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ ; -12 V ≤ $V_{\text{CM}}$ (CAN) ≤ 12 V; CAN Normal Mode	P_8.3.1
Differential Receiver Threshold Voltage, dominant to recessive edge	$V_{\text{diff,dr\_N}}$	0.50	0.60	–	V	$V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ ; -12 V ≤ $V_{\text{CM}}$ (CAN) ≤ 12 V; CAN Normal Mode	P_8.3.2
Dominant state differential input voltage range	$V_{\text{diff\_D\_range}}$	0.9	–	8.0	V	$V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ ; -12 V ≤ $V_{\text{CM}}$ (CAN) ≤ +12 V; CAN Normal Mode	P_8.3.60
Common Mode Range	CMR	-12	–	12	V	4)	P_8.3.3
Recessive state differential input voltage range	$V_{\text{diff\_R\_range}}$	-3.0	–	0.5	V	$V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ ; -12 V ≤ $V_{\text{CM}}$ (CAN) ≤ +12 V; CAN Normal Mode	P_8.3.61
Maximum Differential Bus Voltage	$V_{\text{diff,max}}$	-5	–	10	V	4)	P_8.3.4
CANH, CANL Input Resistance	$R_{\text{i}}$	20	40	50	kΩ	CAN Normal / Wake Capable Mode; Recessive state -2V ≤ $V_{\text{CANH/L}}$ ≤ +7V	P_8.3.5
Differential Input Resistance	$R_{\text{diff}}$	40	80	100	kΩ	CAN Normal / Wake Capable Mode; Recessive state -2V ≤ $V_{\text{CANH/L}}$ ≤ +7V	P_8.3.6
Input Resistance Deviation between CANH and CANL	$DR_{\text{i}}$	-3	–	3	%	4)Recessive state $V_{\text{CANH}} = V_{\text{CANL}} = 5\text{V}$	P_8.3.7

**High Speed CAN Transceiver**

**Table 22 Electrical Characteristics (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{\text{SINT}} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{\text{CAN}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Capacitance CANH, CANL versus GND	$C_{\text{in}}$	–	20	40	pF	<sup>1)</sup> $V_{\text{TXDCAN}} = 5\text{ V}$	P_8.3.8
Differential Input Capacitance	$C_{\text{diff}}$	–	10	20	pF	<sup>1)</sup> $V_{\text{TXDCAN}} = 5\text{ V}$	P_8.3.9
Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{\text{diff,rd}_W}$	–	0.8	1.15	V	$-12\text{ V} \leq V_{\text{CM}}(\text{CAN}) \leq 12\text{ V}$ ; CAN Wake Capable Mode	P_8.3.10
Wake-up Receiver Dominant state differential input voltage range	$V_{\text{diff,D\_range}_W}$	1.15	–	8.0	V	$-12\text{ V} \leq V_{\text{CM}}(\text{CAN}) \leq +12\text{ V}$ ; CAN Wake Capable Mode	P_8.3.62
Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{\text{diff,dr}_W}$	0.4	0.7		V	$-12\text{ V} \leq V_{\text{CM}}(\text{CAN}) \leq 12\text{ V}$ ; CAN Wake Capable Mode	P_8.3.11
Wake-up Receiver Recessive state differential input voltage range	$V_{\text{diff,R\_range}_W}$	-3.0	–	0.4	V	$-12\text{ V} \leq V_{\text{CM}}(\text{CAN}) \leq +12\text{ V}$ ; CAN Wake Capable Mode	P_8.3.63

**CAN Bus Transmitter**

CANH/CANL Recessive Output Voltage (CAN Normal Mode)	$V_{\text{CANL/H\_NM}}$	2.0	–	3.0	V	CAN Normal Mode $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no load	P_8.3.12
CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode)	$V_{\text{CANL/H\_LP}}$	-0.1	–	0.1	V	CAN Wake Capable Mode; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no load	P_8.3.13
CANH, CANL Recessive Output Voltage Difference $V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ (CAN Normal Mode)	$V_{\text{diff}_r\text{N}}$	-500	–	50	mV	CAN Normal Mode; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no load	P_8.3.14
CANH, CANL Recessive Output Voltage Difference $V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$ (CAN Wake Capable Mode)	$V_{\text{diff}_r\text{W}}$	-200	–	200	mV	CAN Wake Capable Mode; $V_{\text{TXDCAN}} = V_{\text{CC1}}$ ; no load	P_8.3.15
CANL Dominant Output Voltage	$V_{\text{CANL}}$	0.5	–	2.25	V	<sup>4)</sup> CAN Normal Mode; $V_{\text{TXDCAN}} = 0\text{ V}$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $50\ \Omega \leq R_L \leq 65\ \Omega$	P_8.3.16

**High Speed CAN Transceiver**

**Table 22 Electrical Characteristics (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{\text{SINT}} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{\text{CAN}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH Dominant Output Voltage	$V_{\text{CANH}}$	2.75	–	4.5	V	<sup>4)</sup> CAN Normal Mode; $V_{\text{TXDCAN}} = 0\text{ V}$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $50\ \Omega \leq R_L \leq 65\ \Omega$	P_8.3.17
CANH, CANL Dominant Output Voltage Difference $V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$	$V_{\text{diff\_d\_N}}$	1.5	2.0	2.5	V	<sup>4)</sup> CAN Normal Mode; $V_{\text{TXDCAN}} = 0\text{ V}$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $50\ \Omega \leq R_L \leq 65\ \Omega$	P_8.3.18
CANH, CANL Dominant Output Voltage Difference (resistance during arbitration) $V_{\text{diff}} = V_{\text{CANH}} - V_{\text{CANL}}$	$V_{\text{diff\_d\_N}}$	1.5	–	5.0	V	<sup>4)</sup> CAN Normal Mode; $V_{\text{TXDCAN}} = 0\text{ V}$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $R_L = 2240\ \Omega$	P_8.3.19
CANH, CANL output voltage difference slope, recessive to dominant	$V_{\text{diff\_slope\_rd}}$	–	–	70	V/us	<sup>4)</sup> 30% to 70% of measured differential bus voltage, $C_L = 100\text{ pF}$ , $R_L = 60\ \Omega$	P_8.3.54
CANH, CANL output voltage difference slope, dominant to recessive	$V_{\text{diff\_slope\_dr}}$	–	–	70	V/us	<sup>4)</sup> 70% to 30% of measured differential bus voltage, $C_L = 100\text{ pF}$ , $R_L = 60\ \Omega$	P_8.3.55
Driver Symmetry $V_{\text{SYM}} = V_{\text{CANH}} + V_{\text{CANL}}$	$V_{\text{SYM}}$	4.5	–	5.5	V	<sup>2)</sup> CAN Normal Mode; $V_{\text{TXDCAN}} = 0\text{ V} / 5\text{ V}$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{SPLIT}} = 4.7\text{ nF}$ ; $50\ \Omega \leq R_L \leq 60\ \Omega$ ;	P_8.3.21
CANH Short Circuit Current	$I_{\text{CANHsc}}$	-115	-80	-50	mA	CAN Normal Mode; $V_{\text{CANHshort}} = -3\text{ V}$	P_8.3.22
CANL Short Circuit Current	$I_{\text{CANLsc}}$	50	80	115	mA	CAN Normal Mode; $V_{\text{CANLshort}} = 18\text{ V}$ ;	P_8.3.23
Leakage Current	$I_{\text{CANH,lk}}$ $I_{\text{CANL,lk}}$	–	5	7.5	$\mu\text{A}$	$V_S = V_{\text{CAN}} = 0\text{ V}$ ; $0\text{ V} \leq V_{\text{CANH,L}} \leq 5\text{ V}$ ; <sup>3)</sup> $R_{\text{test}} = 0 / 47\text{ k}\Omega$	P_8.3.24

**Receiver Output RXDCAN**

High level Output Voltage	$V_{\text{RXDCAN,H}}$	$0.8 \times V_{\text{CC1}}$	–	–	V	CAN Normal Mode; $I_{\text{RXDCAN}} = -2\text{ mA}$	P_8.3.26
Low Level Output Voltage	$V_{\text{RXDCAN,L}}$	–	–	$0.2 \times V_{\text{CC1}}$	V	CAN Normal Mode; $I_{\text{RXDCAN}} = 2\text{ mA}$	P_8.3.27

**High Speed CAN Transceiver**

**Table 22 Electrical Characteristics (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{\text{SINT}} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{\text{CAN}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmission Input TXDCAN							
High Level Input Voltage Threshold	$V_{\text{TXDCAN,H}}$	–	–	$0.7 \times V_{\text{cc1}}$	V	CAN Normal Mode; recessive state	P_8.3.28
Low Level Input Voltage Threshold	$V_{\text{TXDCAN,L}}$	$0.3 \times V_{\text{cc1}}$	–	–	V	CAN Normal Mode; dominant state	P_8.3.29
TXDCAN Input Hysteresis	$V_{\text{TXDCAN,hys}}$	–	$0.12 \times V_{\text{cc1}}$	–	V	<sup>4)</sup>	P_8.3.30
TXDCAN Pull-up Resistance	$R_{\text{TXDCAN}}$	20	50	80	kΩ	-	P_8.3.31
TXDCAN input capacitance	$C_{\text{TXDCAN}}$	–	6	10	pF	<sup>4)</sup>	P_8.3.64
CAN Transceiver Enabling Time	$t_{\text{CAN,EN}}$	8	12	18	μs	<sup>6)</sup> CSN = high to first valid transmitted TXDCAN dominant	P_8.3.32
Dynamic CAN-Transceiver Characteristics							
Min. Dominant Time for Bus Wake-up	$t_{\text{Wake1}}$	0.5	–	1.8	μs	-12 V ≤ $V_{\text{CM}}$ (CAN) ≤ 12 V; CAN Wake Capable Mode	P_8.3.33
Wake-up Time-out, Recessive Bus	$t_{\text{Wake2}}$	0.8	–	10	ms	<sup>6)</sup> CAN Wake Capable Mode	P_8.3.34
Loop delay (recessive to dominant)	$t_{\text{LOOP,f}}$	–	150	255	ns	<sup>2)</sup> CAN Normal Mode; $C_{\text{L}}$ = 100 pF; $R_{\text{L}}$ = 60 Ω; $V_{\text{CAN}}$ = 5 V; $C_{\text{RXDCAN}}$ = 15 pF	P_8.3.35
Loop delay (dominant to recessive)	$t_{\text{LOOP,r}}$	–	150	255	ns	<sup>2)</sup> CAN Normal Mode; $C_{\text{L}}$ = 100 pF; $R_{\text{L}}$ = 60 Ω; $V_{\text{CAN}}$ = 5 V; $C_{\text{RXDCAN}}$ = 15 pF	P_8.3.36
Propagation Delay TXDCAN low to bus dominant	$t_{\text{d(L),T}}$	–	50	140	ns	CAN Normal Mode; $C_{\text{L}}$ = 100 pF; $R_{\text{L}}$ = 60 Ω; $V_{\text{CAN}}$ = 5 V	P_8.3.37
Propagation Delay TXDCAN high to bus recessive	$t_{\text{d(H),T}}$	–	50	140	ns	CAN Normal Mode; $C_{\text{L}}$ = 100 pF; $R_{\text{L}}$ = 60 Ω; $V_{\text{CAN}}$ = 5 V	P_8.3.38

**High Speed CAN Transceiver**

**Table 22 Electrical Characteristics (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{\text{SINT}} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{\text{CAN}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation Delay bus dominant to RXDCAN low	$t_{d(L),R}$	–	100	–	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$	P_8.3.39
Propagation Delay bus recessive to RXDCAN high	$t_{d(H),R}$	–	100	–	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$	P_8.3.40
Received Recessive bit width	$t_{\text{bit(RXD)}}$	400	–	550	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 500\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.42
Transmitted Recessive bit width	$t_{\text{bit(BUS)}}$	435	–	530	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 500\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.43
Receiver timing symmetry <sup>5)</sup>	$\Delta t_{\text{Rec}}$	-65	–	40	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 500\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.44

**High Speed CAN Transceiver**

**Table 22 Electrical Characteristics (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{\text{SINT}} = 5.5\text{ V}$  to  $28\text{ V}$ ;  $V_{\text{CAN}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $R_L = 60\ \Omega$ ; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Received Recessive bit width	$t_{\text{bit(RXD)}}$	120	–	220	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 200\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.45
Transmitted Recessive bit width	$t_{\text{bit(BUS)}}$	155	–	210	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 200\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.46
Receiver timing symmetry $\Delta t_{\text{Rec}} = t_{\text{bit(RXD)}} - t_{\text{bit(BUS)}}$	$\Delta t_{\text{Rec}}$	-45	–	15	ns	CAN Normal Mode; $C_L = 100\text{ pF}$ ; $R_L = 60\ \Omega$ ; $V_{\text{CAN}} = 5\text{ V}$ ; $C_{\text{RXDCAN}} = 15\text{ pF}$ ; $t_{\text{bit(TXD)}} = 200\text{ ns}$ ; Parameter definition in according to <a href="#">Figure 35</a> .	P_8.3.47
TXDCAN Permanent Dominant Time-out	$t_{\text{TXDCAN\_TO}}$	1.6	2.0	2.4	ms	<sup>6)</sup> CAN Normal Mode	P_8.3.48
BUS Permanent Dominant Time-out	$t_{\text{BUS\_CAN\_TO}}$	2.0	2.5	3.0	ms	<sup>6)</sup> CAN Normal Mode	P_8.3.49
Timeout for bus inactivity	$t_{\text{SILENCE}}$	0.6	–	1.2	s	<sup>6)</sup>	P_8.3.50
Bus Bias reaction time	$t_{\text{Bias}}$	–	–	250	$\mu\text{s}$	<sup>6)</sup>	P_8.3.51

- 1) Not subject to production test, specified by design, S2P - Method;  $f = 10\text{ MHz}$
- 2)  $V_{\text{SYM}}$  shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD is simulated by a square signal (50% duty cycle) with a frequency of up to  $1\text{ MHz}$  ( $2\text{ MBit/s}$ ).
- 3)  $R_{\text{tests}}$  between ( $V_s/V_{\text{CAN}}$ ) and  $0\text{V}$  (GND).
- 4) Not subject to production test, specified by design.
- 5)  $\Delta t_{\text{Rec}} = t_{\text{bit(RXD)}} - t_{\text{bit(BUS)}}$ .
- 6) Not subject to production test, tolerance defined by internal oscillator tolerance.

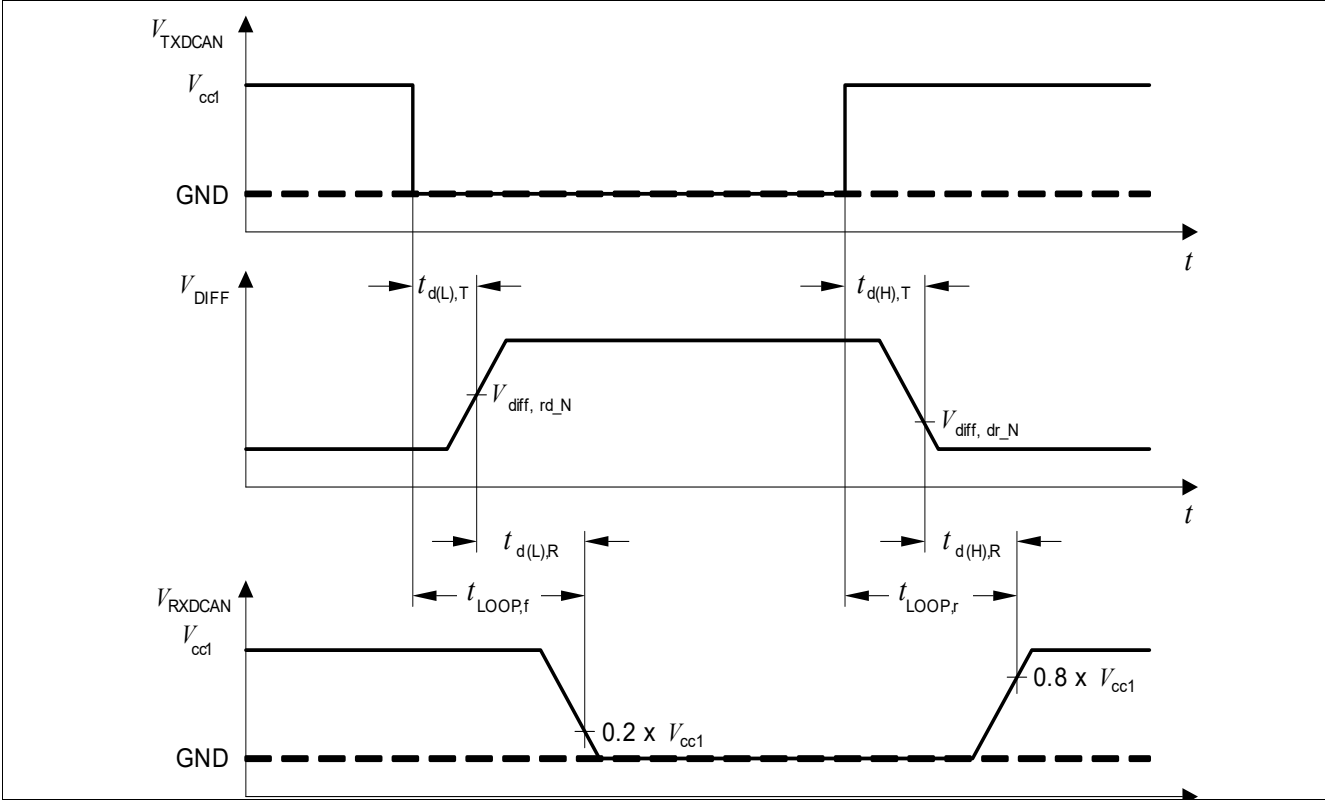


Figure 34 Timing Diagrams for Dynamic Characteristics

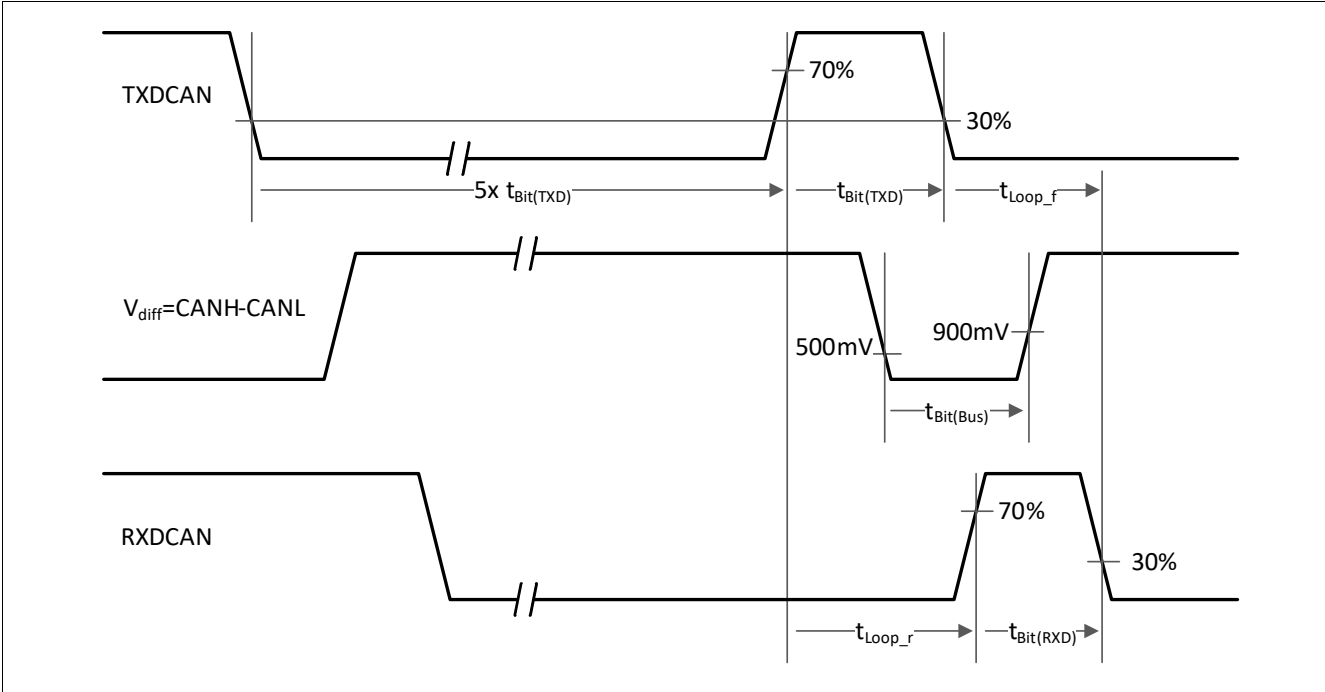
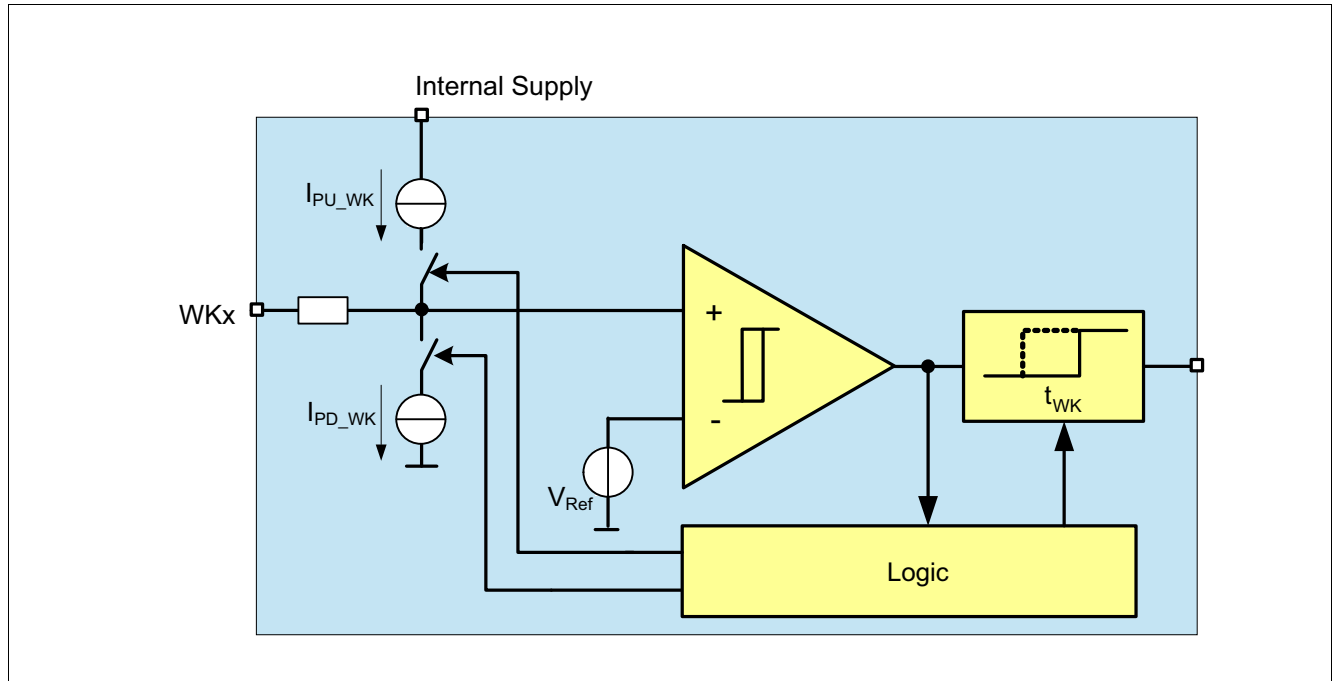


Figure 35 From ISO11898-2:2016: tloop, tbit(TXD), tbit(Bus), tbit(RXD) definitions



## 9 High-Voltage Wake Input

### 9.1 Block Description



**Figure 36** Wake Input Block Diagram

#### Features

- High-Voltage inputs with a 3 V (typ.) threshold voltage except WK5 ( $0.5 \times V_S$ ).
- Wake-up capability for power saving modes.
- Edge sensitive wake feature low to high and high to low.
- Pull-up and Pull-down current sources except for WK5 (pull-up fixed), configurable via SPI.
- Selectable configuration for static sense or cyclic sense.
- In Normal Mode and Stop Mode the level of the WKx pin can be read via SPI unless WK4 is configured as SYNC.
- Synchronization with HSx via WK4 (for cyclic sense).

## 9.2 High-Voltage Wake Function

### 9.2.1 Functional Description

The wake inputs pin are edge-sensitive inputs with a switching threshold of typically 3 V except WK5. Both transitions, high to low and low to high, result in a signalization by the device. The signalization occurs either in triggering the interrupt in Normal Mode and Stop Mode or by a wake up of the device in Sleep Mode and Fail-Safe Mode.

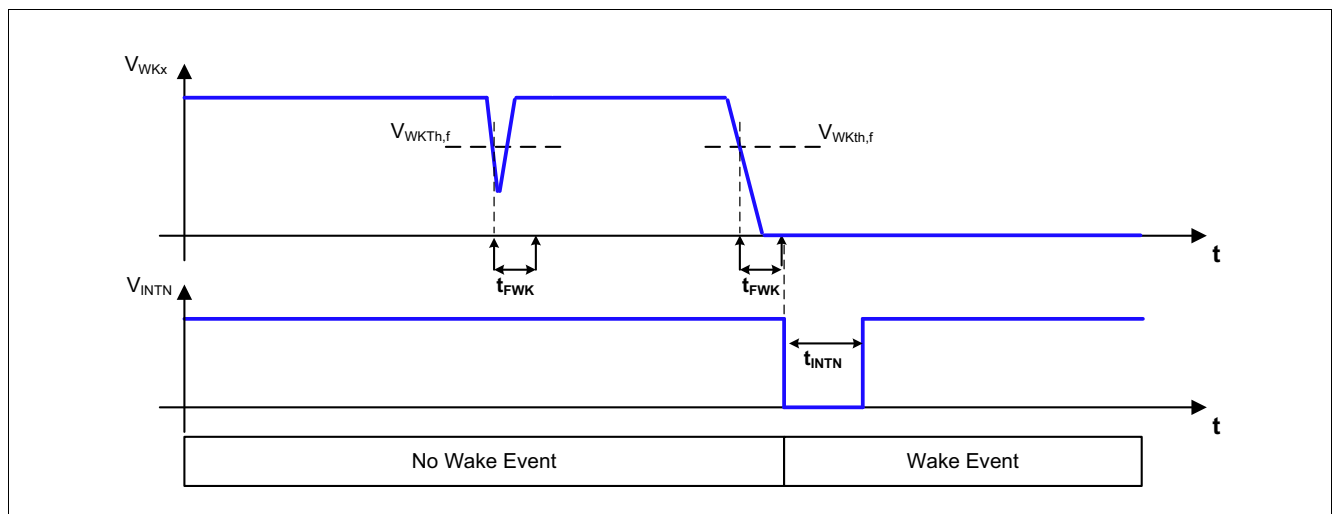
Two different wake detection modes can be selected via SPI:

- Static sense: WK inputs are always active.
- Cyclic sense: WK inputs are only active for a certain time period (see [Chapter 5.7.1](#)).

A filter time  $t_{FWKx}$  is implemented to avoid an unintentional wake-up due to transients or EMC disturbances in static sense configuration.

The filter time ( $t_{FWKx}$ ) is triggered by a level change crossing the switching threshold and a wake signal is recognized if the input level will not cross again the threshold during the selected filter time.

**Figure 37** shows a typical wake-up timing and filtering of transient pulses.



**Figure 37** Wake-up Filter Timing for Static Sense

The wake-up capability for the WKx pin can be enabled or disabled via SPI command.

A wake event via the WKx pin can always be read in the register **WK\_STAT** at the bit **WK5\_WU**.

The actual voltage level of the WKx pin (low or high) can always be read in Normal Mode, Stop Mode and Init Mode in the register **WK\_LVL\_STAT**. During Cyclic Sense, the register shows the sampled levels of the respective WKx pin.

### 9.2.2 Wake Input Configuration

To ensure a defined and stable voltage levels at the internal comparator input it is possible to configure integrated current sources via the SPI register **WK\_CTRL**.

## High-Voltage Wake Input

**Table 23 Pull-Up / Pull-Down Resistor (not valid for WK5)**

WKx_PUPD_ 1	WKx_PUPD_ 0	Current Sources	Note
0	0	no current source	WK input is floating if left open (default setting)
0	1	pull-down	WK input internally pulled to GND
1	0	pull-up	WK input internally pulled to internal 5V supply
1	1	Automatic switching	If a high level is detected at the WK input the pull-up source is activated, if low level is detected the pull down is activated.

*Note: If a WK input is not used, the respective WK input must be tied to GND on board to avoid unintended floating state of the pin.*

One additional configuration is related the filter time of each Wake-up module. The bits **WK\_FILT** permit to set the filter time in static sensing or in cyclic sensing.

*Note: When the device mode is changed to normal (from INIT), in case of static sense, if the WK pin is set, the WK\_STAT register is set in this time (also the interrupt pin).*

### 9.2.3 Wake configuration for Cyclic Sense

The wake-up inputs can also be used for cyclical sensing signals during low-power modes. For this function the WKx input performs a cyclic sensing of the voltage level during the on-time of specific HSx.

A transition of the voltage level will trigger a wake-up event.

See also [Chapter 5.7.1](#) for more details.

### 9.2.4 Wake configuration for Synchronization

The WK4 pin can be configured as SYNC input for driving the HSx.

Prerequisite to configure the WK4 as SYNC input is that the WK4 has to be OFF.

The configuration of the WK4/SYNC bit is done using the **WK\_EN** bits. if the **WK\_EN**=10<sub>B</sub> (SYNC selected), all bits in WK4 bank are ignored and wake-up capability on WK4 is not available.

*Note: If WKx is the only wake source available and is configured with cyclic sense with SYNC (WKx\_FILT = 100), trying to go to Sleep Mode is not possible (restart mode is entered) - because SYNC is driven by the microcontroller which is not supplied in Sleep Mode.*

## High-Voltage Wake Input

### 9.3 Electrical Characteristics

**Table 24 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
WK4 Input Pin Characteristics							
Wake-up/monitoring threshold voltage falling	$V_{WKx\_th,f}$	2.5	3	3.5	V	without external serial resistor $R_S$	P_10.3.1
Wake-up/monitoring threshold voltage rising	$V_{WKx\_th,r}$	3	3.5	4	V	without external serial resistor $R_S$	P_10.3.2
Threshold hysteresis	$V_{WKx\_th,hys}$	0.4	0.6	0.85	V	without external serial resistor $R_S$	P_10.3.3
WK pin Pull-up Current	$I_{PU\_WKx}$	-20	-10	-3	$\mu A$	$V_{WKx} = 4\text{ V}$	P_10.3.4
WK pin Pull-down Current	$I_{PD\_WKx}$	3	10	20	$\mu A$	$V_{WKx} = 2.5\text{ V}$	P_10.3.5
Input leakage current	$I_{LK,lx}$	-2		2	$\mu A$	0 V < $V_{WKx}$ < 40 V; Pull-up / Pull-down disabled	P_10.3.6

#### WK5 Input Pin Characteristics

Wake-up/monitoring threshold voltage falling	$V_{WK5\_th,f}$	$0.4 \times V_S$	$0.45 \times V_S$	-	V		P_10.3.7
Wake-up/monitoring threshold voltage rising	$V_{WK5\_th,r}$	-	$0.55 \times V_S$	$0.6 \times V_S$	V		P_10.3.8
Threshold hysteresis	$V_{WK5\_th,hys}$	$0.07 \times V_S$	$0.1 \times V_S$	$0.175 \times V_S$	V		P_10.3.9
Pull-up resistance on WK5	$R_{WK5,pull-up}$	20	30	47	k $\Omega$		P_10.3.10

#### WK4 as SYNC input pin

LOW input voltage threshold	$WK4_{SYNC\_th,L}$	$0.3 \times V_{CC1}$	-	-	V		P_10.3.11
HIGH input voltage threshold	$WK4_{SYNC\_th,H}$	-	-	$0.7 \times V_{CC1}$	V		P_10.3.12
Pull-down resistance on WK/SYNC	$R_{SYNC}$	20	40	80	k $\Omega$	$V_{SYNC} = 1 \text{ V}$	P_10.3.13

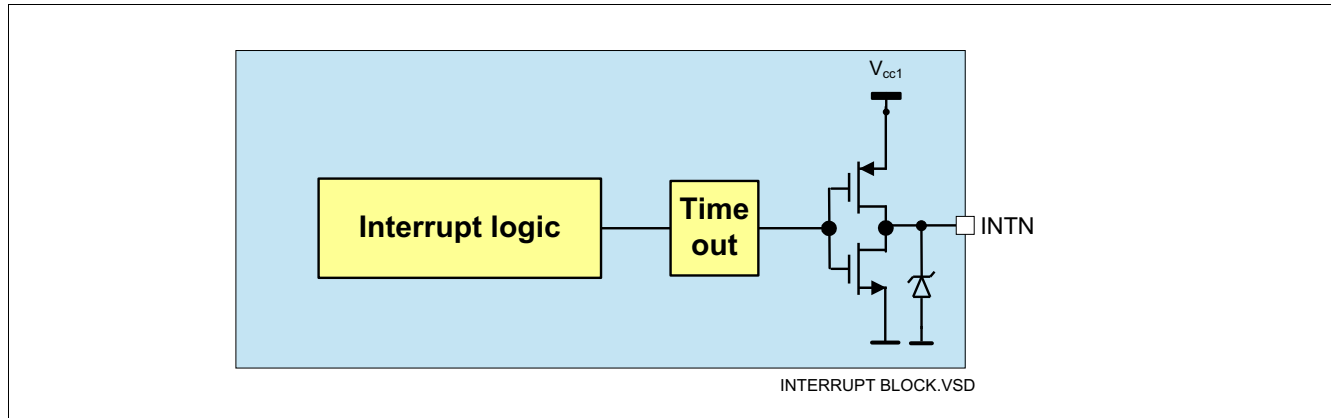
#### Timing

Wake-up filter time 1	$t_{FWK1}$	12	16	22	$\mu\text{s}$	<sup>1)</sup>	P_10.3.16
Wake-up filter time 2	$t_{FWK2}$	50	64	80	$\mu\text{s}$	<sup>1)</sup>	P_10.3.17

1) Not subject to production test, tolerance defined by internal oscillator tolerance.

## 10 Interrupt Function

### 10.1 Block and Functional Description



**Figure 38 Interrupt Block Diagram**

The interrupt is used to signalize special events in real time to the microcontroller. The interrupt block is designed as a push/pull output stage as shown in [Figure 38](#). An interrupt is triggered and the INTN pin is pulled low (active low) for  $t_{INTN}$  in Normal Mode and Stop Mode and it is released again once  $t_{INTN}$  is expired. The minimum high-time of INTN between two consecutive interrupts is  $t_{INTND}$ . An interrupt does not cause a device mode change.

Two different interrupt generation methods are implemented:

- **Interrupt Mask:** One dedicated register (INT\_MASK) is intended to enable or disable set of interrupt sources. The interrupt sources follow the SPI Status Information Field.  
 In details:
  - SUPPLY\_STAT: “OR” of all bits on SUP\_STAT register except POR, VCC1\_UV, VCC1\_SC, VCC1\_OV
  - TEMP\_STAT: “OR” of all bits on THERM\_STAT register except TSD2
  - BUS\_STAT: “OR” of all bits on BUS\_STAT register
  - HS\_STAT: “OR” of all bits on HS\_OL\_OC\_OT\_STAT register
  - BD\_STAT: “OR” of all bits on DSOV register
  - SPI\_CRC\_FAIL: or between SPI\_FAIL and CRC\_FAIL bits on DEV\_STAT register.
- **Wake-up events:** all wake-up events stored in the wake status SPI register WK\_STAT only in case the corresponding input was configured as wake-up source.  
 The wake-up sources are:
  - via CAN (wake-up pattern or wake-up frame)
  - via WK pin
  - via TIMERx (cyclic wake)
  - via LSx\_DSOV\_BRK if any of the brake-feature is enabled

The methods are both available at the same time.

**Note:** *The errors which will cause Restart or Fail-Safe Mode (VCC1\_UV, VCC1\_SC, VCC1\_OV, TSD2) are the exceptions of an INTN generation. Also the bit POR will not generate interrupts. If the above mentioned bits are not cleared after the device is back in Normal Mode or Stop Mode, the INTN is periodically generated (Register based cyclic interrupt generation).*

## Interrupt Function

*Note: Periodical interrupts are only generated by CRC fail and SPI fail from DEV\_STAT register.*

*Note: During Restart Mode the SPI is blocked and the microcontroller is in reset. Therefore the INTN will not be in Restart Mode, which is the same behavior in Fail-Safe Mode or Sleep Mode.*

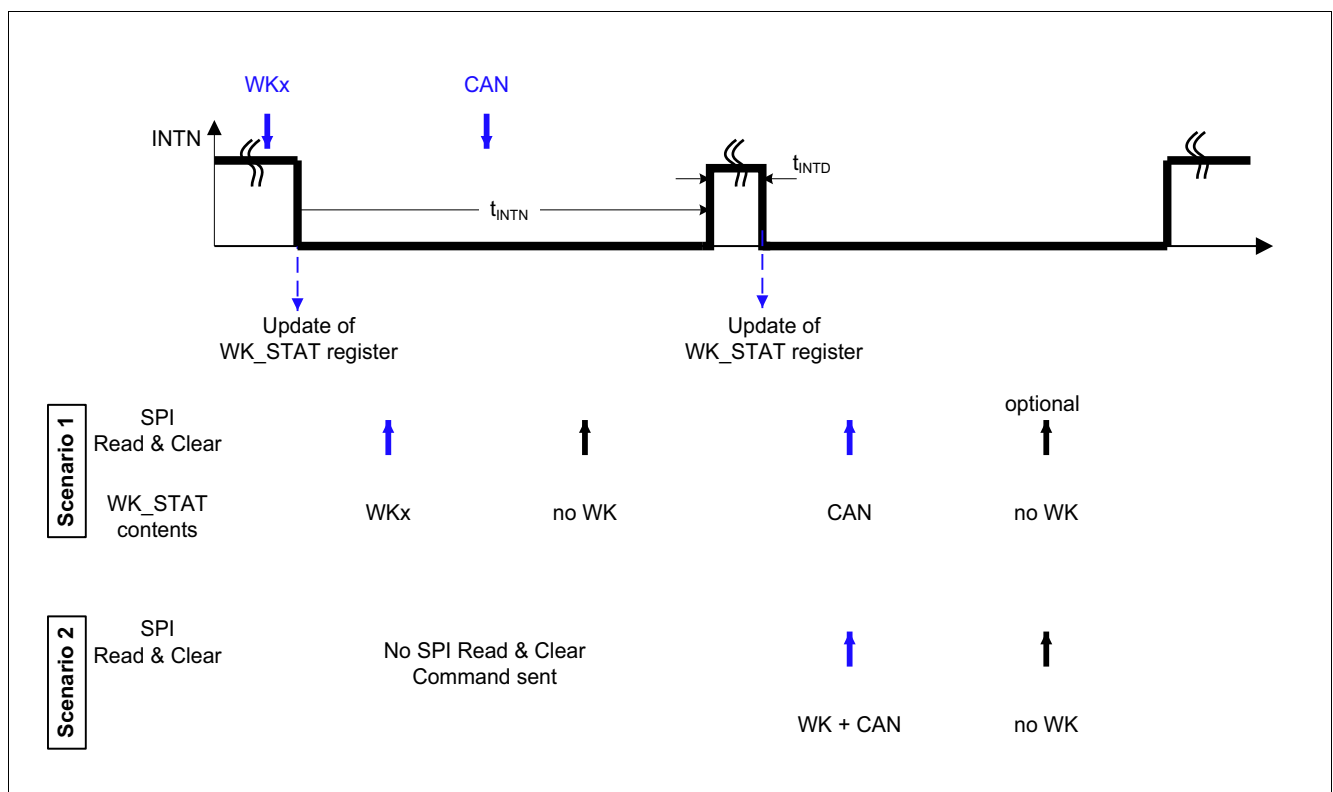
In addition to this behavior, INTN will be triggered when Stop Mode is entered and not all wake source bits were cleared in the WK\_STAT register and also the LSx\_DSOV\_BRK bits in the DSOV register..

The SPI status registers are updated at every falling edge of the INTN pulse. All interrupt events are stored in the respective register until the register is cleared via SPI command. A second SPI read after reading out the respective status register is optional but recommended to verify that the interrupt event is not present anymore. The interrupt behavior is shown in **Figure 39**.

The INTN pin is also used during Init Mode to select the Software Development Mode entry. See **Chapter 5.2** for further information.

In case of pending INTN event (SPI Status registers are not cleared after INTN event), additional periodical INTN events are generated as shown in **Figure 40**.

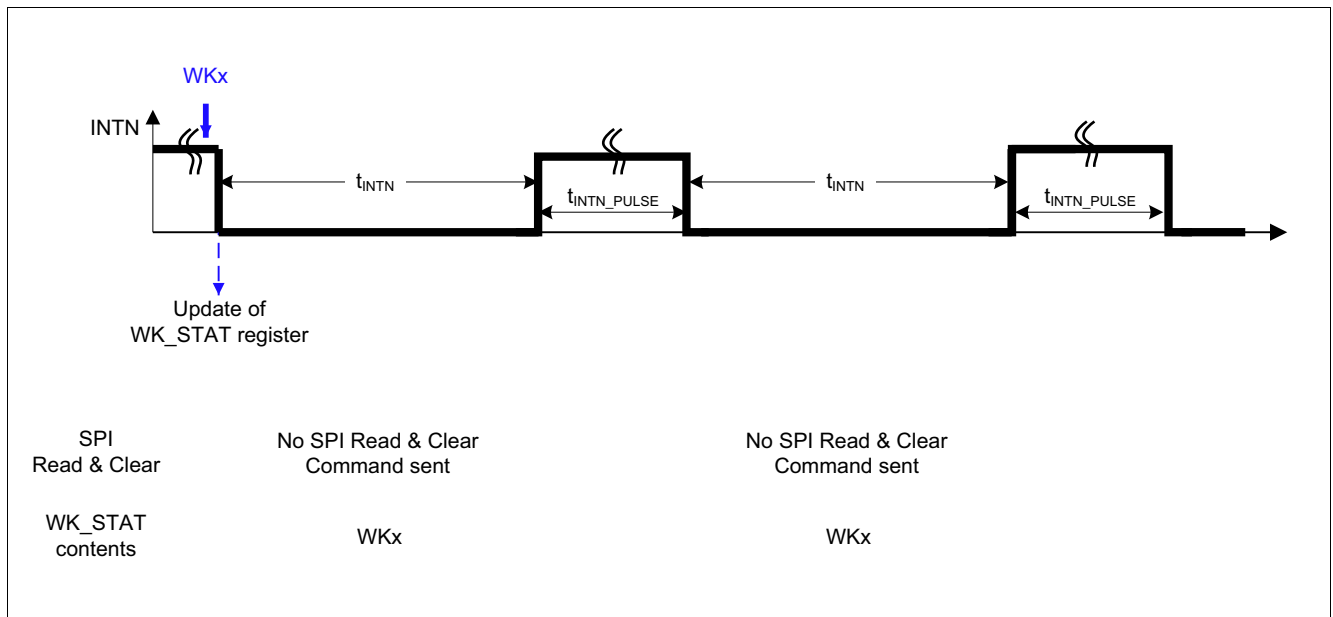
The periodical INTN events generation can be disabled via SPI command using **INTN\_CYC\_EN** bit.



**Figure 39 Interrupt Signalization Behavior**

*Note: For two or more interrupt events at the same time, when INTN pin is low the same time, it will not start multiple toggling.*

## Interrupt Function



**Figure 40** Interrupt Signalization Behavior in case of pending INTN events

## Interrupt Function

### 10.2 Electrical Characteristics

**Table 25 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Interrupt Output; Pin INTN							
INTN High Output Voltage	$V_{INTN,H}$	$0.8 \times V_{CC1}$	–	–	V	<sup>1)</sup> $I_{INTN}$ = -2 mA; INTN = off	P_11.2.1
INTN Low Output Voltage	$V_{INTN,L}$	–	–	$0.2 \times V_{CC1}$	V	<sup>1)</sup> $I_{INTN}$ = 2mA; INTN = on	P_11.2.2
INTN Pulse Width	$t_{INTN}$	80	100	120	μs	<sup>2)</sup>	P_11.2.3
INTN Pulse Minimum Delay Time	$t_{INTND}$	80	100	120	μs	<sup>2)</sup> between consecutive pulses	P_11.2.4
Pulse in case of pending INTN	$t_{INTN\_PULSE}$	4	5	6	ms	<sup>2)</sup> between consecutive pulses	P_11.2.5
SDM Select; Pin INTN							
Config Pull-up Resistance	$R_{SDM}$	30	60	100	kΩ	$V_{INTN}$ = 5 V	P_11.2.6
Config Select Filter Time	$t_{SDM\_F}$	50	64	80	μs	<sup>2)</sup>	P_11.2.7

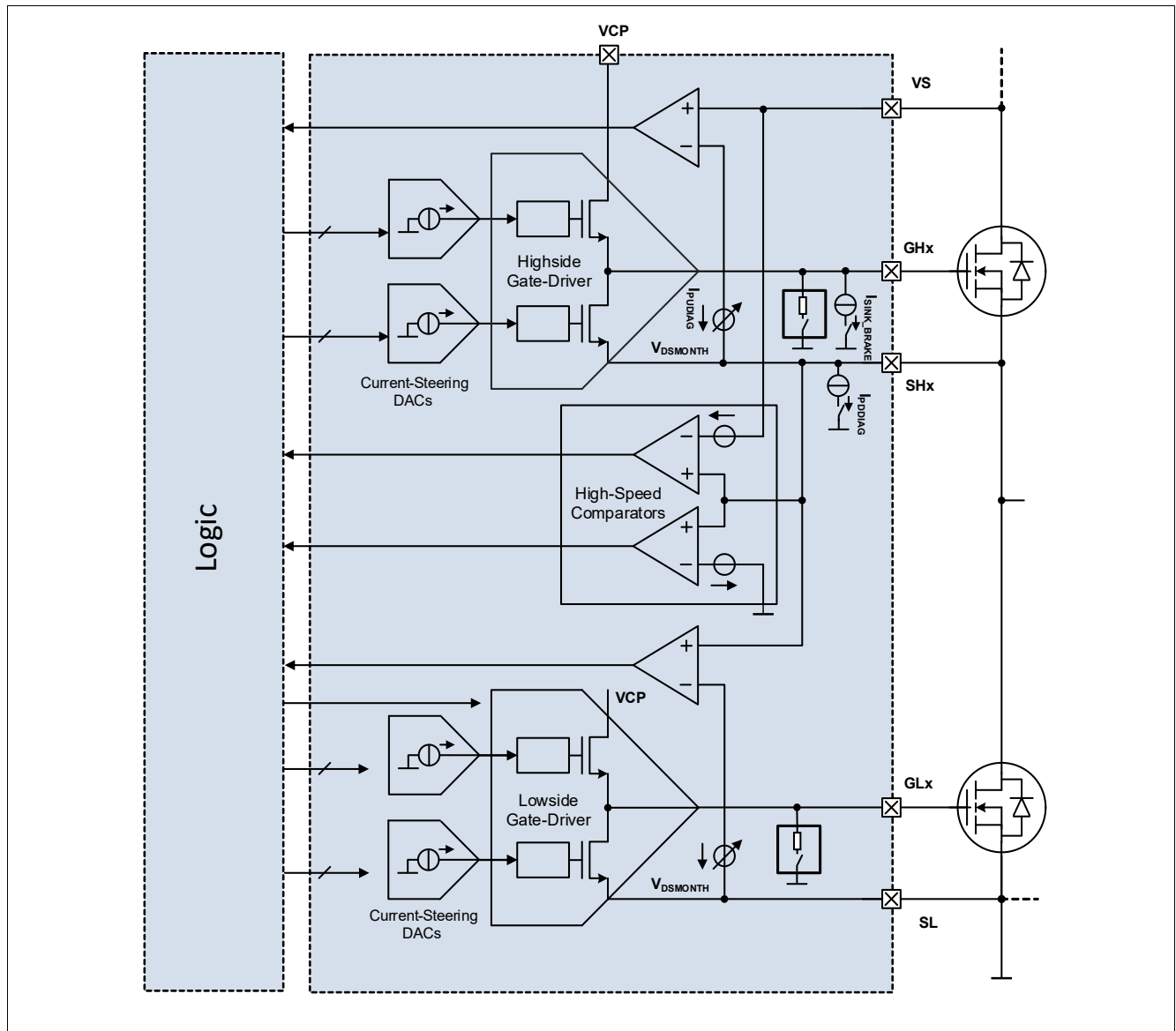
1) Output Voltage Value also determines device configuration during Init Mode.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.



## 11 Gate Drivers

The TLE9563-3QX integrates six floating gate drivers capable of controlling a wide range of N-channel MOSFETs. They are configured as three high-sides and three low-sides, building three half-bridges.



**Figure 41** Half-bridge gate driver - Block diagram

This section describes the MOSFET control in static activation and during PWM operation.

*Note:* PWMx mentioned in this chapter refer to the PWMx pins and signal used by the bridge driver to control the external MOSFETs.

*Note:* In this chapter PWMx **do not refer** to the internal PWM generators used to control the internal high-side switches HSx.

### 11.1 MOSFET control

Depending on the configuration bits HBxMODE[1:0] (refer to **HBMODE**), **CPEN**, each high-side and low-side MOSFETs can be:

## Gate Drivers

- Kept off with the passive discharge.
- Kept off actively.
- Activated (statically, no PWM, HBx\_PWM\_EN = 0).
- Activated in PWM mode (HBx\_PWM\_EN = 1).

Refer to **Table 26** for details.

**Table 26 Half-bridge mode selection**

CPEN	HBxMODE[1:0] <sup>1)</sup>	Configuration of HSx/LSx <sup>1)</sup>
CPEN = 0	Don't care	All MOSFETs are kept off by the passive discharge
CPEN = 1	00 <sub>B</sub>	HBx MOSFETs are kept off by the passive discharge
CPEN = 1	01 <sub>B</sub>	LSx MOSFET is ON, HSx MOSFET is actively kept OFF
CPEN = 1	10 <sub>B</sub>	HSx MOSFET is ON, LSx MOSFET is actively kept OFF
CPEN = 1	11 <sub>B</sub>	LSx and HSx MOSFETs are actively kept OFF with IHOLD

1) x = 1 ... 3

### 11.2 Static activation

In this section, we consider the static activation of the high-side and low-side MOSFET of the half-bridge x: HBx\_PWM\_EN = 0 (in **ST\_ICHG**) and CPEN = 1.

The low-side or high-side MOSFET of HBx is statically activated (no PWM) by setting HBxMODE[1:0] to respectively (0,1) or (1,0).

The configured active cross-current protection and the Drain-Source overvoltage blank times for the Half-Bridge x are noted  $t_{HBxCCP\ ACTIVE}$  and  $t_{HBxBLANK\ ACTIVE}$ .

The charge and discharge currents applied to the static controlled Half-Bridge x are noted ICHGSTx (**ST\_ICHG**).

IHARDOFF is the maximum current that the gate drivers can sink (150 mA typ.). This current is used to keep a MOSFET off, when the opposite MOSFET of the same half-bridge is being turned on. This feature reduces the risk of parasitic cross-current conduction.

ICHGSTx is the current sourced, respectively sunk, by the gate driver to turn-on the high-side x or low-side x. ICHGSTx is configured in the control register **ST\_ICHG**.

**Table 27 Static charge currents**

ICHGSTx[3:0]	Nom. charge current [mA]	Nom. discharge current [mA]	Max. deviation to typ. values
0000 <sub>B</sub>	0.5 ( $I_{CHG0}$ )	0.5 ( $I_{DCHG0}$ )	+/- 60%
0001 <sub>B</sub>	1.8 ( $I_{CHG4}$ )	1.8 ( $I_{DCHG4}$ )	+/- 60 %
0010 <sub>B</sub>	4.7 ( $I_{CHG8}$ )	4.7 ( $I_{DCHG8}$ )	+/- 60 %
0011 <sub>B</sub>	9.4 ( $I_{CHG12}$ )	9.4 ( $I_{DCHG12}$ )	+/- 60 %
0100 <sub>B</sub>	15.3 ( $I_{CHG16}$ )	15.1 ( $I_{DCHG16}$ )	+/- 40 %
0101 <sub>B</sub>	23 ( $I_{CHG20}$ )	22.5 ( $I_{DCHG20}$ )	+/- 40 %

## Gate Drivers

**Table 27 Static charge currents (cont'd)**

ICHGSTx[3:0]	Nom. charge current [mA]	Nom. discharge current [mA]	Max. deviation to typ. values
0110 <sub>B</sub>	31.6 ( $I_{CHG24}$ )	30.9 ( $I_{DCHG24}$ )	+/- 40 %
0111 <sub>B</sub>	41.6 ( $I_{CHG28}$ )	40.8 ( $I_{DCHG28}$ )	+/- 40%
1000 <sub>B</sub>	52.5 ( $I_{CHG32}$ )	51.5 ( $I_{DCHG32}$ )	+/- 30 %
1001 <sub>B</sub>	63.6 ( $I_{CHG36}$ )	62.4 ( $I_{DCHG36}$ )	+/- 30 %
1010 <sub>B</sub>	75.2 ( $I_{CHG40}$ )	73.7 ( $I_{DCHG40}$ )	+/- 30 %
1011 <sub>B</sub>	87.1 ( $I_{CHG44}$ )	85.5 ( $I_{DCHG44}$ )	+/- 30 %
1100 <sub>B</sub>	99.5 ( $I_{CHG48}$ )	97.7 ( $I_{DCHG48}$ )	+/- 30 %
1101 <sub>B</sub>	112.2 ( $I_{CHG52}$ )	110.8 ( $I_{DCHG52}$ )	+/- 30 %
1110 <sub>B</sub>	125.3 ( $I_{CHG56}$ )	124.5 ( $I_{DCHG56}$ )	+/- 30 %
1111 <sub>B</sub>	139 ( $I_{CHG60}$ )	138.7 ( $I_{DCHG60}$ )	+/- 30 %

IHOLD is the hold current used to keep the gate of the external MOSFETs in the desired state. This parameter is configurable with the IHOLD control bit in **GENCTRL**.

If the control bit IHOLD = 0:

- A MOSFET is kept ON with the current  $I_{CHG15}$ .
- A MOSFET is kept OFF with the current  $I_{DCHG15}$ .

If the control bit IHOLD = 1:

- A MOSFET is kept ON with the current  $I_{CHG20}$ .
- A MOSFET is kept OFF with the current  $I_{DCHG20}$ .

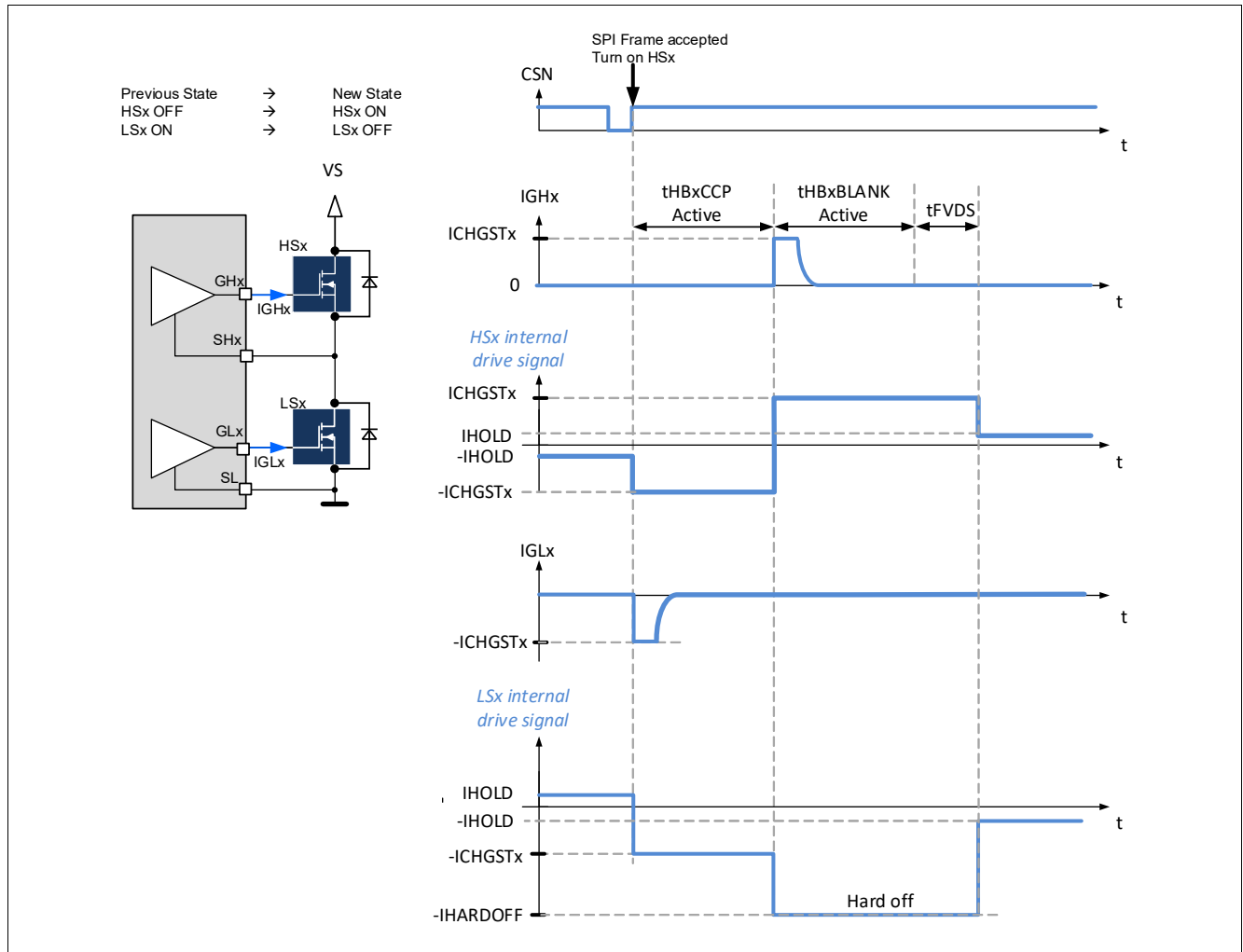
### 11.2.1 Static activation of a high-side MOSFET

#### Turn-on with cross-current protection

If LSx is ON (HBxMODE[1:0] = 01<sub>B</sub>), before the activation of HSx (HBxMODE[1:0] = 10<sub>B</sub>) then the high-side MOSFET is turned on after a cross-current protection time (refer to **Figure 42**):

- After the CSN rising edge and for the duration  $t_{HBXCCP\ ACTIVE}$  :
  - The high-side MOSFET is kept OFF with the current -ICHGSTx.
  - The gate of the low-side MOSFET is discharged with the current -ICHGSTx.
- At the end of  $t_{HBXCCP\ ACTIVE}$  and for the duration  $t_{HBXBLANK\ ACTIVE} + t_{FVDS}$ :
  - The gate of the high-side MOSFET is charged with the current ICHGSTx.
  - Low-side MOSFET is kept OFF with the current -IHARDOFF (hard off phase).
- At the end of  $t_{FVDS}$ :
  - The drive current of the high-side MOSFET is reduced to IHOLD.
  - The drive current of the low-side MOSFET is set to -IHOLD.

**Gate Drivers**



**Figure 42 Turn-on of a high-side MOSFET with cross-current protection**

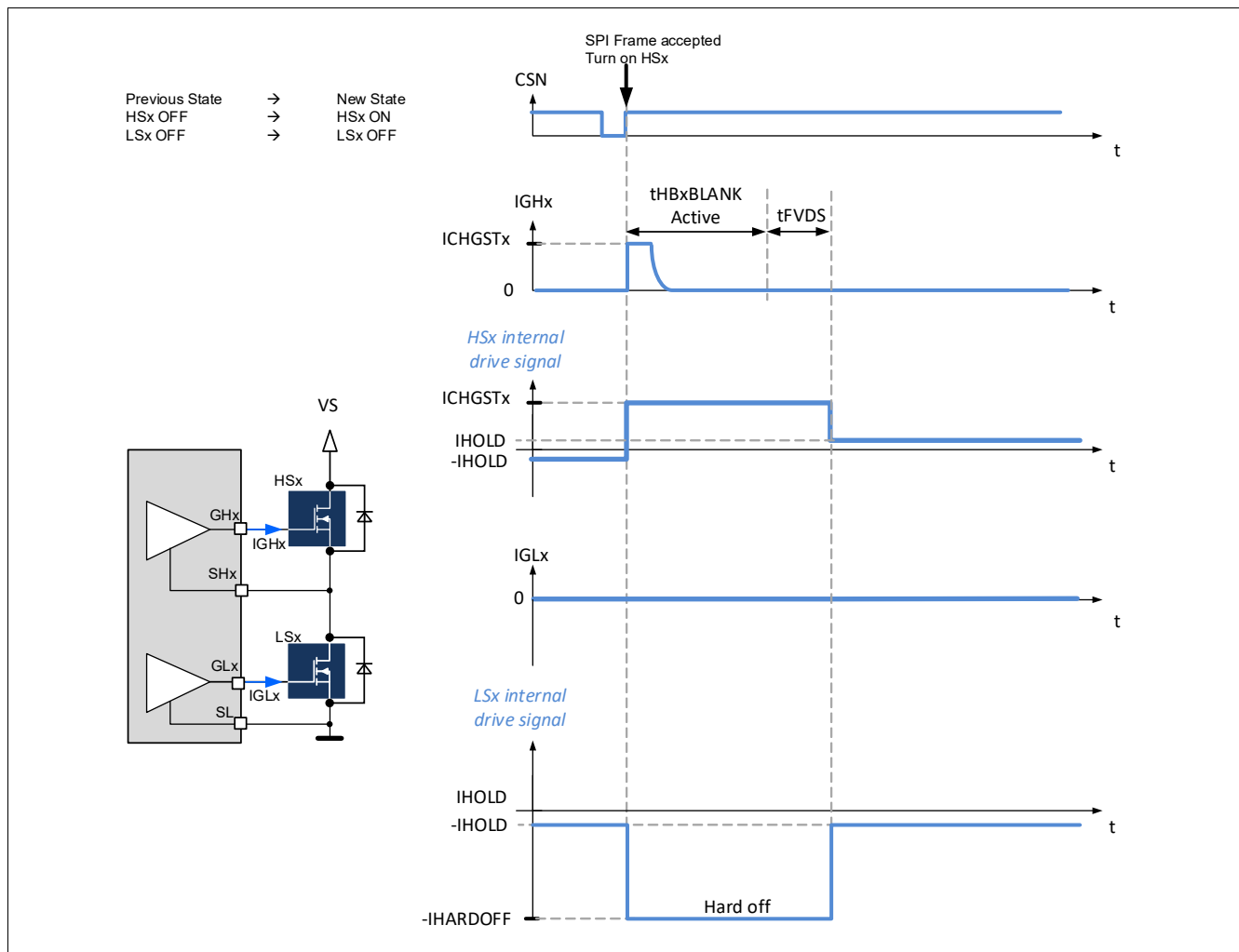
**Note:** The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3  $\mu$ s after the CSN rising edge.

## Gate Drivers

### Turn-on without cross-current protection

If LSx is OFF ( $HBxMODE[1:0] = 11_B$ ), before the activation of HSx ( $HBxMODE[1:0] = 10_B$ ), then the high-side MOSFET is turned on without cross-current protection (refer to [Figure 43](#)):

- right after the CSN rising edge and for a duration  $t_{HBxBLANK\ ACTIVE} + t_{FVDS}$ :
  - The gate of the high-side MOSFET is charged with the current  $ICHGSTx$ .
  - The low-side MOSFET is kept OFF with the current  $-IHARDOFF$ .
- At the end of  $t_{FVDS}$ :
  - The drive current of the high-side MOSFET is reduced to  $IHOLD$ .
  - The drive current of the low-side MOSFET is set to  $-IHOLD$ .



**Figure 43** Turn-on of a high-side MOSFET without cross-current protection

**Note:** The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to  $3\ \mu s$  after the CSN rising edge.

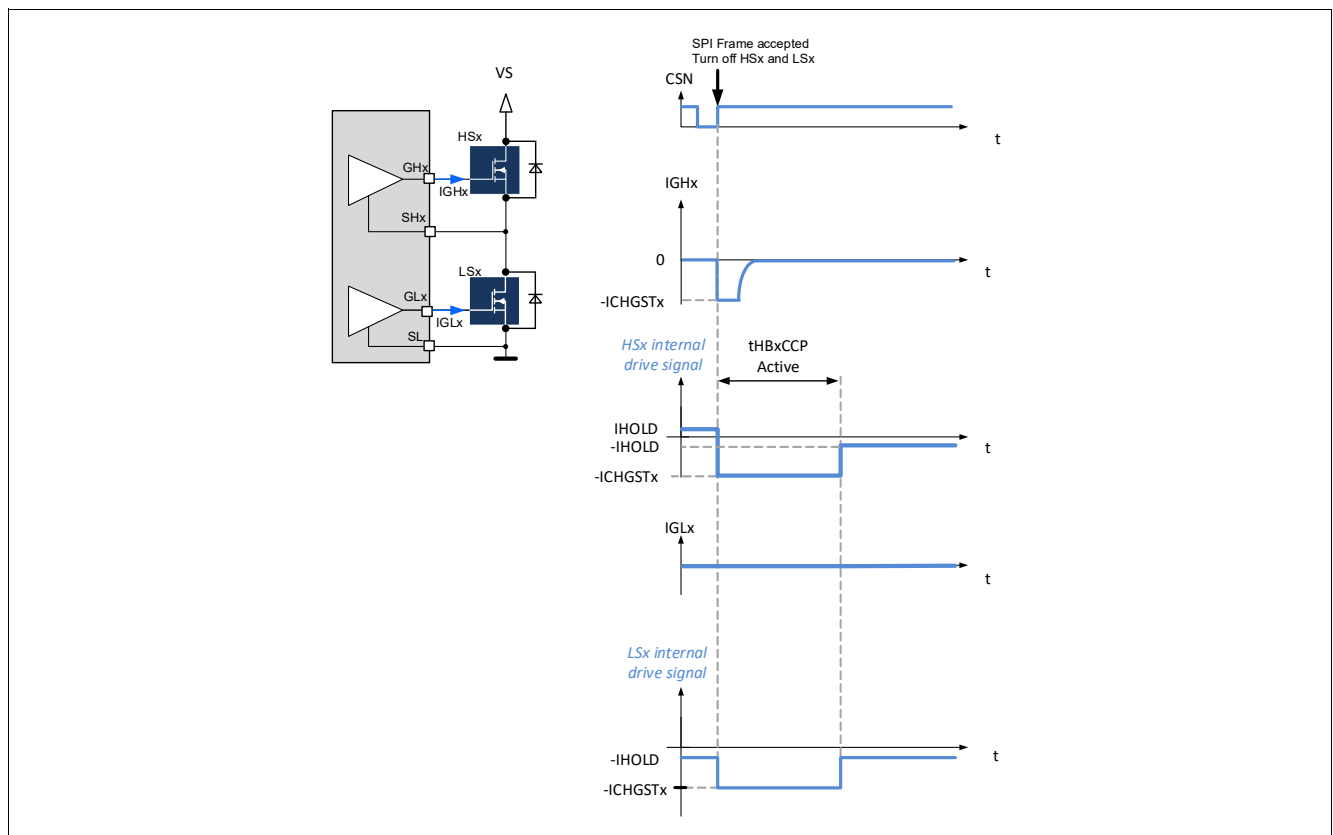
### 11.2.2 Static activation of a low-side MOSFET

The description of the static activation of a low-side x differs from the description of [Chapter 11.2.1](#) only by exchanging high-side x and low-side x.

### 11.2.3 Turn-off of the high-side and low-side MOSFETs of a half-bridge

When the TLE9563-3QX receives a SPI command to turn-off both the high-side and low-side MOSFETs of the half-bridge x ( $\text{HBxMODE}[1:0] = (0,0)$  or  $(1,1)$ ):

- The gate of HSx and LSx are discharged with the current  $-\text{ICHGSTx}$  for the duration  $t_{\text{HBxCCP ACTIVE}}$  ([Figure 44](#)).
- At the end of  $t_{\text{HBxCCP ACTIVE}}$ , the drive current of HSx and LSx are reduced to  $-\text{IHOLD}$ .



**Figure 44** Turn-off of the high-side and low-side MOSFETs of a half-bridge

*Note:* The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to  $3 \mu\text{s}$  after the CSN rising edge.

### 11.3 PWM operation

The half-bridge can be controlled in PWM using either three or six PWM inputs.

The TLE9563-3QX offers the possibility to detect the active and the freewheeling (FW) MOSFET in each half-bridge.

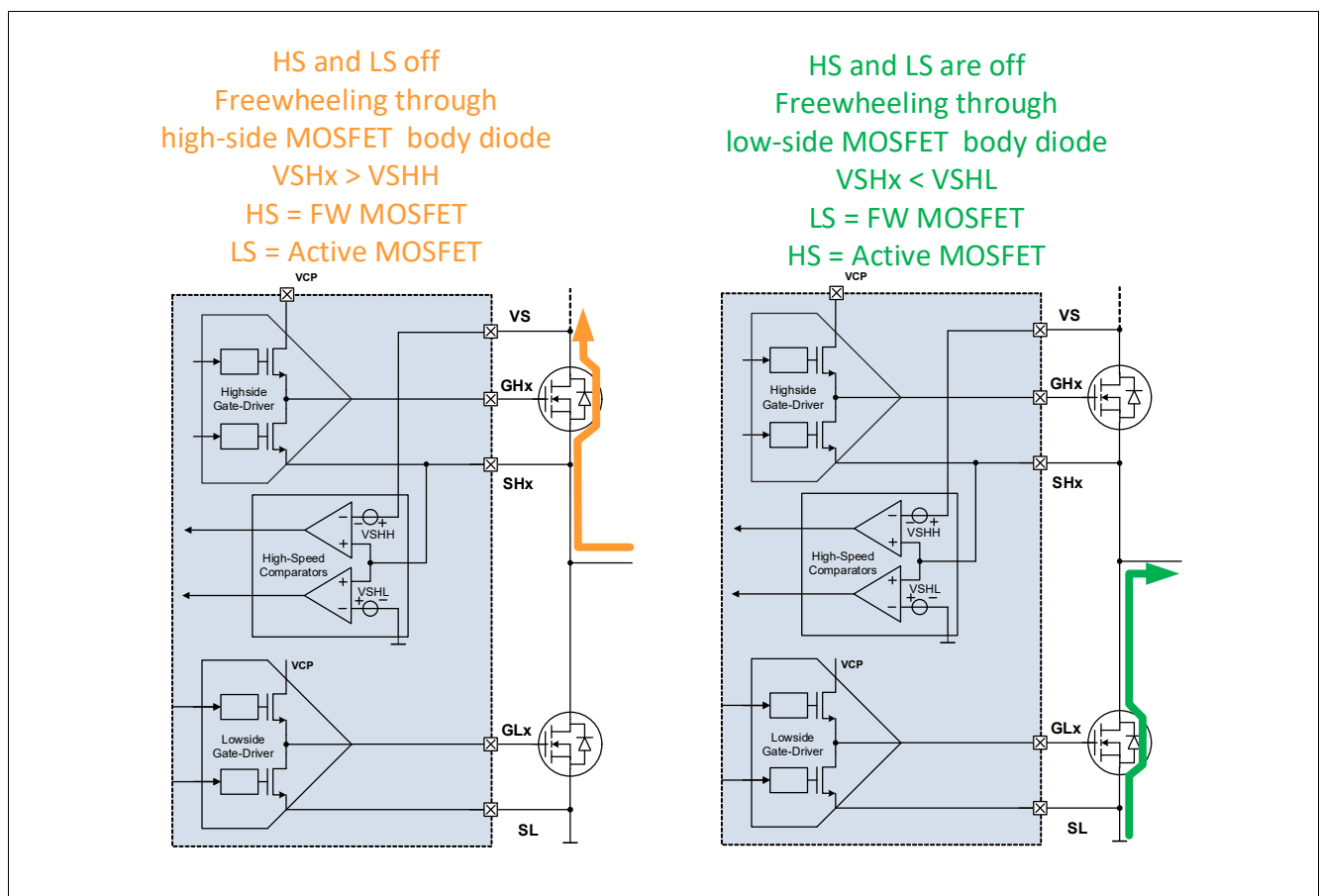
#### 11.3.1 Determination of the active and freewheeling MOSFET

If  $EN\_GEN\_CHECK = 1$ , right before each MOSFET activation, the device detects which MOSFET of the half-bridge is the active MOSFET and which MOSFET is the free-wheeling (FW) MOSFET:

- If  $VSHx > VS - VSHH$ : The high-side MOSFET is the FW MOSFET and the low-side MOSFET is the active MOSFET.
- If  $VSHx < VSHL$ : Then the low-side MOSFET is the FW MOSFET and the high-side MOSFET is the active MOSFET.
- If  $VSHL < VSHx < VS - VSHH$ : No clear distinction between the active FW MOSFET and the active MOSFET. The next MOSFET to be turned on is turned on as if it was the active MOSFET.

If  $EN\_GEN\_CHECK = 0$ , the detection of the active and FW MOSFET is disabled. The PWM MOSFET is considered as the active MOSFET.

**Figure 45** shows the detection of the active and of the FW MOSFET.



**Figure 45** Detection of the active and FW MOSFET - Principle

#### 11.3.2 Configurations in PWM mode

The following sections describe the different control schemes in PWM mode.

## Gate Drivers

### Active gate control (AGC)

The active gate control is configured by the control bits AGC[1:0]. The control scheme during the pre-charge and pre-discharge phases of:

- The active MOSFET (**EN\_GEN\_CHECK**=1).
- The PWM MOSFET (**EN\_GEN\_CHECK**=0).

can be selected.

The following settings are possible:

- Adaptive gate control (AGC[1:0] = (1,0) or (1,1), see **GENCTRL**): In this mode a pre-charge current and a pre-discharge current are applied to the gate of the controlled MOSFET. These currents are used to regulate effective the turn-on and turn-off delays to the respective target values.
- No adaptive gate control (AGC[1:0] = (0,0)): in this mode, the pre-charge and pre-discharge phases are deactivated.
- No adaptive gate control (AGC[1:0] = (0,1)). In this mode:
  - During the pre-charge phase, the MOSFET is discharged with the configured current IPCHGINIT (**HB\_PCHG\_INIT**).
  - During the pre-discharge phase, the MOSFET is discharged with the configured current IPDCHGINIT (**HB\_PCHG\_INIT**).

*Note: It is recommended to configure  $tPCHGx < tHBxBLANK$  Active and  $tPDCHGx < tHBxCCP$  Active (Refer to **TPRECHG** and **CCP\_BLK**) independently from the AGC settings.*

### Active free-wheeling (AFW)

The active free-wheeling is activated for HBx if these conditions are fulfilled:

- $AFW_x = 1$  (**HBMODE**)
- $HBx\_PWM\_EN = 1$  (**HBMODE**)
- **PWM\_NB** = 0

If  $AFW_x = 1$ , a cross-current protection time is applied to HBx (set by **CCP\_BLK**) during the PWM operation.

If  $AFW_x = 0$ , no cross current protection is applied to HBx during the PWM operation.

The active free-wheeling reduces the power dissipation of the free-wheeling MOSFET. If an active MOSFET is OFF, the opposite MOSFET of the same half-bridge is actively turned on. Refer to **Figure 49** and **Figure 50**.

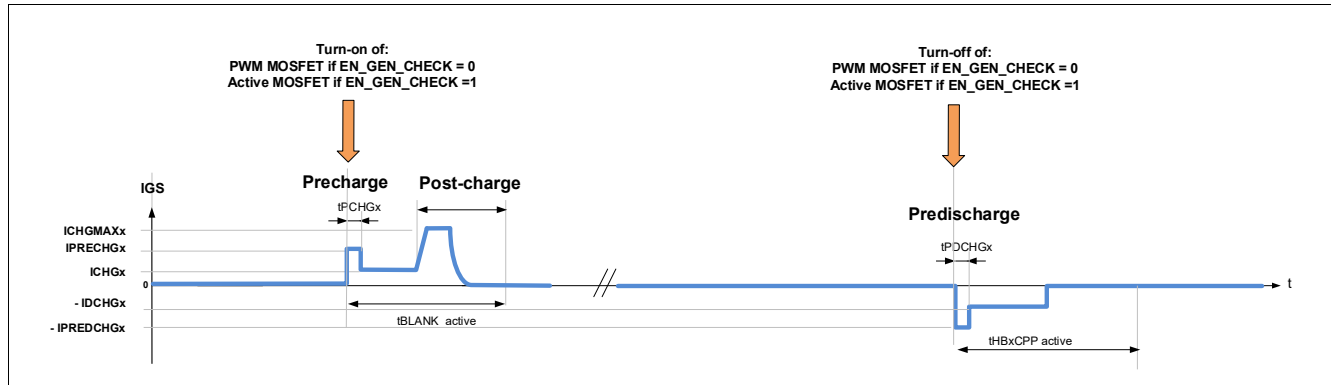


## Gate Drivers

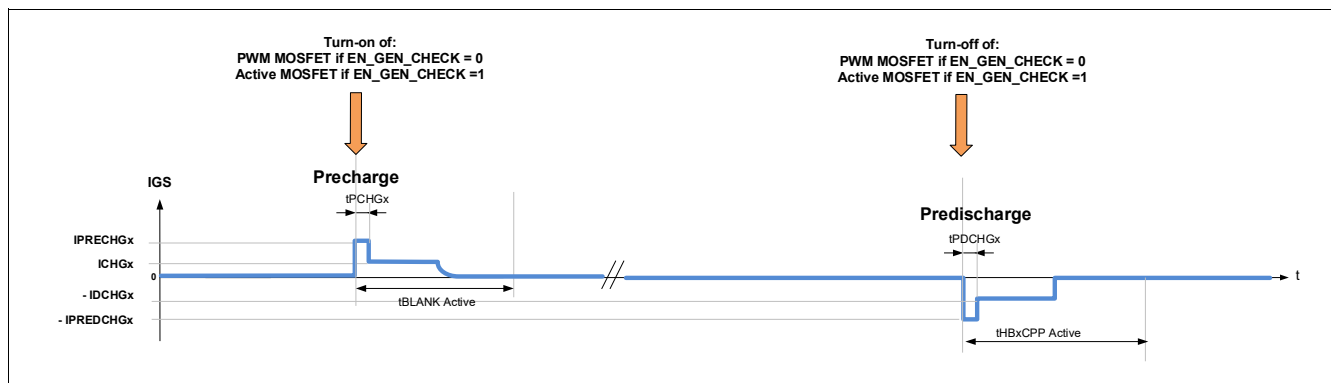
### Post-charge

A post-charge is initiated if POCHGDIS is set to 0 (**GENCTRL**) to reach the minimum MOSFET  $R_{ds(on)}$ :

- **POCHGDIS** = 0: After the charge phase, the control signal for the charge current of LSx is increased by one current step at every bridge driver clock cycle (**BDFREQ**) to ICHGMAXx. Refer to **Figure 46**
- **POCHGDIS** = 1: The post-charge phase is disabled. The charge current is kept to the ICHGx



**Figure 46** PWM overview - AGC = 10<sub>B</sub> or 11<sub>B</sub>, POCHGDIS=0 (post-charge enabled)



**Figure 47** PWM overview - AGC = 10<sub>B</sub> or 11<sub>B</sub>, POCHGDIS=1 (post-charge disabled)

**Table 28** Abbreviations for adaptive turn-on and turn-off phases in PWM configuration

Abbreviation	Definition
Suffix x	Related to the half-bridge x.
VGS_HSx	Gate-Source voltage of high-side MOSFET x.
IGS_HSx	Gate current of high-side MOSFET x. IGS_HSx is positive when the current flows out of GHx.
VGS_LSx	Gate-Source voltage of low-side MOSFET x.
IGS_LSx	Gate current of low-side MOSFET x. IGS_LSx is positive when the current flows out of GLx.
tPWM_SYNCH	Synchronization delay between external and internal PWM signal.
tHBxCCP ACTIVE	Active cross-current protection time of HBx. See control register <b>CCP_BLK</b> .
tHBxBLANK ACTIVE	Active Drain-source overvoltage blank time of HBx. See control register and <b>CCP_BLK</b> .
tHBxCCP FW	Freewheeling cross-current protection time of HBx. See control register <b>CCP_BLK</b> .

**Gate Drivers**

**Table 28 Abbreviations for adaptive turn-on and turn-off phases in PWM configuration (cont'd)**

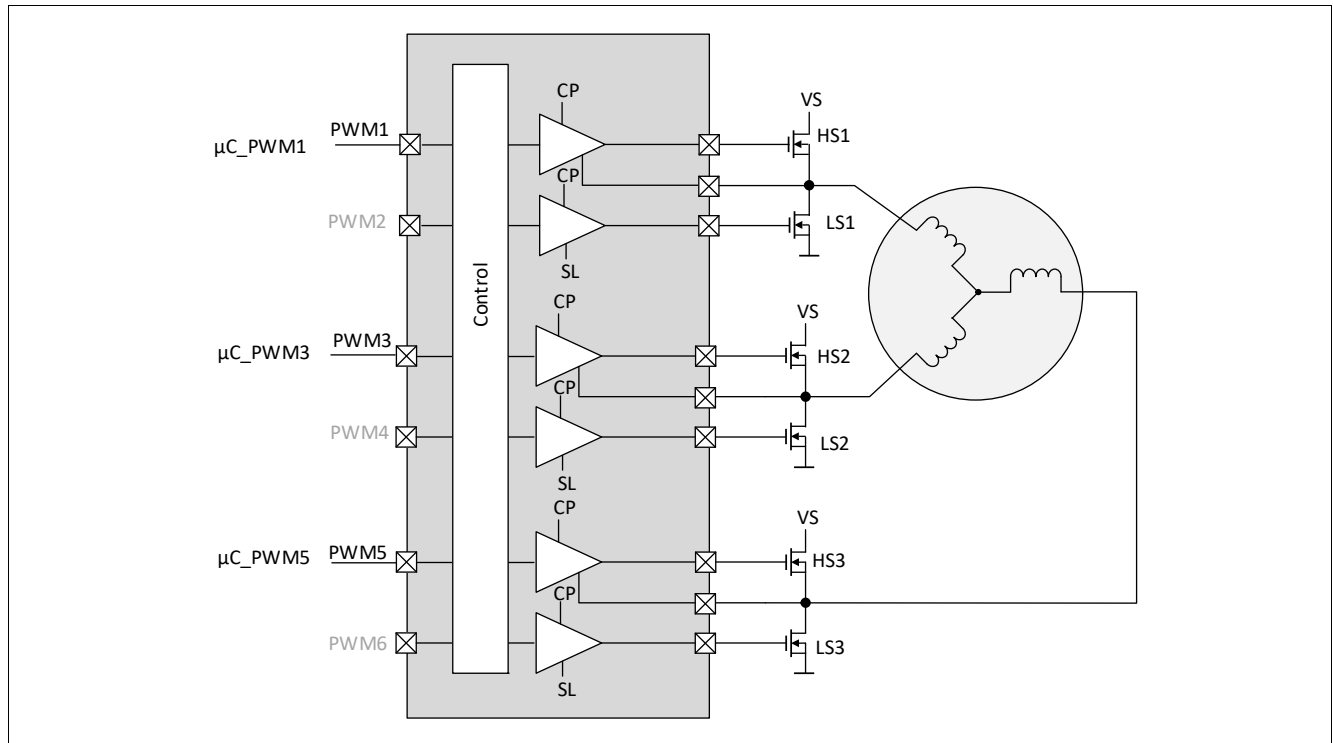
Abbreviation	Definition
tHBxBLANK FW	Freewheeling drain-source overvoltage blank time of HBx. See control register and <b>CCP_BLK</b> .
PWMz	External PWM signal applied to the input pin PWMz.
ICHGMAXx	Maximum drive current of the half-bridge x during the pre-charge and pre-discharge phases. See control register <b>HB_ICHG_MAX</b> . IPRECHGx and IPREDCHGx are limited to ICHGMAXx.
IPRECHGx	Pre-charge current sourced by the gate driver to the active MOSFET of the half-bridge x during tPCHGx ( <b>TPRECHG</b> ). Internal and self-adaptive parameter (if AGC[1:0] = (1,0) or (1,1), <b>GENCTRL</b> ). IPRECHGx is clamped between $I_{CHG0}$ (0.5 mA typ.) and ICHGMAXx.
IPCHGINITx	Initial value of IPRECHGx. Refer to <b>HB_PCHG_INIT</b> .
IPREDCHGx	Pre-discharge-current sunk by the gate driver mapped to the half-bridge x during tPDCHGx. Internal and self-adaptive parameter (if AGC[1:0] = (1,0) or (1,1), <b>GENCTRL</b> ). IPREDCHGx is clamped between $I_{DCHG0}$ (0.5 mA typ.) and ICHGMAXx.
IPDCHGINITx	Initial value of IPREDCHGx. Refer to <b>HB_PCHG_INIT</b> .
ICHGx	Current sourced by the gate driver to the active MOSFET of the half-bridge x during the charge phase. See control register <b>HB_ICHG</b> .
IDCHGx	Current sunk by the gate driver to turn-off the active MOSFET of the half-bridge x during the discharge phase. See control register <b>HB_ICHG</b> .
ICHGFWx	Current sourced or sunk by the gate driver to turn on / turn off the freewheeling MOSFET of the half-bridge x. See control register <b>HB_ICHG</b> .
tPCHGx	Duration of the pre-charge phase of half-bridge x. tPCHGx is configurable by SPI. See control register <b>TPRECHG</b> .
tPDCHGx	Duration of the pre-discharge phase of half-bridge x. tPDCHGx is configurable by SPI. See control register <b>TPRECHG</b> .
tDONx	Turn-on delay of the active MOSFET of HBx.
tDOFFx	Turn-off delay of the active MOSFET of HBx.
IHOLD	Hold current sourced or sunk by the gate driver to keep the MOSFET in the desired state. See IHOLD control bit in <b>GENCTRL</b> .
IHARDOFF	IHARDOFF is the maximum current that the gate drivers can sink. It corresponds to the discharge current when IDCHGx[5:0] = 63 <sub>D</sub> (150 mA typ.).
TFVDS	Drain-Source overvoltage filter time. See <b>LS_VDS</b> .

### 11.3.3 PWM operation with 3 PWM inputs

Each half bridge are controlled by one input if PWM\_NB = 0 (see **CSA**) and HBx\_PWM\_EN (see **HBMODE**):

- PWM1/CRC controls HB1
- PWM3 controls HB2
- PWM5 controls HB3

## Gate Drivers



**Figure 48** Half-bridge PWM control with three PWM inputs, PWM\_NB = 0

**Table 29** Half-bridge PWM settings with 3 PWM inputs

PWM_NB	HBxPWM_EN <sup>1)</sup>	HBxMODE <sup>1)</sup>	AFW	Half-bridge x settings <sup>1)</sup>
0	Don't care	00 <sub>B</sub>	Don't care	LSx and HSx MOSFETs are kept OFF by the passive discharge
0	1	01 <sub>B</sub>	0	PWM signal applied to LSx PWM signal = 1: LSx, ON, HSx OFF PWM signal = 0: LSx OFF, HS x OFF
0	1	10 <sub>B</sub>	1	PWM signal applied to HSx PWM signal= 1: HSx, ON, LSx OFF PWM signal = 0: HSx OFF, LS x ON
0	Don't care	11 <sub>B</sub>	Don't care	LSx and HSx MOSFETs are actively kept OFF

1) x = 1 to 3

### 11.3.3.1 Control signals with active free-wheeling (AFWx = 1)

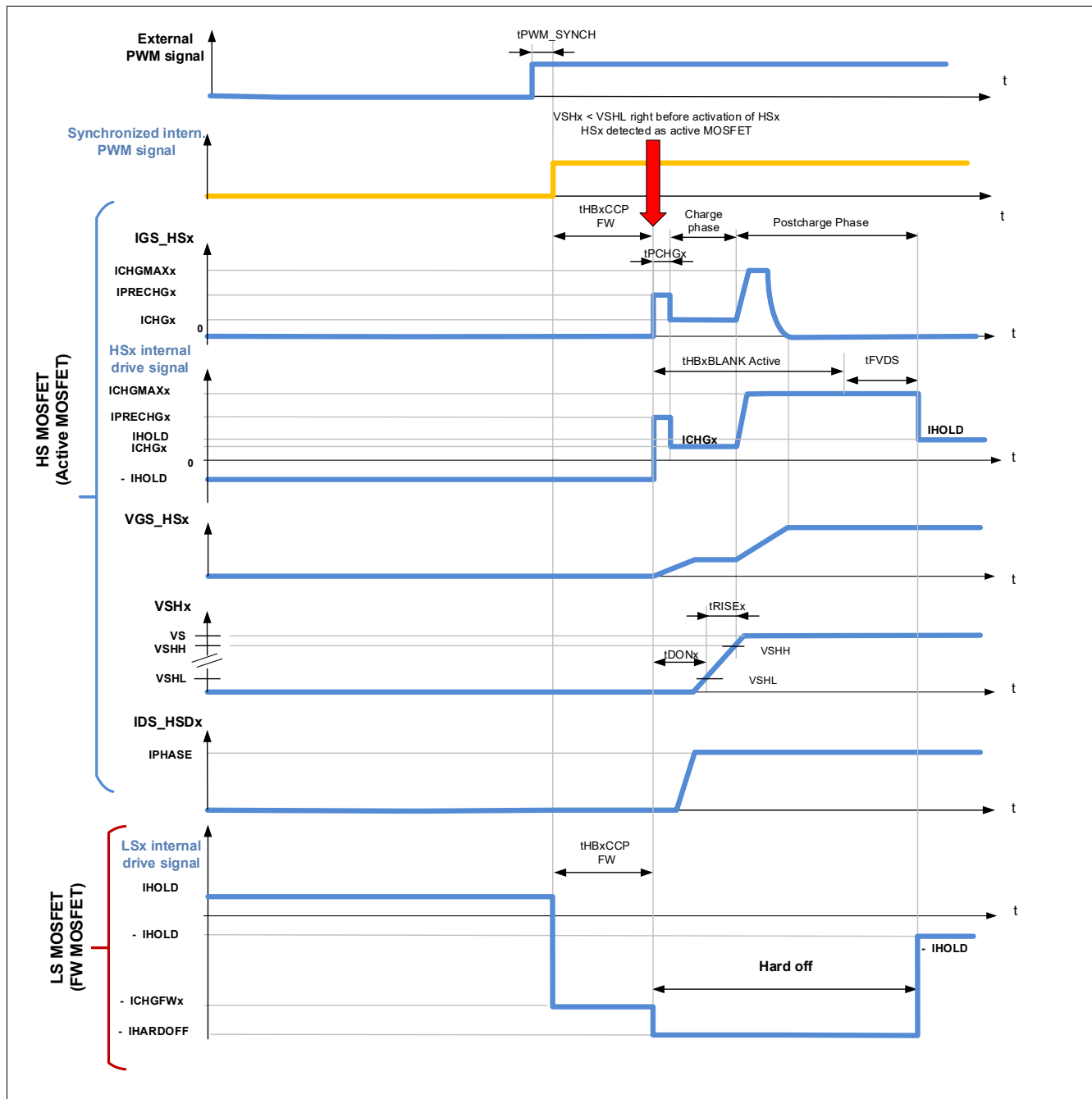
This section describes the MOSFET control signals with active freewheeling and HS PWM:

- The HS PWM MOSFET is the active MOSFET ([Chapter 11.3.3.1.1](#)).
- The HS PWM MOSFET is the free-wheeling MOSFET ([Chapter 11.3.3.1.2](#)).

#### 11.3.3.1.1 The PWM MOSFET is the active MOSFET

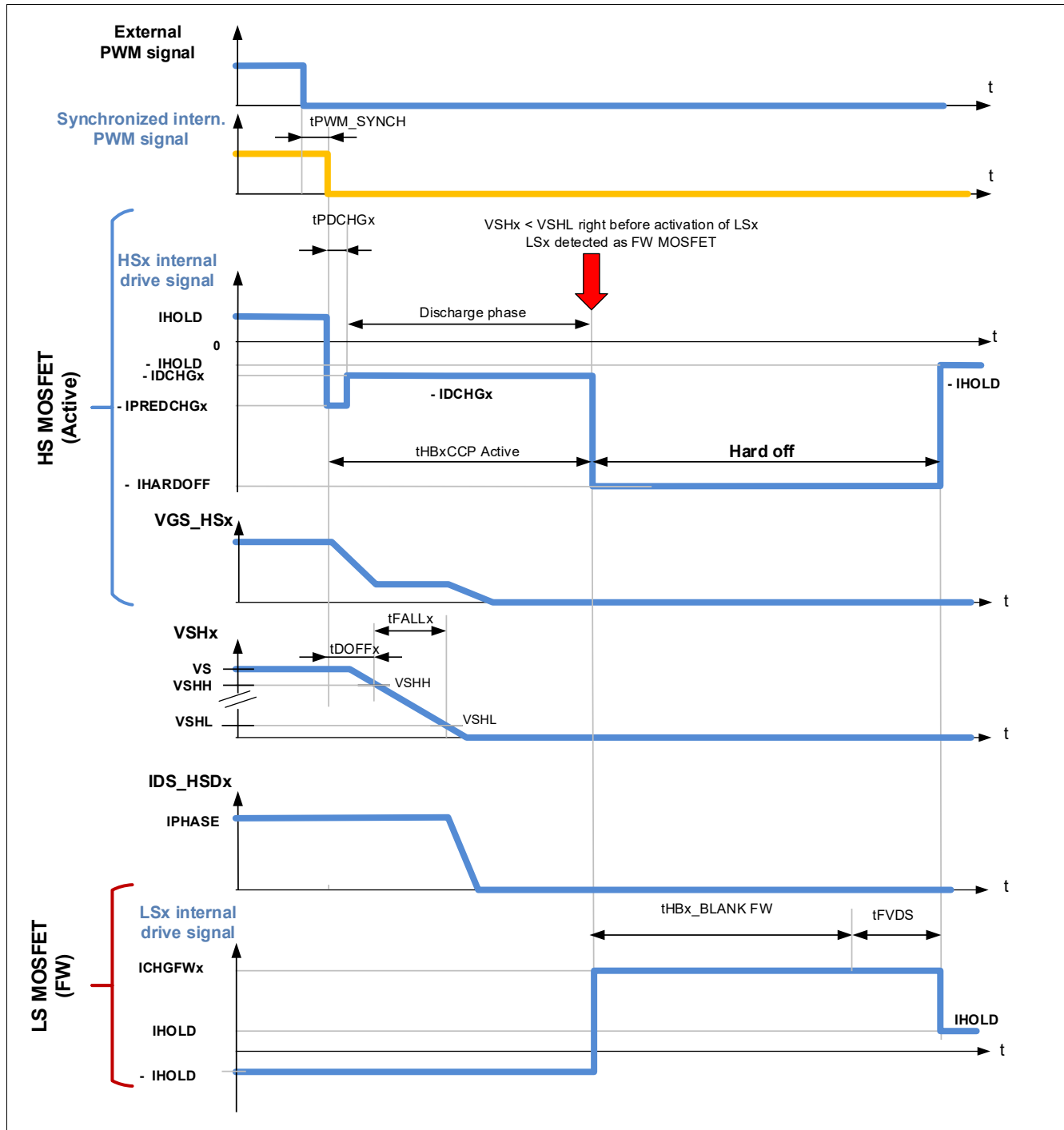
This section shows the control signals of the MOSFET when the PWM is the active MOSFET.

Gate Drivers



**Figure 49** Turn-on of an active MOSFET in PWM mode with active gate control, HS PWM, HS as active MOSFET, LS as FW MOSFET. PWM\_NB = 0 (one PWM input per HB), HBxMODE = 10<sub>B</sub> (HS PWM), AGC = 01<sub>B</sub> or 10<sub>B</sub> (Active Gate Control), EN\_GEN\_CHECK = 1 (detection of active / FW MOSFET), AFWx = 1 (active freewheeling for HBx is activated)

Gate Drivers

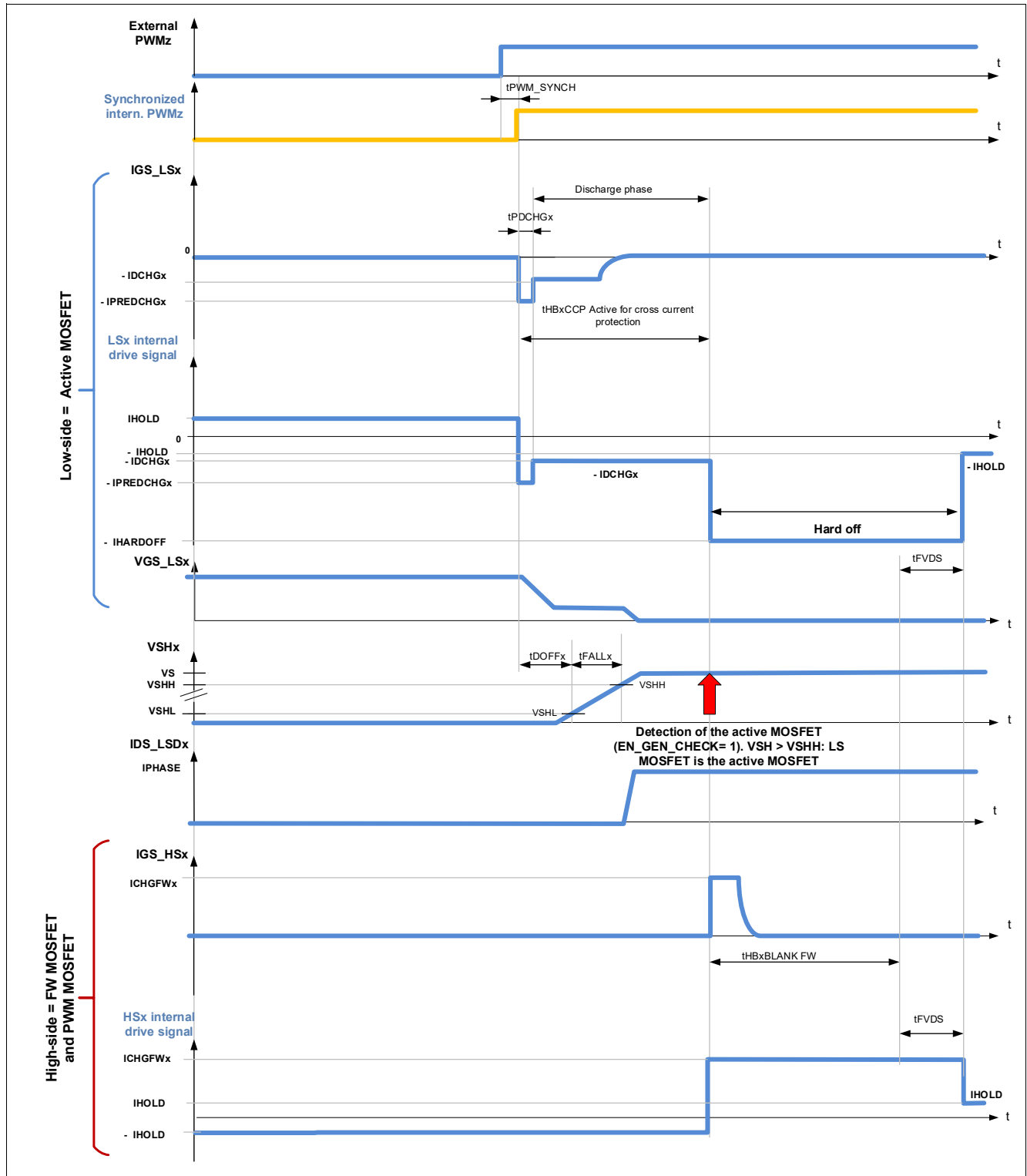


**Figure 50** Turn-off of an active MOSFET in PWM mode with active gate control, HS PWM, HS as active MOSFET, LS as FW MOSFET. PWM\_NB = 0 (one PWM input per HB), HBxMODE = 10<sub>B</sub> (HS PWM), AGC = 01<sub>B</sub> or 10<sub>B</sub> (Active Gate Control), EN\_GEN\_CHECK = 1 (detection of active / FW MOSFET), AFWx = 1 (active freewheeling for HBx is activated)

## Gate Drivers

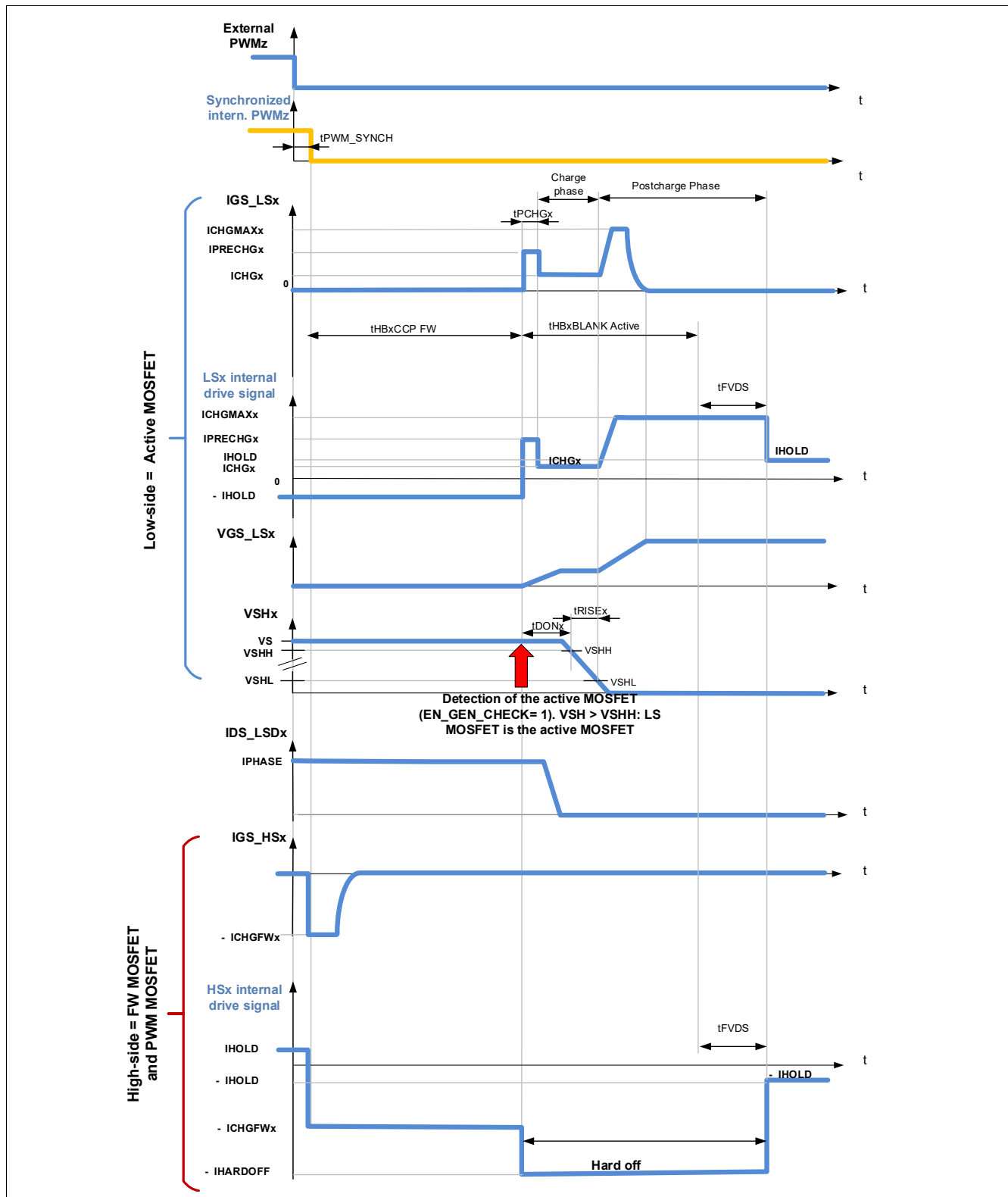
### 11.3.3.1.2 The PWM MOSFET is the free-wheeling MOSFET

This section shows the control signals of the MOSFET when the PWM is the free-wheeling MOSFET.



**Figure 51** PWM rising edge - PWM mode with active gate control, HS PWM (HBxMODE = 10<sub>B</sub>), LS as active MOSFET, HS as FW MOSFET. PWM\_NB = 0 (one PWM input per HB), AGC = 01<sub>B</sub> or 10<sub>B</sub> (Active Gate Control), EN\_GEN\_CHECK = 1 (detection of active / FW MOSFET), AFWx = 1 (active freewheeling for HBx is activated)

Gate Drivers



**Figure 52** PWM falling edge - PWM mode with active gate control, HS PWM ( $HBxMODE = 10_B$ ), LS as active MOSFET, HS as FW MOSFET.  $PWM\_NB = 0$  (one PWM input per HB),  $AGC = 01_B$  or  $10_B$  (Active Gate Control),  $EN\_GEN\_CHECK = 1$  (detection of active / FW MOSFET),  $AFWx = 1$  (active freewheeling for HBx is activated)

### **11.3.3.2 Control signals with passive free-wheeling (AFWx = 0)**

This section describes the MOSFET control signals with active freewheeling and HS PWM:

- The HS PWM MOSFET is the active MOSFET ([Chapter 11.3.3.2.1](#)).
- The HS PWM MOSFET is the free-wheeling MOSFET ([Chapter 11.3.3.2.2](#)).

#### **11.3.3.2.1 The PWM MOSFET is the active MOSFET**

This section shows the control signals of the MOSFET when the PWM is the active MOSFET.



Gate Drivers

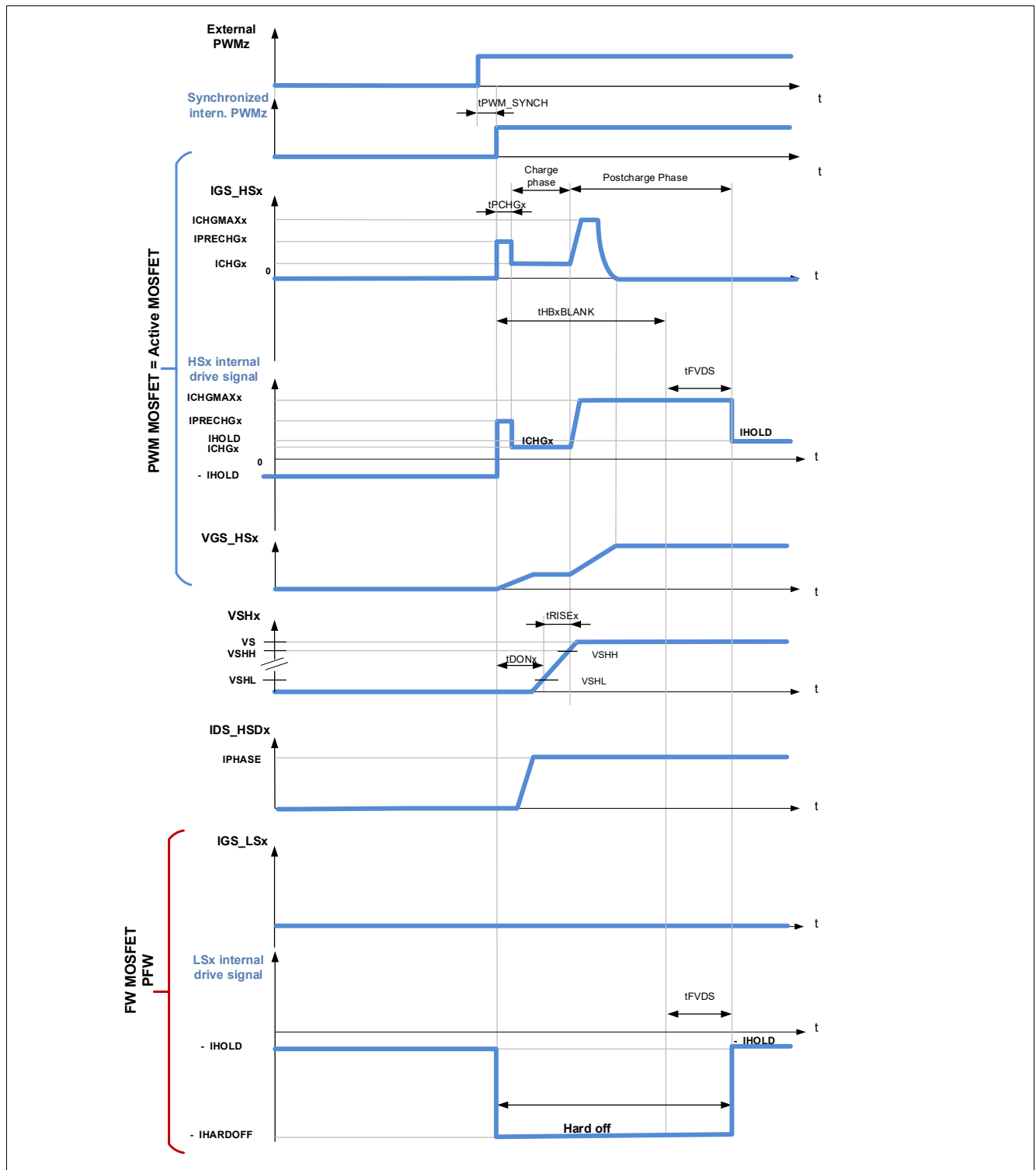
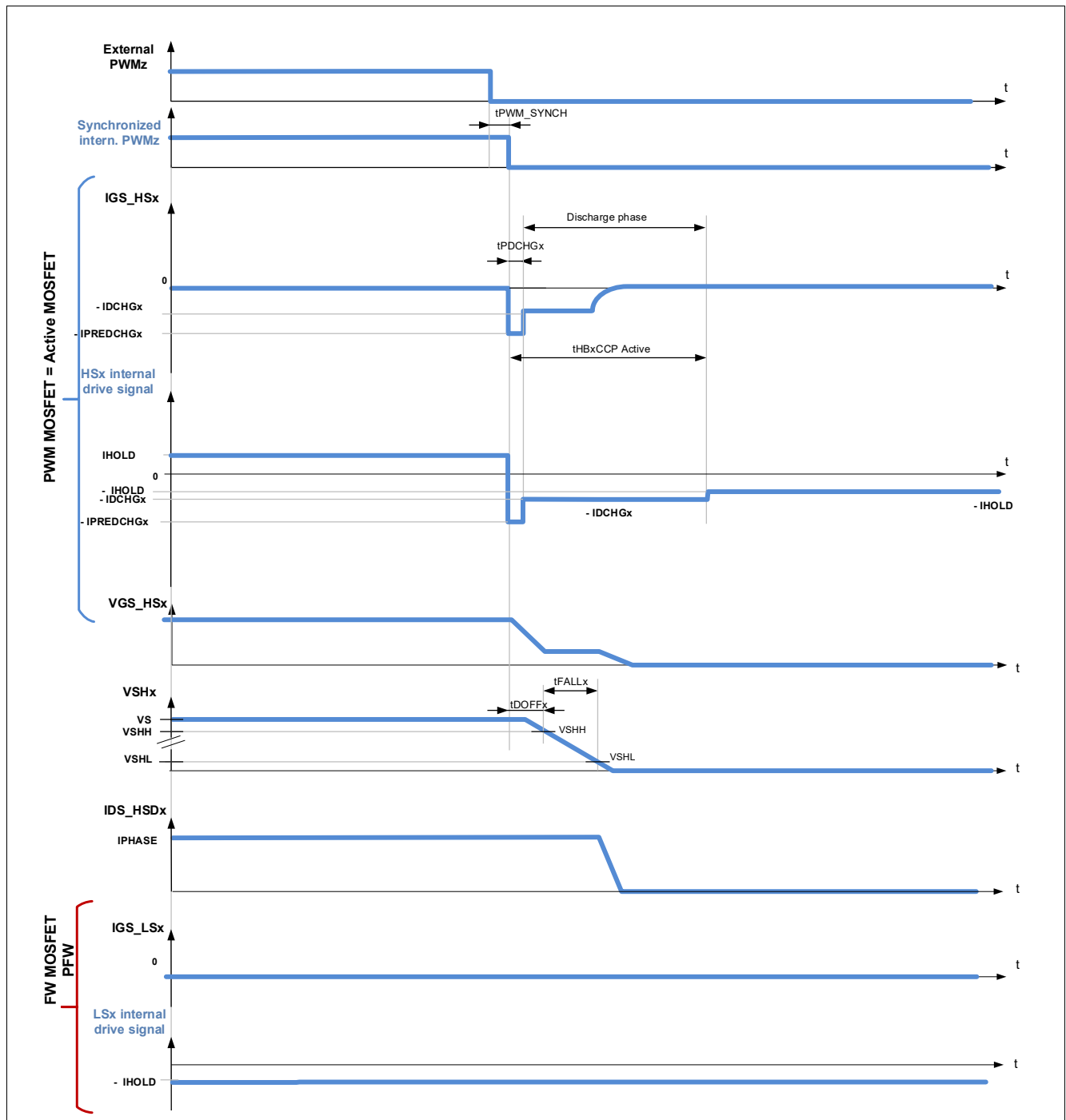


Figure 53 Adaptive turn-on with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0, the PWM MOSFET is the active MOSFET. PWM\_NB=0.



**Figure 54 Adaptive turn-off with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0, the PWM MOSFET is the active MOSFET.PWM\_NB=0.**

### 11.3.3.2.2 The PWM MOSFET is the free-wheeling MOSFET

This section shows the control signals of the MOSFET when the PWM is the free-wheeling MOSFET.

Gate Drivers

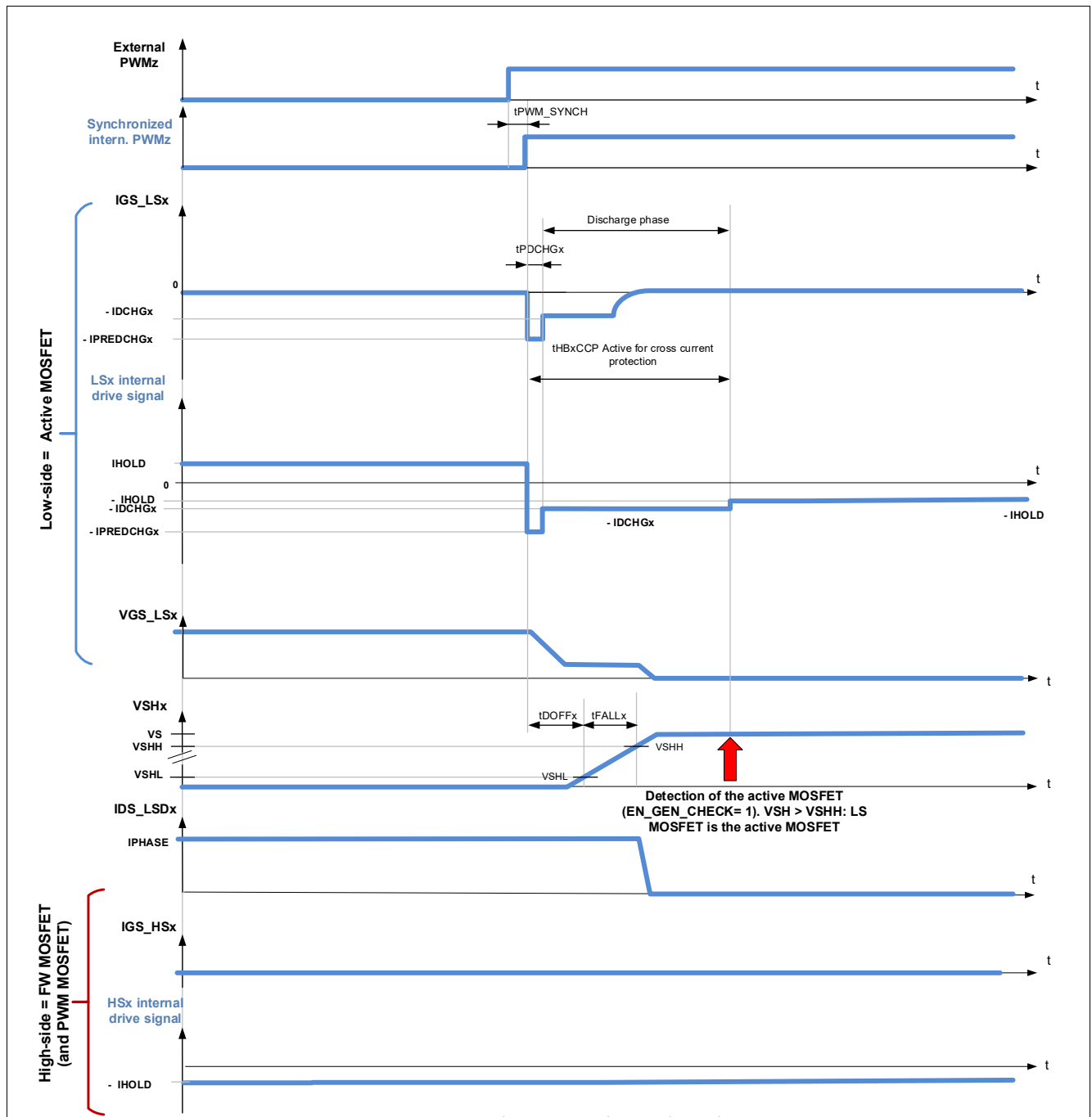


Figure 55 PWM rising edge with adaptive control, EN\_GEN\_CHECK = 1 with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0. The PWM MOSFET is the FW MOSFET. PWM\_NB=0.

**Figure 56** PWM falling edge with adaptive control, EN\_GEN\_CHECK = 1 with high-side PWM, AGC[1:0] = (1,0) or (1,1), AFWx=0, POCHGDIS=0. The PWM MOSFET is the FW MOSFET. PWM\_NB=0.

## Gate Drivers

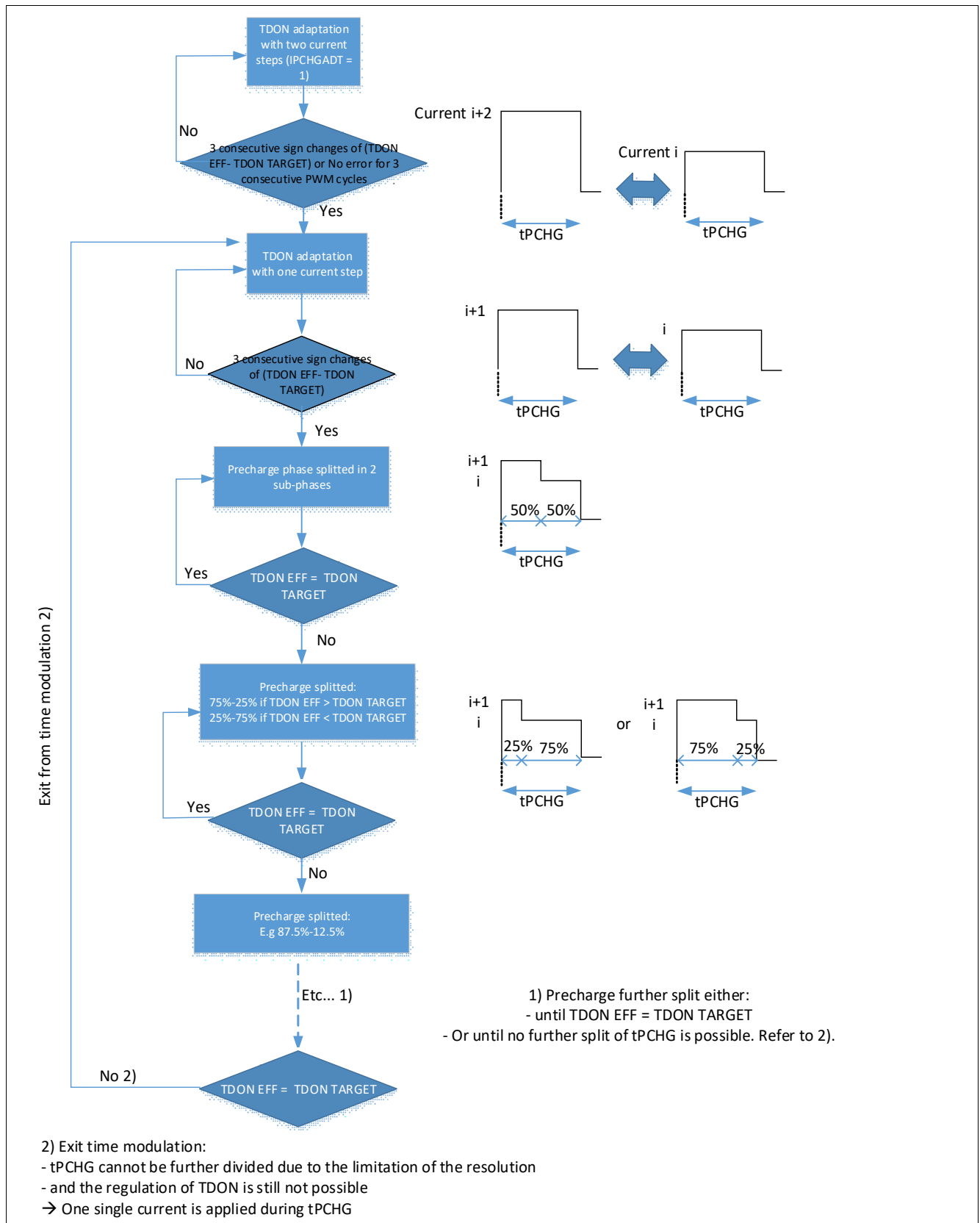
- one single precharge current is applied during  $t_{PCHGx}$  to regulate  $TDON$
- one single precharge current is applied during  $t_{PDCHGx}$  to regulate  $TDOFF$

If **DEEP\_ADAP** = 1 (“deep adaptation” or “time modulation”) it is possible to:

- to divide the precharge phase in two parts, during which two different precharge currents can be applied
- to divide the predischage phase in two parts, during which two different precharge currents can be applied

**Figure 57** describes the principle of the time modulation applied to the precharge phase. The same principle is also applied for the regulation of the pre-discharge phase.

## Gate Drivers



**Figure 57** Principle of the time modulation of the precharge phase, **DEEP\_ADAP = 1**, **AGC = 10<sub>B</sub>** or **11<sub>B</sub>**

#### **11.3.3.4 Operation at high and low duty cycles**

In the particular cases where the on-time is shorter than  $t_{HBxCCP}$  FW or the off-time of the PWM signal is shorter than  $t_{HBxCCP}$  Active:

- No distinction between active MOSFET and FW MOSFET is possible. Therefore PWM MOSFET (selected by  $HBxMODE[1:0]$ ) is controlled as active MOSFET.
- The MOSFET opposite to the PWM MOSFET stays off (passive FW)

#### **11.3.3.5 Measurements of the switching times**

The effective switching times in PWM operation:

- of the PWM MOSFET if **EN\_GEN\_CHECK** = 0
- of the active MOSFET if **EN\_GEN\_CHECK** = 1

are reported in the registers:

**EFF\_TDON\_OFF1, EFF\_TDON\_OFF2, EFF\_TDON\_OFF3.**

If the end of the rise time for a given MOSFET is not detected before  $t_{HBxBLANK}$  Active elapses, then the corresponding status register reports an effective rise time equal to zero.

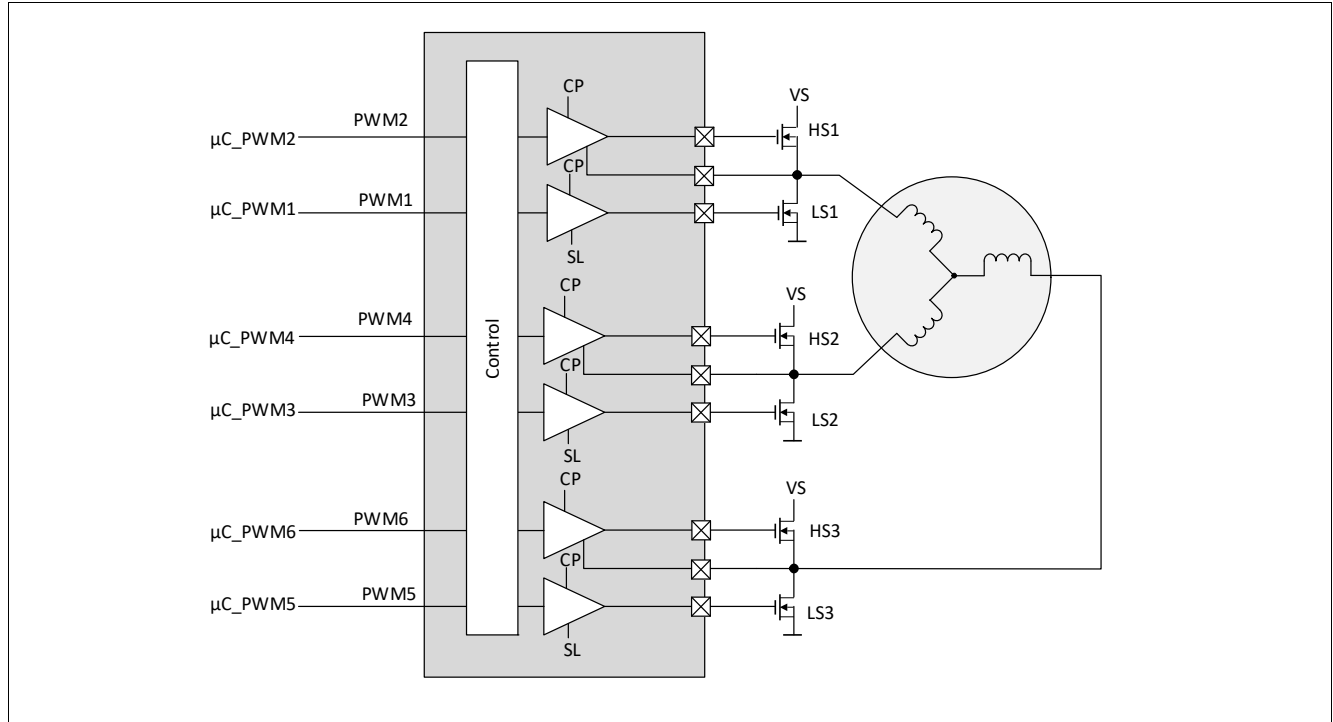
If the end of the fall time for a given MOSFET is not detected before  $t_{HBxCCP}$  Active active elapses, then the corresponding status register reports an effective fall time equal to zero.

The device cannot measure the switching times  $t_{DON}$ ,  $t_{DOFF}$ ,  $t_{RISE}$  and  $t_{FALL}$  at very high and very low duty cycles:  $t_{ON} < t_{HBxCCP}$  FW and  $t_{OFF} < t_{HBxCCP}$  active. In this case, the corresponding registers report effective  $t_{DON}$ ,  $t_{DOFF}$ ,  $t_{RISE}$  and  $t_{FALL}$  equal to zero.

## Gate Drivers

### 11.3.4 PWM operation with 6 PWM inputs

Each high-side MOSFET and each low-side MOSFET is controlled by one PWM input. if PWM\_NB is set to 1 (see [CSA](#)) and HBx\_PWM\_EN are set to 1 (see [HBMODE](#)). Refer to [Table 30](#).



**Figure 58** Half-bridge PWM control with six PWM inputs, PWM\_NB = 1

**Table 30** Half-bridge PWM settings with 6 PWM inputs (PWM\_NB = 1)FW and Active MOSFET

PWM_NB	HBx_PWM_EN <sup>1)</sup>	HBxMODE <sup>1)</sup>	Half-bridge x settings <sup>1)</sup>
1	Don't care	00 <sub>B</sub>	LSx and HSx MOSFETs are kept OFF by the passive discharge (default)
1	1	01 <sub>B</sub>	HBx is controlled by its PWM inputs <ul style="list-style-type: none"> <li>If <a href="#">EN_GEN_CHECK</a> = 0: LSx is always considered as the active MOSFET</li> <li>If <a href="#">EN_GEN_CHECK</a> = 1: The active and the FW MOSFETs are detected according to <a href="#">Chapter 11.3.1</a>, independently from HBxMODE</li> </ul>
1	1	10 <sub>B</sub>	HBx is controlled by its PWM inputs <ul style="list-style-type: none"> <li>If <a href="#">EN_GEN_CHECK</a> = 0: HSx is always considered as the active MOSFET</li> <li>If <a href="#">EN_GEN_CHECK</a> = 1: The active and the FW MOSFETs are detected according to <a href="#">Chapter 11.3.1</a> independently from HBxMODE</li> </ul>
1	Don't care	11 <sub>B</sub>	LSx and HSx MOSFETs are actively kept OFF

1) x = 1 to 3



**Gate Drivers**

**Table 31 PWM Control of HS1 and LS1, PWM\_NB = 1, HB1\_PWM\_EN = 1**

HB1MODE[1:0]	PWM1/CRC	PWM2	HS1	LS1
01	Low	Low	OFF	OFF
01	Low	High	ON	OFF
01	High	Low	OFF	ON
01	High	High	OFF	OFF
10	Low	Low	OFF	OFF
10	Low	High	OFF	ON
10	High	Low	ON	OFF
10	High	High	OFF	OFF

**Table 32 PWM Control of HS2 and LS2, PWM\_NB = 1, HB2\_PWM\_EN = 1**

HB2MODE[1:0]	PWM3	PWM4	HS2	LS2
01	Low	Low	OFF	OFF
01	Low	High	ON	OFF
01	High	Low	OFF	ON
01	High	High	OFF	OFF
10	Low	Low	OFF	OFF
10	Low	High	OFF	ON
10	High	Low	ON	OFF
10	High	High	OFF	OFF

**Table 33 PWM Control of HS3 and LS3, PWM\_NB = 1, HB3\_PWM\_EN = 1**

HB3MODE[1:0]	PWM5	PWM6	HS3	LS3
01	Low	Low	OFF	OFF
01	Low	High	ON	OFF
01	High	Low	OFF	ON
01	High	High	OFF	OFF
10	Low	Low	OFF	OFF
10	Low	High	OFF	ON
10	High	Low	ON	OFF
10	High	High	OFF	OFF

**Figure 59** shows the PWM control of HBx in PWM (HBx\_PWM\_EN = 1): Turn-off of the FW MOSFET (low-side MOSFET in this case) followed by the activation of the active MOSFET (high-side MOSFET in this case)<sup>1)</sup> with PWM\_NB = 1, AGC[1:0]=01<sub>B</sub> or 10<sub>B</sub>, **POCHGDIS** = 0 (post-charge enabled).

This control scheme is applicable for the following cases:

1) If the synchronized HS PWM rising edge occurs after tHBxCCP FW and before the end of tOFF timeout FW, then the LS MOSFET is discharged with IHARDOFF and the HS is turned on, when the HS PWM rising edge is detected

## Gate Drivers

1. **EN\_GEN\_CHECK** = 0 (detection of FW/Active MOSFET disabled); HBxMODE[1:0] = 10<sub>B</sub> (HS MOSFET is considered as active MOSFET by default).
2. **EN\_GEN\_CHECK** = 1 (detection of active / FW MOSFET enabled); HS MOSFET detected as active MOSFET; HBxMODE[1:0] = 01<sub>B</sub> or 10<sub>B</sub>.

*Note: If the synchronized HS PWM rising edge occurs before the end of tHBxCCP active, then the device prevents an activation of the HS MOSFET until tHBxCCP FW elapses. In other words, the HS PWM rising edge is ignored until the end of tHBxCCP FW.*

Gate Drivers

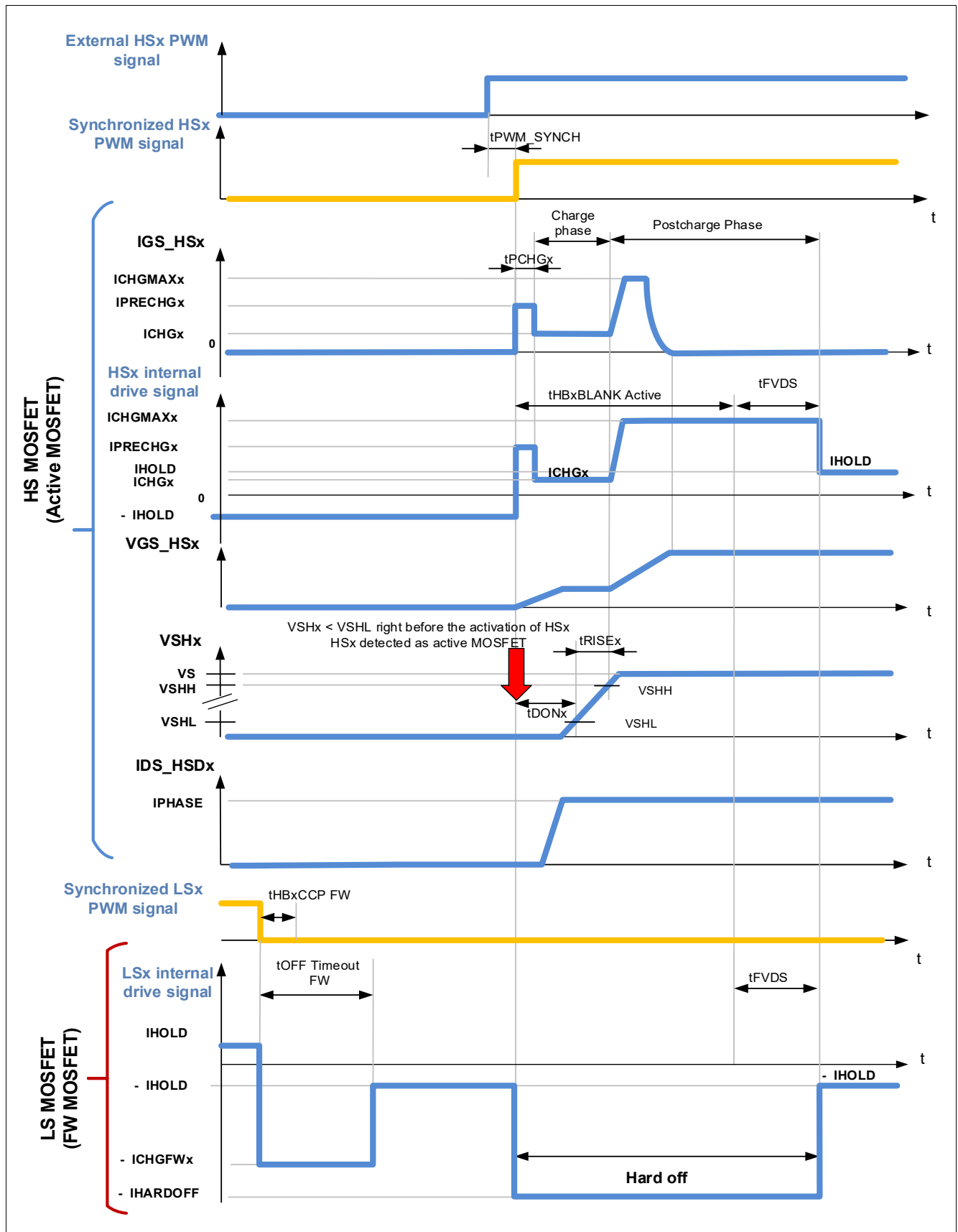


Figure 59 Turn-on of an active MOSFET in PWM mode with active gate control, HS as active MOSFET, LS as FW MOSFET. Two PWM inputs per half-bridge, active gate control enabled. PWM\_EN=1

## Gate Drivers

**Figure 60** shows the PWM control of HBx in PWM (HBx\_PWM\_EN = 1): Turn-off of the active MOSFET (high-side MOSFET in this case) followed by the activation of the FW MOSFET low-side MOSFET in this case) with PWM\_NB = 1, AGC[1:0] = 01<sub>B</sub> or 10<sub>B</sub>, **POCHDIS** = 0 (post-charge enabled).

This control scheme is applicable for the following cases:

1. **EN\_GEN\_CHECK** = 0 (detection of FW/Active MOSFET disabled); HBxMODE[1:0] = 10<sub>B</sub> (HS MOSFET is considered as active MOSFET by default).
2. **EN\_GEN\_CHECK** = 1 (detection of active / FW MOSFET enabled); HS MOSFET detected as active MOSFET; HBxMODE[1:0] = 01<sub>B</sub> or 10<sub>B</sub>.

*Note: If the synchronized LS PWM rising edge occurs before the end of tHBxCCP active, then the device prevents an activation of the LS MOSFET until tHBxCCP active elapses. In other words, the LS PWM rising edge is ignored until the end of tHBxCCP active.*

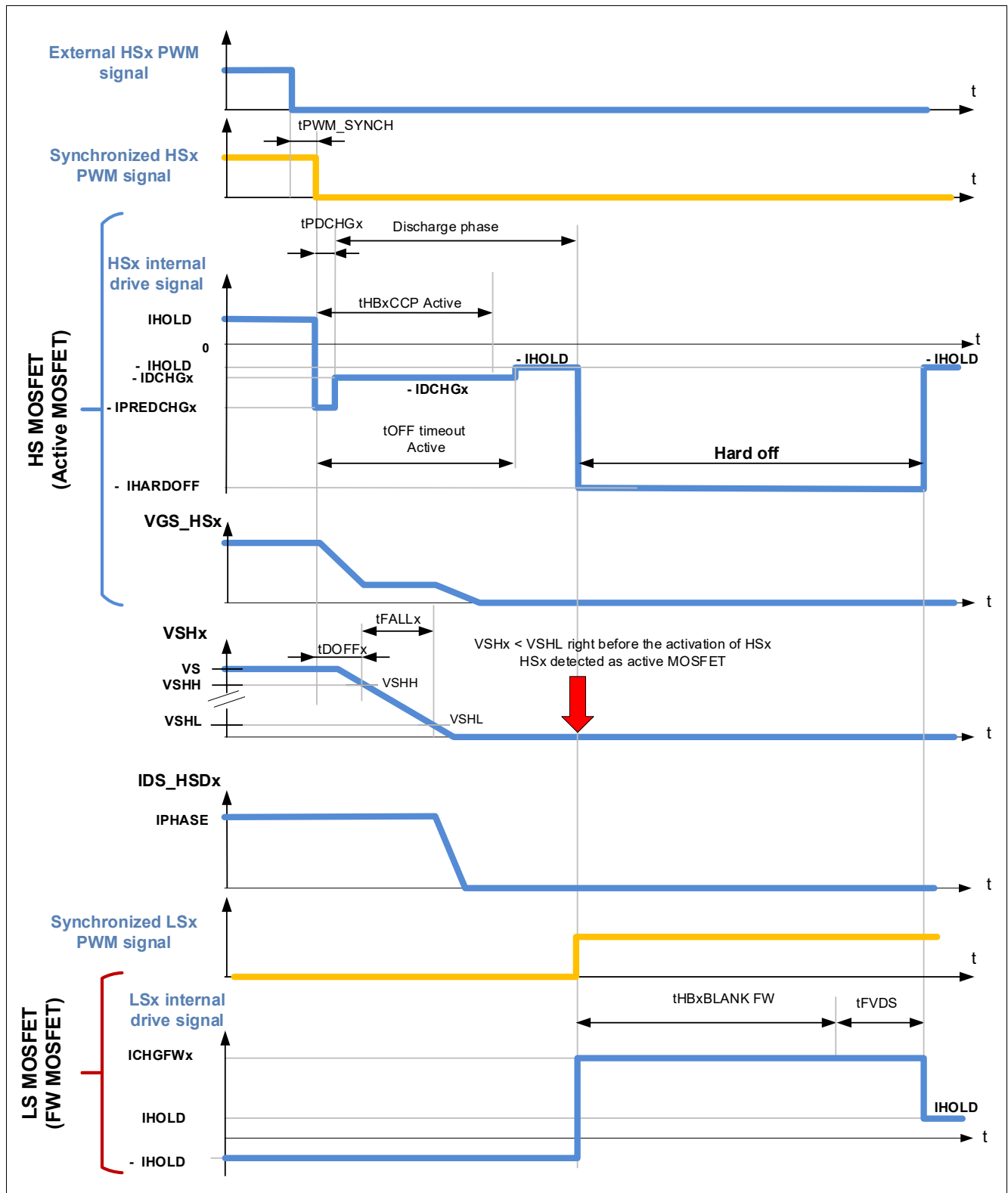


Figure 60 Turn-off of an active MOSFET in PWM mode with active gate control, HS as active MOSFET, LS as FW MOSFET. two PWM inputs per half-bridge, active gate control enabled. PWM\_NB=1.

### 11.3.5 Status bits for regulation of turn-on and turn-off delay times

The control bits TDREGx (**TDREG**) indicate if  $t_{DONx}$  and  $t_{DOFFx}$  of the half-bridge x, using the adaptive control scheme (**AGC** = 10<sub>B</sub> or 11<sub>B</sub>), are in regulation.

## Gate Drivers

The half-bridge x is considered in regulation if one of the following conditions is met:

- Condition 1: The effective turn-on and turn-off delays are equal to the configured delays for at least eight cumulative PWM cycle (HBx tDON counter  $\geq 8$  and HBx tDOFF counter  $\geq 8$ ). For each PWM cycle
  - if  $tDON_{xEFF}^{(1)} = TDON_x^{(2)}$ ,  $x = 1..3$ , HBx tDON counter is incremented
  - if  $tDON_{xEFF}^{(1)} \neq TDON_x^{(2)}$ ,  $x = 1..3$ , HBx tDON counter is decremented
  - if  $tDOFF_{xEFF}^{(1)} = TDOFF_x^{(3)}$ ,  $x = 1..3$ , HBx tDOFF counter is incremented
  - if  $tDOFF_{xEFF}^{(1)} \neq TDOFF_x^{(3)}$ ,  $x = 1..3$ , HBx tDOFF counter is decremented
- Condition 2: The error between the effective delays ((tDON<sub>x</sub>EFF-TDON<sub>x</sub>) and (tDOFF<sub>x</sub>EFF-TDOFF<sub>x</sub>)) changes its sign three times consecutively

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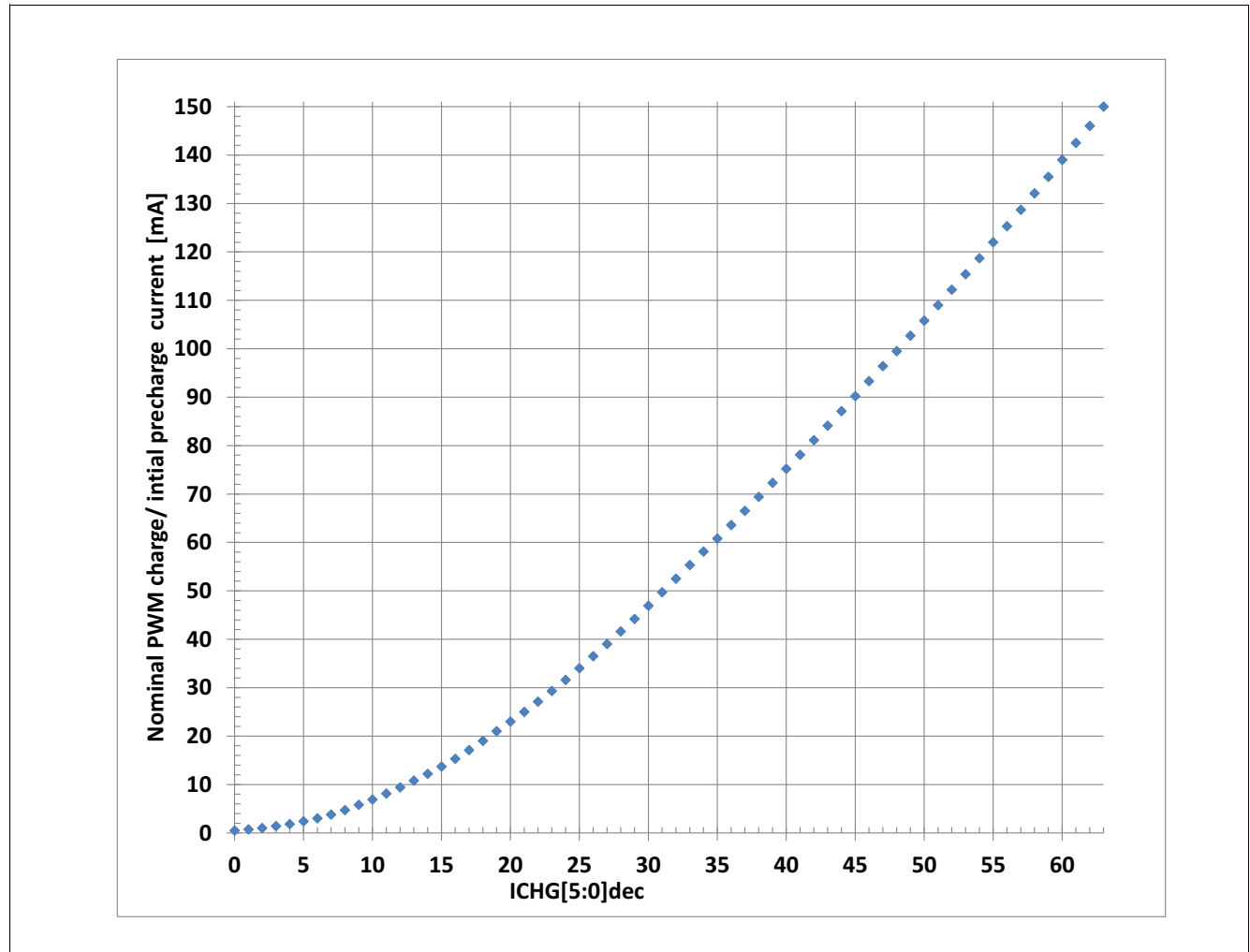
1) Refer to **EFF\_TDON\_OFF1**, **EFF\_TDON\_OFF2**, **EFF\_TDON\_OFF3**

2) Refer to **TDON\_HB\_CTRL**

3) Refer to **TDOFF\_HB\_CTRL**

### 11.3.6 Gate driver current

Each gate driver is able to source and sink currents from 0.5 mA to 150 mA, with 64 steps.



**Figure 61 Configurable discharge currents in PWM operation**

**Gate Drivers**

**Table 34 Charge currents and initial precharge currents**

<b>ICHGx[5:0], PCHGINITx[5:0]</b>	<b>Parameter name</b>	<b>Nom. current [mA]</b>	<b>Max. deviation to nominal values [%]</b>
000000 <sub>B</sub>	$I_{CHG0}$	0.5	+/- 60%
000001 <sub>B</sub>	$I_{CHG1}$	0.7	+/- 60 %
000010 <sub>B</sub>	$I_{CHG2}$	1.0	+/- 60 %
000011 <sub>B</sub>	$I_{CHG3}$	1.4	+/- 60 %
000100 <sub>B</sub>	$I_{CHG4}$	1.8	+/- 60 %
000101 <sub>B</sub>	$I_{CHG5}$	2.4	+/- 60 %
000110 <sub>B</sub>	$I_{CHG6}$	3.0	+/- 60 %
000111 <sub>B</sub>	$I_{CHG7}$	3.8	+/- 60 %
001000 <sub>B</sub>	$I_{CHG8}$	4.7	+/- 55%
001001 <sub>B</sub>	$I_{CHG9}$	5.8	+/- 55%
001010 <sub>B</sub>	$I_{CHG10}$	6.9	+/- 55%
001011 <sub>B</sub>	$I_{CHG11}$	8.1	+/- 55%
001100 <sub>B</sub>	$I_{CHG12}$	9.4	+/- 55%
001101 <sub>B</sub>	$I_{CHG13}$	10.8	+/- 55%
001110 <sub>B</sub>	$I_{CHG14}$	12.2	+/- 40%
001111 <sub>B</sub>	$I_{CHG15}$	13.7	+/- 40%
010000 <sub>B</sub>	$I_{CHG16}$	15.3	+/- 40 %
010001 <sub>B</sub>	$I_{CHG17}$	17.1	+/- 40 %
010010 <sub>B</sub>	$I_{CHG18}$	19	+/- 40%
010011 <sub>B</sub>	$I_{CHG19}$	21	+/- 40 %
010100 <sub>B</sub>	$I_{CHG20}$	23	+/- 40%
010101 <sub>B</sub>	$I_{CHG21}$	25	+/- 40 %
010110 <sub>B</sub>	$I_{CHG22}$	27.1	+/- 40 %
010111 <sub>B</sub>	$I_{CHG23}$	29.3	+/- 40 %
011000 <sub>B</sub>	$I_{CHG24}$	31.6	+/- 40 %
011001 <sub>B</sub>	$I_{CHG25}$	34	+/- 40 %
011010 <sub>B</sub>	$I_{CHG26}$	36.5	+/- 40 %
011011 <sub>B</sub>	$I_{CHG27}$	39	+/- 40 %
011100 <sub>B</sub>	$I_{CHG28}$	41.6	+/- 40 %
011101 <sub>B</sub>	$I_{CHG29}$	44.2	+/- 30 %
011110 <sub>B</sub>	$I_{CHG30}$	46.9	+/- 30 %
011111 <sub>B</sub>	$I_{CHG31}$	49.7	+/- 30 %
100000 <sub>B</sub>	$I_{CHG32}$	52.5	+/- 30 %
100001 <sub>B</sub>	$I_{CHG33}$	55.3	+/- 30 %
100010 <sub>B</sub>	$I_{CHG34}$	58.1	+/- 30 %
100011 <sub>B</sub>	$I_{CHG35}$	60.8	+/- 30 %



**Gate Drivers**

**Table 34** Charge currents and initial precharge currents (cont'd)

<b>ICHGx[5:0], PCHGINITx[5:0]</b>	<b>Parameter name</b>	<b>Nom. current [mA]</b>	<b>Max. deviation to nominal values [%]</b>
100100 <sub>B</sub>	$I_{CHG36}$	63.6	+/- 30 %
100101 <sub>B</sub>	$I_{CHG37}$	66.5	+/- 30 %
100110 <sub>B</sub>	$I_{CHG38}$	69.4	+/- 30 %
100111 <sub>B</sub>	$I_{CHG39}$	72.3	+/- 30 %
101000 <sub>B</sub>	$I_{CHG40}$	75.2	+/- 30 %
101001 <sub>B</sub>	$I_{CHG41}$	78.1	+/- 30 %
101010 <sub>B</sub>	$I_{CHG42}$	81.1	+/- 30 %
101011 <sub>B</sub>	$I_{CHG43}$	84.1	+/- 30 %
101100 <sub>B</sub>	$I_{CHG44}$	87.1	+/- 30 %
101101 <sub>B</sub>	$I_{CHG45}$	90.2	+/- 30 %
101110 <sub>B</sub>	$I_{CHG46}$	93.3	+/- 30 %
101111 <sub>B</sub>	$I_{CHG47}$	96.4	+/- 30 %
110000 <sub>B</sub>	$I_{CHG48}$	99.5	+/- 30 %
110001 <sub>B</sub>	$I_{CHG49}$	102.7	+/- 30 %
110010 <sub>B</sub>	$I_{CHG50}$	105.8	+/- 30 %
110011 <sub>B</sub>	$I_{CHG51}$	109	+/- 30 %
110100 <sub>B</sub>	$I_{CHG52}$	112.2	+/- 30 %
110101 <sub>B</sub>	$I_{CHG53}$	115.4	+/- 30 %
110110 <sub>B</sub>	$I_{CHG54}$	118.7	+/- 30 %
110111 <sub>B</sub>	$I_{CHG55}$	122	+/- 30 %
111000 <sub>B</sub>	$I_{CHG56}$	125.3	+/- 30 %
111001 <sub>B</sub>	$I_{CHG57}$	128.7	+/- 30 %
111010 <sub>B</sub>	$I_{CHG58}$	132.1	+/- 30 %
111011 <sub>B</sub>	$I_{CHG59}$	135.5	+/- 30 %
111100 <sub>B</sub>	$I_{CHG60}$	139	+/- 30 %
111101 <sub>B</sub>	$I_{CHG61}$	142.5	+/- 30 %
111110 <sub>B</sub>	$I_{CHG62}$	146	+/- 30 %
111111 <sub>B</sub>	$I_{CHG63}$	150	+/- 30 %

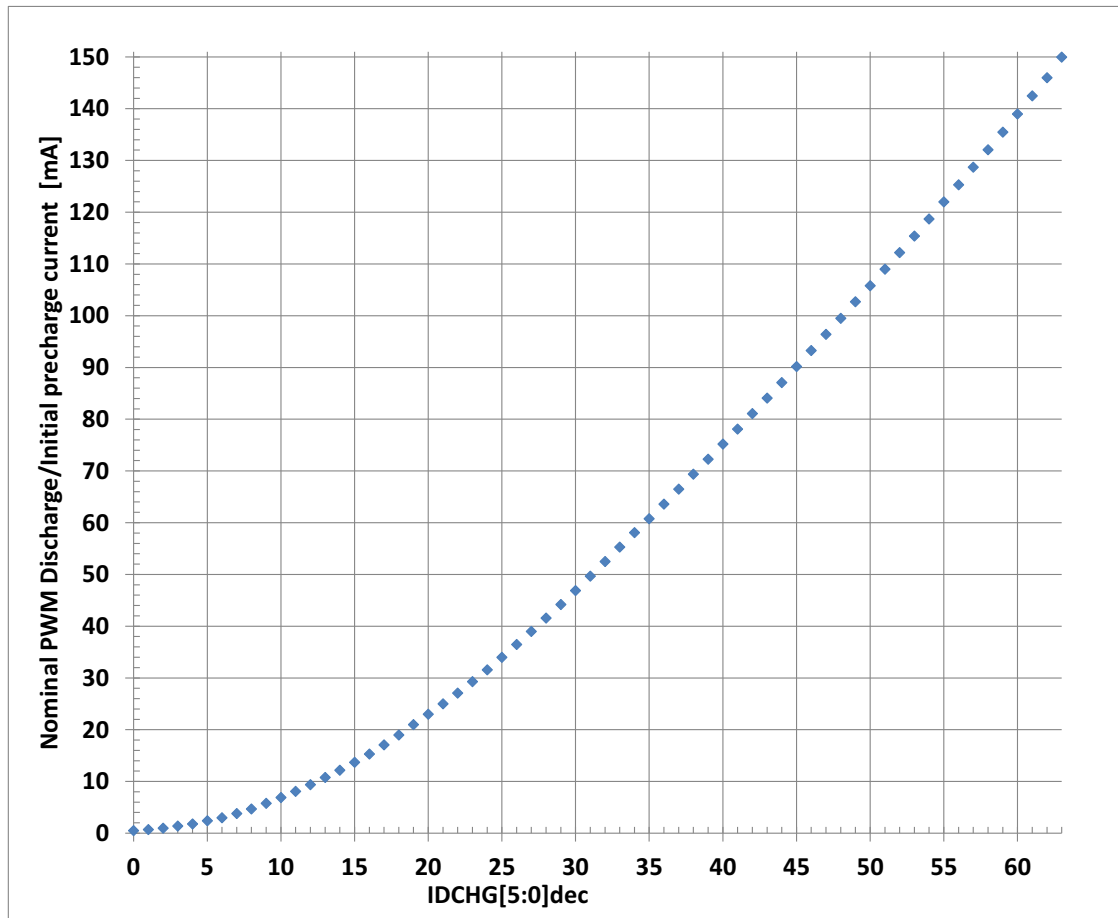


Figure 62 Configurable discharge currents in PWM operation

**Gate Drivers**

**Table 35 Discharge currents and initial predischage currents**

<b>IDCHG[5:0], PDCHGINITx[5:0]</b>	<b>Parameter name</b>	<b>Nom. current [mA]</b>	<b>Max. deviation to nominal values [%]</b>
000000 <sub>B</sub>	$I_{DCHG0}$	0.5	+/- 60%
000001 <sub>B</sub>	$I_{DCHG1}$	0.7	+/- 60 %
000010 <sub>B</sub>	$I_{DCHG2}$	1.0	+/- 60 %
000011 <sub>B</sub>	$I_{DCHG3}$	1.4	+/- 60 %
000100 <sub>B</sub>	$I_{DCHG4}$	1.8	+/- 60 %
000101 <sub>B</sub>	$I_{DCHG5}$	2.4	+/- 60 %
000110 <sub>B</sub>	$I_{DCHG6}$	3.0	+/- 60 %
000111 <sub>B</sub>	$I_{DCHG7}$	3.8	+/- 60 %
001000 <sub>B</sub>	$I_{DCHG8}$	4.7	+/- 60 %
001001 <sub>B</sub>	$I_{DCHG9}$	5.8	+/- 60 %
001010 <sub>B</sub>	$I_{DCHG10}$	6.9	+/- 60 %
001011 <sub>B</sub>	$I_{DCHG11}$	8.1	+/- 60 %
001100 <sub>B</sub>	$I_{DCHG12}$	9.4	+/- 60 %
001101 <sub>B</sub>	$I_{DCHG13}$	10.7	+/- 60 %
001110 <sub>B</sub>	$I_{DCHG14}$	12.1	+/- 40%
001111 <sub>B</sub>	$I_{DCHG15}$	13.5	+/- 40%
010000 <sub>B</sub>	$I_{DCHG16}$	15.1	+/- 40 %
010001 <sub>B</sub>	$I_{DCHG17}$	16.8	+/- 40 %
010010 <sub>B</sub>	$I_{DCHG18}$	18.6	+/- 40%
010011 <sub>B</sub>	$I_{DCHG19}$	20.5	+/- 40 %
010100 <sub>B</sub>	$I_{DCHG20}$	22.5	+/- 40%
010101 <sub>B</sub>	$I_{DCHG21}$	24.5	+/- 40 %
010110 <sub>B</sub>	$I_{DCHG22}$	26.5	+/- 40 %
010111 <sub>B</sub>	$I_{DCHG23}$	28.7	+/- 40 %
011000 <sub>B</sub>	$I_{DCHG24}$	30.9	+/- 40 %
011001 <sub>B</sub>	$I_{DCHG25}$	33.2	+/- 40 %
011010 <sub>B</sub>	$I_{DCHG26}$	35.7	+/- 40 %
011011 <sub>B</sub>	$I_{DCHG27}$	38.2	+/- 40 %
011100 <sub>B</sub>	$I_{DCHG28}$	40.8	+/- 40 %
011101 <sub>B</sub>	$I_{DCHG29}$	43.4	+/- 30 %
011110 <sub>B</sub>	$I_{DCHG30}$	46.1	+/- 30 %
011111 <sub>B</sub>	$I_{DCHG31}$	48.8	+/- 30 %
100000 <sub>B</sub>	$I_{DCHG32}$	51.5	+/- 30 %
100001 <sub>B</sub>	$I_{DCHG33}$	54.2	+/- 30 %
100010 <sub>B</sub>	$I_{DCHG34}$	56.9	+/- 30 %
100011 <sub>B</sub>	$I_{DCHG35}$	59.6	+/- 30 %

**Gate Drivers**

**Table 35** Discharge currents and initial predischage currents (cont'd)

IDCHG[5:0], PDCHGINITx[5:0]	Parameter name	Nom. current [mA]	Max. deviation to nominal values [%]
100100 <sub>B</sub>	$I_{DCHG36}$	62.4	+/- 30 %
100101 <sub>B</sub>	$I_{DCHG37}$	65.2	+/- 30 %
100110 <sub>B</sub>	$I_{DCHG38}$	68	+/- 30 %
100111 <sub>B</sub>	$I_{DCHG39}$	70.8	+/- 30 %
101000 <sub>B</sub>	$I_{DCHG40}$	73.7	+/- 30 %
101001 <sub>B</sub>	$I_{DCHG41}$	76.6	+/- 30 %
101010 <sub>B</sub>	$I_{DCHG42}$	79.5	+/- 30 %
101011 <sub>B</sub>	$I_{DCHG43}$	82.5	+/- 30 %
101100 <sub>B</sub>	$I_{DCHG44}$	85.5	+/- 30 %
101101 <sub>B</sub>	$I_{DCHG45}$	88.5	+/- 30 %
101110 <sub>B</sub>	$I_{DCHG46}$	91.5	+/- 30 %
101111 <sub>B</sub>	$I_{DCHG47}$	94.6	+/- 30 %
110000 <sub>B</sub>	$I_{DCHG48}$	97.7	+/- 30 %
110001 <sub>B</sub>	$I_{DCHG49}$	100.9	+/- 30 %
110010 <sub>B</sub>	$I_{DCHG50}$	104.2	+/- 30 %
110011 <sub>B</sub>	$I_{DCHG51}$	107.5	+/- 30 %
110100 <sub>B</sub>	$I_{DCHG52}$	110.8	+/- 30 %
110101 <sub>B</sub>	$I_{DCHG53}$	114.2	+/- 30 %
110110 <sub>B</sub>	$I_{DCHG54}$	117.6	+/- 30 %
110111 <sub>B</sub>	$I_{DCHG55}$	121	+/- 30 %
111000 <sub>B</sub>	$I_{DCHG56}$	124.5	+/- 30 %
111001 <sub>B</sub>	$I_{DCHG57}$	128	+/- 30 %
111010 <sub>B</sub>	$I_{DCHG58}$	131.5	+/- 30 %
111011 <sub>B</sub>	$I_{DCHG59}$	135.1	+/- 30 %
111100 <sub>B</sub>	$I_{DCHG60}$	138.7	+/- 30 %
111101 <sub>B</sub>	$I_{DCHG61}$	142.3	+/- 30 %
111110 <sub>B</sub>	$I_{DCHG62}$	145.8	+/- 30 %
111111 <sub>B</sub>	$I_{DCHG63}$	150	+/- 30 %

## 11.4 Passive discharge

Resistors ( $R_{GGND}$ ) between the gate of GHx and GND, and between GLx and GND, ensure that the external MOSFETs are turned off in the following conditions:

- $V_{CC1}$  undervoltage
- HBxMODE = 00<sub>B</sub> in Normal Mode
- **CPEN** = 0 in Normal Mode
- CSA Overcurrent detection with **OCEN** = 1 in normal mode

## Gate Drivers

- VS overvoltage or VSINT overvoltage
- Charge pump undervoltage and charge pump blank time ( $t_{CPUVBLANK}$ )
- Charge pump overtemperature (**CP\_OT**)
- VDS overvoltage after active discharge in Normal Mode
- In Init Mode, Stop Mode, Fail Safe Mode, Restart Mode and Sleep Mode (exceptions for low-sides in parking braking and VS / VSINT overvoltage braking, refer to **Chapter 11.6** and **Chapter 12.11.3**)

### 11.5 Slam mode

The slam mode is applicable in Normal Mode.

If the SLAM bit is set in **BRAKE** register:

1. If HBxMODE = 01b or 10b, then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then charge pump is deactivated independently from **CPEN**
3. Then PWM1/CRC input pin is mapped to LS1, LS2, LS3, independently from PWM\_NB, HBxMODE and HBx\_PWM\_EN
  - a) If PWM1/CRC is High, then the low-side MOSFETs are turned on within  $t_{ON\_BRAKE}$ .
  - b) If PWM1/CRC is Low, then the low-side MOSFETs are turned off within  $t_{OFF\_BRAKE}$ .

There is also the possibility to disable selectively the LSx in SLAM mode.

### 11.6 Parking braking mode

If **PARK\_BRK\_EN** bit is set, while the device goes in Sleep Mode or in Stop Mode:

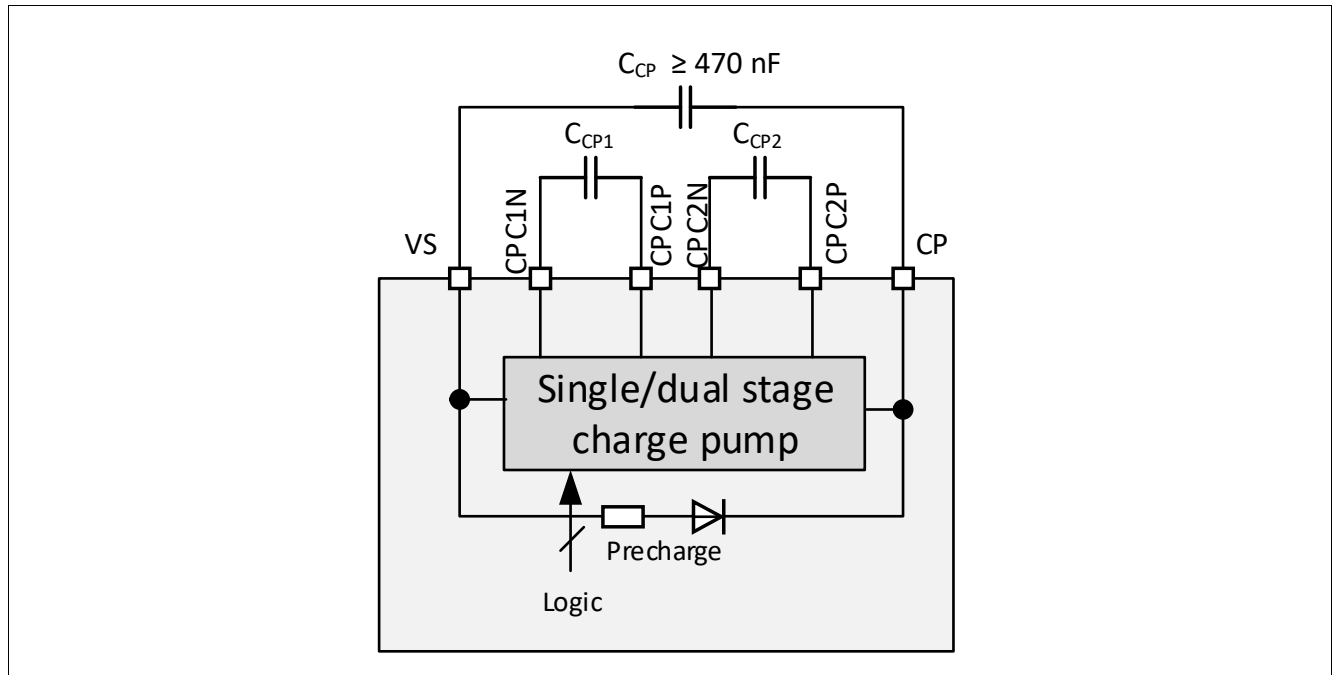
1. If HBxMODE = 01b or 10b, then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then charge pump is deactivated independently from CPEN bit.
3. Then the passive discharge ( $R_{GGND}$ ) of the low-sides is deactivated, the passive discharge of the high-sides are activated
4. If PWM1/CRC is High, then the low-side MOSFETs are turned on within  $t_{ON\_BRAKE}$ .

Refer to **Chapter 12.11.2** for the protection of the of low-side MOSFETs against short circuits when the parking braking mode is activated.

## 11.7 Charge pump

A dual-stage charge pump supplies the gate drivers for the high-side and low-side MOSFETs. It requires three external capacitors connected between CPC1N and CPC1P, CPC2N and CPC2P, VS and CP.

The buffer capacitor between VS and CP must have a capacitance equal or higher than 470 nF.



**Figure 63** Charge pump - Block diagram

### Logic or normal level MOSFETs

The regulation of the charge pump outputs voltage can be configured depending on the type of MOSFET.

**FET\_LVL = 0:** Logic level MOSFETs are selected:

- $V_{CP} - V_S = V_{CP3}$  (11 V typ. at  $V_S > 8$  V).
- The high-side gate-source voltage  $GHx - SHx$  is  $V_{GH4}$  ( $V_S > 8$  V).
- The low-side gate-source voltage  $GLx - SL$  is  $V_{GH3}$  ( $V_S > 8$  V).

**FET\_LVL = 1:** Normal level MOSFETs are selected:

- $V_{CP} - V_S = V_{CP1}$  (15 V typ. at  $V_S > 8$  V).
- The high-side and low-side gate-source voltage  $GHx - SHx$  or  $GLx - SL$  is  $V_{GH1}$  ( $V_S > 8$  V).

$CPSTGA = 0$  (default, see **GENCTRL**), the device operates with the dual-stage charge pump.

If  $CPSTGA = 1$ , the device switches to single-stage or dual-stage charge pump automatically:

- If  $V_S > V_{CPSO\ DS}$ : the TLE9563-3QX switches from a dual-stage to a single-stage charge pump.
- If  $V_S < V_{CPSO\ SD}$ : the TLE9563-3QX switches from single-stage to dual-stage charge pump.

The operation with the single-stage charge pump reduces the current consumption from the VS pin.

## **11.8 Frequency modulation**

A modulation of the charge pump frequency can be activated to reduce the peak emission.

The modulation frequency is set by the control bit FMODE in **GENCTRL**:

- FMODE = 0: No modulation.
- FMODE = 1: Modulation frequency = 15.6 kHz (default).

**Gate Drivers**

## 11.9 Electrical characteristics gate driver

The electrical characteristics related to the gate driver are valid for  $V_{CP} > V_S + 8.5 \text{ V}$

**Table 36 Electrical characteristics: gate drivers**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLx}$  and  $I_{GHx}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Comparators							
SHx High Threshold	$V_{SHH}$	$V_S - 2.6$	–	$V_S - 1.9$	V		P_12.11.1
SHx Low Threshold	$V_{SHL}$	1.9	–	2.6	V	Referred to GND	P_12.11.2
SHx comparator delay	$t_{SHx}$	–	12	30	ns	<sup>1)</sup>	P_12.11.3
MOSFET Driver Output							
High Level Output Voltage GHx vs. SHx and GLx vs. SL	$V_{GH1}$	10	11.5	12.5	V	<sup>2)</sup> $V_S \geq 8\text{ V}$ , $C_{Load} = 10\text{ nF}$ , $I_{CP} = -12\text{ mA}$ , $FET\_LVL = 1$	P_12.11.4
High Level Output Voltage GHx vs. SHx and GLx vs. SL	$V_{GH2}$	7	–	12.5	V	$V_S = 6\text{ V}$ , $C_{Load} = 10\text{ nF}$ , $I_{CP} = -6\text{ mA}$ , $FET\_LVL = 1$	P_12.11.5
High Level Output Voltage GLx vs. SL	$V_{GH3}$	10	–	12.5	V	<sup>3)</sup> $V_S \geq 6\text{ V}$ , $C_{Load} = 10\text{ nF}$ , $FET\_LVL = 0$	P_12.11.6
High Level Output Voltage GHx vs. SHx	$V_{GH4}$	8.5	10	12.5	V	<sup>2)</sup> $V_S \geq 8\text{ V}$ , $C_{Load} = 10\text{ nF}$ , $I_{CP} = -12\text{ mA}$ , $FET\_LVL = 0$	P_12.11.7
High Level Output Voltage GHx vs. SHx	$V_{GH5}$	7	–	12.5	V	$V_S = 6\text{ V}$ , $C_{LOAD} = 10\text{ nF}$ , $I_{CP} = -6\text{ mA}$ , $FET\_LVL = 0$	P_12.11.8
Charge current	$I_{CHG0}$	-60%	0.5	+60%	mA	$ICHG = 0_D$ <sup>1)</sup> $C_{Load} = 2.2\text{ nF}$ $V_S \geq 8V, V_{GS} \leq V_{GS(ON)}$ <sup>4)</sup>	P_12.11.70
Charge current	$I_{CHG8}$	-55%	4.7	+55%	mA	$ICHG = 8_D$ <sup>1)</sup> $C_{Load} = 2.2\text{ nF}$ $V_S \geq 8V, V_{GS} \leq V_{GS(ON)}$ <sup>4)</sup>	P_12.11.71
Charge current	$I_{CHG16}$	-40%	15.3	+40%	mA	$ICHG = 16_D$ <sup>1)</sup> $C_{Load} = 2.2\text{ nF}$ $V_S \geq 8V, V_{GS} \leq V_{GS(ON)}$ <sup>4)</sup>	P_12.11.72
Charge current	$I_{CHG32}$	-30%	52.5	+30%	mA	$ICHG = 32_D$ <sup>1)</sup> $C_{Load} = 10\text{ nF}$ $V_S \geq 8V, V_{GS} \leq V_{GS(ON)}$ <sup>4)</sup>	P_12.11.73



**Gate Drivers**

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLX}$  and  $I_{GHX}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge current	$I_{CHG48}$	-30%	99.5	+30%	mA	$ICHG = 48 \text{ D}^{1)}$ $C_{Load} = 10 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \leq V_{GS(ON)}^{4)}$	P_12.11.74
Charge current	$I_{CHG63}$	-30%	150	+30%	mA	$ICHG = 63 \text{ D}^{1)}$ $C_{Load} = 22 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \leq V_{GS(ON)}^{4)}$	P_12.11.75
Discharge current	$I_{DCH0}$	-60%	-0.5	+60%	mA	$IDCHG = 0 \text{ D}^{1)}$ $C_{Load} = 2.2 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF1)}$	P_12.11.76
Discharge current	$I_{DCH8}$	-55%	-4.7	55%	mA	$IDCHG = 8 \text{ D}^{1)}$ $C_{Load} = 2.2 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF1)}$	P_12.11.77
Discharge current	$I_{DCH16}$	-40%	-15.1	+40%	mA	$IDCHG = 16 \text{ D}^{1)}$ $C_{Load} = 2.2 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF1)}$	P_12.11.78
Discharge current	$I_{DCH32}$	-30%	-51.5	+30%	mA	$IDCHG = 32 \text{ D}^{1)}$ $C_{Load} = 10 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF2)}$	P_12.11.79
Discharge current	$I_{DCH48}$	-30%	-97.7	+30%	mA	$IDCHG = 48 \text{ D}^{1)}$ $C_{Load} = 10 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF2)}$	P_12.11.80
Discharge current	$I_{DCH63}$	-30%	-150	+30%	mA	$IDCHG = 63 \text{ D}^{1)}$ $C_{Load} = 22 \text{ nF}$ $V_S \geq 8 \text{ V}$ , $V_{GS} \geq V_{GS(OFF2)}$	P_12.11.81
Charge current temperature drift	$I_{CHG0,TDrift}$	-37%	-12%	15%		$ICHG = 0 \text{ D}^{1)5)}$	P_12.11.119
Charge current temperature drift	$I_{CHG8,TDrift}$	-17%	1%	20%		$ICHG = 8 \text{ D}^{1)5)}$	P_12.11.120
Charge current temperature drift	$I_{CHG16,TDrift}$	-12%	3%	18%		$ICHG = 16 \text{ D}^{1)5)}$	P_12.11.121
Charge current temperature drift	$I_{CHG32,TDrift}$	-11%	-1%	9%		$ICHG = 32 \text{ D}^{1)5)}$	P_12.11.122
Charge current temperature drift	$I_{CHG48,TDrift}$	-7.5%	0.5%	8%		$ICHG = 48 \text{ D}^{1)5)}$	P_12.11.123
Charge current temperature drift	$I_{CHG63,TDrift}$	-5.5%	1.5%	8.5%		$IDCHG = 63 \text{ D}^{1)5)}$	P_12.11.124
Discharge current temperature drift	$I_{DCHG0,TDrift}$	-29%	-4.5%	20%		$IDCHG = 0 \text{ D}^{1)5)}$	P_12.11.125

**Gate Drivers**

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLx}$  and  $I_{GHx}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Discharge current temperature drift	$I_{DCHG8,TDrift}$	-8%	8.5%	26%		IDCHG = $8_D^{1)5)}$	P_12.11.126
Discharge current temperature drift	$I_{DCHG16,TDrift}$	-4%	9.5%	23%		IDCHG = $16_D^{1)5)}$	P_12.11.127
Discharge current temperature drift	$I_{DCHG32,TDrift}$	-4%	4.5%	13%		IDCHG = $32_D^{1)5)}$	P_12.11.128
Discharge current temperature drift	$I_{DCHG48,TDrift}$	-4%	3.5%	10%		IDCHG = $48_D^{1)5)}$	P_12.11.129
Discharge current temperature drift	$I_{DCHG63,TDrift}$	-3.5%	3.5%	9.5%		IDCHG = $63_D^{1)5)}$	P_12.11.130
Charge current $V_S$ drift	$I_{CHG0,VsDrift}$	3%	4.5%	6%		ICHG = $0_D^{1)6)}$	P_12.11.131
Charge current $V_S$ drift	$I_{CHG8,VsDrift}$	4.5%	6%	7.5%		ICHG = $8_D^{1)6)}$	P_12.11.132
Charge current $V_S$ drift	$I_{CHG16,VsDrift}$	4%	5.8%	7.5%		ICHG = $16_D^{1)6)}$	P_12.11.133
Charge current $V_S$ drift	$I_{CHG32,VsDrift}$	2%	3.8%	5.8%		ICHG = $32_D^{1)6)}$	P_12.11.134
Charge current $V_S$ drift	$I_{CHG48,VsDrift}$	-0.5%	2%	4.5%		ICHG = $48_D^{1)6)}$	P_12.11.135
Charge current $V_S$ drift	$I_{CHG63,VsDrift}$	-2.3%	0.3%	2.8%		ICHG = $63_D^{1)6)}$	P_12.11.136
Discharge current $V_S$ drift	$I_{DCHG0,VsDrift}$	-3%	-1.5%	0%		IDCHG = $0_D^{1)6)}$	P_12.11.137
Discharge current $V_S$ drift	$I_{DCHG8,VsDrift}$	-3%	-0.5%	2%		IDCHG = $8_D^{1)6)}$	P_12.11.138
Discharge current $V_S$ drift	$I_{DCHG16,VsDrift}$	-3.3%	-0.3%	2.3%		IDCHG = $16_D^{1)6)}$	P_12.11.139
Discharge current $V_S$ drift	$I_{DCHG32,VsDrift}$	-2%	0%	2%		IDCHG = $32_D^{1)6)}$	P_12.11.140
Discharge current $V_S$ drift	$I_{DCHG48,VsDrift}$	-1.5%	0%	1.5%		IDCHG = $48_D^{1)6)}$	P_12.11.141
Discharge current $V_S$ drift	$I_{DCHG63,VsDrift}$	-1.5%	0.2%	1.5%		IDCHG = $63_D^{1)6)}$	P_12.11.142
Passive discharge resistance between GHx/GLx and GND	$R_{GGND}$	10	20	30	k $\Omega$	<sup>1)</sup>	P_12.11.22
Resistor between SHx and GND	$R_{SHGND}$	10	20	30	k $\Omega$	<sup>1)7)</sup>	P_12.11.23
Low RDSON mode	$R_{ONCCP}$	–	22	35	$\Omega$	<sup>1)</sup> $V_S = 13.5 \text{ V}$ $V_{CP} = V_S + 14 \text{ V}$  $I_{CHG} = I_{DCHG} = 63_D$	P_12.11.24

**Gate Drivers Dynamic Parameters**

**Gate Drivers**

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLx}$  and  $I_{GHx}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Gate Driver turn-on delay Time	$t_{DGDRV\_ON1}$	–	–	400	ns	<sup>8)</sup> From PWM <sup>9)</sup> rising edge to 20% of $I_{CHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$ , <b>BDFREQ</b> = 0	P_12.11.25
Gate Driver turn-on delay Time	$t_{DGDRV\_ON2}$	–	–	300	ns	<sup>8)</sup> From PWM <sup>9)</sup> rising edge to 20% of $I_{CHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$ , <b>BDFREQ</b> = 1	P_12.11.93
Gate Driver current turn-on rise time	$t_{GDRV\_RISE(ON)}$	–	30	50	ns	<sup>8)</sup> From 20% of $I_{CHGx}$ to $I_{CHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$	P_12.11.26
Gate Driver turn-off delay Time	$t_{DGDRV\_OFF1}$	–	–	400	ns	<sup>8)</sup> From PWM <sup>9)</sup> rising edge to 20% of $I_{DCHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$ , <b>BDFREQ</b> = 0	P_12.11.27
Gate Driver turn-off delay Time	$t_{DGDRV\_OFF2}$	–	–	300	ns	<sup>8)</sup> From PWM <sup>9)</sup> rising edge to 20% of $I_{DCHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$ , <b>BDFREQ</b> = 1	P_12.11.94
Gate Driver current turn-off rise time	$t_{GDRV\_RISE(OFF)}$	–	30	50	ns	<sup>8)</sup> From 20% of $I_{DCHGx}$ to $I_{DCHGx}$ , $x = 0 \text{ to } 63$ , $C_{Load} = 10 \text{ nF}$	P_12.11.28
External MOSFET gate-to-source voltage - ON	$V_{GS(ON)1}$	7	–	–	V	<sup>1)</sup> $V_S \geq 8 \text{ V}$ , <b>FET_LVL</b> = 1	P_12.11.29
External MOSFET gate-to-source voltage - ON	$V_{GS(ON)1}$	7	–	–	V	<sup>1)</sup> $V_S \geq 8 \text{ V}$ , <b>FET_LVL</b> = 1	P_12.11.102
External MOSFET gate-to-source voltage - ON	$V_{GS(ON)2}$	5.5	–	–	V	<sup>1)</sup> $V_S \geq 8 \text{ V}$ , <b>FET_LVL</b> = 0	P_12.11.103
External MOSFET gate-to-source voltage - OFF	$V_{GS(OFF)1}$	–	–	1.5	V	<sup>1)</sup> $IDCHGx \leq 24_D (\leq 41 \text{ mA typ.})$	P_12.11.30

**Gate Drivers**

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLX}$  and  $I_{GHX}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External MOSFET gate-to-source voltage - OFF	$V_{GS(OFF)2}$	–	–	5	V	<sup>1)</sup> $IDCHGx > 28_D(> 41 \text{ mA typ.})$	P_12.11.101
PWM synchronization delay	$t_{PWM\_SYNCH0}$	80	–	200	ns	<sup>1)</sup> <b>BDFREQ</b> = 0	P_12.11.33
PWM synchronization delay	$t_{PWM\_SYNCH1}$	40	–	100	ns	<sup>1)</sup> <b>BDFREQ</b> = 1	P_12.11.82
Bridge driver frequency	$t_{BDFREQ0}$	16.8	18.75	20.7	MHz	<sup>1)</sup> <b>BDFREQ</b> = 0	P_12.11.83
Bridge driver frequency	$t_{BDFREQ1}$	33.7	37.5	42.3	MHz	<sup>1)</sup> <b>BDFREQ</b> = 1	P_12.11.84
Pre-charge time	$t_{PCHG000}$	80	107	140	ns	<sup>1)</sup> $TPCHG = 000$ , <b>BDFREQ</b> = 0 or 1	P_12.11.34
Pre-charge time	$t_{PCHG001}$	130	160	190	ns	<sup>1)</sup> $TPCHG = 001$ , <b>BDFREQ</b> = 0 or 1	P_12.11.35
Pre-charge time	$t_{PCHG010}$	170	214	260	ns	<sup>1)</sup> $TPCHG = 010$ , <b>BDFREQ</b> = 0 or 1	P_12.11.36
Pre-charge time	$t_{PCHG011}$	210	267	330	ns	<sup>1)</sup> $TPCHG = 011$ , <b>BDFREQ</b> = 0 or 1	P_12.11.37
Pre-charge time	$t_{PCHG100}$	250	320	390	ns	<sup>1)</sup> $TPCHG = 100$ , <b>BDFREQ</b> = 0 or 1	P_12.11.85
Pre-charge time	$t_{PCHG101}$	420	533	630	ns	<sup>1)</sup> $TPCHG = 101$ , <b>BDFREQ</b> = 0 or 1	P_12.11.86
Pre-charge time	$t_{PCHG110}$	600	747	900	ns	<sup>1)</sup> $TPCHG = 110$ , <b>BDFREQ</b> = 0 or 1	P_12.11.87
Pre-charge time	$t_{PCHG111}$	840	1067	1260	ns	<sup>1)</sup> $TPCHG = 111$ , <b>BDFREQ</b> = 0 or 1	P_12.11.88
Pre-discharge time	$t_{PDCHG000}$	80	107	140	ns	<sup>1)</sup> $TPDCHG = 000$ , <b>BDFREQ</b> = 0 or 1	P_12.11.38
Pre-discharge time	$t_{PDCHG001}$	130	160	190	ns	<sup>1)</sup> $TPDCHG = 001$ , <b>BDFREQ</b> = 0 or 1	P_12.11.39
Pre-discharge time	$t_{PDCHG010}$	170	214	260	ns	<sup>1)</sup> $TPDCHG = 010$ , <b>BDFREQ</b> = 0 or 1	P_12.11.40
Pre-discharge time	$t_{PDCHG011}$	210	267	330	ns	<sup>1)</sup> $TPDCHG = 011$ , <b>BDFREQ</b> = 0 or 1	P_12.11.41
Pre-discharge time	$t_{PDCHG100}$	250	320	390	ns	<sup>1)</sup> $TPDCHG = 100$ , <b>BDFREQ</b> = 0 or 1	P_12.11.89
Pre-discharge time	$t_{PDCHG101}$	420	533	630	ns	<sup>1)</sup> $TPDCHG = 101$ , <b>BDFREQ</b> = 0 or 1	P_12.11.90
Pre-discharge time	$t_{PDCHG110}$	600	747	900	ns	<sup>1)</sup> $TPDCHG = 110$ , <b>BDFREQ</b> = 0 or 1	P_12.11.91

## Gate Drivers

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLX}$  and  $I_{GHX}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pre-discharge time	$t_{PDCHG111}$	840	1067	1260	ns	<sup>1)</sup> TPDCHG = 111, BDFREQ = 0 or 1	P_12.11.92
Discharge timeout	$t_{OFF\_TIMEOUT}$	3.2	4	4.8	μs	<sup>1)</sup> PWM_NB=1 <sub>B</sub>	P_12.11.9

### Low-side gate driver, CP off - Slam mode, parking braking and VS overvoltage braking

LS turn-on time, CP off	$t_{ON\_BRAKE}$	–	4.5	9	μs	$C_{LOAD} = 10 \text{ nF}$ $V_{GLX-VSL} = 5 \text{ V}$ , $V_S > 8 \text{ V}$ or $V_{SINT} > 8 \text{ V}$	P_12.11.42
LS turn-off time, CP off	$t_{OFF\_BRAKE}$	–	0.7	2	μs	$C_{LOAD} = 10 \text{ nF}$ $V_{GLX-VSL} = 1.5 \text{ V}$ , $V_S > 8 \text{ V}$ or $V_{SINT} > 8 \text{ V}$	P_12.11.43
High output voltage GLX - SL	$V_{GLX\_BRAKE}$	5	–	10	V	$V_S > 8 \text{ V}$ or $V_{SINT} > 8 \text{ V}$	P_12.11.48

### Charge pump

Charge Pump Frequency	$f_{CP}$	–	250	–	kHz	<sup>1)</sup>	P_12.11.49
Output Voltage VCP vs. VS	$V_{CPmin1}$	8.5	–	–	V	$V_S = 6 \text{ V}$ , $I_{CP} = -6 \text{ mA}$ , FET_LVL = 1	P_12.11.50
Output Voltage VCP vs. VS	$V_{CPmin2}$	7.5	–	–	V	$V_S = 6 \text{ V}$ , $I_{CP} = -6 \text{ mA}$ , FET_LVL = 0	P_12.11.51
Regulated CP output voltage, VCP vs. VS	$V_{CP1}$	12	15	17	V	$8 \text{ V} < V_S < 23 \text{ V}$ $I_{CP} = -12 \text{ mA}^{(1)}$ , CPSTGA = 0, FET_LVL = 1	P_12.11.52
Regulated CP output voltage, VCP vs. VS	$V_{CP2}$	12	15	17	V	$18 \text{ V} < V_S < 23 \text{ V}$ $I_{CP} = -12 \text{ mA}^{(1)}$ , CPSTGA = 1, FET_LVL = 1	P_12.11.53
Regulated CP output voltage, VCP vs. VS	$V_{CP3}$	7.5	11	13	V	$8 \text{ V} < V_S < 23 \text{ V}$ $I_{CP} = -12 \text{ mA}^{(1)}$ , CPSTGA = 0, FET_LVL = 0	P_12.11.54
Regulated CP output voltage, VCP vs. VS	$V_{CP4}$	7.5	11	13	V	$13 \text{ V} < V_S < 23 \text{ V}$ $I_{CP} = -12 \text{ mA}^{(1)}$ , CPSTGA = 0, FET_LVL = 0	P_12.11.55
Turn-on time	$t_{ON\_VCP1}$	5	–	60	μs	<sup>1)10)11)</sup> $18 \text{ V} < V_S < 23 \text{ V}$ (25%), $I_{CP} = 0$ , CPSTGA = 1, FET_LVL = 1	P_12.11.56

**Gate Drivers**

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLX}$  and  $I_{GHX}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Rise time	$t_{RISE\_VCP1}$	5	30	60	$\mu\text{s}$	<sup>1)10)11)</sup> $18 \text{ V} < V_S < 23 \text{ V}$ (25%-75%) $I_{CP} = 0$ , CPSTGA = 1, FET_LVL = 1	P_12.11.57
Turn-on time	$t_{ON\_VCP2}$	20	60	120	$\mu\text{s}$	<sup>1)10)11)</sup> $13 \text{ V} < V_S < 23 \text{ V}$ (25%), $I_{CP} = 0$ , CPSTGA = 1, FET_LVL = 0	P_12.11.58
Rise time	$t_{RISE\_VCP2}$	5	30	60	$\mu\text{s}$	<sup>1)10)11)</sup> $13 \text{ V} < V_S < 23 \text{ V}$ (25%-75%) $I_{CP} = 0$ , CPSTGA = 1, FET_LVL = 0	P_12.11.59
Automatic switch over dual to single stage charge pump	$V_{CPSO\_DS}$	16	17	18	V	CPSTGA = 1, FET_LVL = 1, VS rising	P_12.11.60
Automatic switch over dual to single stage charge pump	$V_{CPSO\_DS}$	11.5	12.25	13	V	CPSTGA = 1, FET_LVL = 0, VS rising	P_12.11.61
Automatic switch over single to dual stage charge pump	$V_{CPSO\_SD}$	15.5	16.5	17.5	V	CPSTGA = 1, FET_LVL = 1, VS falling	P_12.11.62
Automatic switch over single to dual stage charge pump	$V_{CPSO\_SD}$	11	11.75	12.5	V	CPSTGA = 1, FET_LVL = 0, VS falling	P_12.11.64
Charge pump switch over hysteresis	$V_{CPSO\_HY}$	–	0.5	–	V	<sup>1)</sup> CPSTGA = 1 $V_{CPSO\_DS} - V_{CPSO\_SD}$	P_12.11.65
Charge pump minimum output current	$I_{CPOC1}$	–	–	-12	mA	<sup>11)</sup> $8 \text{ V} < V_S < 28 \text{ V}$ CPSTGA = 0 FET_LVL = 1	P_12.11.68
Charge pump minimum output current	$I_{CPOC2}$	–	–	-12	mA	<sup>11)</sup> $8 \text{ V} < V_S < 28 \text{ V}$ CPSTGA = 0 FET_LVL = 0	P_12.11.69

## Gate Drivers

**Table 36 Electrical characteristics: gate drivers (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,

$V_{CP} > V_S + 8.5 \text{ V}$ ,  $V_S = 6 \text{ to } 19 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin except for  $I_{GLx}$  and  $I_{GHx}$  (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital PWMx Inputs							
High Level Input Voltage Threshold	$V_{PWHH}$	–	–	$0.7 \times V_{CC1}$	V	–	P_12.11.95
Low Level Input Voltage Threshold	$V_{PWML}$	$0.3 \times V_{CC1}$	–	–	V	–	P_12.11.96
PWMx Input Hysteresis	$V_{PWM,hys}$	–	$0.12 \times V_{CC1}$	–	V	1)	P_12.11.97
PWMx Pull-down Resistance	$R_{PD\_PWM}$	20	40	80	kΩ	–	P_12.11.98
CRC Select; Pin PWM1/CRC							
Config Pull-up Resistance	$R_{CFG}$		100		kΩ	12)	P_12.11.99
Config Select Filter Time	$t_{CFG\_F}$	5	10	14	μs	1)	P_12.11.105

1) Not subject to production test, specified by design.

2) Independent from **CPSTGA**.

3)  $ICP = -12 \text{ mA}$  for  $V_S \geq 8 \text{ V}$ ,  $ICP = 6 \text{ mA}$  for  $V_S = 6 \text{ V}$ .

4)  $V_{GS(ON)} = V_{GS(ON)1}$  if **FET\_LVL** = 1,  $V_{GS(ON)} = V_{GS(ON)2}$  if **FET\_LVL** = 0.

5)  $T_j$  reference =  $25^\circ\text{C}$

6) Valid for  $V_S = 8 \text{ to } 19 \text{ V}$ ,  $V_S$  reference =  $13.5 \text{ V}$

7) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to  $0.6 \text{ V typ.}$  before it is discharged through the resistor.

8) Not subject to production test, specified by design.

9) External PWM signal.

10) Parameter dependent on the capacitance  $C_{CP}$ .

11)  $C_{CPC1} = C_{CPC2} = 220 \text{ nF}$ ,  $C_{CP} = 470 \text{ nF}$ . Other  $C_{CP}$  values higher than  $470 \text{ nF}$  can be used. Note that this capacitor influences the charge pump rise and turn-on times, and the charge,  $V_{CP}$  ripple voltage when charging the gate of a MOSFET.

12) Config Pull-up will be only active during startup-phase for checking external pull-down. After checking, the typ.  $40 \text{ k}\Omega$  Pull-down resistance will be present.

## 12 Supervision Functions

### 12.1 Reset Function

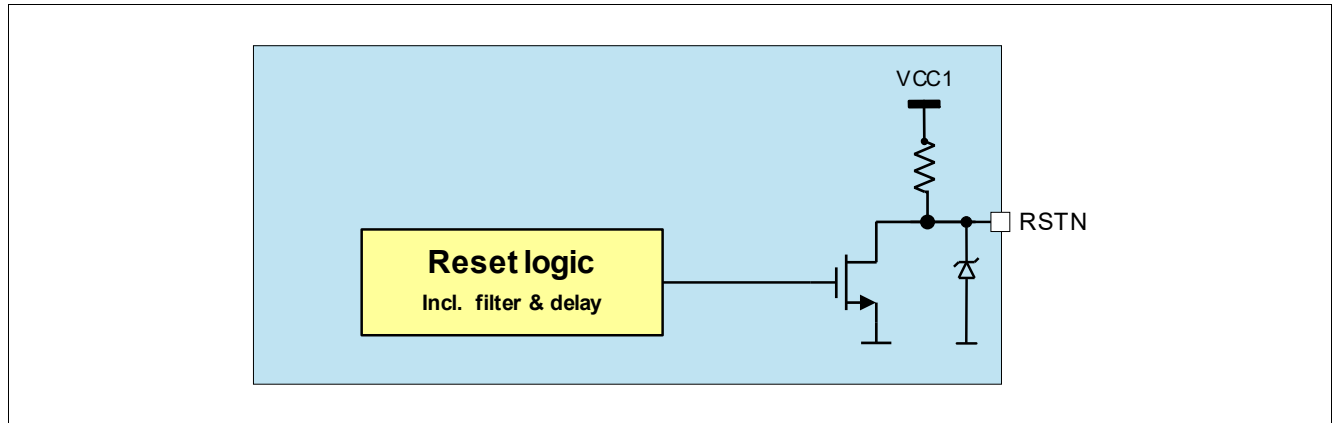


Figure 64 Reset Block Diagram

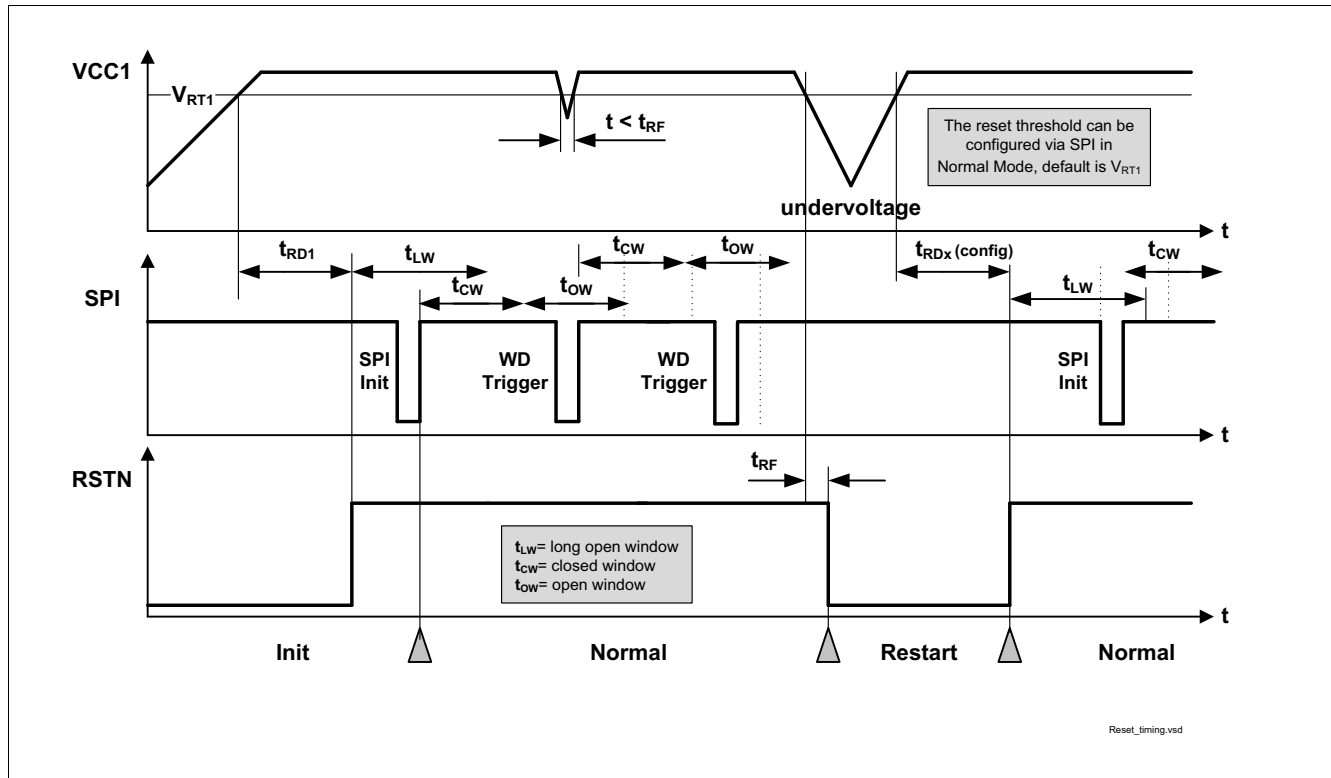
#### 12.1.1 Reset Output Description

The reset output pin RSTN provides a reset information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold  $V_{RTX}$ . In case of a reset event, the reset output RSTN is pulled to low after the filter time  $t_{RF}$  and stays low as long as the reset event is present plus a reset delay time  $t_{RD1}$  or  $t_{RD2}$  depending on the value in **RSTN\_DEL**. When connecting the device to battery voltage, the reset signal remains low initially. When the output voltage VCC1 has reached the reset default threshold  $V_{RT1,f}$ , the reset output RSTN is released to high after the reset delay time  $t_{RD1}$ . A reset can also occur due to a watchdog trigger failure. The reset threshold can be adjusted via SPI, the default reset threshold is  $V_{RT1,f}$ . The RSTN pin has an integrated pull-up resistor. In case reset is triggered, it will be pulled low for  $VCC1 \geq 1V$  and for  $VSINT \geq V_{POR,f}$  (see also **Chapter 12.3**).

The timings for the RSTN triggering regarding VCC1 undervoltage and watchdog trigger is shown in **Figure 65**.



## Supervision Functions



**Figure 65** Reset Timing Diagram

### 12.1.2 Soft Reset Description

In Normal Mode and Stop Mode, it is also possible to trigger a device internal reset via a SPI command in order to bring the device into a defined state in case of failures. In this case the microcontroller must send a SPI command and set the **MODE** bits to '11' in the **M\_S\_CTRL** register. As soon as this command becomes valid, the device is set back to Init Mode and all SPI registers are set to their default values (see SPI [Chapter 13.5.1](#) and [Chapter 13.6.1](#)).

Two different soft reset configurations are possible via the SPI bit **SOFT\_RESET\_RO**:

- **SOFT\_RESET\_RO** = '0': The reset output (RSTN) is triggered when the soft reset is executed (default setting) The configured reset delay time **t\_RD1** or **t\_RD2** is applied depending on the value in **RSTN\_DEL**.
- **SOFT\_RESET\_RO** = '1': The reset output (RSTN) is not triggered when the soft reset is executed.

*Note:* The device must be in Normal Mode or Stop Mode when sending this command. Otherwise, the command will be ignored.

*Note:* Allow CRC configuration after software-reset - or better check once again via SPI after software reset.

## Supervision Functions

### 12.2 Watchdog Function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset or move the device to Fail Safe Mode, if the microcontroller stops serving the watchdog due to a lock up in the software.

Two different types of watchdog functions are implemented and can be selected via the bit **WD\_CFG**:

- Time-Out Watchdog (default value)
- Window Watchdog

The respective watchdog functions can be selected and programmed in Normal Mode. The configuration stays unchanged in Stop Mode.

Please refer to **Table 37** to match the device modes with the respective watchdog modes.

**Table 37 Watchdog Functionality by modes**

Mode	Watchdog Mode	Remarks
Init Mode	Starts with Long Open Window	Watchdog starts with Long Open Window after RSTN is released.
Normal Mode	WD Programmable	Window Watchdog, Time-Out watchdog or switched off for Stop Mode.
Stop Mode	Watchdog is fixed or off	
Sleep Mode	Off	Device will start with Long Open Window when entering Normal Mode.
Restart Mode	Off	Device will start with Long Open Window when entering Normal Mode.

The watchdog timing is programmed via SPI command in the register **WD\_CTRL**. As soon as the watchdog is programmed, the timer starts with the new setting and the watchdog must be served. The watchdog is triggered by sending a valid SPI-write command to the watchdog configuration register. The watchdog trigger command is executed when the SPI command is interpreted.

When coming from Init Mode, Restart Mode or in certain cases from Stop Mode, the watchdog timer is always started with a long open window. The long open window ( $t_{LW}$ ) allows the microcontroller to run its initialization sequences and then to trigger the watchdog via SPI.

The watchdog timer period can be selected via SPI (**WD\_TIMER**). The timer setting is valid for both watchdog types.

The following watchdog timer periods are available:

- WD Setting 1: 10 ms
- WD Setting 2: 20 ms
- WD Setting 3: 50 ms
- WD Setting 4: 100 ms
- WD Setting 5: 200 ms
- WD Setting 6: 500 ms
- WD Setting 7: 1 s
- WD Setting 8: 10 s

In case of a reset, Restart Mode or Fail-Safe Mode is entered according to the configuration and the SPI bits **WD\_FAIL** are set. Once the RSTN goes high again the watchdog immediately starts with a long open window the device enters automatically Normal Mode.

The Watchdog behaviour in Software Development Mode is described in **Chapter 5.4.7**.

## Supervision Functions

In case a watchdog-trigger was missed in Software Development Mode, the watchdog will start with the long-open-window once again.

The **WD\_FAIL** bits will be set after a watchdog trigger failure.

The **WD\_FAIL** bits are cleared automatically when following conditions apply:

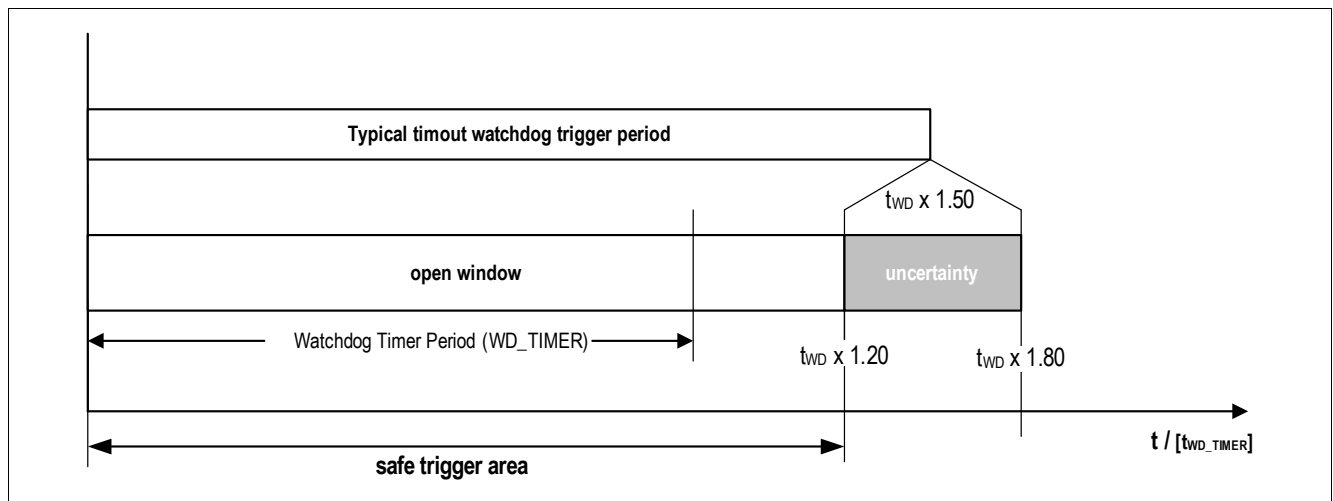
- After a successful watchdog trigger.
- When the watchdog is off: in Stop Mode after successfully disabling it, in Sleep Mode, or in Fail-Safe Mode (except for a watchdog failure).

### 12.2.1 Time-Out Watchdog

The time-out watchdog is an easier and less secure watchdog than a window watchdog as the watchdog trigger can be done at any time within the configured watchdog timer period.

A correct watchdog service immediately results in starting a new watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the safe trigger area as defined in **Figure 66**.

If the time-out watchdog period elapses, a watchdog reset is created by setting the reset output RSTN low and the device switches to Restart Mode or Fail-Safe Mode.



**Figure 66 Time-out Watchdog Definitions**

### 12.2.2 Window Watchdog

Compared to the time-out watchdog the characteristic of the window watchdog is that the watchdog timer period is divided between a closed and an open window. The watchdog must be triggered within the open window.

A correct watchdog trigger results in starting the window watchdog period by a closed window followed by an open window.

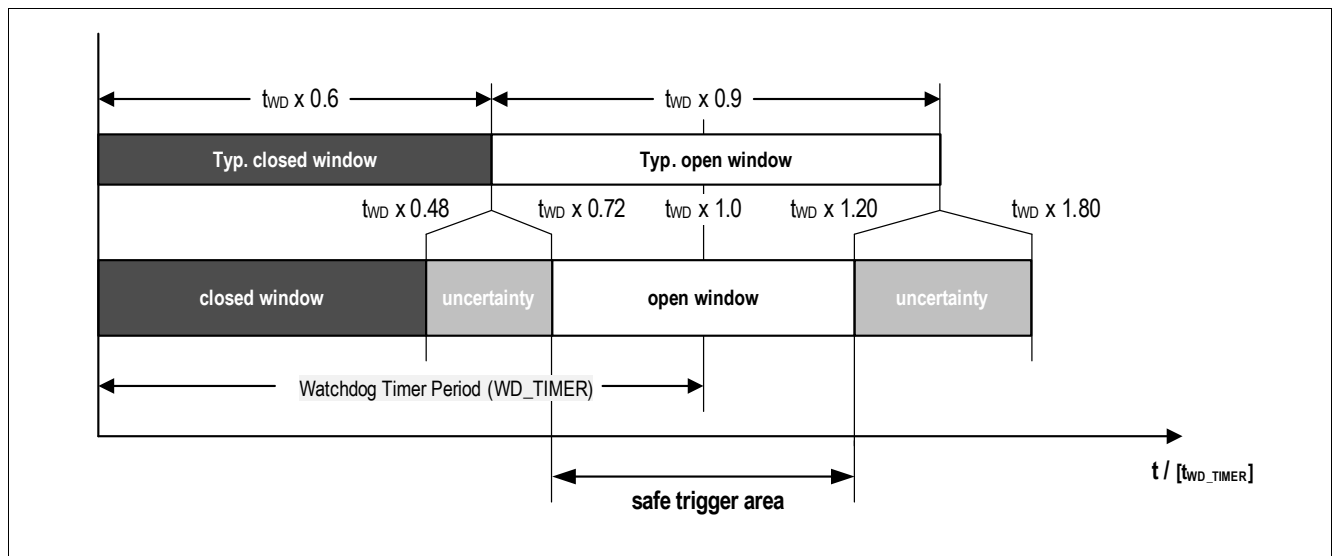
The watchdog timer period is at the same time the typical trigger time and defines the middle of the open window. Taking the oscillator tolerances into account leads to a safe trigger area of:

$$t_{WD} \times 0.72 < \text{safe trigger area} < t_{WD} \times 1.20.$$

The typical closed window is defined to a width of 60% of the selected window watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the timings as defined in **Figure 67**.

A correct watchdog service immediately results in starting the next closed window.

If the trigger signal meet the closed window or if the watchdog timer period elapses, then a watchdog reset is triggered (RSTN low) and the device switches to Restart Mode or Fail-Safe Mode.



**Figure 67 Window Watchdog Definitions**

### 12.2.3 Watchdog Setting Check Sum

A check sum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting.

The sum of the 16 data bits in the register **WD\_CTRL** needs to have even parity (see **Equation (12.1)**). This is realized by either setting the bit **CHECKSUM** to 0 or 1. If the check sum is wrong, then the SPI command is ignored, i.e. the watchdog is not triggered or the settings are not changed and the bit **SPI\_FAIL** is set.

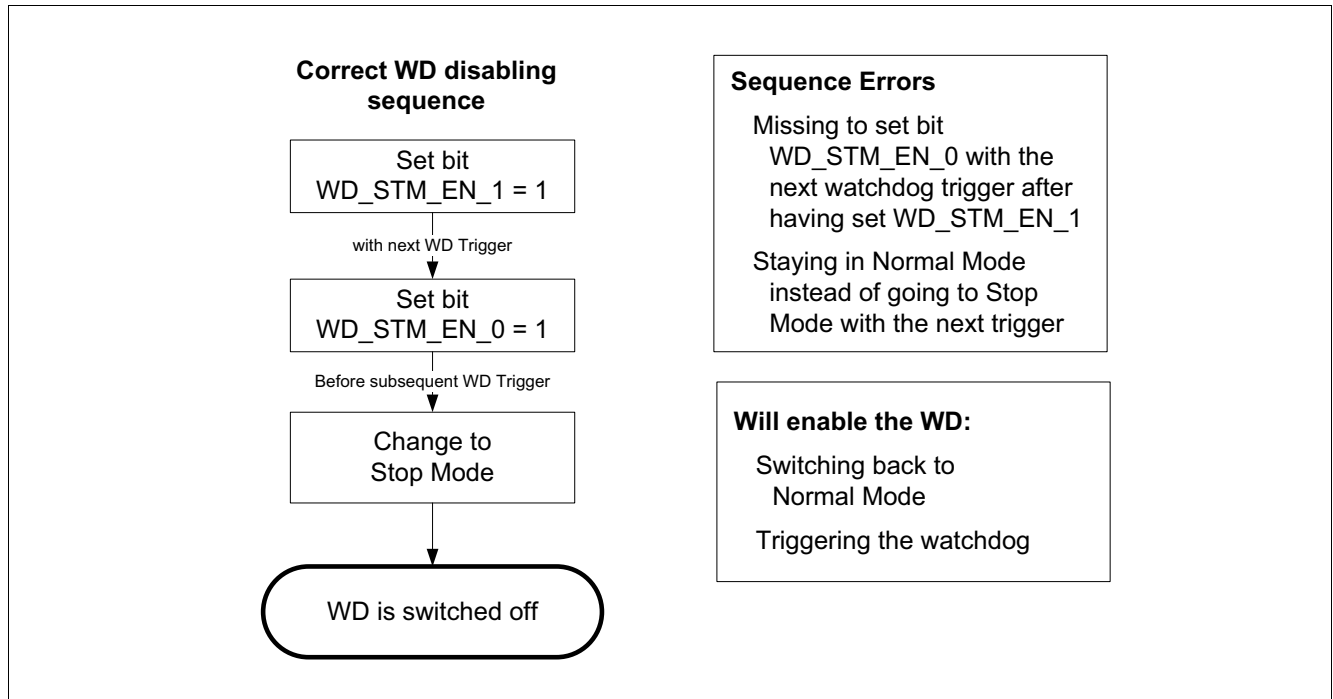
The written value of the reserved bits of the **WD\_CTRL** register is considered (even if read as '0' in the SPI output) for checksum calculation, i.e. if a 1 is written on the reserved bit position, then a 1 will be used in the checksum calculation.

(12.1)

$$\text{Bit}(\text{CHECKSUM}) = \text{Bit}22 \oplus \dots \oplus \text{Bit}8$$

### 12.2.4 Watchdog during Stop Mode

The watchdog can be disabled for Stop Mode in Normal Mode. For safety reasons, there is a special sequence to be followed in order to disable the watchdog as described in [Figure 68](#). Two different SPI bits (**WD\_STM\_EN\_0**, **WD\_STM\_EN\_1**) in the registers **HW\_CTRL** and **WD\_CTRL** need to be set.



**Figure 68 Watchdog disabling sequence in Stop Mode**

If a sequence error occurs, then the bit **WD\_STM\_EN\_1** will be cleared and the sequence has to be started again.

The watchdog can be enabled by triggering the watchdog in Stop Mode or by switching back to Normal Mode via SPI command. In both cases the watchdog will start with a long open window and the bits **WD\_STM\_EN\_1** and **WD\_STM\_EN\_0** are cleared. After the long open window the watchdog has to be served as configured in the **WD\_CTRL** register.

*Note: The bit **WD\_STM\_EN\_0** will be cleared automatically when the sequence is started and it was 1 before. **WD\_STM\_EN\_0** can also not be set if **WD\_STM\_EN\_1** isn't yet set.*

### 12.2.5 Watchdog Start in Stop Mode due to Bus Wake

In Stop Mode the Watchdog can be disabled. In addition a feature is available which will start the watchdog with any BUS wake (CAN, ) during Stop Mode. The feature is enabled by setting the bit **WD\_EN\_WK\_BUS** = 1 (default value after POR). The bit can only be changed in Normal Mode and needs to be programmed before starting the watchdog disable sequence.

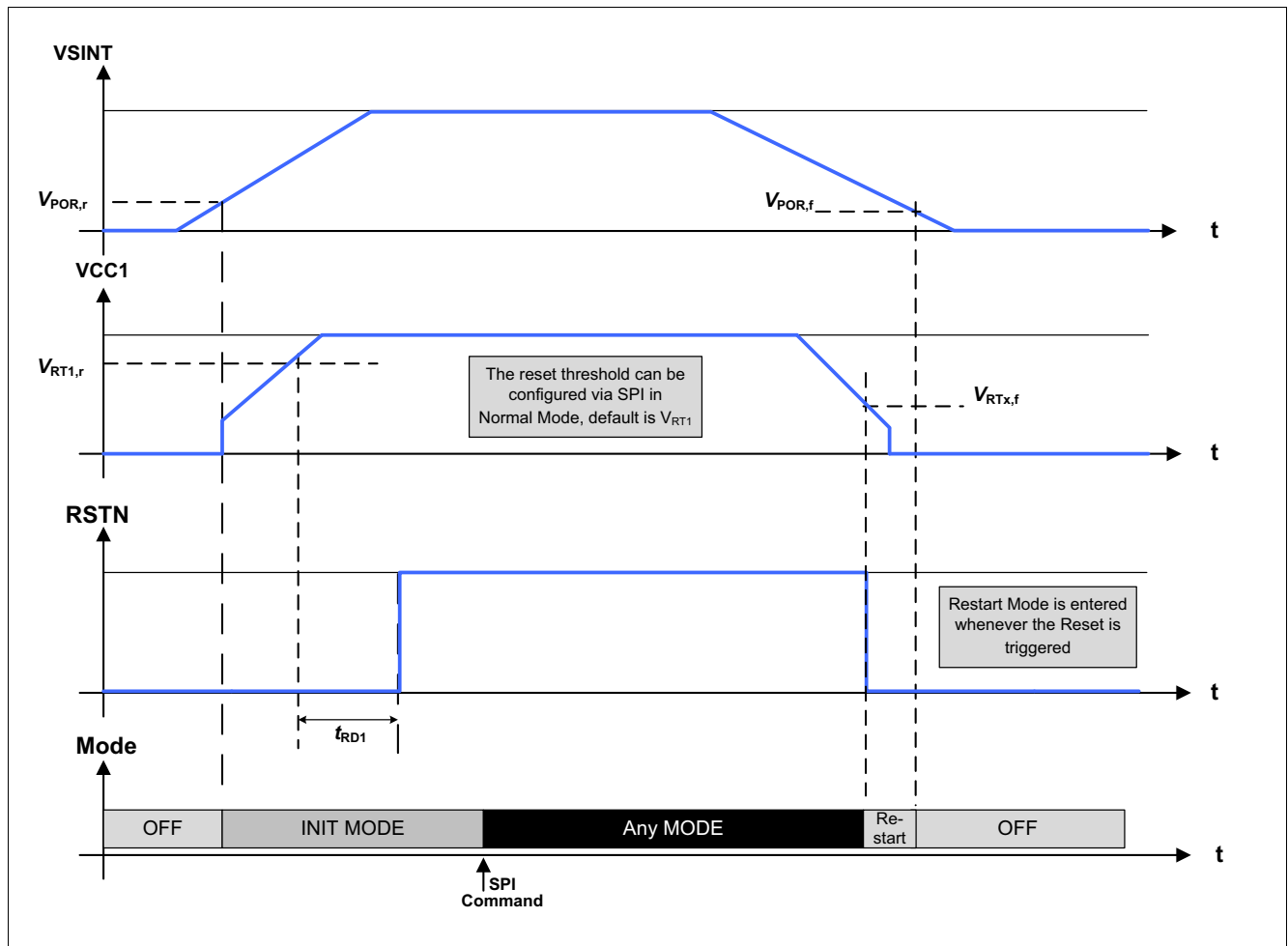
A wake on the Bus will generate an interrupt and the RXDCAN, is pulled to low. By these signals the microcontroller is informed that the watchdog is started with a long open window. After the long open window the watchdog has to be served as configured in the **WD\_CTRL** register.

To disable the watchdog again, the device needs to be switched to Normal Mode and the sequence needs to be sent again.

### 12.3 VSINT Power On Reset

At power up of the device, the Power on Reset is detected when  $VSINT > V_{POR,r}$  and the SPI bit **POR** is set to indicate that all SPI registers are set to POR default settings. VCC1 is starting up and the reset output will be kept low and will only be released once VCC1 has crossed  $V_{RT1,r}$  and after  $t_{RD1}$  has elapsed.

In case  $VSINT < V_{POR,f}$  an device internal reset will be generated and the device is switched off and will restart in Init Mode at the next VSINT rising. This is shown in **Figure 69**.



**Figure 69** Ramp up / down example of Supply Voltage

## **12.4 VSINT Under- and Overvoltage**

### **12.4.1 VSINT Undervoltage**

The VSINT under-voltage monitoring is always active in Init Mode, Restart Mode, Normal Mode. If the supply voltage VSINT drops below  $V_{SINT,UV}$  for more than  $t_{VSUV\_FLT}$ , then the device does the following measures:

- The VCC1 short circuit diagnosis becomes inactive (see [Chapter 12.8](#)). However, the thermal protection of the device remains active. If the undervoltage threshold is exceeded (VSINT rising) then the function will be automatically enabled again.
- The status bit **VSINT\_UV** is set and latched until a clear command of **SUP\_STAT** is received.

*Note: VSINT under-voltage monitoring is not available in Stop Mode due to current consumption saving requirements except if the VCC1 load current is above the active peak threshold ( $I_{PEAK\_TH}$ ) or if VCC1 is below the VCC1 prewarning threshold.*

### **12.4.2 VSINT Overvoltage**

The VSINT over-voltage monitoring is always active in Init Mode, Restart Mode and Normal Mode. If VSINT rises above  $V_{S,OVD1}$ ,  $V_{S,OVD2}$  for more than  $t_{VSOV\_FLT}$  then the device does the following measures:

1. If HBxMODE = 01b or 10b, then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated.
3. The status bits **VSINT\_OV** is set and latched until a clear command of **SUP\_STAT** is received.

If VS or VSINT fall below  $V_{S,OVD1}$  or  $V_{S,OVD2}$ :

- If **CPEN** = 0 : the charge pumps stays and the bridge driver stay off.
- If **CPEN** = 1 :
  - If **BDOV\_REC** = 0 : Then the charge pump is reactivated but the bridge driver stays off until **VS\_OV** and **VSINT\_OV** are cleared. The current sense amplifier is reactivated (provided that **CSA\_OFF** = 0)
  - If **BDOV\_REC** = 1 : Then the charge pump and the current sense amplifier are reactivated and the bridge driver is enabled if  $V_{CP} > V_{CPUVx}$ , even if **VS\_OV** or **VSINT\_OV** is set. The state of the external MOSFETs is according to the control registers.

## **12.5 VS Under- and Overvoltage**

### **12.5.1 VS Undervoltage**

The VS under-voltage monitoring is always active in Init-, Restart Mode and Normal Mode. If VS drops below  $V_{S,UV}$  for more than  $t_{VSUV\_FILT}$ , then the device does the following measures:

1. If HBxMODE = 01b or 10b, then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated and the current sense amplifier is turned off.
3. The status bits **VS\_UV** is set and latched until a clear command of **SUP\_STAT** is received.

If VS rises above  $V_{S,UV}$ , then the charge pump is reactivated (provided that **CPEN** is set) and the current sense amplifier is reactivated (provided **CSA\_OFF** = 0) but the bridge driver stays off until **VS\_UV** is cleared. The bridge driver will be reactivated once the VS\_UV bit is cleared.

### **12.5.2 VS Overvoltage**

The VS over-voltage monitoring is always active in Init-, Restart Mode and Normal Mode or when the charge pump is enabled. If VS rises above  $V_{S,OVD1}$  or  $V_{S,OVD2}$  for more than  $t_{VSOV\_FILT}$ , then the device does the following measures:

1. If HBxMODE = 01b or 10b, then the corresponding MOSFETs are actively turned off with their static discharge current during their respective tHBxCCP Active.
2. Then the charge pump is turned off and the passive discharge is activated and current sense amplifier is turned off.
3. The status bits **VS\_OV** is set and latched until a clear command of **SUP\_STAT** is received.

If VS and VSINT fall below  $V_{S,OVD1}$  or  $V_{S,OVD2}$ :

- If **CPEN** = 0 : the charge pumps and the bridge driver stay off.
- If **CPEN** = 1 :
  - If **BDOV\_REC** = 0 : Then the charge pump is reactivated but the bridge driver stays off until **VS\_OV** and **VSINT\_OV** are cleared. The current sense amplifier is reactivated provided that **CSA\_OFF** = 0
  - If **BDOV\_REC** = 1 : Then the charge pump and the current sense amplifier are reactivated and the bridge driver is enabled if  $V_{CP} > V_{CPUVx}$ , even if **VS\_OV** or **VSINT\_OV** is set. The state of the external MOSFETs is according to the control registers.



## **12.6 VS Under- Overvoltage for high-side**

### **12.6.1 VS Undervoltage for high-side**

If the supply voltage VS passes below the undervoltage threshold ( $V_{SHS,UV}$ ) the device does the following measures:

- HS1...3 are acting accordingly to the SPI setting (refer also to [Chapter 7.2.1](#)).
- SPI bit **HS\_UV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore.

### **12.6.2 VS Overvoltage for high-side**

If the supply voltage VSHS reaches the overvoltage threshold ( $V_{SHS,OVD}$ ) the device triggers the following measures:

- HS1...3 are acting accordingly to the SPI setting (refer also to [Chapter 7.2.2](#)).
- The status bit **HS\_OV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore.

## 12.7 VCC1 Over-/ Undervoltage and Undervoltage Prewarning

### 12.7.1 VCC1 Undervoltage and Undervoltage Prewarning

This function is always active when the VCC1 voltage regulator is enabled.

A first-level voltage detection threshold is implemented as a prewarning for the microcontroller. The prewarning event is signaled with the bit **VCC1\_WARN**. No other actions are taken.

As described in [Chapter 12.1](#) and [Figure 70](#), a reset will be triggered (RSTN pulled low) when the  $V_{CC1}$  output voltage falls below the selected undervoltage threshold ( $V_{RTx}$ ). The device will enter Restart Mode and the bit **VCC1\_UV** is set when RSTN is released again.

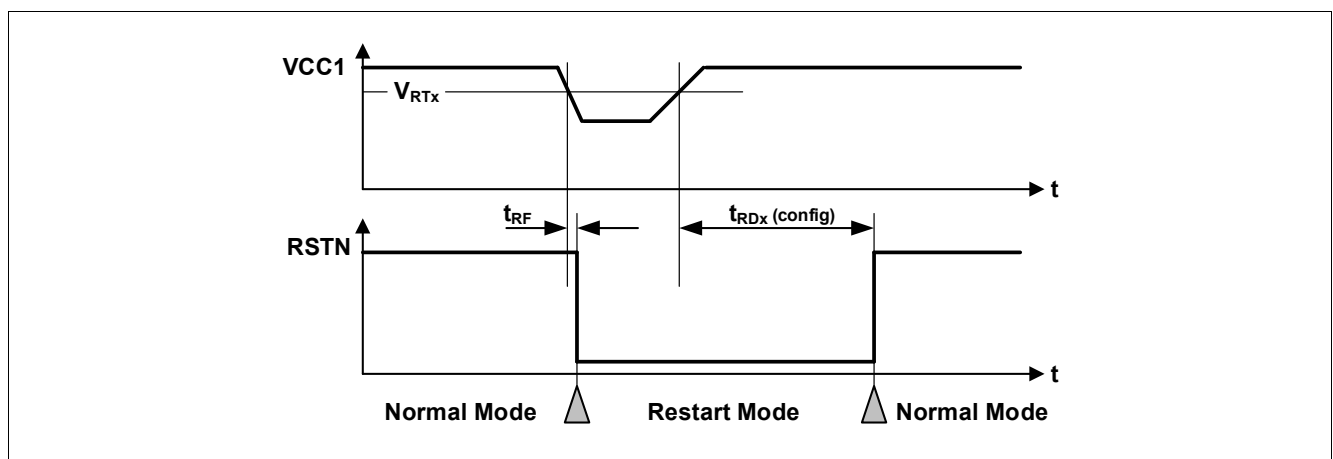
The hysteresis of the VCC1 undervoltage threshold can be increased by setting the bit **RSTN\_HYS**. In this case always the highest rising threshold ( $V_{RT1,R}$ ) is used for the release of the undervoltage reset. The falling reset threshold remains as configured.

An additional safety mechanism is implemented to avoid repetitive VCC1 undervoltage resets due to high dynamic loads on VCC1:

- A counter is increased for every consecutive VCC1 undervoltage event (regardless on the selected reset threshold).
- The counter is active in Init Mode, Normal Mode and Stop Mode.
- For  $V_S < V_{SINT,UV}$  the counter will be stopped in Normal Mode (i.e. the VS UV comparator is always enabled in Normal Mode).
- A 4th consecutive VCC1 undervoltage event will lead to Fail-Safe Mode entry and to setting the bit **VCC1\_UV\_FS**.
- This counter is cleared:
  - When Fail-Safe Mode is entered.
  - When the bit **VCC1\_UV** is cleared.
  - When a Soft-Reset is triggered.

**Note:** After 4 consecutive **VCC1\_UV** events, the device will enter Fail-Safe Mode and the **VCC1\_UV\_FS** bit is set.

**Note:** The **VCC1\_WARN** or **VCC1\_UV** bits are not set in Sleep Mode as  $V_{CC1} = 0\text{ V}$  in this case.



**Figure 70 VCC1 Undervoltage Timing Diagram**

## Supervision Functions

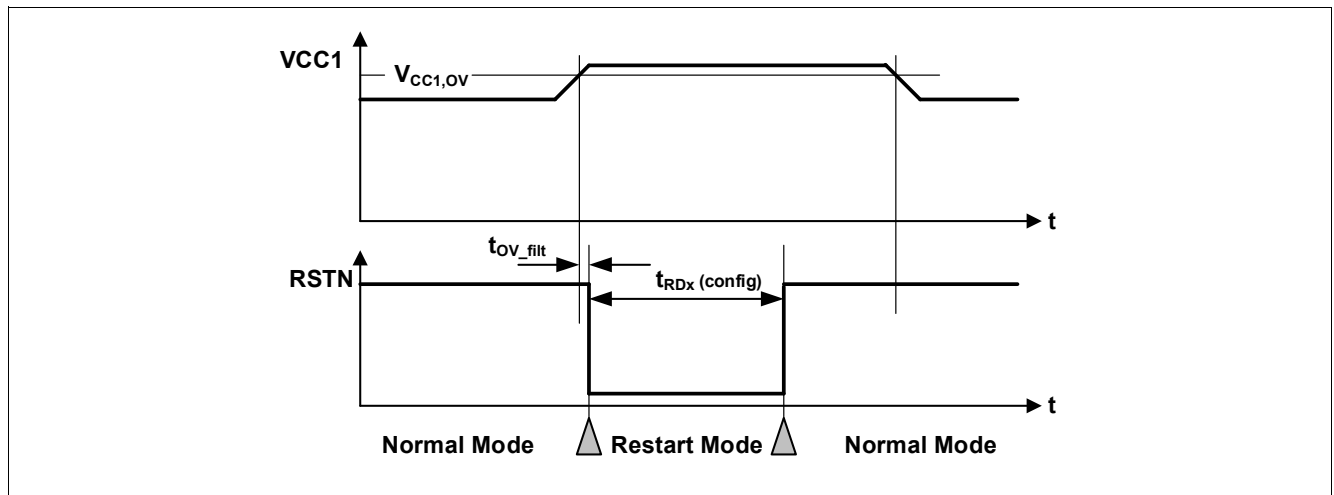
*Note: It is recommended to clear the **VCC1\_WARN** and **VCC1\_UV** bit once it is detected by the microcontroller software to verify if the undervoltage still exists or not.*

### 12.7.2 VCC1 Overvoltage

For fail-safe reasons a configurable VCC1 over voltage detection feature is implemented. It is active when the VCC1 voltage regulator is enabled.

In case the  $V_{CC1,OV,r}$  threshold is crossed, the device triggers following measures depending on the configuration:

- The bit **VCC1\_OV** is always set.
- Based on the configuration of **VCC1\_OV\_MOD**, different kind of event are generated from device.
- If the **VCC1\_OV\_MOD**=11<sub>B</sub>, in case of the device enters in Fail Safe Mode.



**Figure 71 VCC1 Over Voltage Timing Diagram**

### 12.8 VCC1 Short Circuit Diagnostics

The short circuit protection feature for  $V_{CC1}$  is implemented as follows:

- The short circuit detection is only enabled if  $V_S > V_{SINT,UV}$ .
- If  $V_{CC1}$  is not above the  $V_{RTX}$  within  $t_{VCC1,SC}$  after device power up or after waking from Sleep Mode or Fail-Safe Mode (i.e. after  $V_{CC1}$  is enabled) then the SPI bit **VCC1\_SC** is set,  $V_{CC1}$  is turned off, the FO pin is enabled, **FAILURE** is set and Fail-Safe Mode is entered. The device can be activated again via a wake-up sources.
- The same behavior applies, if  $V_{CC1}$  falls below  $V_{RTX}$  for longer than  $t_{VCC1,SC}$ .

### 12.9 VCAN Undervoltage

An undervoltage warning is implemented for VCAN as follows:

- $V_{CAN}$  undervoltage detection: In case the CAN module is enabled and the voltage on  $V_{CAN}$  will drop below the  $V_{CAN\_UV,f}$  threshold, then the SPI bit **VCAN\_UV** is set and can be only cleared via SPI.

## **12.10 Thermal Protection**

Three independent and different thermal protection features are implemented in the device according to the system impact:

- Individual thermal shutdown of specific blocks
- Temperature prewarning of VCC1 voltage regulator
- Device thermal shutdown due to VCC1 overtemperature

### **12.10.1 Individual Thermal Shutdown**

As a first-level protection measure, CAN, HSx and the charge pump are independently switched off if the respective block reaches the temperature threshold  $T_{jTSD1}$ . Then the **TSD1** bit is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Independent of the device mode the thermal shutdown protection is only active if the respective block is ON.

The respective modules behave as follows:

- CAN: The transmitter is disabled and stays in CAN Normal Mode acting like CAN Receive Only Mode. The status bits **CAN\_FAIL** are set to '01'. Once the overtemperature condition is not present anymore, then the CAN transmitter is automatically switched on.
- HSx: If one or more HSx switches reach the TSD1 threshold, then the HSx switches are turned OFF (depending on configuration either individually or all at once) and the control bits for HSx are cleared based on **HS\_OT\_SD\_DIS** setting. The status bits HSx\_OT are set (see register **HS\_OL\_OC\_OT\_STAT**). Once the over temperature condition is not present anymore, then HSx has to be configured again by SPI.
- Charge pump: If the charge pump reaches  $T_{jTSD1}$ , then **CP\_OT** is set, **CPEN** is cleared and the activated MOSFETs are actively discharged with their respective static currents during their respective active cross current protection times (tHBxCCP active). When all tHBxCCP active elapsed, then the charge pump and the MOSFETs active discharge are disabled and the current sense amplifier is deactivated. Once the over temperature condition is not present anymore, then **CPEN** has to be configured again by SPI.

*Note: The diagnosis bits are not cleared automatically and have to be cleared via SPI once the overtemperature condition is not present anymore.*

### **12.10.2 Temperature Prewarning**

As a next level of thermal protection a temperature prewarning is implemented if the main supply VCC1 reaches the thermal prewarning temperature threshold  $T_{jPW}$ . Then the status bit **TPW** is set. This bit can only be cleared via SPI once the overtemperature is not present anymore.

### **12.10.3 Thermal Shutdown**

As a highest level of thermal protection a temperature shutdown of the device is implemented if the main supply VCC1 reaches the thermal shutdown temperature threshold  $T_{jTSD2}$ . Once a TSD2 event is detected Fail-Safe Mode is entered. Only when device temperature falls below the TSD2 threshold then the device remains in Fail-Safe Mode for  $t_{TSD2}$  to allow the device to cool down. After this time has expired, the device will automatically change via Restart Mode to Normal Mode (see also [Chapter 5.4.6](#)).

When a TSD2 event is detected, then the status bit **TSD2** is set. This bit can only be cleared via SPI in Normal Mode once the overtemperature is not present anymore.

For increased robustness requirements it is possible to extend the TSD2 waiting time by 64x of  $t_{TSD2}$  after 16 consecutive TSD2 events by setting the SPI bit **TSD2\_DEL**. The counter is incremented with each TSD2 event even if the bit **TSD2** is not cleared. Once the counter has reached the value 16, then the bit **TSD2\_SAFE** is set

## **Supervision Functions**

and the extended TSD2 waiting time is active. The extended waiting time will be kept until **TSD2\_SAFE** is cleared. The TSD counter is cleared when **TSD2** or **TSD2\_DEL** is cleared.

*Note: In case a TSD2 overtemperature occurs while entering Sleep Mode then Fail-Safe Mode is still entered.*

*Note: In case of a TSD2 event, the **FAILURE** bit is set to '1' and the **DEV\_STAT** field is set to '01' inside the **DEV\_STAT** register.*

## Supervision Functions

### 12.11 Bridge driver

This section describes the supervision functions related to the bridge driver.

#### 12.11.1 Bridge driver supervision with activated charge pump

This section describes the supervision functions when the charge pump is activated.

##### 12.11.1.1 Drain-source voltage monitoring

Voltage comparators monitor the activated MOSFETs to protect high-side MOSFETs and low-side MOSFETs against a short circuit respectively to ground and to the battery during ON-state.

A drain-source overvoltage is detected on a low-side MOSFET if the voltage difference between VSHx and SL exceeds the threshold voltage configured by **LS\_VDS** (see [Table 38](#)). Consequently, the corresponding half-bridge is latched off with the static discharge current.

A drain-source overvoltage is detected on a high-side MOSFET if the voltage difference between VS and VSHx exceeds the threshold voltage configured by **HS\_VDS** (see [Table 39](#)). Consequently, the corresponding half-bridge is latched off with the static discharge current.

**Table 38 Low-side drain-source overvoltage threshold**

<b>LSxVDSTH[2:0]</b>	<b>Drain-Source overvoltage threshold for LSx (typical)</b>
000 <sub>B</sub>	160 mV
001 <sub>B</sub>	200 mV (default)
010 <sub>B</sub>	300 mV
011 <sub>B</sub>	400 mV
100 <sub>B</sub>	500 mV
101 <sub>B</sub>	600 mV
110 <sub>B</sub>	800 mV
111 <sub>B</sub>	2 V

**Table 39 High-side drain-source overvoltage threshold**

<b>HSxVDSTH[2:0]</b>	<b>Drain-Source overvoltage threshold for HSx (typical)</b>
000 <sub>B</sub>	160 mV
001 <sub>B</sub>	200 mV (default)
010 <sub>B</sub>	300 mV
011 <sub>B</sub>	400 mV
100 <sub>B</sub>	500 mV
101 <sub>B</sub>	600 mV
110 <sub>B</sub>	800 mV
111 <sub>B</sub>	2 V

**Attention:** 2 V threshold is dedicated for the diagnostic in off-state. It is highly recommended to select another drain-source overvoltage threshold once the routine of the diagnostic in off-state has been performed to avoid additional current consumption from VS and from the charge pump.

The device reports a Drain-Source overvoltage error if both conditions are met:

## Supervision Functions

- After expiration of the blank time .
- If the Drain-Source voltage monitoring exceeds the configured threshold for a duration longer than the configured filter time (refer to [Table 40](#) and [LS\\_VDS](#) TFVDS bits).

**Table 40 Drain-Source overvoltage filter time**

TFVDS[2:0]	Drain-Source overvoltage filter time (typical)
00 <sub>B</sub>	0.5 $\mu$ s (default)
01 <sub>B</sub>	1 $\mu$ s
10 <sub>B</sub>	2 $\mu$ s
11 <sub>B</sub>	6 $\mu$ s

If a short circuit is detected by the Drain-Source voltage monitoring:

- The impacted half-bridge is latched off with the static discharge current for the configured cross-current protection time.
- The corresponding bit in the status register [DSOV](#) is set.
- The DSOV bit in Global Status Register [GEN\\_STAT](#) is set.

If a Drain-Source overvoltage is detected for one of the MOSFETs, then the status register [DSOV](#) must be cleared in order to re-enable the faulty half-bridge.

### 12.11.1.2 Cross-current protection and drain-source overvoltage blank time

All gate drivers feature a cross-current protection time and a Drain-Source overvoltage blank time.

The cross-current protection avoids the simultaneous activation of the high-side and the low-side MOSFETs of the same half-bridge.

During the blank time, the drain-source overvoltage detection is disabled, to avoid a wrong fault detection during the activation phase of a MOSFET.

*Note: The setting of the cross-current protection and of the blank times may be changed by the microcontroller only if all HBx\_PWM\_EN bits are reset.*

*Note: Changing the Drain-Source overvoltage of a half-bridge x (HBx) in on-state (HBxMODE[1:0]=(0,1) or (1,0)) may result in a wrong VDS overvoltage detection on HBx. Therefore it is highly recommended to change this threshold when HBxMODE[1:0]=(0,0) or (1,1)*

#### 12.11.1.2.1 Cross-current protection

The active and freewheeling cross-current protection times of each half-bridge is configured individually with the control register [CCP\\_BLK](#).

The typical cross-current protection time applied to the freewheeling MOSFET of the half-bridge x is 587 ns + 266 ns x TCCP[3:0]<sub>D</sub>, where TCCP[3:0]<sub>D</sub> is the decimal value of the control bits TCCP.

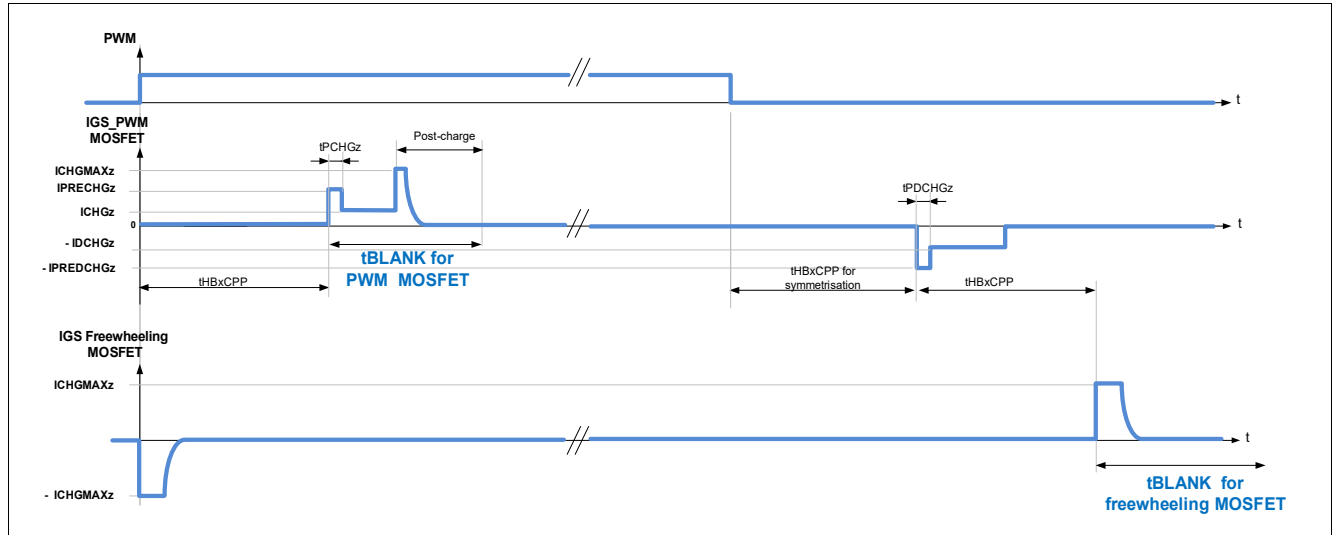
#### 12.11.1.2.2 Drain-source overvoltage blank time

A configurable blank time for the Drain-Source monitoring is applied at the turn-on of the MOSFETs. During the blank time, a Drain-Source overvoltage error is masked.

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For Half-Bridges in PWM mode with AFWx = 1:

- the blank time of the PWM MOSFET starts at the expiration of the cross-current protection time of the PWM MOSFET. Refer to [Figure 72](#).
- the blank time of the free-wheeling MOSFET starts after expiration of the cross-current protection time at turn-off of the PWM MOSFET. Refer to [Figure 72](#).



**Figure 72** Blank time for half-bridges in PWM operation with AFW = 1

For statically activated half-bridges, the blank time starts:

- Case1: at expiration of the cross-current protection ([Figure 42](#)), if the opposite MOSFET was previously activated.
- Case 2: right after the decoding of the SPI command to turn on a MOSFET, if the half-bridge was in high impedance ([Figure 43](#)).

The blank times of the active and FW MOSFETs can be configured with the control register **CCP\_BLK**.

The typical blank is  $587 \text{ ns} + 266 \text{ ns} \times \text{TBLK}[3:0]_D$ .

*Note:* The blank time is implemented at every new activation of a MOSFET, including a recovery from VS undervoltage, VS overvoltage, VSINT overvoltage, CP UV, CP OT.

### 12.11.1.3 OFF-state diagnostic

In order to support the off-state diagnostic (HBxMODE= 11 and **CPEN** = 1), the gate driver of each MOSFET provides pull-up ( $I_{PUDiag}$ ) and a pull-down currents ( $I_{PDDiag}$ ) at the SHx pins. This function requires an activated charge pump.

The pull-up current source of a given half-bridge is on when the half-bridge is active: HBxMODE= 01, 10 or 11 and **CPEN** = 1.

The pull-down current of each low-side gate driver is activated by the control bits HBx (**HB\_ICHG\_MAX** register).

During the off-state diagnostic routine performed by the microcontroller, the drain-source overvoltage threshold of the relevant half-bridges must be set to 2V nominal. Refer to [Table 38](#). Once the routine is finished, it is highly recommended to decrease the drain-source overvoltage threshold to a lower value, avoiding additional current consumption from the VS input.



## Supervision Functions

The following failures can be detected:

- MOSFET short circuit to GND
- MOSFET short circuit the battery
- Open load (disconnected motor)

The status of the output voltages VOUTx, can be read back with status bit HBxVOUT (register **GEN\_STAT**) when the corresponding half-bridge is in off-state (HBxMODE[1:0] = 11).

*Note:* HBxVOUT = 0 if the half-bridge x is not actively off (HBxMODE[1:0] = (0,0), (0,1) or (1,0) and **CPEN**=1) or when the charge pump is deactivated (**CPEN**=0).

### 12.11.1.4 Charge pump undervoltage

The voltage of the charge pump output (VCP) is monitored in order to ensure a correct control of the external MOSFETs.

The charge pump undervoltage threshold is configurable by the control bits **FET\_LVL** and **CPUVTH**.

**Table 41** Charge pump undervoltage thresholds

	<b>FET_LVL = 0</b>	<b>FET_LVL = 1</b>
CPUVTH = 0	<b>V<sub>CPUV1</sub></b> (6 V typ. referred to VS)	<b>V<sub>CPUV3</sub></b> (7.5 V typ. referred to VS)
CPUVTH = 1	<b>V<sub>CPUV2</sub></b> (6.5 V typ. referred to VS)	<b>V<sub>CPUV4</sub></b> (8 V typ. referred to VS)

If VCP falls below the configured charge pump undervoltage threshold while **CPEN** = 1:

- If one of the MOSFET is on, then all MOSFETs are actively turned off with their configured static discharge current during their respective tHBxCCP active.
- Then the gate drivers are turned off and CSA is turned off.
- **CP\_UV** is set and latched.

The **CP\_UV** is reset and the normal operation is resumed once **SUP\_STAT** is cleared and VCP > VCPUV.

The charge pump undervoltage detection is blanked (**t<sub>CPUVBLANK</sub>**) during each new activation of the charge pump<sup>1)</sup>.

### 12.11.1.5 Switching parameters of MOSFETs in PWM mode

The effective switching parameters of the active MOSFETs (**EN\_GEN\_CHECK**=1), respectively PWM MOSFET (**EN\_GEN\_CHECK**=0) can be read out with dedicated status registers:

- The turn-on and turn off delays, noted tDON and tDOFF are reported by the status register **EFF\_TDON\_OFF1**, **EFF\_TDON\_OFF2**, **EFF\_TDON\_OFF3**.
- The rise and fall times, noted tRISE and tFALL, are reported by the status register **TRISE\_FALL1**, **TRISE\_FALL2**, **TRISE\_FALL3**.

### 12.11.2 Low-side drain-source voltage monitoring during braking

The low-side MOSFETs are turned-on while the charge pump is deactivated in the following conditions:

- The slam mode is activated and PWM1/CRC is High.

<sup>1)</sup> Including **CPEN** set to 1, recovery from VS under/overvoltage, VSINT overvoltage and CP\_OT

## Supervision Functions

- The parking braking mode is activated and the device is in Sleep Mode or Stop Mode.
- VS overvoltage brake is activated and ( $VS > VS$  Overvoltage braking or  $VSINT > VSINT$  Overvoltage braking) in all device modes if **OV\_BRK\_EN** is set.

Under these conditions, the drain-source voltage of the low-sides are monitored and the applied drain-source overvoltage thresholds are according to **VDSTH\_BRK**.

The applied blank time, which starts at the beginning of the brake activation, is:

- **t<sub>BLK\_BRAKE1</sub>** if **TBLK\_BRK** = 0
- **t<sub>BLK\_BRAKE2</sub>** if **TBLK\_BRK** = 1

During the blank time, a drain-source overvoltage of the low-sides is masked.

The applied filter time is **t<sub>FVDS\_BRAKE</sub>**.

If a drain-source overvoltage is detected during braking, then all low-side MOSFETs are turned off (latched) within **t<sub>OFF\_BRAKE</sub>**. **SLAM\_LSx\_DIS** (**BRAKE**, **SLAM**, **PARK\_BRK\_EN**, **OV\_BRK\_EN** are unchanged. The corresponding status bit LSxDSOV\_BRK is set in **DSOV**.

The low-sides can be reactivated only if all LSxDSOV\_BRK bits (**DSOV**) are cleared (even in slam mode with the respective LSx disabled by the **SLAM\_LSx\_DIS** bit).

If any of the status bits LSxDSOV\_BRK is set, then the charge pump stays off (**CPEN**=1 command is accepted but the charge pump stays disabled until all LSxDSOV\_BRK are cleared).

### 12.11.3 VS or VSINT Overvoltage braking

The VS and VSINT overvoltage braking is activated if the **OV\_BRK\_EN** bit in **BRAKE** register is set regardless of the device mode.

If VS, respectively VSINT, exceeds  $V_{OVBR,cfgr,x}$  ( $x = 0$  to  $7$ ), then all low-sides MOSFETs are turned-on within **t<sub>ON\_BRAKE</sub>**. The status bits **VS OV BRAKE\_ST**, respectively **VSINT OV BRAKE\_ST**, is set and latched (see **DSOV** register).

If VS and VSINT decrease below  $V_{OVBR,cfgr,x} - V_{HYS,cfgr,x}$  ( $x = 0$  to  $7$ ), then all low-sides MOSFETs are turned-off within **t<sub>OFF\_BRAKE</sub>** after the filter time **t<sub>OV\_BR\_FILT</sub>**.

If ( $VSHx - VSL$ ) exceeds the configured threshold, then all low-sides MOSFETs are turned-off within **t<sub>OFF\_BRAKE</sub>** after the filter time **t<sub>FVDS\_BRAKE</sub>**. The threshold is:

- **V<sub>VDSMONTH0\_BRAKE</sub>** if **VDSTH\_BRK** = 0
- **V<sub>VDSMONTH1\_BRAKE</sub>** if **VDSTH\_BRK** = 1

## 12.12 Current sense amplifier

The current sense amplifier (CSA) allows current measurements with external shunt resistor in low-side configuration. The CSA is supplied by the charge pump (CP). Therefore, if the CP is off, then the CSA is deactivated.

### 12.12.1 Unidirectional and bidirectional operation

The current sense amplifier (CSA) can work either as unidirectional or bi-directional operation. Refer to CSA register.

**Unidirectional operation** **CSD** = 0

## Supervision Functions

In unidirectional operation, the CSA is optimized to measure the current flowing through the external shunt resistor when  $V_{CSAP} \geq V_{CSAN}$ .

$V_{CSO} = V_{REF\ Unidir} + (V_{CSAP} - V_{CSAN} + V_{OS}) \times G_{DIFF}$  provided that  $V_{CSO}$  is in the linear range<sup>1) 2)</sup>.

### Bidirectional operation **CSD = 1**

In bidirectional operation, the CSA measures the current flowing through the external shunt resistor in both directions:  $V_{CSAP} \geq V_{CSAN}$  or  $V_{CSAP} \leq V_{CSAN}$ .

The output CSO works at half-scale range:  $V_{CSO} = V_{REF\ Bidir} + (V_{CSAP} - V_{CSAN} + V_{OS}) \times G_{DIFF}$ , provided that  $V_{CSO}$  is in the linear range<sup>2)</sup>.

### 12.12.2 Gain configuration

The gain of the current sense amplifier is configurable by the configuration bits CSAG bits. Refer to [Table 42](#).

**Table 42 Configuration of the current sense amplifier gain**

CSAG[1:0]	Current sense amplifier gain $G_{DIFF}$
00 <sub>B</sub>	$G_{DIFF10}$
01 <sub>B</sub>	$G_{DIFF20}$
10 <sub>B</sub>	$G_{DIFF40}$
11 <sub>B</sub>	$G_{DIFF60}$

### 12.12.3 Overcurrent Detection

A comparator at CSO detects overcurrent conditions. The overcurrent threshold is configurable with the OCTH bits. Refer to [Table 43](#) for unidirectional operation and [Table 44](#) for bidirectional operation.

**Table 43 Overcurrent detection thresholds in unidirectional operation (CSD = 0)**

OCTH[1:0]	Typical Overcurrent Detection Threshold
00 <sub>B</sub>	$V_{CSO} > V_{CC1}/2$
01 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + V_{CC1}/10$
10 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 2 \times V_{CC1}/10$
11 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 3 \times V_{CC1}/10$

1) Valid if  $0.5\text{ V} \leq V_{CSO} \leq V_{CC1} - 0.5\text{ V}$ .

2)  $V_{CSO}$  is clamped between  $V_{CC1}$  and GND.

Supervision Functions

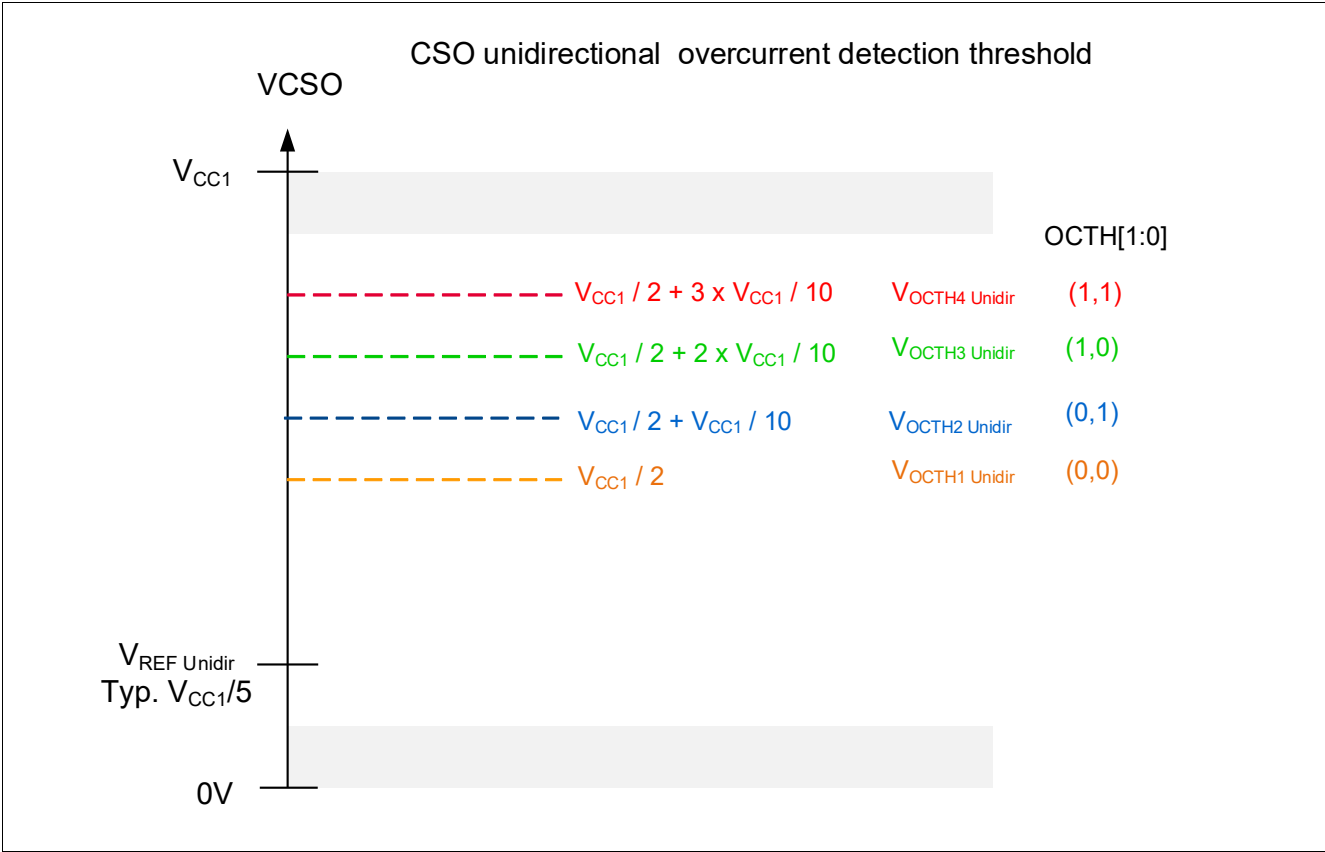
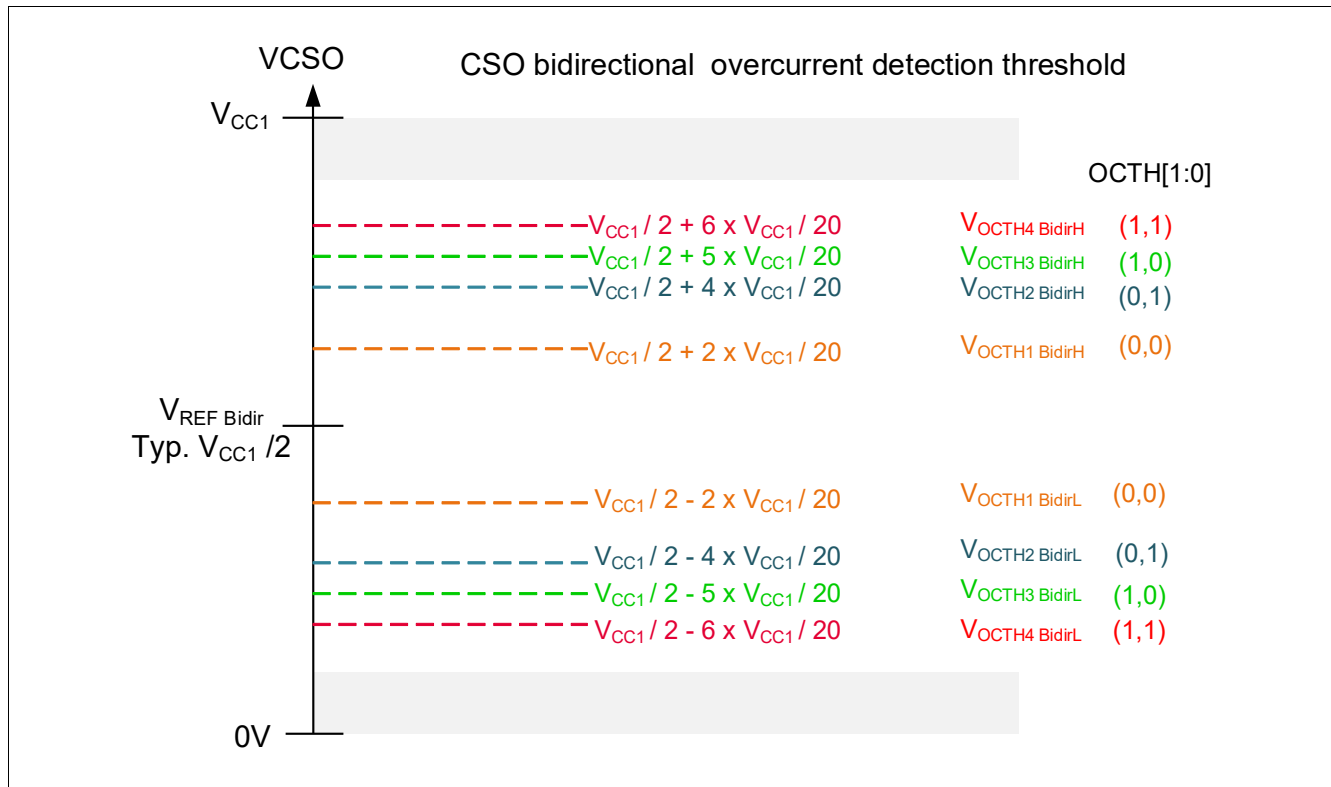


Figure 73 Overcurrent detection thresholds in unidirectional operation (CSD = 0)

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**Table 44 Overcurrent detection thresholds in bidirectional operation (CSD = 1)**

OCTHx[1:0]	Typical Overcurrent Detection Threshold
00 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 2 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 2 \times V_{CC1}/20$
01 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 4 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 4 \times V_{CC1}/20$
10 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 5 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 5 \times V_{CC1}/20$
11 <sub>B</sub>	$V_{CSO} > V_{CC1}/2 + 6 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 6 \times V_{CC1}/20$



**Figure 74 Overcurrent detection thresholds in bidirectional operation (CSD = 1)**

It is possible to program the device behavior when an overcurrent condition is detected:

- OCEN bit = 0 (see CSA): the device only reports the overcurrent event ( bit is set), without any change of the gate driver states.
- OCEN bit = 1 (see CSA): the device reports the overcurrent event ( bit is set) and actively turns off all MOSFETs with static discharge current:
  - The MOSFETs can be reactivated by clearing **OC\_CSA** or by resetting the **OCEN** bit.

The overcurrent filter time is configurable (refer to  $t_{FOC}$ ) by the OCFILT control bits.

$t_{FOC}$  refers to the output of the current sense amplifier. The CSO settling time (2  $\mu s$  max,  $t_{SET}$ ) and the analog propagation delay (< 1  $\mu s$ ) are not taken into account by the overcurrent filter time.

### 12.12.4 CSO output capacitor

The capacitor connected to CSO (CCSO) must be between 10 pF and 2.2 nF. The control bit **CSO\_CAP** optimizes the current consumption for  $CCSO < 400\ pF$  or  $400\ pF < CCSO < 2.2\ nF$ <sup>1)</sup>.

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**12.13 Electrical Characteristics**

**Table 45 Electrical Characteristics**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VCC1 Monitoring; VCC1 = 5.0V Version							
Undervoltage Prewarning Threshold Voltage PW,f	$V_{PW,f}$	4.53	4.70	4.84	V	VCC1 falling, SPI bit is set	P_13.12.1
Undervoltage Prewarning Threshold Voltage PW,r	$V_{PW,r}$	4.60	4.75	4.90	V	VCC1 rising	P_13.12.2
Undervoltage Prewarning Threshold Voltage hysteresis	$V_{PW,hys}$	30	50	90	mV	6)	P_13.12.3
VCC1 UV Prewarning Detection Filter Time	$t_{VCC1,PW\_F}$	5	10	14	us	2) rising and falling	P_13.12.4
Reset Threshold Voltage RT1,f	$V_{RT1,f}$	4.45	4.6	4.75	V	default setting; VCC1 falling	P_13.12.5
Reset Threshold Voltage RT1,r	$V_{RT1,r}$	4.58	4.74	4.90	V	default setting; VCC1 rising	P_13.12.6
Reset Threshold Voltage RT2,f	$V_{RT2,f}$	3.70	3.85	4.00	V	VCC1 falling	P_13.12.7
Reset Threshold Voltage RT2,r	$V_{RT2,r}$	3.85	4.0	4.15	V	VCC1 rising	P_13.12.8
Reset Threshold Voltage RT3,f	$V_{RT3,f}$	3.24	3.40	3.55	V	$V_S \geq 4\text{ V}$ ; VCC1 falling	P_13.12.9
Reset Threshold Voltage RT3,r	$V_{RT3,r}$	3.39	3.54	3.70	V	$V_S \geq 4\text{ V}$ ; VCC1 rising	P_13.12.10
Reset Threshold Voltage RT4,f	$V_{RT4,f}$	2.49	2.65	2.8	V	$V_S \geq 4\text{ V}$ ; VCC1 falling	P_13.12.11
Reset Threshold Voltage RT4,r	$V_{RT4,r}$	2.65	2.76	2.95	V	$V_S \geq 4\text{ V}$ ; VCC1 rising	P_13.12.12
Reset Threshold Hysteresis	$V_{RT,hys}$	70	140	220	mV	6)	P_13.12.13
VCC1 Over Voltage Detection Threshold Voltage	$V_{CC1,OV,r}$	5.5	5.65	5.8	V	1)6) rising VCC1	P_13.12.26
VCC1 Over Voltage Detection Threshold Voltage	$V_{CC1,OV,f}$	5.4	5.55	5.7	V	6) falling VCC1	P_13.12.27
VCC1 OV Detection Filter Time	$t_{VCC1,OV\_F}$	51	64	80	us	2)	P_13.12.31

1) for  $400 \text{ pF} < CCSO < 2.2 \text{ nF}$ , a seial resistor of min. 45 Ohm between the CSO pin and the CCSO capacitor is required,

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**Table 45 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VCC1 Short to GND Filter Time	$t_{VCC1,SC}$	3.2	4	4.8	ms	<sup>2)</sup> blanking time during power-up, short circuit detection for $V_S \geq V_{S,UV}$	P_13.12.32

### Reset Generator; Pin RSTN

Reset Low Output Voltage	$V_{RSTN,L}$	–	0.2	0.4	V	$I_{RSTN} = 1 \text{ mA}$ for $V_{CC1} \geq 1 \text{ V}$ & $V_S \geq V_{POR,f}$	P_13.12.33
Reset High Output Voltage	$V_{RSTN,H}$	$0.8 \times V_{CC1}$	–	$V_{CC1} + 0.3 \text{ V}$	V	$I_{RSTN} = -20 \mu\text{A}$	P_13.12.34
Reset Pull-up Resistor	$R_{RSTN}$	10	20	40	k $\Omega$	$V_{RSTN} = 0 \text{ V}$	P_13.12.35
Reset Filter Time	$t_{RF}$	4	10	26	$\mu\text{s}$	<sup>2)</sup> $V_{CC1} < V_{RT1x}$ to RSTN = L see also <a href="#">Chapter 12.3</a>	P_13.12.36
Reset Delay Time 1	$t_{RD1}$	8	10	12	ms	<sup>2)</sup> <b>RSTN_DEL</b> = 0	P_13.12.37
Reset Delay Time 2	$t_{RD2}$	1.6	2	2.4	ms	<sup>2)</sup> <b>RSTN_DEL</b> = 1	P_13.12.64

### VCAN Monitoring

CAN Supply undervoltage detection threshold (falling)	$V_{CAN\_UV,f}$	4.5	–	4.75	V	VCAN falling	P_13.12.38
CAN Supply undervoltage detection threshold (rising)	$V_{CAN\_UV,r}$	4.6	–	4.85	V	VCAN rising	P_13.12.39
$V_{CAN}$ Undervoltage detection hysteresis	$V_{CAN,UV,hys}$	50	90	130	mV	<sup>6)</sup>	P_13.12.40
VCAN UV detection Filter Time	$t_{VCAN,UV,F}$	5	10	14	$\mu\text{s}$	<sup>2)</sup> VCAN rising and falling	P_13.12.41

### Watchdog Generator / Internal Oscillator

Long Open Window	$t_{LW}$	160	200	240	ms	<sup>2)</sup>	P_13.12.42
Internal Clock Generator Frequency	$f_{CLKSBC,1}$	0.8	1.0	1.2	MHz	–	P_13.12.43

### Minimum Waiting time during Fail-Safe Mode

Min. waiting time Fail-Safe	$t_{FS,min}$	80	100	120	ms	<sup>2)3)</sup>	P_13.12.45
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### Power-on Reset, Over / Undervoltage Protection

VSINT Power on reset rising	$V_{POR,r}$	–	–	4.5	V	VSINT increasing	P_13.12.46
VSINT Power on reset falling	$V_{POR,f}$	–	–	3	V	VSINT decreasing	P_13.12.47

**Supervision Functions**

**Table 45 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VSINT Undervoltage Detection Threshold	$V_{SINT,UV}$	5.3	–	6.0	V	Supply UV threshold for VCC1 SC detection; hysteresis included; includes rising and falling threshold	P_13.12.48
VSHS Overvoltage Detection Threshold	$V_{SHS,OVD}$	20	–	22	V	Supply OV supervision for HSx; hysteresis included	P_13.12.55
VSHS Overvoltage Detection hysteresis	$V_{SHS,OVD,hys}$	100	500	–	mV	<sup>6)</sup>	P_13.12.56
VSHS Undervoltage Detection Threshold	$V_{SHS,UVD}$	4.8	–	5.5	V	Supply UV supervision for HSx; hysteresis included	P_13.12.57
VSHS Undervoltage Detection hysteresis	$V_{SHS,UVD,hys}$	50	200	350	mV	<sup>6)</sup>	P_13.12.58
VSHS Undervoltage Detection Filter Time	$t_{VSHS,UV}$	5	10	14	us	<sup>2)</sup> rising and falling	P_13.12.300
VSHS Overvoltage Detection Filter Time	$t_{VSHS,OV}$	5	10	14	us	<sup>2)</sup> rising and falling	P_13.12.301

**Charge Pump Undervoltage**

Charge Pump Undervoltage Referred to VS	$V_{CPUV1}$	5.4	5.9	6.4	V	<b>FET_LVL</b> = 0 <b>CPUVTH</b> = 0 falling threshold, VS ≥ 6 V	P_13.12.59
Charge Pump Undervoltage Referred to VS	$V_{CPUV2}$	5.85	6.35	6.85	V	<b>FET_LVL</b> = 0 <b>CPUVTH</b> = 1 falling threshold, VS ≥ 6 V	P_13.12.60
Charge Pump Undervoltage Referred to VS	$V_{CPUV3}$	6.85	7.35	7.85	V	<b>FET_LVL</b> = 1 <b>CPUVTH</b> = 0 falling threshold, VS ≥ 6 V	P_13.12.61



## Supervision Functions

**Table 45 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge Pump Undervoltage Referred to VS	$V_{CPUV4}$	7.5	8	8.5	V	<b>FET_LVL</b> = 1 <b>CPUVTH</b> = 1 falling threshold, $VS \geq 6 \text{ V}$	P_13.12.62
Charge Pump Undervoltage Filter Time	$t_{CPUV}$	51	64	80	$\mu\text{s}$	<sup>6)</sup> $VS \geq 6 \text{ V}$	P_13.12.63
Charge Pump Undervoltage Blank Time	$t_{CPUVBLANK}$	400	500	600	$\mu\text{s}$	<sup>6)</sup> $VS \geq 6 \text{ V}$	P_13.12.175

### VS monitoring

VS undervoltage threshold	$V_{S,UV}$	4.7	–	5.4	V	hysteresis included	P_13.12.66
VS overvoltage threshold detection 1	$V_{S,OVD1}$	19	–	22.5	V	hysteresis included, <b>VS_OV_SEL</b> = 0	P_13.12.68
VS overvoltage threshold detection 2	$V_{S,OVD2}$	27.75	–	31.25	V	hysteresis included, <b>VS_OV_SEL</b> = 1	P_13.12.65
VS undervoltage filter time	$t_{VSUV\_FILT}$	5	10	14	$\mu\text{s}$	<sup>2)</sup> rising and falling	P_13.12.71
VS overvoltage filter time	$t_{VSOV\_FILT}$	5	10	14	$\mu\text{s}$	<sup>2)</sup> rising and falling	P_13.12.72

### Off-state open load diagnosis

Pull-up diagnosis current	$I_{PUDiag}$	-600	-400	-270	$\mu\text{A}$	$VS \geq 6 \text{ V}$	P_13.12.73
Pull-down diagnosis current	$I_{PDDiag}$	1600	2200	2800	$\mu\text{A}$	$VS \geq 6 \text{ V}$	P_13.12.74
Diagnosis current ratio	$I_{Diag\_ratio}$	4.25	5.25	6.25		Ratio $I_{PDDiag} / I_{PUDiag}$	P_13.12.302

### Drain-source monitoring CP activated

Blank time	$t_{BLANK}$	typ-20%	587 +266 xTBLK	typ+20%	ns	<sup>6)</sup> TBLK: decimal value of TBLK[3:0], $VS \geq 6 \text{ V}$	P_13.12.75
Cross-current protection time	$t_{CCP}$	typ-20%	587 +266 xTCCP	typ+20%	ns	<sup>6)</sup> TCCP: decimal value of TCCPx[3:0], $VS \geq 6 \text{ V}$	P_13.12.76
HS/LS Drain-source overvoltage 0	$V_{VDSMONTH0\_CPON}$	0.115	0.16	0.195	V	VDSTH[2:0] = 000 <sub>B</sub> , $VS \geq 6 \text{ V}$ , TFVDS=00 <sub>B</sub>	P_13.12.77
HS/LS Drain-source overvoltage 1	$V_{VDSMONTH1\_CPON}$	0.16	0.2	0.25	V	VDSTH[2:0] = 001 <sub>B</sub> , $VS \geq 6 \text{ V}$ , TFVDS=00 <sub>B</sub>	P_13.12.78
HS/LS Drain-source overvoltage 2	$V_{VDSMONTH2\_CPON}$	0.24	0.3	0.36	V	VDSTH[2:0] = 010 <sub>B</sub> , $VS \geq 6 \text{ V}$ , TFVDS=00 <sub>B</sub>	P_13.12.79

## Supervision Functions

**Table 45 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
HS/LS Drain-source overvoltage 3	$V_{VDSMONTH3\_CPON}$	0.32	0.4	0.48	V	$VDSTH[2:0] = 011_B$ , $VS \geq 6 \text{ V}$ , $TFVDS = 00_B$	P_13.12.80
HS/LS Drain-source overvoltage 4	$V_{VDSMONTH4\_CPON}$	0.4	0.5	0.6	V	$VDSTH[2:0] = 100_B$ , $VS \geq 6 \text{ V}$ , $TFVDS = 00_B$	P_13.12.81
HS/LS Drain-source overvoltage 5	$V_{VDSMONTH5\_CPON}$	0.48	0.6	0.72	V	$VDSTH[2:0] = 101_B$ , $VS \geq 6 \text{ V}$ , $TFVDS = 00_B$	P_13.12.82
HS/LS Drain-source overvoltage 6	$V_{VDSMONTH6\_CPON}$	0.64	0.8	0.96	V	$VDSTH[2:0] = 110_B$ , $VS \geq 6 \text{ V}$ , $TFVDS = 00_B$	P_13.12.83
HS/LS Drain-source overvoltage 7	$V_{VDSMONTH7\_CPON}$	1.75	2.0	2.25	V	$VDSTH[2:0] = 111_B$ , $VS \geq 6 \text{ V}$ , $TFVDS = 00_B$	P_13.12.84
<b>Drain-Source monitoring - Slam mode, parking braking and VS overvoltage braking, VS or VSINT <math>\geq 8 \text{ V}</math></b>							
Blank time	$t_{BLK\_BRAKE1}$	4.5	7	9.5	$\mu\text{s}$	<b>TBLK_BRK</b> = 0, $VS$ or $VSINT \geq 8 \text{ V}$	P_13.12.85
Blank time	$t_{BLK\_BRAKE2}$	9	11	13	$\mu\text{s}$	<b>TBLK_BRK</b> = 1, $VS$ or $VSINT \geq 8 \text{ V}$	P_13.12.86
VDS Filter time	$t_{FVDS\_BRAKE}$	0.5	1	2.5	$\mu\text{s}$	$VS$ or $VSINT \geq 8 \text{ V}$	P_13.12.87
LS Drain-source monitoring thresholds	$V_{VDSMONTH0\_BRAKE}$	0.56	0.8	1.05	V	$VS$ or $VSINT \geq 8 \text{ V}$ <b>VDSTH_BRK</b> = 0	P_13.12.89
LS Drain-source monitoring thresholds	$V_{VDSMONTH1\_BRAKE}$	0.15	0.22	0.29	V	$VS$ or $VSINT \geq 8 \text{ V}$ <b>VDSTH_BRK</b> = 1	P_13.12.90
<b>VS Overvoltage Braking Mode</b>							
VS Overvoltage braking config 0 rising	$V_{OVBR, cfig0, r}$	25.65	27	28.35	V	<b>OV_BRK_TH</b> =000 <sub>B</sub>	P_13.12.97
VS Overvoltage braking config 1 rising	$V_{OVBR, cfig1, r}$	26.60	28	29.40	V	<b>OV_BRK_TH</b> =001 <sub>B</sub>	P_13.12.98
VS Overvoltage braking config 2 rising	$V_{OVBR, cfig2, r}$	27.55	29	30.45	V	<b>OV_BRK_TH</b> =010 <sub>B</sub>	P_13.12.99
VS Overvoltage braking config 3 rising	$V_{OVBR, cfig3, r}$	28.50	30	31.50	V	<b>OV_BRK_TH</b> =011 <sub>B</sub>	P_13.12.100
VS Overvoltage braking config 4 rising	$V_{OVBR, cfig4, r}$	29.45	31	32.55	V	<b>OV_BRK_TH</b> =100 <sub>B</sub>	P_13.12.101
VS Overvoltage braking config 5 rising	$V_{OVBR, cfig5, r}$	30.40	32	33.60	V	<b>OV_BRK_TH</b> =101 <sub>B</sub>	P_13.12.102
VS Overvoltage braking config 6 rising	$V_{OVBR, cfig6, r}$	31.35	33	34.65	V	<b>OV_BRK_TH</b> =110 <sub>B</sub>	P_13.12.103
VS Overvoltage braking config 7 rising	$V_{OVBR, cfig7, r}$	32.30	34	35.70	V	<b>OV_BRK_TH</b> =111 <sub>B</sub>	P_13.12.104
VS Overvoltage braking config 0	$V_{HYS, cfig0}$	0.64	0.75	0.85	V	<b>OV_BRK_TH</b> =000 <sub>B</sub>	P_13.12.105

## Supervision Functions

**Table 45 Electrical Characteristics** (cont'd)

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS Overvoltage braking config 1	$V_{HYS, cfg1}$	0.74	0.82	0.9	V	<b>OV_BRK_TH=001<sub>B</sub></b>	<b>P_13.12.109</b>
VS Overvoltage braking config 2	$V_{HYS, cfg2}$	0.80	0.89	0.98	V	<b>OV_BRK_TH=010<sub>B</sub></b>	<b>P_13.12.113</b>
VS Overvoltage braking config 3	$V_{HYS, cfg3}$	0.85	0.95	1.05	V	<b>OV_BRK_TH=011<sub>B</sub></b>	<b>P_13.12.117</b>
VS Overvoltage braking config 4	$V_{HYS, cfg4}$	0.93	1.03	1.13	V	<b>OV_BRK_TH=100<sub>B</sub></b>	<b>P_13.12.121</b>
VS Overvoltage braking config 5	$V_{HYS, cfg5}$	0.97	1.08	1.19	V	<b>OV_BRK_TH=101<sub>B</sub></b>	<b>P_13.12.125</b>
VS Overvoltage braking config 6	$V_{HYS, cfg6}$	1.03	1.15	1.27	V	<b>OV_BRK_TH=110<sub>B</sub></b>	<b>P_13.12.129</b>
VS Overvoltage braking config 7	$V_{HYS, cfg7}$	1.1	1.23	1.36	V	<b>OV_BRK_TH=111<sub>B</sub></b>	<b>P_13.12.133</b>
VS and VSINT overvoltage braking filter time	$t_{OV\_BR\_FLT}$	10	15	20	$\mu\text{s}$	<sup>6)</sup>	<b>P_13.12.200</b>

### Current sense amplifier<sup>4)</sup>

Operating common mode input voltage range referred to GND (CSAP - GND) or (CSAN - GND)	$V_{CM}$	-2.0	–	2.0	V		<b>P_13.12.138</b>
Common Mode Rejection Ratio	CMRR	63 69 75 77	– – – –	– – – –	dB	<sup>6)</sup> CSAG = (0,0) CSAG = (0,1) CSAG = (1,0) CSAG = (1,1) DC to 50 kHz $V_{CM} = -2 \dots 2 \text{ V}$ $V_{CSAP} = V_{CSAN}$	<b>P_13.12.139</b>
Settling time to 98%	$t_{SET}$	–	1500	2000	ns	<sup>6)</sup>	<b>P_13.12.140</b>
Settling time to 98% after gain change	$t_{SET\_GAIN}$	–	–	5000	ns	<sup>6)</sup> After gain change from CSN rising edge	<b>P_13.12.141</b>
Input Offset voltage	$V_{OS}$	-1	0	1	mV		<b>P_13.12.142</b>
Current Sense Amplifier DC Gain (uncalibrated)	$G_{DIFF10}$	9.91	10.04	10.17	V/V	CSAG = (0,0)	<b>P_13.12.143</b>
Current Sense Amplifier DC Gain (uncalibrated)	$G_{DIFF20}$	19.79	20.05	20.31	V/V	CSAG = (0,1)	<b>P_13.12.144</b>
Current Sense Amplifier DC Gain (uncalibrated)	$G_{DIFF40}$	39.53	40.05	40.57	V/V	CSAG = (1,0)	<b>P_13.12.145</b>

**Supervision Functions**

**Table 45 Electrical Characteristics (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Amplifier DC Gain (uncalibrated)	$G_{DIFF60}$	59.34	60.12	60.91	V/V	CSAG = (1,1)	P_13.12.146
Gain drift	$G_{DRIFT}$	-0.5	–	0.5	%	<sup>6)</sup> Gain drift after calibration	P_13.12.151
CSO single ended output voltage range (linear range)	$V_{CSO}$	0.5	–	$V_{CC1} - 0.5$	V	<sup>6)</sup>	P_13.12.152
Reference voltage for unidirectional CSAx	$V_{REF \text{ Unidir}}$	-1.25%	$V_{CC1}/5$	+1.25%	V	CSD = 0 $V_{CSAP} = V_{CSAN}$	P_13.12.153
Reference voltage for bidirectional CSAx	$V_{REF \text{ Bidir}}$	-1%	$V_{CC1}/2$	+1%	V	CSD = 1 $V_{CSAP} = V_{CSAN}$	P_13.12.154

**Overcurrent detection**

Overcurrent filter time	$t_{FOC}$	4 7 40 80	6 10 50 100	8 13 60 120	$\mu\text{s}$	<sup>5)6)</sup> OCFILT = 00 <sub>B</sub> OCFILT = 01 <sub>B</sub> OCFILT = 10 <sub>B</sub> OCFILT = 11 <sub>B</sub>	P_13.12.155
OC threshold, unidirectional	$V_{OCTH1 \text{ Unidir}}$	-4%	$V_{CC1}/2$	+4%	V	CSD = 0, OCTH[1:0] = 00 <sub>B</sub>	P_13.12.156
OC threshold, unidirectional	$V_{OCTH2 \text{ Unidir}}$	-4%	$V_{CC1}/2$ + $V_{CC1}/10$	+4%	V	CSD = 0, OCTH[1:0] = 01 <sub>B</sub>	P_13.12.157
OC threshold, unidirectional	$V_{OCTH3 \text{ Unidir}}$	-4%	$V_{CC1}/2$ + 2x $V_{CC1}/10$	+4%	V	CSD = 0, OCTH[1:0] = 10 <sub>B</sub>	P_13.12.158
OC threshold, unidirectional	$V_{OCTH4 \text{ Unidir}}$	-4%	$V_{CC1}/2$ + 3x $V_{CC1}/10$	+4%	V	CSD = 0, OCTH[1:0] = 11 <sub>B</sub>	P_13.12.159
High OC threshold, bidirectional	$V_{OCTH1 \text{ BidirH}}$	-4%	$V_{CC1}/2$ + 2x $V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 00 <sub>B</sub>	P_13.12.160
High OC threshold, bidirectional	$V_{OCTH2 \text{ BidirH}}$	-4%	$V_{CC1}/2$ + 4x $V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 01 <sub>B</sub>	P_13.12.161
High OC threshold, bidirectional	$V_{OCTH3 \text{ BidirH}}$	-4%	$V_{CC1}/2$ + 5x $V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 10 <sub>B</sub>	P_13.12.162
High OC threshold, bidirectional	$V_{OCTH4 \text{ BidirH}}$	-4%	$V_{CC1}/2$ + 6x $V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 11 <sub>B</sub>	P_13.12.163

## Supervision Functions

**Table 45 Electrical Characteristics (cont'd)**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ; Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low OC threshold, bidirectional	$V_{OCTH1 \text{ BidirL}}$	-4%	$V_{CC1}/2 - 2 \times V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 00 <sub>B</sub>	P_13.12.164
Low OC threshold, bidirectional	$V_{OCTH2 \text{ BidirL}}$	-4%	$V_{CC1}/2 - 4 \times V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 01 <sub>B</sub>	P_13.12.165
Low OC threshold, bidirectional	$V_{OCTH3 \text{ BidirL}}$	-4%	$V_{CC1}/2 - 5 \times V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 10 <sub>B</sub>	P_13.12.166
Low OC threshold, bidirectional	$V_{OCTH4 \text{ BidirL}}$	-4%	$V_{CC1}/2 - 6 \times V_{CC1}/20$	+4%	V	CSD = 1, OCTH[1:0] = 11 <sub>B</sub>	P_13.12.167

### Current Sense Amplifier Dynamic Parameters

Power Supply Rejection Ratio	PSRR	60	–	–	dB	<sup>6)</sup> VCP modulated with sinewave (100 kHz, 1 Vpp)	P_13.12.168
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### Overtemperature Shutdown<sup>6)</sup>

Thermal Prewarning Temperature	$T_{jPW}$	125	145	165	°C	$T_j$ rising	P_13.12.169
Thermal Shutdown TSD1	$T_{jTSD1}$	170	185	200	°C	$T_j$ rising	P_13.12.170
Thermal Shutdown TSD2	$T_{jTSD2}$	170	185	200	°C	$T_j$ rising	P_13.12.171
Thermal Shutdown hysteresis	$T_{jTSD,hys}$	–	25	–	°C	<sup>6)</sup>	P_13.12.172
TSD/TPW Filter Time	$t_{TSD\_TPW\_F}$	5	10	15	us	rising and falling, applies to all thermal sensors (TPW, TSD1, TSD2)	P_13.12.173
Deactivation time after thermal shutdown TSD2	$t_{TSD2}$	0.8	1	1.2	s	<sup>2)</sup>	P_13.12.174

1) It is ensured that the threshold  $V_{CC1,OV,r}$  is always higher than the highest regulated  $V_{CC1}$  output voltage  $V_{CC1,out4}$ .

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

3) This time applies for all failure entries except a device thermal shutdown (TSD2 has a typ. 1 s waiting time  $t_{TSD2}$ ).

4)  $6 \text{ V} \leq V_S \leq 23 \text{ V}$

5)  $t_{FOC}$  refers to the output of the current sense amplifier. The CSO settling time (2  $\mu\text{s}$  max,  $t_{SET}$ ) and the analog propagation delay (< 1  $\mu\text{s}$ ) are not taken into account by the overcurrent filter time.

6) Not subject to production test, specified by design.

## 13 Serial Peripheral Interface

The Serial Peripheral Interface is the communication link between the device and the microcontroller. The TLE9563-3QX is supporting multi-slave operation in full-duplex mode with 32-bit data access.

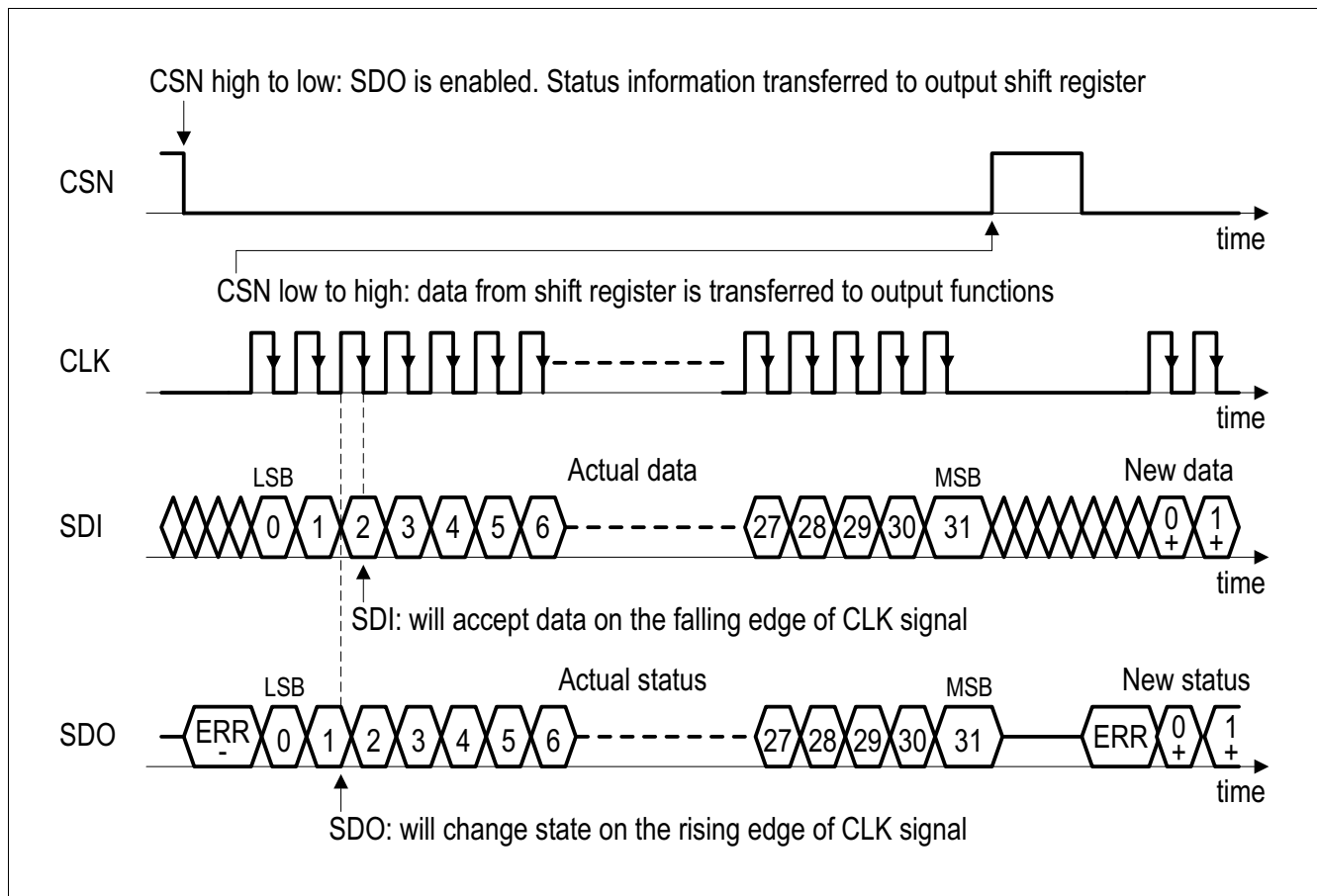
The SPI behavior for the different device modes is as follows:

- The SPI is enabled in Init Mode, Normal Mode and Stop Mode.
- The SPI is OFF in Sleep Mode, Restart Mode and Fail-Safe Mode.

### 13.1 SPI Block Description

The Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see [Figure 75](#) with a 32-bit data access example).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus for other use. The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the device is not daisy chain capable.



**Figure 75 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)**

## **13.2 Failure Signalization in the SPI Data Output**

When the microcontroller sends a wrong SPI command to the device, the device ignores the information. Wrong SPI commands are either invalid device mode commands or commands which are prohibited by the state machine to avoid undesired device or system states (see below). In this case the diagnosis bit **SPI\_FAIL** is set and the SPI Write command is ignored (no partial interpretation). This bit can be only reset by actively clearing it via a SPI command.

**Invalid SPI Commands leading to **SPI\_FAIL** are listed below (in this case the SPI command is ignored):**

- Illegal state transitions:
  - Going from Stop Mode to Sleep Mode. In this case the device enters Restart Mode.
  - Trying to go to Stop Mode or Sleep Mode from Init Mode<sup>1)</sup>. In this case Normal Mode is entered.
- Uneven parity in the data bit of the **WD\_CTRL** register. In this case the watchdog trigger is ignored and/or the new watchdog settings are ignored respectively.
- In Stop Mode: attempting to change any SPI settings, e.g. changing the watchdog configuration, PWM settings and HSx configuration settings during Stop Mode, etc.; the SPI command is ignored in this case; only WD trigger, returning to Normal Mode, triggering a device soft reset, and read & clear status registers commands are valid SPI commands in Stop Mode; **Note:** No failure handling is done for the attempt to go to Stop Mode when all bits in the registers **BUS\_CTRL** and **WK\_CTRL** are cleared because the microcontroller can leave this mode via SPI.
- When entering Stop Mode and **WK\_STAT** is not cleared; **SPI\_FAIL** will not be set but the INTN pin will be triggered.
- Changing from Stop Mode to Normal Mode and changing the other bits of the **M\_S\_CTRL** register. The other modifications will be ignored.
- Sleep Mode: attempt to go to Sleep Mode without any wake source set, i.e. when all bits in the **BUS\_CTRL** and **WK\_CTRL** registers are cleared. In this case the **SPI\_FAIL** bit is set and the device enters Restart Mode. Even though the Sleep Mode command is not entered in this case, the rest of the command is executed but restart values apply during Restart Mode; **Note:** At least one wake source must be activated in order to avoid a deadlock situation in Sleep Mode.  
If the only wake source is a timer and the timer is OFF, then the device will wake immediately from Sleep Mode and enter Restart Mode.
- Setting a longer or equal on-time than the timer period of the respective timer.
- SDI stuck at HIGH or LOW, e.g. SDI received all '0' or all '1'.
- Configured the HSx controlled by SYNC when the WK4/SYNC is not configured as SYNC-input.

*Note: There is no SPI fail information for unused addresses.*

*Note: In case that the register or banking are accessed but they are not valid as address or banks, the **SPI\_FAIL** is not triggered and the cmd is ignored.*

### **Signalization of the ERR Flag (high active) in the SPI Data Output (see Figure 75):**

The ERR flag presents an additional diagnosis possibility for the SPI communication. The ERR flag is being set for following conditions:

1) If the device is externally configured to use SPI with CRC (by PWM1/CRC pin), the attempt to go to Stop or Sleep from Init, will generate SPI\_FAIL even if it is a SPI command with correct CRC. Still, the first SPI command will put the device from Init to Normal Mode even if CRC is not correct (CRC\_FAIL status bit will be set).



## **Serial Peripheral Interface**

- in case the number of received SPI clocks is not 0 or 32.
- in case RSTN is LOW and SPI frames are being sent at the same time.

*Note: In order to read the SPI ERR flag properly, CLK must be low when CSN is triggered, i.e. the ERR bit is not valid if the CLK is high on a falling edge of CSN.*

### **The number of received SPI clocks is not 0 or 32:**

The number of received input clocks is supervised to be 0 or 32 clock cycles and the input word is discarded in case of a mismatch (0 clock cycle to enable ERR signalization). The error logic also recognizes if CLK was high during CSN edges. Both errors ( 0 or 32 bit CLK mismatch or CLK high during CSN edges ) are flagged in the following SPI output by a “HIGH” at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received. The complete SPI command is ignored in this case.

### **RSTN is LOW and SPI frames are being sent at the same time:**

The ERR flag will be set when the RSTN pin is triggered (during device restart) and SPI frames are being sent to the device at the same time. The behavior of the ERR flag will be signalized at the next SPI command for below conditions:

- If the command begins when RSTN is HIGH and it ends when RSTN is LOW.
- If a SPI command will be sent while RSTN is LOW.
- If a SPI command begins when RSTN is LOW and it ends when RSTN is HIGH.

And the SDO output will behave as follows:

- Always when RSTN is LOW then SDO will be HIGH.
- When a SPI command begins when RSTN is LOW and ends when RSTN is HIGH, then the SDO should be ignored because wrong data will be sent.

*Note: It is possible to quickly check for the ERR flag without sending any data bits. i.e. only the CSN is pulled low and SDO is observed - no SPI Clocks are sent in this case.*

*Note: The ERR flag could also be set after the device has entered Fail-Safe Mode because the SPI communication is stopped immediately.*



### 13.3 SPI Programming

For the TLE9563-3QX, 7 bits are used for the address selection (BIT 6...0). Bit 7 is used to decide between Read Only and Read & Clear for the status bits, and between Write and Read Only for configuration bits. For the actual configuration and status information, 16 data bits (BIT 23...8) are used.

Writing, clearing and reading is done word wise. The SPI status bits are not cleared automatically and must be cleared by the microcontroller. Some of the configuration bits will automatically be cleared by the device (refer to the respective register descriptions for detailed information). In Restart Mode, the device ignores all SPI communication, i.e. it does not interpret it.

There are two types of SPI registers:

- Control registers: These registers are used to configure the device, e.g. mode, watchdog trigger, etc.
- Status registers: These registers indicate the status of the device, e.g. wake events, warnings, failures, etc.

For the status registers, the requested information is given in the same SPI command in the data out (SDO). For the control registers, the status of each byte is shown in the same SPI command as well. However, configuration changes of the same register are only shown in the next SPI command (configuration changes inside the device become valid only after CSN changes from low to high). See [Figure 76](#).

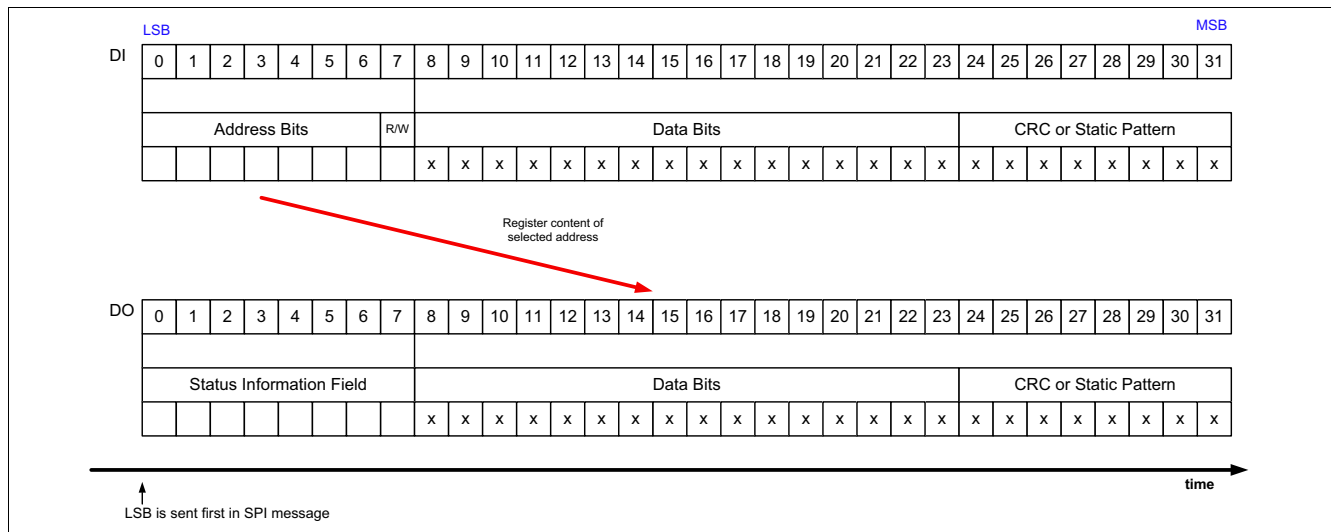
Writing of control registers is possible in Init and Normal Mode. During Stop Mode only the change to Normal Mode and triggering the watchdog is allowed as well as reading and clearing the status registers.

No status information can be lost, even if a bit changes right after the first 7 SPI clock cycles before the SPI frame ends. In this case the status information field will be updated with the next SPI command. However, the flag is already set in the relevant status register. The device status information from the SPI status registers is transmitted in a compressed format with each SPI response on SDO in the so-called Status Information Field register (see also [Table 46](#)). The purpose of this register is to quickly signal changes in dedicated SPI status registers to the microcontroller.

**Table 46 Status Information Field**

Bit in Status Information Field	Corresponding Address Bit	Status Register Description
0		SUPPLY_STAT = OR of all bits on SUP_STAT register
1		TEMP_STAT = OR of all bits on THERM_STAT register
2		BUS_STAT = OR of all bits on BUS_STAT register
3		WAKE_UP = OR of all bits on WK_STAT register
4		HS_STAT = OR of all bits on HS_OL_OC_OT_STAT register
5		DEV_STAT = OR of all bits on DEV_STAT except CRC_STAT and SW_DEV
6		BD_STAT = OR of all bits on DSOV register
7		SPI_CRC_FAIL = (SPI_FAIL) OR (CRC_FAIL)

## Serial Peripheral Interface



**Figure 76 SPI Operation Mode**

### 13.3.1 CRC

The SPI interface includes also 8 Bits (bits 24 to 31) used for Cyclic Redundancy Check (CRC) to ensure data integrity on sent or received SPI command.

The implemented CRC is based on Autosar specification of CRC Routines revision 4.3.0 and in particular the function CRC8-2FH.

The specification are based on the follow table:

**Table 47 CRC8x2FH definition**

CRC result width:	8 bits
Polynomial	2F <sub>H</sub>
Initial Value	FF <sub>H</sub>
Input data reflected	No
Result data reflected	No
XOR value	FF <sub>H</sub>
Check	DF <sub>H</sub>
Magic check	42 <sub>H</sub>

Some examples of CRC calculation are shown in the follow table:

**Table 48 CRC8x2FH calculation example**

Data Bytes (hexadecimal)									CRC
00	00	00	00						12
F2	01	83							C2
0F	AA	00	55						C6
00	FF	55	11						77
33	22	55	AA	BB	CC	DD	EE	FF	11
92	6B	55							33
FF	FF	FF	FF						6C

## Serial Peripheral Interface

### Polynomial

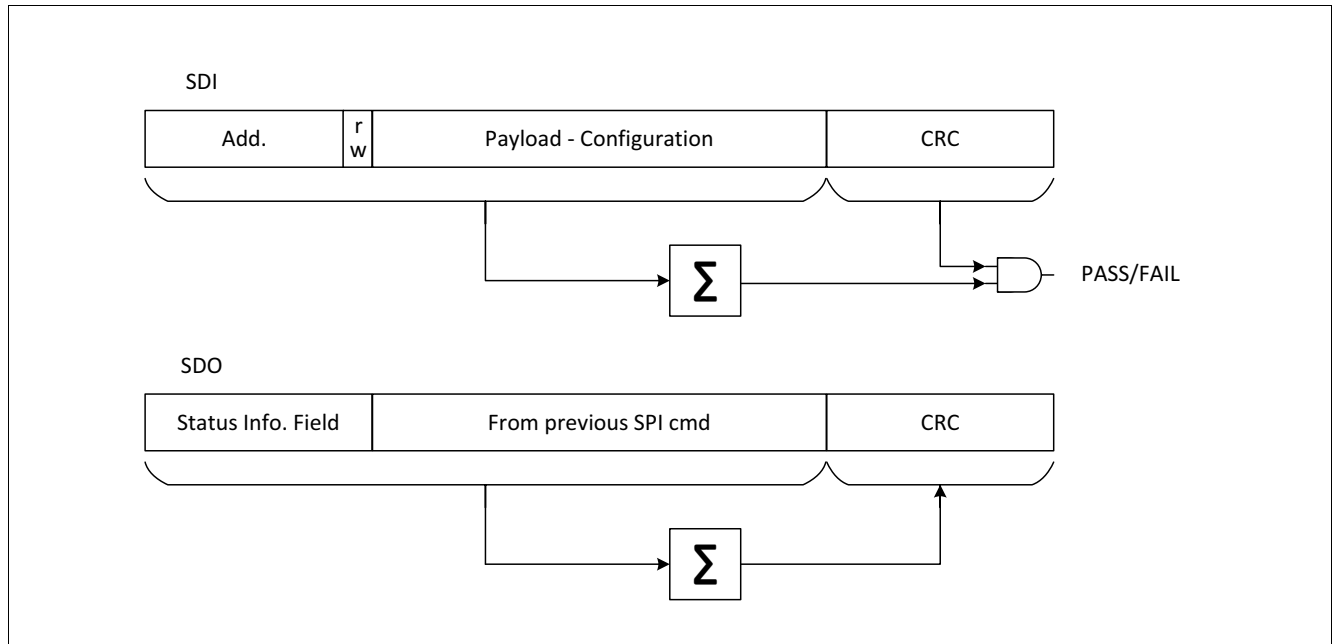
The polynomial is:

$$x^8 + x^5 + x^3 + x^2 + x^1 + x^0 \quad (13.1)$$

### Calculation in SDI and SDO

The calculation of the CRC is done considering the first 24 bits (BIT 0..23) either of SDI or SDO.

The content of SDO Payload (BIT 8..23) is referring the previous data written at the addressed register via SDI.



**Figure 77 CRC calculation**

### CRC Activation and status information

For CRC activation, refer to [Chapter 5.2](#).

The CRC status ([CRC\\_STAT](#)) and failure ([CRC\\_FAIL](#)) are readable on [DEV\\_STAT](#).

Read out of the register which contains the [CRC\\_STAT](#) and [CRC\\_FAIL](#) is done ignoring the CRC field and no failure flag are set.

The [DEV\\_STAT](#) register shall be cleared considering the CRC setting (ON or OFF).

The [CRC\\_STAT](#) bit is read only.

The [CRC\\_FAIL](#) is set in the follow conditions:

- If the CRC is enabled and the  $\mu$ C sends wrong CRC field.
- If the CRC is disabled and the  $\mu$ C sends wrong static pattern (no A5<sub>H</sub>).

### CRC field in case of CRC disabled

In case that the CRC is not activated, the bits needed for CRC field have to be filled with static pattern.

In case of SDI, the CRC field has to be filled with A5<sub>H</sub> (bits 24:31).

In case of SDO, the device will always answer with 5A<sub>H</sub> (bits 24:31).

The status of the CRC is updated accordingly in [CRC\\_STAT](#) bit.

## **13.4 SPI Bit Mapping**

The following figures show the mapping of the registers and the SPI bits of the respective registers.

The Control Registers are Read/Write Register with the following structure:

- Device Control Registers from 000 0001<sub>B</sub> to 000 1011<sub>B</sub>.
- Bridge Driver Control Registers from 001 0000<sub>B</sub> to 001 1101<sub>B</sub>.
- SWK Control Registers from 011 0000<sub>B</sub> to 011 1111<sub>B</sub>.

Depending on bit 7 the bits are only read (setting bit 7 to '0') or also written (setting bit 7 to '1'). The new setting of the bit after a write can be seen with a new read / write command.

The Status Registers are Read/Clear with the following structure:

- Device Status Registers from 100 0000<sub>B</sub> to 100 0110<sub>B</sub>.
- Bridge Driver Status Registers from 101 0000<sub>B</sub> to 101 1011<sub>B</sub>.
- SWK Status Registers from 110 0000<sub>B</sub> to 110 0011<sub>B</sub>.
- Product Family is 111 0000<sub>B</sub>.

The registers can be read or can be cleared (if clearing is possible) depending on bit 7. To clear the payload of one of the Status Registers bit 7 must be set to 1.

The registers **WK\_LVL\_STAT**, and **FAM\_PROD\_STAT**, **SWK\_OSC\_CAL\_STAT**, **SWK\_ECNT\_STAT**, **SWK\_CDR\_STAT** are an exception as they show the actual voltage level at the respective WKx pin (LOW/HIGH), or a fixed family/ product ID respectively and can thus not be cleared.

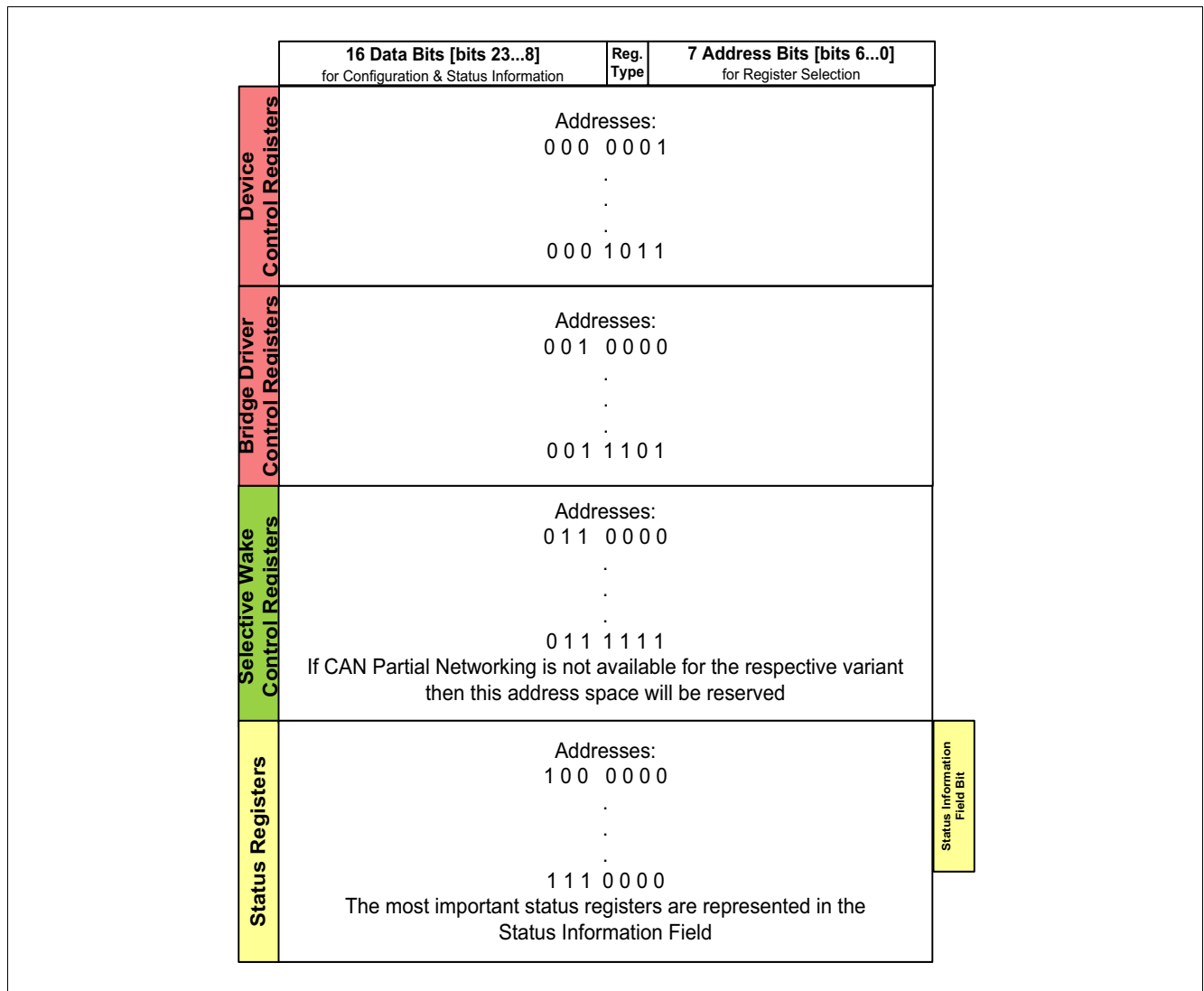
It is recommended for proper diagnosis to clear respective status bits for wake events or failure.

When changing to a different device mode, certain configurations bits will be cleared automatically or modified:

- The device mode bits are updated to the actual status, e.g. when returning to Normal Mode.
- When changing to a low-power mode (Stop Mode or Sleep Mode), the diagnosis bits of the integrated module are not cleared.
- When changing to Stop Mode, the CAN, control bits will not be modified.
- When changing to Sleep Mode, the CAN, control bits will be modified if they were not OFF or wake capable before.

*Note: The detailed behavior of the respective SPI bits and control functions is described in [Chapter 13.5](#), [Chapter 13.6](#) and in the respective module chapter. The bit type be marked as 'rwh' in case the device will modify respective control bits.*

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**Figure 78 SPI Register Mapping Structure**

The detailed register mappings for control registers and status registers are shown in [Table 49](#) and [Table 93](#) respectively.

### 13.4.1 Register Banking

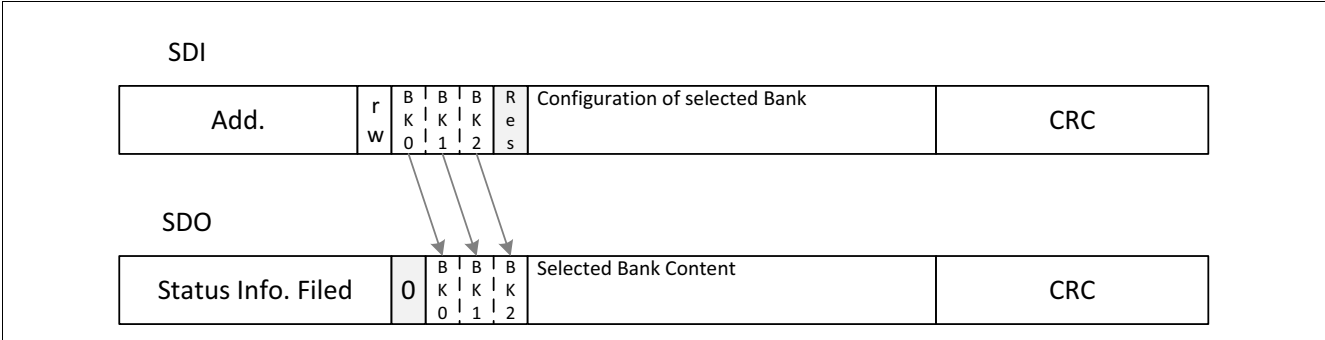
In order to minimize the number of configuration registers, seven registers follow a bank structure.

The banked registers are:

- [WK\\_CTRL](#)
- [PWM\\_CTRL](#)
- [CCP\\_BLK](#)
- [TPRECHG](#)
- [HB\\_ICHG](#)
- [HB\\_PCHG\\_INIT](#)
- [TDON\\_HB\\_CTRL](#)
- [TDOFF\\_HB\\_CTRL](#)

Serial Peripheral Interface

In these register, the first 3 bits of the payload (bit 8 to 10) select the bank that has to be configured. The rest of the payload is used to configure the selected bank (for more details refer to the specific banked register). In case that CRC is used, the CRC calculation is done considering the first 24 bits (from bit 0 to 23). The banked registers can be read like the other configuration registers but in the SDO one '0' is automatically added after the status information field. **Figure 79** shows the structure of SDO in banked register.



**Figure 79 Register read Out of banked register (3 bit banking)**

### 13.5 SPI control registers

READ/WRITE Operation (see also [Chapter 13.3](#)):

- The 'POR / Soft Reset Value' defines the register content after POR or device reset.
- The 'Restart Value' defines the register content after device restart, where 'x' means the bit is unchanged.
- There are different bit types:
  - 'r' = READ: read only bits (or reserved bits).
  - 'rw' = READ/WRITE: readable and writable bits.
  - 'rwh' = READ/WRITE/Hardware: readable/writable bits, which can also be modified by the device hardware.
- Reserved bits are marked as "Reserved" and always read as "0". The respective bits shall also be programmed as "0".
- Reading a register is done word wise by setting the SPI bit 7 to "0" (= Read Only).
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI programming. Exceptions to this behavior are stated at the respective register description and the respective bit type is marked with a 'h' meaning that the device is able to change the register content.

The registers are addressed wordwise.

**Table 49 Register Overview**

Register Short Name	Register Long Name	Offset Address	Page Number
<b>SPI control registers, Device Control Registers</b>			
<a href="#">M_S_CTRL</a>	Mode and Supply Control	0000001 <sub>B</sub>	<a href="#">177</a>
<a href="#">HW_CTRL</a>	Hardware Control	0000010 <sub>B</sub>	<a href="#">179</a>
<a href="#">WD_CTRL</a>	Watchdog Control	0000011 <sub>B</sub>	<a href="#">181</a>
<a href="#">BUS_CTRL</a>	CAN Control	0000100 <sub>B</sub>	<a href="#">183</a>
<a href="#">WK_CTRL</a>	Wake-up Control	0000101 <sub>B</sub>	<a href="#">185</a>
<a href="#">TIMER_CTRL</a>	Timer 1 and Timer 2 Control and Selection	0000110 <sub>B</sub>	<a href="#">187</a>
<a href="#">SW_SD_CTRL</a>	High-Side Switch Shutdown Control	0000111 <sub>B</sub>	<a href="#">189</a>
<a href="#">HS_CTRL</a>	High-Side Switch Control	0001000 <sub>B</sub>	<a href="#">191</a>
<a href="#">INT_MASK</a>	Interrupt Mask Control	0001001 <sub>B</sub>	<a href="#">193</a>
<a href="#">PWM_CTRL</a>	PWM Configuration Control	0001010 <sub>B</sub>	<a href="#">195</a>
<a href="#">SYS_STAT_CTRL</a>	System Status Control	0001011 <sub>B</sub>	<a href="#">196</a>
<b>SPI control registers, Control registers bridge driver</b>			
<a href="#">GENCTRL</a>	General Bridge Control	0010000 <sub>B</sub>	<a href="#">197</a>
<a href="#">CSA</a>	Current sense amplifier	0010001 <sub>B</sub>	<a href="#">199</a>
<a href="#">LS_VDS</a>	Drain-Source monitoring threshold	0010010 <sub>B</sub>	<a href="#">201</a>
<a href="#">HS_VDS</a>	Drain-Source monitoring threshold	0010011 <sub>B</sub>	<a href="#">203</a>
<a href="#">CCP_BLK</a>	CCP and times selection	0010100 <sub>B</sub>	<a href="#">205</a>
<a href="#">HBMODE</a>	Half-Bridge MODE	0010101 <sub>B</sub>	<a href="#">206</a>
<a href="#">TPRECHG</a>	PWM pre-charge and pre-discharge time	0010110 <sub>B</sub>	<a href="#">208</a>

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**Table 49 Register Overview** (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
<b>ST_ICHG</b>	Static charge/discharge current	0010111 <sub>B</sub>	<b>209</b>
<b>HB_ICHG</b>	PWM charge/discharge current	0011000 <sub>B</sub>	<b>210</b>
<b>HB_ICHG_MAX</b>	PWM max. pre-charge/pre-discharge current and diagnostic pull-down	0011001 <sub>B</sub>	<b>211</b>
<b>HB_PCHG_INIT</b>	PWM pre-charge/pre-discharge initialization	0011010 <sub>B</sub>	<b>213</b>
<b>TDON_HB_CTRL</b>	PWM inputs TON configuration	0011011 <sub>B</sub>	<b>214</b>
<b>TDOFF_HB_CTRL</b>	PWM inputs TOFF configuration	0011100 <sub>B</sub>	<b>215</b>
<b>BRAKE</b>	Brake control	0011101 <sub>B</sub>	<b>216</b>
<b>SPI control registers, Selective Wake Registers</b>			
<b>SWK_CTRL</b>	CAN Selective Wake Control	0110000 <sub>B</sub>	<b>218</b>
<b>SWK_BTL1_CTRL</b>	SWK Bit Timing Control	0110001 <sub>B</sub>	<b>219</b>
<b>SWK_ID1_CTRL</b>	SWK WUF Identifier bits 28...13	0110010 <sub>B</sub>	<b>220</b>
<b>SWK_ID0_CTRL</b>	SWK WUF Identifier bits 12...0	0110011 <sub>B</sub>	<b>221</b>
<b>SWK_MASK_ID1_CTRL</b>	SWK WUF Identifier Mask bits 28...13	0110100 <sub>B</sub>	<b>222</b>
<b>SWK_MASK_ID0_CTRL</b>	SWK WUF Identifier Mask bits 12...0	0110101 <sub>B</sub>	<b>224</b>
<b>SWK_DLC_CTRL</b>	SWK Frame Data Length Code Control	0110110 <sub>B</sub>	<b>226</b>
<b>SWK_DATA3_CTRL</b>	SWK Data7-Data6 Register	0110111 <sub>B</sub>	<b>227</b>
<b>SWK_DATA2_CTRL</b>	SWK Data5-Data4 Register	0111000 <sub>B</sub>	<b>228</b>
<b>SWK_DATA1_CTRL</b>	SWK Data3-Data2 Register	0111001 <sub>B</sub>	<b>229</b>
<b>SWK_DATA0_CTRL</b>	SWK Data1-Data0 Register	0111010 <sub>B</sub>	<b>230</b>
<b>SWK_CAN_FD_CTRL</b>	CAN FD Configuration Control Register	0111011 <sub>B</sub>	<b>231</b>
<b>SPI control registers, Selective Wake trim and configuration Registers</b>			
<b>SWK_OSC_TRIM_CTRL</b>	SWK Oscillator Trimming and option Register	0111100 <sub>B</sub>	<b>232</b>
<b>SWK_OSC_CAL_STAT</b>	SWK Oscillator Calibration Register	0111101 <sub>B</sub>	<b>233</b>
<b>SWK_CDR_CTRL</b>	Clock Data Recovery Control Register	0111110 <sub>B</sub>	<b>234</b>
<b>SWK_CDR_LIMIT</b>	SWK Clock Data Recovery Limit Control	0111111 <sub>B</sub>	<b>236</b>



### 13.5.1 Device Control Registers

#### Mode and Supply Control

##### M\_S\_CTRL

##### Mode and Supply Control

(000 0001<sub>B</sub>)

Reset Value: see [Table 50](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE		RES			VCC1_OV_MOD		RES	RSTN_HYS	RES	I_PEAK_TH	RES			VCC1_RT	
rwh		r			rwh		r	rw	r	rw	r			rw	

Field	Bits	Type	Description
<b>MODE</b>	15:14	rwh	<b>Device Mode Control</b> 00 <sub>B</sub> <b>NORMAL</b> , Normal Mode 01 <sub>B</sub> <b>SLEEP</b> , Sleep Mode 10 <sub>B</sub> <b>STOP</b> , Stop Mode 11 <sub>B</sub> <b>RESET</b> , Device reset: Soft reset is executed (configuration of RSTN triggering in bit <a href="#">SOFT_RESET_RO</a> )
<b>RES</b>	13:11	r	<b>Reserved, always reads as 0</b>
<b>VCC1_OV_MOD</b>	10:9	rwh	<b>Reaction in case of VCC1 Over Voltage</b> 00 <sub>B</sub> <b>NO</b> , no reaction 01 <sub>B</sub> <b>INTN</b> , INTN event is generated 10 <sub>B</sub> <b>RSTN</b> , RSTN event is generated 11 <sub>B</sub> <b>FAILSAFE</b> , Fail-Safe Mode is entered
<b>RES</b>	8	r	<b>Reserved, always reads as 0</b>
<b>RSTN_HYS</b>	7	rw	<b>VCC1 Undervoltage Reset Hysteresis Selection (see also <a href="#">Chapter 12.7.1</a> for more information)</b> 0 <sub>B</sub> <b>DEFAULT</b> , default hysteresis applies as specified in the electrical characteristics table 1 <sub>B</sub> <b>HIGHEST</b> , the highest rising threshold (VRT1,R) is always used for the release of the undervoltage reset
<b>RES</b>	6	r	<b>Reserved, always reads as 0</b>
<b>I_PEAK_TH</b>	5	rw	<b>VCC1 Active Peak Threshold Selection</b> 0 <sub>B</sub> <b>LOW</b> , low VCC1 active peak threshold selected 1 <sub>B</sub> <b>HIGH</b> , high VCC1 active peak threshold selected
<b>RES</b>	4:2	r	<b>Reserved, always reads as 0</b>
<b>VCC1_RT</b>	1:0	rw	<b>VCC1 Reset Threshold Control</b> 00 <sub>B</sub> <b>VRT1</b> , Vrt1 selected (highest threshold) 01 <sub>B</sub> <b>VRT2</b> , Vrt2 selected 10 <sub>B</sub> <b>VRT3</b> , Vrt3 selected 11 <sub>B</sub> <b>VRT4</b> , Vrt4 selected

**Table 50**    Reset of **M\_S\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 x0x0 00xx <sub>B</sub>			

**Notes**

1. *It is not possible to change from Stop Mode to Sleep Mode via SPI Command. See also the State Machine Chapter.*
2. *After entering Restart Mode, the MODE bits will be automatically set to Normal Mode.*
3. *The SPI output will always show the previously written state with a Write Command (what has been programmed before).*

## Serial Peripheral Interface

### Hardware Control

#### HW\_CTRL

#### Hardware Control

(000 0010<sub>B</sub>)

Reset Value: see [Table 51](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			TSD2_DEL	VS_OV_SEL	SH_DISABLE	RSTN_DEL	RES		SOFT_RESET_RO	RES	RES		WD_STM_EN_1		RES
r			rw	rw	rw	rw	r		rw	r	r		rwh		r

Field	Bits	Type	Description
RES	15:13	r	<b>Reserved, always reads as 0</b>
TSD2_DEL	12	rw	<b>TSD2 minimum Waiting Time Selection</b> 0 <sub>B</sub> <b>1s</b> , Minimum waiting time until TSD2 is released again is always 1 s 1 <sub>B</sub> <b>64s</b> , Minimum waiting time until TSD2 is released again is 1 s, after >16 TSD2 consecutive events, it will extended x 64
VS_OV_SEL	11	rw	<b>VS OV comparator threshold change</b> 0 <sub>B</sub> <b>20V</b> , Default threshold setting ( $V_{S,OVD1}$ ) 1 <sub>B</sub> <b>30V</b> , increased threshold setting ( $V_{S,OVD2}$ )
SH_DISABLE	10	rw	<b>Sample and hold circuitry disable</b> 0 <sub>B</sub> <b>ENABLED</b> , Gate driver S&H circuitry enabled 1 <sub>B</sub> <b>DISABLED</b> , Gate driver S&H circuitry disabled
RSTN_DEL	9	rw	<b>Reset delay time</b> 0 <sub>B</sub> <b>10ms</b> , Reset delay time 10 ms ( $t_{RD1}$ ) 1 <sub>B</sub> <b>2ms</b> , Reset delay time to 2 ms ( $t_{RD2}$ )
RES	8:7	r	<b>Reserved, always reads as 0</b>
SOFT_RESET_RO	6	rw	<b>Soft Reset Configuration</b> 0 <sub>B</sub> <b>RSTN</b> , RSTN will be triggered (pulled low) during a Soft Reset 1 <sub>B</sub> <b>NO_RSTN</b> , no RSTN trigger during a Soft Reset
RES	5	r	<b>Reserved, always reads as 0</b>
RES	4:3	r	<b>Reserved, always reads as 0</b>
WD_STM_EN_1	2	rwh	<b>Watchdog Deactivation during Stop Mode, bit1</b> 0 <sub>B</sub> <b>ACTIVE</b> , Watchdog is active in Stop Mode 1 <sub>B</sub> <b>INACTIVE</b> , Watchdog is deactivated in Stop Mode
RES	1:0	r	<b>Reserved, always reads as 0</b>

**Table 51** Reset of **HW\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR	0000 0000 0000 0000 <sub>B</sub>			
Soft reset	0000 00x0 0000 0000 <sub>B</sub>			
Restart	000x 00x0 0x00 0000 <sub>B</sub>			

**Notes**

1. *WD\_STM\_EN\_1 will also be cleared when changing from Stop Mode to Normal Mode .*

**Serial Peripheral Interface**

**Watchdog Control**

**WD\_CTRL**

**Watchdog Control**

(000 0011<sub>B</sub>)

Reset Value: see [Table 52](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CHEC KSUM</b>									<b>WD_S TM_E N_0</b>	<b>WD_C FG</b>	<b>WD_E N_WK _BUS</b>	<b>RES</b>			
rw									rwh	rw	rwh	r			rwh

Field	Bits	Type	Description
<b>CHECKSUM</b>	15	rw	<b>Watchdog Setting Check Sum Bit</b> 0 <sub>B</sub> <b>0</b> , Counts as 0 for checksum calculation 1 <sub>B</sub> <b>1</b> , Counts as 1 for checksum calculation
<b>RES</b>	14:7	r	<b>Reserved, always reads as 0</b>
<b>WD_STM_EN_0</b>	6	rwh	<b>Watchdog Deactivation during Stop Mode, bit0</b> 0 <sub>B</sub> <b>ACTIVE</b> , Watchdog is active in Stop Mode 1 <sub>B</sub> <b>INACTIVE</b> , Watchdog is deactivated in Stop Mode
<b>WD_CFG</b>	5	rw	<b>Watchdog Configuration</b> 0 <sub>B</sub> <b>TIMEOUT</b> , Watchdog works as a Time-Out watchdog 1 <sub>B</sub> <b>WINDOW</b> , Watchdog works as a Window watchdog
<b>WD_EN_WK_BUS</b>	4	rwh	<b>Watchdog Enable after Bus Wake in Stop Mode</b> 0 <sub>B</sub> <b>DISABLED</b> , Watchdog will not start after a CAN wake-up event 1 <sub>B</sub> <b>ENABLED</b> , Watchdog starts with a long open window after CAN Wake-up event
<b>RES</b>	3	r	<b>Reserved, always reads as 0</b>
<b>WD_TIMER</b>	2:0	rwh	<b>Watchdog Timer Period</b> 000 <sub>B</sub> <b>10ms</b> , 10ms 001 <sub>B</sub> <b>20ms</b> , 20ms 010 <sub>B</sub> <b>50ms</b> , 50ms 011 <sub>B</sub> <b>100ms</b> , 100ms 100 <sub>B</sub> <b>200ms</b> , 200ms 101 <sub>B</sub> <b>500ms</b> , 500ms 110 <sub>B</sub> <b>1s</b> , 1s 111 <sub>B</sub> <b>10s</b> , 10s

**Table 52** Reset of **WD\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0001 0100 <sub>B</sub>			
Restart	0000 0000 000x 0100 <sub>B</sub>			

**Notes**

1. See also [Chapter 12.2.4](#) for more information on disabling the watchdog in Stop Mode.
2. See chapter [Chapter 12.2.5](#) for more information on the effect of the bit `WD_EN_WK_BUS`.
3. See chapter [Chapter 12.2.3](#) for calculation of checksum.

## Serial Peripheral Interface

### CAN Control

#### BUS\_CTRL

#### CAN Control

(000 0100<sub>B</sub>)

Reset Value: see [Table 53](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								RES	RES	RES	RES		CAN		
r								r	r	r	r		rwh		

Field	Bits	Type	Description
RES	15:8	r	Reserved, always reads as 0
RES	7	r	Reserved, always reads as 0
RES	6	r	Reserved, always reads as 0
RES	5	r	Reserved, always reads as 0
RES	4:3	r	Reserved, always reads as 0
CAN	2:0	rwh	<b>HS-CAN Module Modes</b> 000 <sub>B</sub> <b>OFF</b> , CAN OFF 001 <sub>B</sub> <b>WAKE</b> , CAN is wake capable (no SWK) 010 <sub>B</sub> <b>RECEIVE</b> , CAN Receive Only Mode (no SWK) 011 <sub>B</sub> <b>NORMAL</b> , CAN Normal Mode (no SWK) 100 <sub>B</sub> <b>OFF</b> , CAN OFF 101 <sub>B</sub> <b>WAKE_SWK</b> , CAN is wake capable with SWK 110 <sub>B</sub> <b>RECEIVE_SWK</b> , CAN Receive Only Mode with SWK 111 <sub>B</sub> <b>NORMAL_SWK</b> , CAN Normal Mode with SWK

**Table 53** Reset of **BUS\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0010 0000			
Restart	0000 0000 0000 0xy <sub>B</sub>			

### Notes

- The reset values for CAN, transceivers are marked with 'y' because they will vary depending on the cause of change.
- See [Figure 30](#), for detailed state changes of CAN, transceivers for different device modes.
- The bit CAN\_2 is not modified by the device but can only be changed by the user. Therefore, the bit type is 'rw' compared to bits CAN\_0 and CAN\_1.
- In case SYSERR = 0 and the CAN transceiver is configured to 'x11' while going to Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged. The Receive Only Mode has to be selected by the user before entering Stop Mode. Please refer to [Chapter 5.9](#) for detailed information on the Selective Wake Mode changes.
- Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure, then **BUS\_CTRL** is modified by the device to 0000 0000 xxx0 1001<sub>B</sub> to ensure that the device can be woken again. See also the

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**Serial Peripheral Interface**

*description in [Chapter 8.1](#), and [Chapter 9.2.1](#) for [WK\\_CTRL](#) for other wake sources when entering Fail-Safe Mode.*

6. *When in Software Development Mode the POR/Soft Reset value are: CAN=001<sub>B</sub>, .*



## Serial Peripheral Interface

### Wake-up Control

#### WK\_CTRL

#### Wake-up Control

(000 0101<sub>B</sub>)

Reset Value: see [Table 54](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	RES	WK_FILT			WK_PUPD		RES	WK_EN		RES	WK_BNK				
r	r	rw			rw		r	rw		r	rw				

Field	Bits	Type	Description
RES	15	r	<b>Reserved, always reads as 0</b>
RES	14	r	<b>Reserved, always reads as 0</b>
WK_FILT	13:11	rw	<b>Wake-up Filter Time Configuration</b> 000 <sub>B</sub> <b>16us</b> , Filter with 16 μs filter time (static sensing) 001 <sub>B</sub> <b>64us</b> , Filter with 64 μs filter time (static sensing) 010 <sub>B</sub> <b>TIMER1</b> , Filtering at the end of the on-time; filter time of 16 μs (cyclic sensing) is selected, Timer1 011 <sub>B</sub> <b>TIMER2</b> , Filtering at the end of the on-time; filter time of 16 μs (cyclic sensing) is selected, Timer2 100 <sub>B</sub> <b>SYNC</b> , Filter at the end of settle time (80 μs), filter time of 16 μs (cyclic sensing) is selected, SYNC <sup>1/2)</sup> 101 <sub>B</sub> , reserved 110 <sub>B</sub> , reserved 111 <sub>B</sub> , reserved
WK_PUPD	10:9	rw	<b>WKx Pull-Up/Pull-Down Configuration</b> 00 <sub>B</sub> <b>NO</b> , No pull-up/pull-down selected 01 <sub>B</sub> <b>PULL_DOWN</b> , Pull-down resistor selected 10 <sub>B</sub> <b>PULL_UP</b> , Pull-up resistor selected <sup>3)</sup> 11 <sub>B</sub> <b>AUTO</b> , Automatic switching to pull-up or pull-down
RES	8:7	r	<b>Reserved, always reads as 0</b>
WK_EN	6:5	rw	<b>WKx Enable</b> 00 <sub>B</sub> <b>WK_OFF</b> , WKx module OFF 01 <sub>B</sub> <b>WK_ON</b> , WKx module ON 10 <sub>B</sub> <b>SYNC</b> , OFF or (in case of WK4), it is configured as SYNC input 11 <sub>B</sub> <b>OFF</b> , OFF
RES	4:3	r	<b>Reserved, always reads as 0</b>
WK_BNK	2:0	rw	<b>WKs input Banking</b> 011 <sub>B</sub> <b>WK4</b> , WK4 Module (Bank 4) 100 <sub>B</sub> <b>WK5</b> , WK5 Module (Bank 5) <sup>3)</sup> 101 <sub>B</sub> , reserved 110 <sub>B</sub> , reserved 111 <sub>B</sub> , reserved

1) This setting is available only in case of WK4 configured as [WK\\_EN=10<sub>B</sub>](#).

2) The min TON time for cyclic sense with SYNC is 100 μs.

3) WK5 has a fixed pull-up resistor and is not configurable. So in Bank 5, the [WK\\_PUPD](#) field is reserved.

**Table 54**    **Reset of *WK\_CTRL***

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0010 0000 <sub>B</sub>			
Restart	00xx xxx0 0xx0 0000 <sub>B</sub>			

**Notes**

1. The SYNC functionality is accessible only if the Bank 4 is selected.
2. When selecting a filter time configuration, the user must make sure to also assign the respective timer/SYNC to at least one HS switch during cyclic sense operation.
3. At Fail-Safe Mode entry *WK\_EN* will be automatically changed (by the device) in "01". WK4 if configured as SYNC previously
4. During Fail-Safe Mode the *WK\_FILT* bits are ignored and static-sense with 16 µs filter time is used by default.

**Serial Peripheral Interface**

**Timer 1 and Timer2 Control and Selection**

**TIMER\_CTRL**

**Timer 1 and Timer2 Control and Selection (000 0110<sub>B</sub>)**

Reset Value: see [Table 55](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER2_ON			RES	TIMER2_PER			CYCWK	TIMER1_ON			RES	TIMER1_PER			
rwh			r	rwh			rwh	rwh			r	rwh			

Field	Bits	Type	Description
<b>TIMER2_ON</b>	15:13	rwh	<b>Timer2 On-Time Configuration</b> 000 <sub>B</sub> <b>OFF_LOW</b> , OFF / Low (timer not running, HSx output is low) 001 <sub>B</sub> <b>100us</b> , 0.1ms on-time 010 <sub>B</sub> <b>300us</b> , 0.3ms on-time 011 <sub>B</sub> <b>1ms</b> , 1.0ms on-time 100 <sub>B</sub> <b>10ms</b> , 10ms on-time 101 <sub>B</sub> <b>20ms</b> , 20ms on-time 110 <sub>B</sub> <b>OFF_HIGH</b> , OFF / HIGH (timer not running, HSx output is high) 111 <sub>B</sub> , reserved, same behaviour as 110 <sub>B</sub>
<b>RES</b>	12	r	<b>Reserved, always reads as 0</b>
<b>TIMER2_PER</b>	11:9	rwh	<b>Timer2 Period Configuration</b> 000 <sub>B</sub> <b>10ms</b> , 10ms 001 <sub>B</sub> <b>20ms</b> , 20ms 010 <sub>B</sub> <b>50ms</b> , 50ms 011 <sub>B</sub> <b>100ms</b> , 100ms 100 <sub>B</sub> <b>200ms</b> , 200ms 101 <sub>B</sub> <b>500ms</b> , 500ms 110 <sub>B</sub> <b>1s</b> , 1s 111 <sub>B</sub> <b>2s</b> , 2s
<b>CYCWK</b>	8:7	rwh	<b>Cyclic Wake Configuration</b> 00 <sub>B</sub> <b>DISABLED</b> , Timer1 and Timer2 disabled as wake-up sources 01 <sub>B</sub> <b>TIMER1</b> , Timer1 is enabled as wake-up source (Cyclic Wake) 10 <sub>B</sub> <b>TIMER2</b> , Timer2 is enabled as wake-up source (Cyclic Wake) 11 <sub>B</sub> , reserved

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>TIMER1_ON</b>	6:4	rwh	<b>Timer1 On-Time Configuration</b> 000 <sub>B</sub> <b>OFF_LOW</b> , OFF / Low (timer not running, HSx output is low) 001 <sub>B</sub> <b>100us</b> , 0.1ms on-time 010 <sub>B</sub> <b>300us</b> , 0.3ms on-time 011 <sub>B</sub> <b>1ms</b> , 1.0ms on-time 100 <sub>B</sub> <b>10ms</b> , 10ms on-time 101 <sub>B</sub> <b>20ms</b> , 20ms on-time 110 <sub>B</sub> <b>OFF_HIGH</b> , OFF / HIGH (timer not running, HSx output is high) 111 <sub>B</sub> , reserved, same behaviour as 110 <sub>B</sub>
<b>RES</b>	3	r	<b>Reserved, always reads as 0</b>
<b>TIMER1_PER</b>	2:0	rwh	<b>Timer1 Period Configuration</b> 000 <sub>B</sub> <b>10ms</b> , 10ms 001 <sub>B</sub> <b>20ms</b> , 20ms 010 <sub>B</sub> <b>50ms</b> , 50ms 011 <sub>B</sub> <b>100ms</b> , 100ms 100 <sub>B</sub> <b>200ms</b> , 200ms 101 <sub>B</sub> <b>500ms</b> , 500ms 110 <sub>B</sub> <b>1s</b> , 1s 111 <sub>B</sub> <b>2s</b> , 2s

**Table 55**    **Reset of TIMER\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0000 0000 <sub>B</sub>			

**Notes**

1. The timer must be first assigned and is then automatically activated as soon as the on-time is configured.
2. If cyclic sense is selected and the HSx switch is cleared during Restart Mode then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection. However, the timer settings are not cleared in case of failure not leading to Restart Mode.
3. In case the timer is set as wake sources and cyclic sense is running, then both cyclic sense and cyclic wake will be active at the same time.
4. Timer accuracy is linked to the oscillator accuracy (see Parameter P\_13.12.43).

Serial Peripheral Interface

High-Side Switch Shutdown Control

SW\_SD\_CTRL

High-Side Switch Shutdown Control

(000 0111<sub>B</sub>)

Reset Value: see [Table 56](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	HS3_OV_REC	HS2_OV_REC	HS1_OV_REC	HS_OT_SD_DIS	RES	HS3_OV_SDN_DIS	HS2_OV_SDN_DIS	HS1_OV_SDN_DIS	HS_OT_V_SDN_DIS	HS_OT_V_SD_DIS	RES	HS_UV_REC			
r	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	r	rw			r

Field	Bits	Type	Description
RES	15	r	Reserved, always reads as 0
HS3_OV_REC	14	rw	<b>Switch recovery after removal of VS Overvoltage for HS3</b> 0 <sub>B</sub> <b>DISABLED</b> , Switch recovery is disabled 1 <sub>B</sub> <b>PREVIOUS</b> , Previous state before VS Overvoltage is enabled after Overvoltage condition is removed
HS2_OV_REC	13	rw	<b>Switch recovery after removal of VS Overvoltage for HS2</b> 0 <sub>B</sub> <b>DISABLED</b> , Switch recovery is disabled 1 <sub>B</sub> <b>PREVIOUS</b> , Previous state before VS Overvoltage is enabled after Overvoltage condition is removed
HS1_OV_REC	12	rw	<b>Switch recovery after removal of VS Overvoltage for HS1</b> 0 <sub>B</sub> <b>DISABLED</b> , Switch recovery is disabled 1 <sub>B</sub> <b>PREVIOUS</b> , Previous state before VS Overvoltage is enabled after Overvoltage condition is removed
HS_OT_SD_DIS	11	rw	<b>Shutdown Disabling of all HS in case of Overtemperature event</b> 0 <sub>B</sub> <b>ALL</b> , shutdown for all HSx in case of Overtemperature 1 <sub>B</sub> <b>INDIVIDUAL</b> , individual shutdown in case of Overtemperature
RES	10	r	Reserved, always reads as 0
HS3_OV_SDN_DIS	9	rw	<b>Shutdown Disabling of HS3 in case of input supply overvoltage in Normal Mode</b> 0 <sub>B</sub> <b>ENABLED</b> , shutdown enabled in case of VS Overvoltage 1 <sub>B</sub> <b>DISABLED</b> , shutdown disabled in case of VS Overvoltage

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>HS2_OV_SDN_DIS</b>	8	rw	<b>Shutdown Disabling of HS2 in case of input supply overvoltage in Normal Mode</b> $0_B$ <b>ENABLED</b> , shutdown enabled in case of VS Overvoltage $1_B$ <b>DIASBLED</b> , shudown disabled in case of VS Overvoltage
<b>HS1_OV_SDN_DIS</b>	7	rw	<b>Shutdown Disabling of HS1 in case of input supply overvoltage in Normal Mode</b> $0_B$ <b>ENABLED</b> , shudown enabled in case of VS Overvoltage $1_B$ <b>DISABLED</b> , shudown disabled in case of VS Overvoltage
<b>HS_OV_SDS_DIS</b>	6	rw	<b>Shutdown Disabling of HSx in case of input supply overvoltage in Stop Mode or Sleep Mode</b> $0_B$ <b>ENABLED</b> , shudown enabled in case of VS Overvoltage $1_B$ <b>DISABLED</b> , shudown disabled in case of VS Overvoltage
<b>HS_UV_SD_DIS</b>	5	rw	<b>Shutdown Disabling of HSx in case of input supply undervoltage</b> $0_B$ <b>ENABLED</b> , shudown enabled in case of VS Undervoltage $1_B$ <b>DISABLED</b> , shudown disabled in case of VS Undervoltage
<b>RES</b>	4	r	<b>Reserved, always reads as 0</b>
<b>HS_UV_REC</b>	3	rw	<b>Switch recovery after removal of Undervoltage for HSx</b> $0_B$ <b>DISABLED</b> , Switch recovery is disabled $1_B$ <b>PREVIOUS</b> , Previous state before VS Undervoltage is enabled after Undervoltage considtion is removed
<b>RES</b>	2:0	r	<b>Reserved, always reads as 0</b>

**Table 56**    **Reset of [SW\\_SD\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0xxx x0xx xxx0 x000 <sub>B</sub>			

**Serial Peripheral Interface**

**High-Side Switch Control**

**HS\_CTRL**

**High-Side Switch Control**

**(000 1000<sub>B</sub>)**

**Reset Value: see Table 57**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>				<b>HS3</b>				<b>HS2</b>				<b>HS1</b>			
r				rwh				rwh				rwh			

Field	Bits	Type	Description
<b>RES</b>	15:12	r	<b>Reserved, always reads as 0</b>
<b>HS3</b>	11:8	rwh	<b>HS3 Configuration</b> 0000 <sub>B</sub> <b>OFF</b> , OFF 0001 <sub>B</sub> <b>ON</b> , ON 0010 <sub>B</sub> <b>TIMER1</b> , Controlled by Timer1 0011 <sub>B</sub> <b>TIMER2</b> , Controlled by Timer2 0100 <sub>B</sub> <b>PWM1</b> , Controlled by PWM1 0101 <sub>B</sub> <b>PWM2</b> , Controlled by PWM2 0110 <sub>B</sub> <b>PWM3</b> , Controlled by PWM3 0111 <sub>B</sub> <b>PWM4</b> , Controlled by PWM4 1000 <sub>B</sub> <b>WK4_SYNC</b> , Synchronized with WK4/SYNC 1001 <sub>B</sub> , reserved 1010 <sub>B</sub> , reserved 1011 <sub>B</sub> , reserved 1100 <sub>B</sub> , reserved 1101 <sub>B</sub> , reserved 1110 <sub>B</sub> , reserved 1111 <sub>B</sub> , reserved
<b>HS2</b>	7:4	rwh	<b>HS2 Configuration</b> 0000 <sub>B</sub> <b>OFF</b> , OFF 0001 <sub>B</sub> <b>ON</b> , ON 0010 <sub>B</sub> <b>TIMER1</b> , Controlled by Timer1 0011 <sub>B</sub> <b>TIMER2</b> , Controlled by Timer2 0100 <sub>B</sub> <b>PWM1</b> , Controlled by PWM1 0101 <sub>B</sub> <b>PWM2</b> , Controlled by PWM2 0110 <sub>B</sub> <b>PWM3</b> , Controlled by PWM3 0111 <sub>B</sub> <b>PWM4</b> , Controlled by PWM4 1000 <sub>B</sub> <b>WK4_SYNC</b> , Synchronized with WK4/SYNC 1001 <sub>B</sub> , reserved 1010 <sub>B</sub> , reserved 1011 <sub>B</sub> , reserved 1100 <sub>B</sub> , reserved 1101 <sub>B</sub> , reserved 1110 <sub>B</sub> , reserved 1111 <sub>B</sub> , reserved

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>HS1</b>	3:0	rwh	<b>HS1 Configuration</b> 0000 <sub>B</sub> <b>OFF</b> , OFF 0001 <sub>B</sub> <b>ON</b> , ON 0010 <sub>B</sub> <b>TIMER1</b> , Controlled by Timer1 0011 <sub>B</sub> <b>TIMER2</b> , Controlled by Timer2 0100 <sub>B</sub> <b>PWM1</b> , Controlled by PWM1 0101 <sub>B</sub> <b>PWM2</b> , Controlled by PWM2 0110 <sub>B</sub> <b>PWM3</b> , Controlled by PWM3 0111 <sub>B</sub> <b>PWM4</b> , Controlled by PWM4 1000 <sub>B</sub> <b>WK4_SYNC</b> , Synchronized with WK4/SYNC 1001 <sub>B</sub> , reserved 1010 <sub>B</sub> , reserved 1011 <sub>B</sub> , reserved 1100 <sub>B</sub> , reserved 1101 <sub>B</sub> , reserved 1110 <sub>B</sub> , reserved 1111 <sub>B</sub> , reserved

**Table 57**    **Reset of [HS\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0000 0000 <sub>B</sub>			

PWMx in this register designates the internal PWM generators for the integrated high-side switches.



**Serial Peripheral Interface**

**Interrupt Mask Control<sup>1)</sup>**

**INT\_MASK**

**Interrupt Mask Control**

(000 1001<sub>B</sub>)

Reset Value: see [Table 58](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES							INTN_CYC_EN	WD_SDM_DISABLE	WD_SDM	SPI_CRC_FAIL	BD_STAT	HS_STAT	BUS_STAT	TEMP_STAT	SUPPLY_STAT
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>RES</b>	15:9	r	<b>Reserved, always reads as 0</b>
<b>INTN_CYC_EN</b>	8	rw	<b>Periodical INTN generation</b> 0 <sub>B</sub> <b>DISABLED</b> , no periodical INTN event generated in case of pending interrupts 1 <sub>B</sub> <b>ENABLED</b> , periodical INTN event generated in case of pending interrupts
<b>WD_SDM_DISABLE</b>	7	rw	<b>Disable Watchdog in Software Development Mode</b> 0 <sub>B</sub> <b>ENABLED</b> , WD is enabled in Software Development Mode 1 <sub>B</sub> <b>DISABLED</b> , WD is disabled in Software Development Mode
<b>WD_SDM</b>	6	rw	<b>Watchdog failure in Software Development Mode</b> 0 <sub>B</sub> <b>DISABLED</b> , no INTN event generated in case of WD trigger failure in Software Development Mode 1 <sub>B</sub> <b>ENABLED</b> , one INTN event is generated in case of WD trigger failure in Software Development Mode
<b>SPI_CRC_FAIL</b>	5	rw	<b>SPI and CRC interrupt generation</b> 0 <sub>B</sub> <b>DISABLED</b> , no INTN event generated in case of SPI_FAIL or CRC_FAIL 1 <sub>B</sub> <b>ENABLED</b> , one INTN event is generated in case of SPI_FAIL or CRC_FAIL
<b>BD_STAT</b>	4	rw	<b>Bridge Driver Interrupt generation</b> 0 <sub>B</sub> <b>DISABLED</b> , no INTN event generated in case BD_STAT (on Status Information Field) is set 1 <sub>B</sub> <b>ENABLED</b> , one INTN event generated in case BD_STAT (on Status Information Field) is set
<b>HS_STAT</b>	3	rw	<b>High Side Interrupt generation</b> 0 <sub>B</sub> <b>DISABLED</b> , no INTN event generated in case HS_STAT (on Status Information Field) is set 1 <sub>B</sub> <b>ENABLED</b> , one INTN event generated in case HS_STAT (on Status Information Field) is set

1) Every event will generate a signal on the INTN pin (when masked accordingly).  
Even if the status-bit was already set in the corresponding status-register it can still trigger a signal on the INTN pin.

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>BUS_STAT</b>	2	rw	<b>BUS Interrupt generation</b> $0_B$ <b>DISABLED</b> , no INTN event generated in case BUS_STAT (on Status Information Field) is set $1_B$ <b>ENABLED</b> , one INTN event generated in case BUS_STAT (on Status Information Field) is set
<b>TEMP_STAT</b>	1	rw	<b>Temperature Interrupt generation</b> $0_B$ <b>DISABLED</b> , no INTN event generated in case TEMP_STAT (on Status Information Field) is set $1_B$ <b>ENABLED</b> , one INTN event generated in case TEMP_STAT (on Status Information Field) is set
<b>SUPPLY_STAT</b>	0	rw	<b>SUPPLY Status Interrupt generation</b> $0_B$ <b>DISABLED</b> , no INTN event generated in case SUPPLY_STAT (on Status Information Field) is set $1_B$ <b>ENABLED</b> , one INTN event generated in case SUPPLY_STAT (on Status Information Field) is set

**Table 58**    **Reset of INT\_MASK**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0001 0100 0000 <sub>B</sub>			
Restart	0000 000x xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

**PWM Configuration Control**

**PWM\_CTRL**

**PWM Configuration Control**

(000 1010<sub>B</sub>)

Reset Value: see [Table 59](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	PWM_FREQ	PWM_DC										RES	PWM_BNK		
r	rw	rw										r	rw		

Field	Bits	Type	Description
RES	15	r	<b>Reserved, always reads as 0</b>
PWM_FREQ	14	rw	<b>PWM generator Frequency Setting</b> 0 <sub>B</sub> <b>100Hz</b> , 100Hz is selected 1 <sub>B</sub> <b>200Hz</b> , 200Hz is selected
PWM_DC	13:4	rw	<b>PWM Duty Cycle Setting (bit4 = LSB; bit13 = MSB)</b> 00 0000 0000 <sub>B</sub> , 100% OFF, i.e. HS = OFF xx xxxx xxxx <sub>B</sub> , ON with duty cycle fraction of 1024 11 1111 1111 <sub>B</sub> , 100% ON, i.e. HS = ON
RES	3	r	<b>Reserved, always reads as 0</b>
PWM_BNK	2:0	rw	<b>Internal PWM generator selection</b> 000 <sub>B</sub> <b>PWM1</b> , PWM1 Module 001 <sub>B</sub> <b>PWM2</b> , PWM2 Module 010 <sub>B</sub> <b>PWM3</b> , PWM3 Module 011 <sub>B</sub> <b>PWM4</b> , PWM4 Module 1xx <sub>B</sub> , Don't care

**Table 59 Reset of PWM\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0xxx xxxx xxxx 0000 <sub>B</sub>			

PWMx in this register designates the internal PWM generators for the integrated high-side switches.

**Notes**

1. 0% and 100% duty cycle settings are used to have the switch turned ON or OFF respectively.
2. The desired duty cycle should be set first before the HSx is enabled as PWM.
3. The PWM signal is correct only after at least one PWM pulse.
4. PWM generator accuracy is linked to the oscillator accuracy (see parameter P\_13.12.43).

**Serial Peripheral Interface**

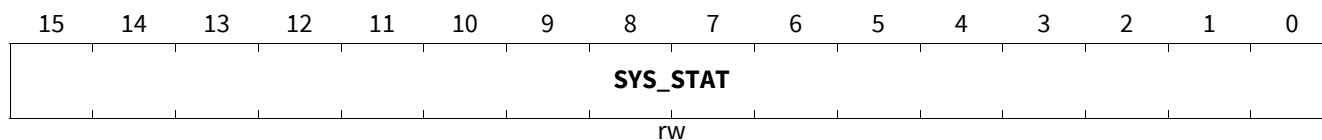
**System Status Control**

**SYS\_STAT\_CTRL**

**System Status Control**

**(000 1011<sub>B</sub>)**

**Reset Value: see Table 60**



Field	Bits	Type	Description
<b>SYS_STAT</b>	15:0	rw	<b>System Status Control (bit0=LSB; bit15=MSB)</b> Dedicated bytes for system configuration, access only by microcontroller. Cleared after power up and soft reset.

**Table 60**    **Reset of SYS\_STAT\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR / Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

*Note:        This register is intended for storing system configuration of the ECU by the microcontroller and is only accessible in Normal Mode. The register is not accessible by the TLE9563-3QX and is also not cleared after Fail-Safe or Restart Mode. It allows the microcontroller to quickly store system configuration without losing data.*

## 13.5.2 Control registers bridge driver

### General Bridge Control

#### GENCTRL

#### General Bridge Control

(001 0000<sub>B</sub>)

Reset Value: see [Table 61](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>BDFREQ</b>	<b>RES</b>	<b>RES</b>	<b>CPUVTH</b>	<b>FET_LVL</b>	<b>CPSTGA</b>	<b>BDOV_REC</b>	<b>IPCHGADT</b>		<b>AGC</b>	<b>CPEN</b>	<b>POCHGDIS</b>	<b>AGCFILT</b>	<b>EN_GEN_CH_ECK</b>	<b>IHOLD</b>	<b>FMODE</b>
rw	r	r	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>BDFREQ</b>	15	rw	<b>Bridge driver synchronization frequency</b> 0 <sub>B</sub> <b>18MHz</b> , typ. 18.75 MHz (default) 1 <sub>B</sub> <b>37MHz</b> , typ. 37.5 MHz
<b>RES</b>	14	r	<b>Reserved, always reads as 0</b>
<b>RES</b>	13	r	<b>Reserved, always reads as 0</b>
<b>CPUVTH</b>	12	rw	<b>Charge pump under voltage (referred to VS)</b> 0 <sub>B</sub> <b>TH1</b> , (default) CPUV threshold 1 for FET_LVL = 0, CPUV threshold 1 for FET_LVL = 1 1 <sub>B</sub> <b>TH2</b> , CPUV threshold 2 for FET_LVL = 0, CPUV threshold 2 for FET_LVL = 1
<b>FET_LVL</b>	11	rw	<b>External MOSFET normal / logic level selection</b> 0 <sub>B</sub> <b>LOGIC</b> , Logic level MOSFET selected 1 <sub>B</sub> <b>NORMAL</b> , Normal level MOSFET selected(default)
<b>CPSTGA</b>	10	rw	<b>Automatic switchover between dual and single charge pump stage</b> 0 <sub>B</sub> <b>INACTIVE</b> , Automatic switch over deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Automatic switch over activated
<b>BDOV_REC</b>	9	rw	<b>Bridge driver recover from VS and VSINT Overvoltage</b> 0 <sub>B</sub> <b>INACTIVE</b> , Recover deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Recover activated
<b>IPCHGADT</b>	8	rw	<b>Adaptation of the pre-charge and pre-discharge current</b> 0 <sub>B</sub> <b>1STEP</b> , 1 current step (default) 1 <sub>B</sub> <b>2STEPS</b> , 2 current steps

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>AGC</b>	7:6	rw	<b>Adaptive gate control</b> 00 <sub>B</sub> <b>INACTIVE1</b> , (default) Adaptive gate control disabled, pre-charge and pre-discharge disabled 01 <sub>B</sub> <b>INACTIVE2</b> , Adaptive gate control disabled, precharge is enabled with IPRECHG = IPCHGINIT, predischage is enabled with IPREDCHG = IPDCHGINIT 10 <sub>B</sub> <b>ACTIVE</b> , Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted 11 <sub>B</sub> , reserved. Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted
<b>CPEN</b>	5	rw	<b>CPEN</b> 0 <sub>B</sub> <b>DISABLED</b> , Charge pump disabled (default) 1 <sub>B</sub> <b>ENABLED</b> , Charge pump enabled
<b>POCHGDIS</b>	4	rw	<b>Postcharge disable bit</b> 0 <sub>B</sub> <b>ENABLED</b> , The postcharge phase is enabled during PWM (default) 1 <sub>B</sub> <b>DISABLED</b> , The postcharge phase is disabled during PWM
<b>AGCFILT</b>	3	rw	<b>Filter for adaptive gate control</b> 0 <sub>B</sub> <b>NO_FILT</b> , No filter applied (default) 1 <sub>B</sub> <b>FILT_APPL</b> , Filter applied
<b>EN_GEN_CHECK</b>	2	rw	<b>Detection of active / FW MOSFET</b> 0 <sub>B</sub> <b>DISABLED</b> , Detection disabled (default) 1 <sub>B</sub> <b>ENABLED</b> , Detection enabled
<b>IHOLD</b>	1	rw	<b>Gate driver hold current IHOLD</b> 0 <sub>B</sub> <b>TH1</b> , (default) Charge: $I_{CHG15}$ , discharge $I_{DCHG15}$ 1 <sub>B</sub> <b>TH2</b> , Charge: $I_{CHG20}$ , discharge: $I_{DCHG20}$
<b>FMODE</b>	0	rw	<b>Frequency modulation of the charge pump</b> 0 <sub>B</sub> <b>NO</b> , No modulation 1 <sub>B</sub> <b>15KHz</b> , Modulation frequency 15.6 kHz (default)

**Table 61** Reset of **GENCTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 1000 0000 0001 <sub>B</sub>			
Restart	x00x xxxx xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

**Current sense amplifier**

**CSA**

**Current sense amplifier**

**(001 0001<sub>B</sub>)**

**Reset Value: see Table 62**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>					<b>PWM_NB</b>	<b>CSO_CAP</b>	<b>CSD</b>	<b>OCFILT</b>		<b>CSA_OFF</b>	<b>OCTH</b>		<b>CSAG</b>		<b>OCEN</b>
r					rw	rw	rw	rw		rw	rw		rw		rw

Field	Bits	Type	Description
<b>RES</b>	15:11	r	<b>Reserved, always reads as 0</b>
<b>PWM_NB</b>	10	rw	<b>Selection of 3 or 6 PWM inputs</b> 0 <sub>B</sub> <b>3PWM</b> , 3 PWM inputs (default) 1 <sub>B</sub> <b>6PWM</b> , 6 PWM inputs
<b>CSO_CAP</b>	9	rw	<b>Capacitance connected to the current sense amplifier output (CCSO), see also Chapter 12.12.4</b> 0 <sub>B</sub> <b>400pF</b> , CCSO < 400 pF (default) 1 <sub>B</sub> <b>2nF</b> , 400 pF < CCSO < 2.2 nF
<b>CSD</b>	8	rw	<b>Direction of the current sense amplifier</b> 0 <sub>B</sub> <b>UNI</b> , Unidirectional 1 <sub>B</sub> <b>BI</b> , Bidirectional (default)
<b>OCFILT</b>	7:6	rw	<b>Overcurrent filter time of CSO</b> 00 <sub>B</sub> <b>6us</b> , 6 μs (default) 01 <sub>B</sub> <b>10us</b> , 10 μs 10 <sub>B</sub> <b>50us</b> , 50 μs 11 <sub>B</sub> <b>100us</b> , 100 μs
<b>CSA_OFF</b>	5	rw	<b>CSA OFF</b> 0 <sub>B</sub> <b>CSA_ON</b> , CSA enabled 1 <sub>B</sub> <b>CSA_OFF</b> , CSA disabled (default)
<b>OCTH</b>	4:3	rw	<b>Overcurrent detection threshold of CSO</b> 00 <sub>B</sub> <b>TH1</b> , $V_{CSO} > V_{CC1}/2 + 2 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 2 \times V_{CC1}/20$ (default) 01 <sub>B</sub> <b>TH2</b> , $V_{CSO} > V_{CC1}/2 + 4 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 4 \times V_{CC1}/20$ 10 <sub>B</sub> <b>TH3</b> , $V_{CSO} > V_{CC1}/2 + 5 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 5 \times V_{CC1}/20$ 11 <sub>B</sub> <b>TH4</b> , $V_{CSO} > V_{CC1}/2 + 6 \times V_{CC1}/20$ or $V_{CSO} < V_{CC1}/2 - 6 \times V_{CC1}/20$
<b>CSAG</b>	2:1	rw	<b>Gain of the current sense amplifier</b> 00 <sub>B</sub> <b>10VV</b> , $G_{DIFF10}$ (default) 01 <sub>B</sub> <b>20VV</b> , $G_{DIFF20}$ 10 <sub>B</sub> <b>40VV</b> , $G_{DIFF40}$ 11 <sub>B</sub> <b>60VV</b> , $G_{DIFF60}$
<b>OCEN</b>	0	rw	<b>Overcurrent shutdown Enable</b> 0 <sub>B</sub> <b>DISABLED</b> , Disabled 1 <sub>B</sub> <b>ENABLED</b> , Enabled (default)

**Table 62**    **Reset of CSA**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0001 0010 0001 <sub>B</sub>			
Restart	0000 0xxx xxxx xxx1 <sub>B</sub>			



**Serial Peripheral Interface**

**Drain-Source monitoring threshold LS1-3**

**LS\_VDS**

**VDS monitoring threshold LS1-3**

**(001 0010<sub>B</sub>)**

**Reset Value: see Table 63**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>		<b>TFVDS</b>		<b>RES</b>		<b>LS3VDSTH</b>		<b>LS2VDSTH</b>		<b>LS1VDSTH</b>					
r		rw		r		rw		rw		rw		rw			

Field	Bits	Type	Description
<b>RES</b>	15:14	r	<b>Reserved. Always read as 0</b>
<b>TFVDS</b>	13:12	rw	<b>Filter time of drain-source voltage monitoring</b> 00 <sub>B</sub> <b>500ns</b> , 0.5 μs (default) 01 <sub>B</sub> <b>1us</b> , 1 μs 10 <sub>B</sub> <b>2us</b> , 2 μs 11 <sub>B</sub> <b>6us</b> , 6 μs
<b>RES</b>	11:9	r	<b>Reserved, always reads as 0</b>
<b>LS3VDSTH</b>	8:6	rw	<b>LS3 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16 V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V
<b>LS2VDSTH</b>	5:3	rw	<b>LS2 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V
<b>LS1VDSTH</b>	2:0	rw	<b>LS1 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16 V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V

**Table 63**    Reset of **LS\_VDS**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0100 1001 <sub>B</sub>	0000 0000 0000 0000		
Restart	0000 000x xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

**Drain-Source monitoring Threshold HS1-3**

**HS\_VDS**

**VDS monitoring threshold HS1-3**

**(001 0011<sub>B</sub>)**

**Reset Value: see Table 64**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>		<b>RES</b>	<b>DEEP_ADAP</b>	<b>RES</b>			<b>HS3VDSTH</b>			<b>HS2VDSTH</b>			<b>HS1VDSTH</b>		
r		rw	rw	r			rw			rw			rw		

Field	Bits	Type	Description
<b>RES</b>	15:14	r	<b>Reserved. Always read as 0</b>
<b>RES</b>	13	rw	<b>Reserved. This bit must be programmed to '0'</b>
<b>DEEP_ADAP</b>	12	rw	<b>Deep adaptation enable</b> 0 <sub>B</sub> <b>NO_DEEP_ADAP</b> , Deep adaptation disabled (default) 1 <sub>B</sub> <b>DEEP_ADAP</b> , Deep adaptation enabled
<b>RES</b>	11:9	r	<b>Reserved, always reads as 0</b>
<b>HS3VDSTH</b>	8:6	rw	<b>HS3 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16 V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V
<b>HS2VDSTH</b>	5:3	rw	<b>HS2 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16 V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V
<b>HS1VDSTH</b>	2:0	rw	<b>HS1 drain-source overvoltage threshold</b> 000 <sub>B</sub> <b>160mV</b> , 0.16 V 001 <sub>B</sub> <b>200mV</b> , 0.20 V (default) 010 <sub>B</sub> <b>300mV</b> , 0.30 V 011 <sub>B</sub> <b>400mV</b> , 0.40 V 100 <sub>B</sub> <b>500mV</b> , 0.50 V 101 <sub>B</sub> <b>600mV</b> , 0.60 V 110 <sub>B</sub> <b>800mV</b> , 0.80 V 111 <sub>B</sub> <b>2V</b> , 2.0 V

**Table 64**    Reset of **HS\_VDS**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0100 1001 <sub>B</sub>			
Restart	00xx 000x xxxx xxxx <sub>B</sub>			

## Serial Peripheral Interface

### CCP and times selection

#### CCP\_BLK

#### CCP and times selection

(001 0100<sub>B</sub>)

Reset Value: see [Table 65](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLANK				TCCP				RES				CCP_BNK			
rw				rw				r				rw			

Field	Bits	Type	Description
TBLANK	15:12	rw	<b>Blank time</b> $\text{nom. tHBxBLANK} = 587 \text{ ns} + 266 \times T[3:0]_D$ The CCP_BNK bits select the blank time for the FW or active MOSFET and the half-bridge HBx Reset of active and FW tHBxBLANK: 2450 ns typ.
TCCP	11:8	rw	<b>Cross-current protection time</b> $\text{nom. tHBxCCP} = 587 \text{ ns} + 266 \times TCCP[3:0]_D$ The CCP_BNK bits select the cross-current protection time for the FW or active MOSFET and the half-bridge HBx Reset of all active and FW tHBxCCP: 2450 ns typ.
RES	7:3	r	<b>Reserved, always reads as 0</b>
CCP_BNK	2:0	rw	<b>Cross-current and time banking</b> 000 <sub>B</sub> <b>ACT_HB1</b> , Active blank and cross-current prot. times for HB1 (default) 001 <sub>B</sub> <b>ACT_HB2</b> , Active blank and cross-current prot. times for HB2 010 <sub>B</sub> <b>ACT_HB3</b> , Active blank and cross-current prot. times for HB3 011 <sub>B</sub> <b>RES</b> , reserved 100 <sub>B</sub> <b>FW_HB1</b> , FW blank and cross-current prot. times for HB1 101 <sub>B</sub> <b>FW_HB2</b> , FW blank and cross-current prot. times for HB2 110 <sub>B</sub> <b>FW_HB3</b> , FW blank and cross-current prot. for times for HB3 111 <sub>B</sub> <b>RES</b> , reserved

**Table 65** Reset of **CCP\_BLK**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0111 0111 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx 0000 0000 <sub>B</sub>			

**Serial Peripheral Interface**

**Half-Bridge MODE**

**HBMODE**

**Half-Bridge MODE**

(001 0101<sub>B</sub>)

Reset Value: see [Table 66](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				HB3MODE		AFW3	HB3_PWM_EN	HB2MODE		AFW2	HB2_PWM_EN	HB1MODE		AFW1	HB1_PWM_EN
r				rw		rw	rw	rw		rw	rw	rw		rw	rw

Field	Bits	Type	Description
<b>RES</b>	15:12	r	<b>Reserved, always reads as 0</b>
<b>HB3MODE</b>	11:10	rw	<b>Half-bridge 3 MODE selection</b> 00 <sub>B</sub> <b>PASSIVE_OFF</b> , LS3 and HS3 are off by passive discharge (default) 01 <sub>B</sub> <b>LS3_ON</b> , LS3 is ON 10 <sub>B</sub> <b>HS3_ON</b> , HS3 is ON 11 <sub>B</sub> <b>ACTIVE_OFF</b> , LS3 and HS3 kept off by the active discharge
<b>AFW3</b>	9	rw	<b>Active freewheeling for half-bridge 3 during PWM</b> 0 <sub>B</sub> <b>DISABLED</b> , active freewheeling disabled 1 <sub>B</sub> <b>ENABLED</b> , active freewheeling enabled (default)
<b>HB3_PWM_EN</b>	8	rw	<b>PWM mode for half-bridge 3</b> 0 <sub>B</sub> <b>INACTIVE</b> , PWM deactivated for HB2(default) 1 <sub>B</sub> <b>ACTIVE</b> , PWM activated for HB2
<b>HB2MODE</b>	7:6	rw	<b>Half-bridge 2 MODE selection</b> 00 <sub>B</sub> <b>PASSIVE_OFF</b> , LS2 and HS2 are off by passive discharge (default) 01 <sub>B</sub> <b>LS2_ON</b> , LS2 is ON 10 <sub>B</sub> <b>HS2_ON</b> , HS2 is ON 11 <sub>B</sub> <b>ACTIVE_OFF</b> , LS2 and HS2 kept off by the active discharge
<b>AFW2</b>	5	rw	<b>Active freewheeling for half-bridge 2 during PWM</b> 0 <sub>B</sub> <b>DISABLED</b> , active freewheeling disabled 1 <sub>B</sub> <b>ENABLED</b> , active freewheeling enabled (default)
<b>HB2_PWM_EN</b>	4	rw	<b>PWM mode for half-bridge 2</b> 0 <sub>B</sub> <b>INACTIVE</b> , PWM deactivated for HB2(default) 1 <sub>B</sub> <b>ACTIVE</b> , PWM activated for HB2
<b>HB1MODE</b>	3:2	rw	<b>Half-bridge 1 MODE selection</b> 00 <sub>B</sub> <b>PASSIVE_OFF</b> , LS1 and HS1 are off by passive discharge (default) 01 <sub>B</sub> <b>LS1_ON</b> , LS1 is ON 10 <sub>B</sub> <b>HS1_ON</b> , HS1 is ON 11 <sub>B</sub> <b>ACTIVE_OFF</b> , LS1 and HS1 kept off by the active discharge

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>AFW1</b>	1	rw	<b>Active freewheeling for half-bridge 1 during PWM</b> $0_B$ <b>DISABLED</b> , active freewheeling disabled $1_B$ <b>ENABLED</b> , active freewheeling enabled (default)
<b>HB1_PWM_EN</b>	0	rw	<b>PWM mode for half-bridge 1</b> $0_B$ <b>INACTIVE</b> , PWM deactivated for HB1 (default) $1_B$ <b>ACTIVE</b> , PWM activated for HB1

**Table 66** Reset of **HBMODE**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0010 0010 0010 <sub>B</sub>			
Restart	0000 0010 0010 0010 <sub>B</sub>			

**Serial Peripheral Interface**

**HB pre-charge and pre-discharge time**

**TPRECHG**

**HB pre-charge and pre-discharge time**

**(001 0110<sub>B</sub>)**

**Reset Value: see Table 67**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>			<b>TPCHG3</b>			<b>TPCHG2</b>			<b>TPCHG1</b>			<b>RES</b>	<b>TPCHG_BNK</b>		
r			rw			rw			rw			r	rw		

Field	Bits	Type	Description
<b>RES</b>	15:13	r	<b>Reserved, always reads as 0</b>
<b>TPCHG3</b>	12:10	rw	<b>If TPCHG_BNK=0: precharge time of HB 3, If TPCHG_BNK=1: predischage time of HB 3</b>
<b>TPCHG2</b>	9:7	rw	<b>If TPCHG_BNK=0: precharge time of HB 2, If TPCHG_BNK=1: predischage time of HB 2</b>
<b>TPCHG1</b>	6:4	rw	<b>If TPCHG_BNK=0: precharge time of HB 1, If TPCHG_BNK=1: predischage time of HB 1</b>
<b>RES</b>	3	r	<b>Reserved, always read as 0</b>
<b>TPCHG_BNK</b>	2:0	rw	<b>Precharge/predischage time selection</b> 000 <sub>B</sub> <b>PRECHARGE</b> , Precharge time selected (default) 001 <sub>B</sub> <b>PREDISCHARGE</b> , Predischage time selected x1x <sub>B</sub> , wrong setting of TPCHG_BNK 1xx <sub>B</sub> , wrong setting of TPCHG_BNK

**Table 67 Reset of TPRECHG**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	000x xxxx xxxx 0000 <sub>B</sub>			



**Serial Peripheral Interface**

**Static charge/discharge current**

**ST\_ICHG**

**Static charge/discharge current**

**(001 0111<sub>B</sub>)**

**Reset Value: see Table 68**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>				<b>ICHGST3</b>				<b>ICHGST2</b>				<b>ICHGST1</b>			
r				rw				rw				rw			

Field	Bits	Type	Description
<b>RES</b>	15:12	r	<b>Reserved, always read as 0</b>
<b>ICHGST3</b>	11:8	rw	<b>Static charge and discharge currents of HB3</b> Refer to <a href="#">Table 27</a> Default: 0100 <sub>B</sub> - charge: $I_{CHG16}$ , 15.3 mA typ., discharge: $I_{DCHG16}$ , 15.1 mA typ.
<b>ICHGST2</b>	7:4	rw	<b>Static charge and discharge currents of HB2</b> Refer to Default: 0100 <sub>B</sub> - charge: $I_{CHG16}$ , 15.3 mA typ., discharge: $I_{DCHG16}$ , 15.1 mA typ.
<b>ICHGST1</b>	3:0	rw	<b>Static charge and discharge currents of HB1</b> Refer to <a href="#">Table 27</a> Default: 0100 <sub>B</sub> - charge: $I_{CHG16}$ , 15.3 mA typ., discharge: $I_{DCHG16}$ , 15.1 mA typ.

**Table 68 Reset of ST\_ICHG**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0100 0100 0100 <sub>B</sub>			
Restart	0000 xxxx xxxx xxxx <sub>B</sub>			

Serial Peripheral Interface

HB charge/discharge currents for PWM operation

HB\_ICHG

HB charge/discharge currents for PWM operation

(001 1000<sub>B</sub>)

Reset Value: see [Table 69](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDCHG						ICHG						RES	ICHG_BNK		
rw						rw						r	rw		

Field	Bits	Type	Description
IDCHG	15:10	rw	<p>If <b>ICHG_BNK</b>=0xx<sub>B</sub>: Discharge current of HBx active MOSFET</p> <p>If <b>ICHG_BNK</b>=1xx<sub>B</sub>: Reserved. Always read as '0'</p> <p>Default value for all active MOSFETs discharge currents: 001111<sub>B</sub>, I<sub>DCHG15</sub></p> <p>Refer to <a href="#">Table 35</a> for the configuration of the discharge current</p>
ICHG	9:4	rw	<p>If <b>ICHG_BNK</b>=0xx<sub>B</sub>: Charge current of HBx active MOSFET</p> <p>If <b>ICHG_BNK</b>=1xx<sub>B</sub>: Charge and discharge current of HBx FW MOSFETs</p> <p>Default value for all active MOSFETs charge currents and all FW MOSFETs charge/discharge currents: 001101<sub>B</sub>, I<sub>CHG13</sub></p> <p>Refer to <a href="#">Table 34</a> for the configuration of the charge current of the active and FW MOSFET</p> <p>Refer to <a href="#">Table 35</a> for the configuration of the discharge current of the FW MOSFET</p>
RES	3	r	Reserved, always read as 0
ICHG_BNK	2:0	rw	<p><b>Banking bits for charge and discharge currents of active MOSFETs</b></p> <p>000<sub>B</sub> <b>ACT_HB1</b>, Active MOSFET of HB1 is selected (default)</p> <p>001<sub>B</sub> <b>ACT_HB2</b>, Active MOSFET of HB2 is selected</p> <p>010<sub>B</sub> <b>ACT_HB3</b>, Active MOSFET of HB3 is selected</p> <p>011<sub>B</sub> <b>RES</b>, reserved</p> <p>100<sub>B</sub> <b>FW_HB1</b>, FW MOSFET of HB1 is selected</p> <p>101<sub>B</sub> <b>FW_HB2</b>, FW MOSFET of HB2 is selected</p> <p>110<sub>B</sub> <b>FW_HB3</b>, FW MOSFET of HB3 is selected</p> <p>111<sub>B</sub> <b>RES</b>, reserved</p>

**Table 69** Reset of **HB\_ICHG**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0011 1100 1101 0000 <sub>B</sub>			POR value valid for ICHG_BNK = 0
Restart	xxxx xxxx xxxx 0000 <sub>B</sub>			

Serial Peripheral Interface

HB max. pre-charge/pre-discharge in PWM operation current and diagnostic pull-down

HB\_ICHG\_MAX

HB max. pre-charge/pre-discharge in PWM operation current and diagnostic pull-down

(001 1001<sub>B</sub>)

Reset Value: see [Table 70](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	HB3ID IAG	HB2ID IAG	HB1ID IAG	RES				RES		ICHGMAX3		ICHGMAX2		ICHGMAX1	
r	rrw	rw	rw	r				r		rw		rw		rw	

Field	Bits	Type	Description
RES	15	r	Reserved, always read as 0
HB3ID IAG	14	rrw	Control of HB3 off-state current source and current sink 0 <sub>B</sub> <b>INACTIVE</b> , Pull-down deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Pull-down activated
HB2ID IAG	13	rw	Control of HB2 pull-down for off-state diagnostic 0 <sub>B</sub> <b>INACTIVE</b> , Pull-down deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Pull-down activated
HB1ID IAG	12	rw	Control of HB1 pull-down for off-state diagnostic 0 <sub>B</sub> <b>INACTIVE</b> , Pull-down deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Pull-down activated
RES	11:8	r	Reserved, always read as 0
RES	7:6	r	Reserved, always reads as 0
ICHGMAX3	5:4	rw	Maximum drive current of HB3 during the pre-charge and pre-discharge phases <sup>1)</sup> 00 <sub>B</sub> <b>31mA</b> , charge I <sub>CHG24</sub> : typ. 31.6 mA, discharge I <sub>DCHG24</sub> : typ. 30.9 mA (default) 01 <sub>B</sub> <b>52mA</b> , charge I <sub>CHG32</sub> : typ. 52.5 mA, discharge I <sub>DCHG32</sub> : typ. 51.5 mA 10 <sub>B</sub> <b>112mA</b> , charge I <sub>CHG52</sub> : typ. 112.2mA, discharge I <sub>DCHG52</sub> : typ. 110.8 mA 11 <sub>B</sub> <b>150mA</b> , charge I <sub>CHG63</sub> : typ. 150 mA, discharge I <sub>DCHG63</sub> : typ. 150 mA
ICHGMAX2	3:2	rw	Maximum drive current of HB2 during the pre-charge phase and pre-discharge phases <sup>1)</sup> 00 <sub>B</sub> <b>31mA</b> , charge I <sub>CHG24</sub> : typ. 31.6 mA, discharge I <sub>DCHG24</sub> : typ. 30.9 mA (default) 01 <sub>B</sub> <b>52mA</b> , charge I <sub>CHG32</sub> : typ. 52.5 mA, discharge I <sub>DCHG32</sub> : typ. 51.5 mA 10 <sub>B</sub> <b>112mA</b> , charge I <sub>CHG52</sub> : typ. 112.2mA, discharge I <sub>DCHG52</sub> : typ. 110.8 mA 11 <sub>B</sub> <b>150mA</b> , charge I <sub>CHG63</sub> : typ. 150 mA, discharge I <sub>DCHG63</sub> : typ. 150 mA

**Serial Peripheral Interface**

Field	Bits	Type	Description
ICHGMAX1	1:0	rw	<b>Maximum drive current of HB1 during the pre-charge and pre-discharge phases<sup>1)</sup></b> 00 <sub>B</sub> <b>31mA</b> , charge $I_{CHG24}$ : typ. 31.6 mA, discharge $I_{DCHG24}$ : typ. 30.9 mA (default) 01 <sub>B</sub> <b>52mA</b> , charge $I_{CHG32}$ : typ. 52.5 mA, discharge $I_{DCHG32}$ : typ. 51.5 mA 10 <sub>B</sub> <b>112mA</b> , charge $I_{CHG52}$ : typ. 112.2mA, discharge $I_{DCHG52}$ : typ. 110.8 mA 11 <sub>B</sub> <b>150mA</b> , charge $I_{CHG63}$ : typ. 150 mA, discharge $I_{DCHG63}$ : typ. 150 mA

1) ICHGMAX is also the current applied during the post-charge of the PWM MOSFET.

**Table 70**    **Reset of [HB\\_ICHG\\_MAX](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0xxx 0000 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

HBx pre-charge/pre-discharge initialization configuration in PWM operation

HB\_PCHG\_INIT

HBx pre-charge/pre-discharge initialization configuration in PWM operation

(001 1010<sub>B</sub>)

Reset Value: see [Table 71](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDCHGINIT						PCHGINIT						RES	INIT_BNK		
rw						rw						r	rw		

Field	Bits	Type	Description
PDCHGINIT	15:10	rw	<b>Initial predischage current of HBx, IPDCHGINITx</b> The INIT_BNK bits select the addressed half-bridge Default: 001111 <sub>B</sub> Refer to <a href="#">Table 34</a>
PCHGINIT	9:4	rw	<b>Initial precharge current of HBx, IPCHGINITx</b> The INIT_BNK bits select the addressed half-bridge Default: 001101 <sub>B</sub> Refer to <a href="#">Table 34</a>
RES	3	r	<b>Reserved, always reads as 0</b>
INIT_BNK	2:0	rw	<b>Banking bits for Precharge an Predischage Initial Current</b> 000 <sub>B</sub> <b>HB1</b> , precharge/discharge init. for HB1 selected (default) 001 <sub>B</sub> <b>HB2</b> , precharge/discharge init. for HB2 selected 010 <sub>B</sub> <b>HB3</b> , precharge/discharge init. for HB3 selected 010 <sub>B</sub> <b>RES</b> , reserved 011 <sub>B</sub> <b>RES</b> , reserved 1xx <sub>B</sub> , wrong setting of INIT_BANK

**Table 71** Reset of [HB\\_PCHG\\_INIT](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0011 1100 1101 0000 <sub>B</sub>			
Restart	xxxx xxxx xxxx 0000 <sub>B</sub>			

**Serial Peripheral Interface**

**HBx inputs TDON configuration**

**TDON\_HB\_CTRL**

**HBx inputs TDON configuration**

**(001 1011<sub>B</sub>)**

**Reset Value: see Table 72**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>		<b>TDON</b>						<b>RES</b>				<b>HB_TDON_BNK</b>			
r		rw						r				rw			

Field	Bits	Type	Description
<b>RES</b>	15:14	r	<b>Reserved, always read as 0</b>
<b>TDON</b>	13:8	rw	<b>Turn-on delay time of active MOSFET of HBx</b> The <b>HB_TDON_BNK</b> bits selects the turn-on delay time of the active MOSFET of the half-bridge HBx Nominal tDON = 53.3 ns x TDON[5:0] <sub>D</sub> Default: 00 1100 <sub>B</sub> : 640 ns typ.
<b>RES</b>	7:3	r	<b>Reserved, always read as 0</b>
<b>HB_TDON_BNK</b>	2:0	rw	<b>Banking bits for turn-on delay time</b> 000 <sub>B</sub> <b>HB1</b> , tDON of HB1 selected (default) 001 <sub>B</sub> <b>HB2</b> , tDON of HB2 selected 010 <sub>B</sub> <b>HB3</b> , tDON of HB3 selected 011 <sub>B</sub> <b>RES</b> , reserved 1xx <sub>B</sub> , wrong setting of PWM_TDON_BNK

**Table 72 Reset of TDON\_HB\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 1100 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 0000 0000 <sub>B</sub>			

## Serial Peripheral Interface

### HBx TDOFF configuration

#### TDOFF\_HB\_CTRL

#### HBx TDOFF configuration

(001 1100<sub>B</sub>)

Reset Value: see [Table 73](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TDOFF						RES				HB_TDOFF_BNK			
r		rw						r				rw			

Field	Bits	Type	Description
RES	15:14	r	<b>Reserved, always read as 0</b>
TDOFF	13:8	rw	<b>Turn-off delay time of active MOSFET of HBx</b> The <b>HB_TDOFF_BNK</b> bits selects the turn-off delay time of the active MOSFET of the half-bridge HBx Nominal tDOFF = 53.3 ns x TDOFF[5:0] <sub>D</sub> Default: 0000 1100 <sub>B</sub> : 640 ns
RES	7:3	r	<b>Reserved, always read as 0</b>
HB_TDOFF_BNK	2:0	rw	<b>Banking bits for turn-off delay time</b> 000 <sub>B</sub> <b>HB1</b> , tDOFF of HB1 selected (default) 001 <sub>B</sub> <b>HB2</b> , tDOFF of HB2 selected 010 <sub>B</sub> <b>HB3</b> , tDOFF of HB3 selected 1xx <sub>B</sub> , wrong setting of PWM_TDOFF_BNK

**Table 73** Reset of **TDOFF\_HB\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 1100 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 0000 0000 <sub>B</sub>			

## Serial Peripheral Interface

### Brake control

#### BRAKE

#### Brake control

(001 1101<sub>B</sub>)

Reset Value: see [Table 74](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	RES	SLAM_LS3_DIS	SLAM_LS2_DIS	SLAM_LS1_DIS	SLAM	VDSTH_BRK	TBLK_BRK	PARK_BRK_EN	OV_BRK_EN	RES	RES	RES	RES	OV_BRK_TH	
r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
RES	15:14	r	Reserved, always read as 0
RES	13	r	Reserved, always read as 0
SLAM_LS3_DIS	12	rw	<b>LS3 output disable during SLAM mode</b> 0 <sub>B</sub> <b>ACTIVE</b> , LS3 control active in Slam mode (default) 1 <sub>B</sub> <b>DISABLED</b> , LS3 control disabled in Slam mode
SLAM_LS2_DIS	11	rw	<b>LS2 output disable during SLAM mode</b> 0 <sub>B</sub> <b>ACTIVE</b> , LS2 control active in Slam mode (default) 1 <sub>B</sub> <b>DISABLED</b> , LS2 control disabled in Slam mode
SLAM_LS1_DIS	10	rw	<b>LS1 output disable during SLAM mode</b> 0 <sub>B</sub> <b>ACTIVE</b> , LS1 control active in Slam mode (default) 1 <sub>B</sub> <b>DISABLED</b> , LS1 control disabled in Slam mode
SLAM	9	rw	<b>Slam mode</b> 0 <sub>B</sub> <b>INACTIVE</b> , Slam mode deactivated (default) 1 <sub>B</sub> <b>ACTIVE</b> , Slam mode activated
VDSTH_BRK	8	rw	<b>VDS Overvoltage for LS1-3 during braking</b> 0 <sub>B</sub> <b>800mV</b> , <a href="#">V<sub>VDSMONTH0_BRAKE</sub></a> , 0.8 V, typ. (default) 1 <sub>B</sub> <b>220mV</b> , <a href="#">V<sub>VDSMONTH1_BRAKE</sub></a> , 0.22 V typ.
TBLK_BRK	7	rw	<b>Blank time of VDS overvoltage during braking</b> 0 <sub>B</sub> <b>7uS</b> , <a href="#">t<sub>BLK_BRAKE1</sub></a> , 7 μs typ. 1 <sub>B</sub> <b>11uS</b> , <a href="#">t<sub>BLK_BRAKE2</sub></a> , 11 μs typ. (default)
PARK_BRK_EN	6	rw	<b>Parking brake enable</b> 0 <sub>B</sub> <b>DISABLED</b> , Parking brake disabled (default) 1 <sub>B</sub> <b>ENABLED</b> , Parking brake enabled
OV_BRK_EN	5	rw	<b>Overvoltage brake enable</b> 0 <sub>B</sub> <b>DISABLED</b> , Overvoltage brake disabled 1 <sub>B</sub> <b>ENABLED</b> , Overvoltage brake enabled (default)
RES	4:3	rw	Reserved, to be set to 0



**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>OV_BRK_TH</b>	2:0	rw	<b>Overvoltage brake threshold</b> 000 <sub>B</sub> <b>27V</b> , typ. 27V (default) 001 <sub>B</sub> <b>28V</b> , typ. 28V 010 <sub>B</sub> <b>29V</b> , typ. 29V 011 <sub>B</sub> <b>30V</b> , typ. 30V 100 <sub>B</sub> <b>31V</b> , typ. 31V 101 <sub>B</sub> <b>32V</b> , typ. 32V 110 <sub>B</sub> <b>33V</b> , typ. 33V 111 <sub>B</sub> <b>34V</b> , typ. 34V

**Table 74**    **Reset of BRAKE**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 1010 0000 <sub>B</sub>			
Restart	000x xxxx xxx0 0xxx <sub>B</sub>			

*Note:*        For min and max values of **OV\_BRK\_TH**, refer to **Chapter 12.13**.

### 13.5.3 Selective Wake Registers

#### CAN Selective Wake Control

##### SWK\_CTRL

##### CAN Selective Wake Control

(011 0000<sub>B</sub>)

Reset Value: see [Table 75](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								OSC_CAL	TRIM_EN	CANTO_MASK	RES	CFG_VAL			
r								rw	rw	rw	r	rwh			

Field	Bits	Type	Description
RES	15:8	r	Reserved, always reads as 0
OSC_CAL	7	rw	<b>Oscillator Calibration Mode</b> 0 <sub>B</sub> <b>DISABLED</b> , Oscillator Calibration is disabled 1 <sub>B</sub> <b>ENABLED</b> , Oscillator Calibration is enabled
TRIM_EN	6:5	rw	<b>(Un)locking mechanism of oscillator recalibration</b> 00 <sub>B</sub> <b>LOCKED</b> , locked 01 <sub>B</sub> <b>LOCKED</b> , locked 10 <sub>B</sub> <b>LOCKED</b> , locked 11 <sub>B</sub> <b>UNLOCKED</b> , unlocked
CANTO_MASK	4	rw	<b>CAN Time Out Masking</b> 0 <sub>B</sub> <b>MASKED</b> , CAN time-out is masked - no interrupt (on pin INTN) is triggered 1 <sub>B</sub> <b>UNMASKED</b> , CAN time-out is signaled on INTN
RES	3:1	r	Reserved, always reads as 0
CFG_VAL	0	rwh	<b>SWK Configuration valid</b> 0 <sub>B</sub> <b>NOT_VALID</b> , Configuration is not valid (SWK not possible) 1 <sub>B</sub> <b>VALID</b> , SWK configuration valid, needs to be set to enable SWK

**Table 75** Reset of [SWK\\_CTRL](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 xxxx 0000 <sub>B</sub>			

#### Notes

1. TRIM\_EN unlocks the oscillation calibration mode. Only the bit combination '11' is the valid unlock. The pin TXDCAN is used for oscillator synchronisation (trimming).
2. The microcontroller needs to validate the SWK configuration and set 'CFG\_VAL' to '1'. The device will only enable SWK if CFG\_VAL' to '1'. The bit will be cleared automatically by the device after a wake up or POR or if a SWK configuration data is changed by the microcontroller.

## Serial Peripheral Interface

3. *CANTO bit will only be updated inside BUS\_STAT while CAN\_2 is set. Therefore, an interrupt is only signaled upon occurrence of CANTO while CAN\_2 (SWK is enabled) is set in Normal Mode and Stop Mode.*

## SWK Bit Timing Control

### SWK\_BTL1\_CTRL

#### SWK Bit Timing Control

(011 0001<sub>B</sub>)

Reset Value: see [Table 76](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SP						RES		TBIT							
rw						r		rw							

Field	Bits	Type	Description
SP	15:10	rw	<b>Sampling Point Position</b> Represents the sampling point position (fractional number < 1). Example: 0011 0011 = 0.796875 (~80%)
RES	9:8	r	<b>Reserved, always reads as 0</b>
TBIT	7:0	rw	<b>Number of Time Quanta in a Bit Time</b> Represents the number of time quanta in a bit time. Quanta is depending on x<1:0> from the x register.

**Table 76** Reset of [SWK\\_BTL1\\_CTRL](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	1100 1100 1001 0110 <sub>B</sub>			
Restart	xxxx xx00 xxxx xxxx <sub>B</sub>			

## Serial Peripheral Interface

### SWK WUF Identifier bits

#### SWK\_ID1\_CTRL

SWK WUF Identifier bits 28...13

(011 0010<sub>B</sub>)

Reset Value: see [Table 77](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ID28</b>	<b>ID27</b>	<b>ID26</b>	<b>ID25</b>	<b>ID24</b>	<b>ID23</b>	<b>ID22</b>	<b>ID21</b>	<b>ID20</b>	<b>ID19</b>	<b>ID18</b>	<b>ID17</b>	<b>ID16</b>	<b>ID15</b>	<b>ID14</b>	<b>ID13</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>ID28</b>	15	rw	<b>WUF Identifier Bit 28</b>
<b>ID27</b>	14	rw	<b>WUF Identifier Bit 27</b>
<b>ID26</b>	13	rw	<b>WUF Identifier Bit 26</b>
<b>ID25</b>	12	rw	<b>WUF Identifier Bit 25</b>
<b>ID24</b>	11	rw	<b>WUF Identifier Bit 24</b>
<b>ID23</b>	10	rw	<b>WUF Identifier Bit 23</b>
<b>ID22</b>	9	rw	<b>WUF Identifier Bit 22</b>
<b>ID21</b>	8	rw	<b>WUF Identifier Bit 21</b>
<b>ID20</b>	7	rw	<b>WUF Identifier Bit 20</b>
<b>ID19</b>	6	rw	<b>WUF Identifier Bit 19</b>
<b>ID18</b>	5	rw	<b>WUF Identifier Bit 18</b>
<b>ID17</b>	4	rw	<b>WUF Identifier Bit 17</b>
<b>ID16</b>	3	rw	<b>WUF Identifier Bit 16</b>
<b>ID15</b>	2	rw	<b>WUF Identifier Bit 15</b>
<b>ID14</b>	1	rw	<b>WUF Identifier Bit 14</b>
<b>ID13</b>	0	rw	<b>WUF Identifier Bit 13</b>

**Table 77** Reset of [SWK\\_ID1\\_CTRL](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

**Serial Peripheral Interface**

**SWK WUF Identifier bits**

**SWK\_ID0\_CTRL**

**SWK WUF Identifier bits 12...0**

**(011 0011<sub>B</sub>)**

**Reset Value: see Table 78**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ID12</b>	<b>ID11</b>	<b>ID10</b>	<b>ID9</b>	<b>ID8</b>	<b>ID7</b>	<b>ID6</b>	<b>ID5</b>	<b>RES</b>	<b>ID4</b>	<b>ID3</b>	<b>ID2</b>	<b>ID1</b>	<b>ID0</b>	<b>RTR</b>	<b>IDE</b>
rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>ID12</b>	15	rw	<b>WUF Identifier Bit 12</b>
<b>ID11</b>	14	rw	<b>WUF Identifier Bit 11</b>
<b>ID10</b>	13	rw	<b>WUF Identifier Bit 10</b>
<b>ID9</b>	12	rw	<b>WUF Identifier Bit 9</b>
<b>ID8</b>	11	rw	<b>WUF Identifier Bit 8</b>
<b>ID7</b>	10	rw	<b>WUF Identifier Bit 7</b>
<b>ID6</b>	9	rw	<b>WUF Identifier Bit 6</b>
<b>ID5</b>	8	rw	<b>WUF Identifier Bit 5</b>
<b>RES</b>	7	r	<b>Reserved, always reads as 0</b>
<b>ID4</b>	6	rw	<b>WUF Identifier Bit 4</b>
<b>ID3</b>	5	rw	<b>WUF Identifier Bit 3</b>
<b>ID2</b>	4	rw	<b>WUF Identifier Bit 2</b>
<b>ID1</b>	3	rw	<b>WUF Identifier Bit 1</b>
<b>ID0</b>	2	rw	<b>WUF Identifier Bit 0</b>
<b>RTR</b>	1	rw	<b>Remote Transmission Request Field (acc. ISO11898-2:2016)</b> 0 <sub>B</sub> <b>NORMAL</b> , Normal Data Frame 1 <sub>B</sub> <b>REMOTE</b> , Remote Transmission Request
<b>IDE</b>	0	rw	<b>Identifier Extension Bit</b> 0 <sub>B</sub> <b>STD</b> , Standard Identifier Length (11 bit) 1 <sub>B</sub> <b>EXT</b> , Extended Identifier Length (29 bit)

**Table 78 Reset of SWK\_ID0\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx 0xxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

**SWK WUF Identifier Mask bits 28...13**

**SWK\_MASK\_ID1\_CTRL**

**SWK WUF Identifier Mask bits 28...13**

**(011 0100<sub>B</sub>)**

**Reset Value: see Table 79**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>MASK_ID28</b>	<b>MASK_ID27</b>	<b>MASK_ID26</b>	<b>MASK_ID25</b>	<b>MASK_ID24</b>	<b>MASK_ID23</b>	<b>MASK_ID22</b>	<b>MASK_ID21</b>	<b>MASK_ID20</b>	<b>MASK_ID19</b>	<b>MASK_ID18</b>	<b>MASK_ID17</b>	<b>MASK_ID16</b>	<b>MASK_ID15</b>	<b>MASK_ID14</b>	<b>MASK_ID13</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>MASK_ID28</b>	15	rw	<b>WUF Identifier Mask Bit 28</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID27</b>	14	rw	<b>WUF Identifier Mask Bit 27</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID26</b>	13	rw	<b>WUF Identifier Mask Bit 26</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID25</b>	12	rw	<b>WUF Identifier Mask Bit 25</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID24</b>	11	rw	<b>WUF Identifier Mask Bit 24</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID23</b>	10	rw	<b>WUF Identifier Mask Bit 23</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID22</b>	9	rw	<b>WUF Identifier Mask Bit 22</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID21</b>	8	rw	<b>WUF Identifier Mask Bit 21</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID20</b>	7	rw	<b>WUF Identifier Mask Bit 20</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID19</b>	6	rw	<b>WUF Identifier Mask Bit 19</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID18</b>	5	rw	<b>WUF Identifier Mask Bit 18</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>MASK_ID17</b>	4	rw	<b>WUF Identifier Mask Bit 17</b> $0_B$ <b>UNMASKED</b> , Unmasked - bit is ignored $1_B$ <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID16</b>	3	rw	<b>WUF Identifier Mask Bit 16</b> $0_B$ <b>UNMASKED</b> , Unmasked - bit is ignored $1_B$ <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID15</b>	2	rw	<b>WUF Identifier Mask Bit 15</b> $0_B$ <b>UNMASKED</b> , Unmasked - bit is ignored $1_B$ <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID14</b>	1	rw	<b>WUF Identifier Mask Bit 14</b> $0_B$ <b>UNMASKED</b> , Unmasked - bit is ignored $1_B$ <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID13</b>	0	rw	<b>WUF Identifier Mask Bit 13</b> $0_B$ <b>UNMASKED</b> , Unmasked - bit is ignored $1_B$ <b>MASKED</b> , Masked - bit is compared in CAN frame

**Table 79**    **Reset of [SWK\\_MASK\\_ID1\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

**Serial Peripheral Interface**

**SWK WUF Identifier Mask bits 12...0**

**SWK\_MASK\_ID0\_CTRL**

**SWK WUF Identifier Mask bits 12...0**

**(011 0101<sub>B</sub>)**

**Reset Value: see [Table 80](#)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>MASK_ID12</b>	<b>MASK_ID11</b>	<b>MASK_ID10</b>	<b>MASK_ID9</b>	<b>MASK_ID8</b>	<b>MASK_ID7</b>	<b>MASK_ID6</b>	<b>MASK_ID5</b>	<b>RES</b>	<b>MASK_ID4</b>	<b>MASK_ID3</b>	<b>MASK_ID2</b>	<b>MASK_ID1</b>	<b>MASK_ID0</b>	<b>RES</b>	
rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw		r

Field	Bits	Type	Description
<b>MASK_ID12</b>	15	rw	<b>WUF Identifier Mask Bit 12</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID11</b>	14	rw	<b>WUF Identifier Mask Bit 11</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID10</b>	13	rw	<b>WUF Identifier Mask Bit 10</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID9</b>	12	rw	<b>WUF Identifier Mask Bit 9</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID8</b>	11	rw	<b>WUF Identifier Mask Bit 8</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID7</b>	10	rw	<b>WUF Identifier Mask Bit 7</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID6</b>	9	rw	<b>WUF Identifier Mask Bit 6</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID5</b>	8	rw	<b>WUF Identifier Mask Bit 5</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>RES</b>	7	r	<b>Reserved, always reads as 0</b>
<b>MASK_ID4</b>	6	rw	<b>WUF Identifier Mask Bit 4</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID3</b>	5	rw	<b>WUF Identifier Mask Bit 3</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID2</b>	4	rw	<b>WUF Identifier Mask Bit 2</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame



**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>MASK_ID1</b>	3	rw	<b>WUF Identifier Mask Bit 1</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>MASK_ID0</b>	2	rw	<b>WUF Identifier Mask Bit 0</b> 0 <sub>B</sub> <b>UNMASKED</b> , Unmasked - bit is ignored 1 <sub>B</sub> <b>MASKED</b> , Masked - bit is compared in CAN frame
<b>RES</b>	1:0	r	<b>Reserved, always reads as 0</b>

**Table 80**    **Reset of [SWK\\_MASK\\_ID0\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx 0xxx xx00 <sub>B</sub>			

## Serial Peripheral Interface

### SWK Frame Data Length Code Control

#### SWK\_DLC\_CTRL

#### SWK Frame Data Length Code Control

(011 0110<sub>B</sub>)

Reset Value: see [Table 81](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES												DLC			
r												rw			

Field	Bits	Type	Description
RES	15:4	r	Reserved, always reads as 0
DLC	3:0	rw	<b>Payload length in number of bytes</b> 0000 <sub>B</sub> 0, Frame Data Length = 0 or cleared 0001 <sub>B</sub> 1, Frame Data Length = 1 0010 <sub>B</sub> 2, Frame Data Length = 2 0011 <sub>B</sub> 3, Frame Data Length = 3 0100 <sub>B</sub> 4, Frame Data Length = 4 0101 <sub>B</sub> 5, Frame Data Length = 5 0110 <sub>B</sub> 6, Frame Data Length = 6 0111 <sub>B</sub> 7, Frame Data Length = 7 1000 <sub>B</sub> 8, to 1111 <sub>B</sub> Frame Data Length = 8

**Table 81** Reset of **SWK\_DLC\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0000 xxxx <sub>B</sub>			

**Note:** The number of transmitted bytes in the data field has to be indicated by the DLC. The DLC value consists of four bits. The admissible number of data bytes for a data frame is in a range from zero to eight. DLCs in the range of zero to seven indicates data fields of length of zero to seven bytes. DLCs in the range from eight to fifteen indicate data fields with a length of eight bytes. The configured DLC value has to match bit by bit with the DLC in the received wake-up frame (refer also to [Chapter 5.9.2.2](#)).

**Serial Peripheral Interface**

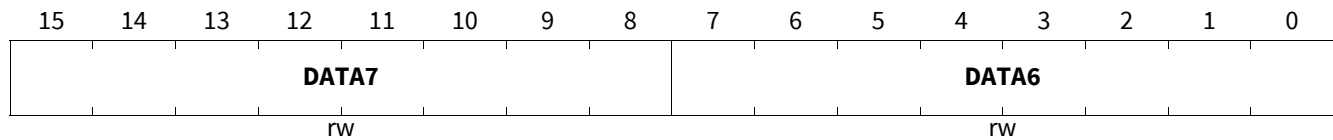
**SWK Data7-Data6 Register**

**SWK\_DATA3\_CTRL**

**SWK Data7-Data6 Register**

**(011 0111<sub>B</sub>)**

**Reset Value: see [Table 82](#)**



Field	Bits	Type	Description
DATA7	15:8	rw	Data7 byte content(bit0=LSB; bit7=MSB)
DATA6	7:0	rw	Data6 byte content(bit0=LSB; bit7=MSB)

**Table 82**    **Reset of [SWK\\_DATA3\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

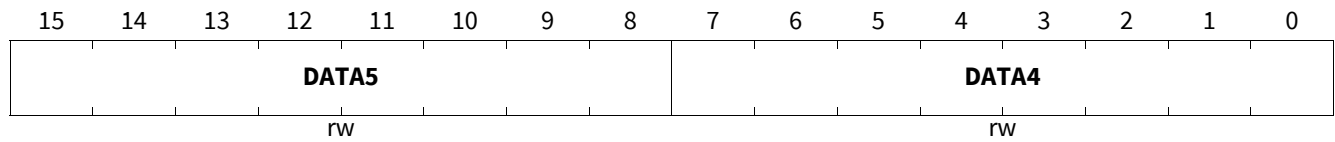
**SWK Data5-Data4 Register**

**SWK\_DATA2\_CTRL**

**SWK Data5-Data4 Register**

**(011 1000<sub>B</sub>)**

**Reset Value: see [Table 83](#)**



Field	Bits	Type	Description
DATA5	15:8	rw	Data5 byte content(bit0=LSB; bit7=MSB)
DATA4	7:0	rw	Data4 byte content(bit0=LSB; bit7=MSB)

**Table 83**    **Reset of [SWK\\_DATA2\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

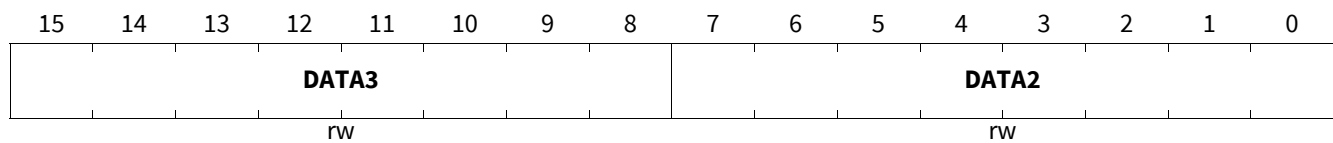
**SWK Data3-Data2 Register**

**SWK\_DATA1\_CTRL**

**SWK Data3-Data2 Register**

**(011 1001<sub>B</sub>)**

**Reset Value: see [Table 84](#)**



Field	Bits	Type	Description
DATA3	15:8	rw	Data3 byte content(bit0=LSB; bit7=MSB)
DATA2	7:0	rw	Data2 byte content(bit0=LSB; bit7=MSB)

**Table 84**    **Reset of [SWK\\_DATA1\\_CTRL](#)**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	xxxxxx xxxx xxxx xxxx <sub>B</sub>			

**Serial Peripheral Interface**

**SWK Data1-Data0 Register**

**SWK\_DATA0\_CTRL**

**SWK Data1-Data0 Register**

**(011 1010<sub>B</sub>)**

**Reset Value: see Table 85**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DATA1</b>								<b>DATA0</b>							
rw								rw							

Field	Bits	Type	Description
<b>DATA1</b>	15:8	rw	<b>Data1 byte content(bit0=LSB; bit7=MSB)</b>
<b>DATA0</b>	7:0	rw	<b>Data0 byte content(bit0=LSB; bit7=MSB)</b>

**Table 85** Reset of **SWK\_DATA0\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

Serial Peripheral Interface

CAN FD Configuration Control Register

SWK\_CAN\_FD\_CTRL

CAN FD Configuration Control Register (011 1011<sub>B</sub>)

Reset Value: see Table 86

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES										DIS_ERR_CNT	RES	FD_FILTER		CAN_FD_EN	
r										rwh	r	rw		rw	

Field	Bits	Type	Description
RES	15:6	r	Reserved, always reads as 0
DIS_ERR_CNT	5	rwh	<b>Error Counter Disable Function</b> 0 <sub>B</sub> <b>ENABLED</b> , Error Counter is enabled during SWK 1 <sub>B</sub> <b>DISABLED</b> , Error counter is disabled during SWK only if CAN_FD_EN = '1'
RES	4	r	Reserved, always reads as 0
FD_FILTER	3:1	rw	<b>CAN FD Dominant Filter Time</b> 000 <sub>B</sub> <b>50ns</b> , 50 ns 001 <sub>B</sub> <b>100ns</b> , 100 ns 010 <sub>B</sub> <b>150ns</b> , 150 ns 011 <sub>B</sub> <b>200ns</b> , 200 ns 100 <sub>B</sub> <b>250ns</b> , 250 ns 101 <sub>B</sub> <b>300ns</b> , 300 ns 110 <sub>B</sub> <b>350ns</b> , 350 ns 111 <sub>B</sub> <b>775ns</b> , 775 ns
CAN_FD_EN	0	rw	<b>Enable CAN FD Tolerant Mode</b> 0 <sub>B</sub> <b>DISABLED</b> , CAN FD Tolerant Mode disabled 1 <sub>B</sub> <b>ENABLED</b> , CAN FD Tolerant Mode enabled

Table 86 Reset of SWK\_CAN\_FD\_CTRL

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 00x0 xxxx <sub>B</sub>			

Notes

1. **DIS\_ERR\_CNT** is cleared by the device at tsilence expiration.
2. The Normal Mode CAN Receiver (**RX\_WK\_SEL** = 0<sub>B</sub>) has to selected with a CAN FD tolerant operation for baud rates > 2 MBit/s.

### 13.5.4 Selective Wake trim and configuration Registers

#### SWK Oscillator Trimming and option Register

##### SWK\_OSC\_TRIM\_CTRL

##### SWK Oscillator Trimming and option Register

(011 1100<sub>B</sub>)

Reset Value: see [Table 87](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RES		RX_WK_K_SEL		RES		TEMP_COEF						TRIM_OSC					
r		rw		r		rw						rw					

Field	Bits	Type	Description
RES	15	r	Reserved, always reads as 0
RX_WK_SEL	14	rw	SWK Receiver selection (only accessible if TRIM_EN = '11') 0 <sub>B</sub> LOW_POWER, Low-Power Receiver selected during SWK 1 <sub>B</sub> STD, Standard Receiver selected during SWK
RES	13:12	r	Reserved, always reads as 0
TEMP_COEF	11:7	rw	Trimming of temp_coef (only writable if TRIM_EN = '11')
TRIM_OSC	6:0	rw	Trimming of oscillator (only writable if TRIM_EN = '11')

**Table 87** Reset of [SWK\\_OSC\\_TRIM\\_CTRL](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0x00 xxxx xxxx xxxx <sub>B</sub>			

#### Notes

1. The bit RX\_WK\_SEL is used to select the respective receiver during Selective Wake operation. The lowest quiescent current during Frame Detect Mode is achieved with the default setting RX\_WK\_SEL = '0', i.e. the Low-Power Receiver is already selected.
2. TRIM\_OSC[6:0] represent the 128-steps coarse trimming range, which is not monotonous. It is not recommended to change these values.



**Serial Peripheral Interface**

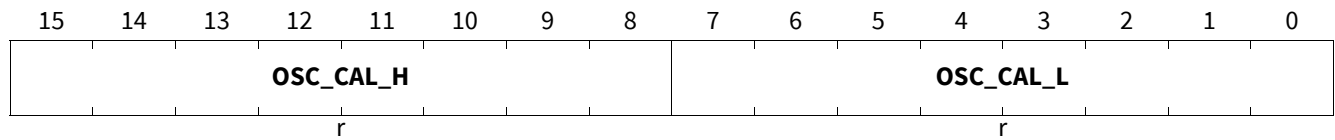
**SWK Oscillator Calibration Register**

**SWK\_OSC\_CAL\_STAT**

**SWK Oscillator Calibration Register**

(011 1101<sub>B</sub>)

Reset Value: see [Table 88](#)



Field	Bits	Type	Description
OSC_CAL_H	15:8	r	Oscillator Calibration High Register
OSC_CAL_L	7:0	r	Oscillator Calibration Low Register

**Table 88** Reset of [SWK\\_OSC\\_CAL\\_STAT](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

**Serial Peripheral Interface**

**Clock Data Recovery Control Register**

**SWK\_CDR\_CTRL**

**Clock Data Recovery Control Register**

**(011 1110<sub>B</sub>)**

**Reset Value: see Table 89**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								SEL_OSC_CLK	RES	SELFILT	RES	CDR_EN			
r								rw	r	rw	r	rw			

Field	Bits	Type	Description
RES	15:7	r	<b>Reserved, always reads as 0</b>
SEL_OSC_CLK	6:5	rw	<b>Input Frequency for CDR module</b> See <a href="#">Table 90</a> and <a href="#">Table 91</a>
RES	4	r	<b>Reserved, always reads as 0</b>
SELFILT	3:2	rw	<b>Select Time Constant of Filter</b> 00 <sub>B</sub> <b>8</b> , Time constant 8 01 <sub>B</sub> <b>16</b> , Time constant 16 (default) 10 <sub>B</sub> <b>32</b> , Time constant 32 11 <sub>B</sub> <b>ADAPTIVE</b> , adapt distance between falling edges 2, 3 bit: Time constant 32 distance between f. edges 4, 5, 6, 7, 8 bit: Time constant 16 distance between falling edges 9, 10 bit: Time constant 8
RES	1	r	<b>Reserved, always reads as 0</b>
CDR_EN	0	rw	<b>Enable CDR</b> 0 <sub>B</sub> <b>DISABLED</b> , CDR disabled 1 <sub>B</sub> <b>ENABLED</b> , CDR enabled

**Table 89 Reset of SWK\_CDR\_CTRL**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0100 <sub>B</sub>			
Restart	0000 0000 0xx0 xx0x <sub>B</sub>			

**Table 90 Frequency Settings of Internal Clock for the CDR**

SEL_OSC_CLK[1:0]	int. Clock for CDR
00	75 MHz
01	37.5 MHz
10	18.75 MHz
11	9.375 MHz

**Serial Peripheral Interface**

**Table 91 Recommended CDR Settings for Different Baud Rates**

<b>SEL_OSC_CLK [1:0]</b>	<b>Baudrate</b>	<b>SWK_BTL1_CTRL Value</b>	<b>SWK_CDR_LIMIT Value</b>
00	500k	xxxx xxxx 1001 0110	1001 1101 1000 1111
01	500k	xxxx xxxx 0100 1011	0100 1110 0100 0111
10	500k	CDR Setting not recommended for this baudrate due to insufficient precision	
11	500k	CDR Setting not recommended for this baudrate due to insufficient precision	
00	250k	CDR Setting not to be used due to excessive time quanta (counter overflow)	
01	250k	xxxx xxxx 1001 0110	1001 1101 1000 1111
10	250k	xxxx xxxx 0100 1011	0100 1110 0100 0111
11	250k	CDR Setting not recommended for this baudrate due to insufficient precision	
00	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)	
01	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)	
10	125k	xxxx xxxx 1001 0110	1001 1101 1000 1111
11	125k	xxxx xxxx 0100 1011	0100 1110 0100 0111

**Serial Peripheral Interface**

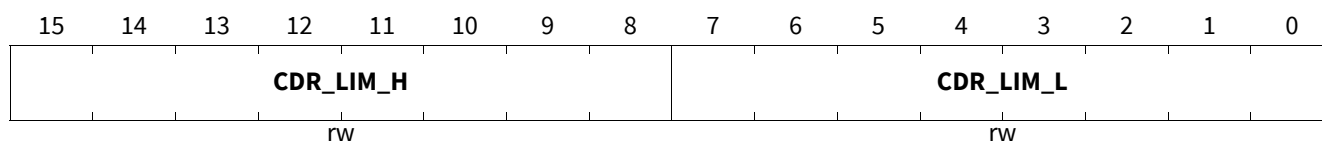
**SWK Clock Data Recovery Limit Control**

**SWK\_CDR\_LIMIT**

**SWK Clock Data Recovery Limit Control**

**(011 1111<sub>B</sub>)**

**Reset Value: see Table 92**



Field	Bits	Type	Description
CDR_LIM_H	15:8	rw	<b>Upper Bit Time Detection Range of Clock and Data Recovery</b> x values > + 5% will be clamped
CDR_LIM_L	7:0	rw	<b>Lower Bit Time Detection Range of Clock and Data Recovery</b> x values > - 5% will be clamped

**Table 92 Reset of SWK\_CDR\_LIMIT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	1001 1101 1000 1111 <sub>B</sub>			
Restart	XXXX XXXX XXXX XXXX <sub>B</sub>			

### 13.6 SPI status information registers

READ/CLEAR Operation (see also [Chapter 13.3](#)):

- One 32-bit SPI command consist of four bytes:
  - The 7-bit address and one additional bit for the register access mode and
  - following the two data bytes and the CRC.
 The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...23 (see also figure).
- There are two different bit types:
  - 'r' = READ: read only bits (or reserved bits).
  - 'rc' = READ/CLEAR: readable and clearable bits.
- Reading a register is done word wise by setting the SPI bit 7 to "0" (= Read Only).
- Clearing a register is done word wise by setting the SPI bit 7 to "1". No single bits can be cleared. Therefore the content of a SPI message (bit 8..23) doesn't matter.
- SPI status registers are in general not cleared or changed automatically (an exception are the x bits). This must be done by the microcontroller via SPI command.

The registers are addressed wordwise.

**Table 93 Register Overview**

Register Short Name	Register Long Name	Offset Address	Page Number
<b>SPI status information registers, Device Status Registers</b>			
<b>SUP_STAT</b>	Supply Voltage Fail Status	1000000 <sub>B</sub>	<b>239</b>
<b>THERM_STAT</b>	Thermal Protection Status	1000001 <sub>B</sub>	<b>241</b>
<b>DEV_STAT</b>	Device Information Status	1000010 <sub>B</sub>	<b>242</b>
<b>BUS_STAT</b>	Bus Communication Status	1000011 <sub>B</sub>	<b>244</b>
<b>WK_STAT</b>	Wake-up Source and Information Status	1000100 <sub>B</sub>	<b>246</b>
<b>WK_LVL_STAT</b>	WK Input Level	1000101 <sub>B</sub>	<b>247</b>
<b>HS_OL_OC_OT_STAT</b>	High-Side Switch Status	1000110 <sub>B</sub>	<b>248</b>
<b>SPI status information registers, Status registers bridge driver</b>			
<b>GEN_STAT</b>	GEN Status register	1010000 <sub>B</sub>	<b>250</b>
<b>TDREG</b>	Turn-on/off delay regulation register	1010001 <sub>B</sub>	<b>252</b>
<b>DSOV</b>	Drain-source overvoltage HBVOUT	1010010 <sub>B</sub>	<b>254</b>
<b>EFF_TDON_OFF1</b>	Effective MOSFET turn-on/off delay - PWM half-bridge 1	1010011 <sub>B</sub>	<b>256</b>
<b>EFF_TDON_OFF2</b>	Effective MOSFET turn-on/off delay - PWM half-bridge 2	1010100 <sub>B</sub>	<b>257</b>
<b>EFF_TDON_OFF3</b>	Effective MOSFET turn-on/off delay - PWM half-bridge 3	1010101 <sub>B</sub>	<b>258</b>
<b>TRISE_FALL1</b>	MOSFET rise/fall time - PWM half-bridge 1	1010111 <sub>B</sub>	<b>259</b>
<b>TRISE_FALL2</b>	MOSFET rise/fall time - PWM half-bridge 2	1011000 <sub>B</sub>	<b>260</b>
<b>TRISE_FALL3</b>	MOSFET rise/fall time - PWM half-bridge 3	1011001 <sub>B</sub>	<b>261</b>
<b>SPI status information registers, Selective wake status registers</b>			
<b>SWK_STAT</b>	Selective Wake Status	1100000 <sub>B</sub>	<b>262</b>

**Serial Peripheral Interface**

**Table 93 Register Overview** (cont'd)

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">SWK_ECNT_STAT</a>	Selective Wake ECNT Status	1100001 <sub>B</sub>	<a href="#">263</a>
<a href="#">SWK_CDR_STAT</a>	Selective Wake CDR Status	1100011 <sub>B</sub>	<a href="#">264</a>
<a href="#">SPI status information registers, Family and product information register</a>			
<a href="#">FAM_PROD_STAT</a>	Family and Product Identification Register	1110000 <sub>B</sub>	<a href="#">265</a>

### 13.6.1 Device Status Registers

#### Supply Voltage Fail Status

##### SUP\_STAT

##### Supply Voltage Fail Status

(100 0000<sub>B</sub>)

Reset Value: see [Table 94](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR	RES	CP_OT	VCC1_UV_FS	HS_UV	HS_OV	VSINT_UV	VSINT_OV	VS_UV	VS_OV	CP_UV	VCC1_SC	VCC1_UV	VCC1_OV	VCC1_WARN	
rc	r	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
POR	15	rc	<b>Power-On reset detection</b> 0 <sub>B</sub> <b>NO_POR</b> , No POR 1 <sub>B</sub> <b>POR</b> , POR occurred
RES	14:13	r	<b>Reserved, always reads as 0</b>
CP_OT	12	rc	<b>Charge pump overtemperature</b> 0 <sub>B</sub> <b>NO_CP_OT</b> , No charge pump OT detected 1 <sub>B</sub> <b>CP_OT</b> , Charge pump OT detected
VCC1_UV_FS	11	rc	<b>4th consecutive VCC1 UV-Detection</b> 0 <sub>B</sub> <b>NO_FAILSAFE</b> , No Fail-Safe Mode entry due to 4th consecutive VCC1_UV 1 <sub>B</sub> <b>FAILSAFE</b> , Fail-Safe Mode entry due to 4th consecutive VCC1_UV
HS_UV	10	rc	<b>HS Supply UV-Detection</b> 0 <sub>B</sub> <b>NO_UV</b> , No Undervoltage 1 <sub>B</sub> <b>UV_EVENT</b> , HS Supply Undervoltage detected
HS_OV	9	rc	<b>HS Supply OV-Detection</b> 0 <sub>B</sub> <b>NO_OV</b> , No Overvoltage 1 <sub>B</sub> <b>OV_EVENT</b> , HS Supply Overvoltage detected
VSINT_UV	8	rc	<b>VSINT UV-Detection</b> 0 <sub>B</sub> <b>NO_UV</b> , No Undervoltage 1 <sub>B</sub> <b>UV_EVENT</b> , VSINT Undervoltage detected
VSINT_OV	7	rc	<b>VSINT OV-Detection</b> 0 <sub>B</sub> <b>NO_OV</b> , No Overvoltage 1 <sub>B</sub> <b>OV_EVENT</b> , VSINT Overvoltage detected
VS_UV	6	rc	<b>VS Undervoltage Detection (V<sub>s,uv</sub>)</b> 0 <sub>B</sub> <b>NO_VS</b> , No VS undervoltage detected 1 <sub>B</sub> <b>VS_EVENT</b> , VS undervoltage detected (detection is only active when VCC1 is enabled)
VS_OV	5	rc	<b>VS Overvoltage Detection (V<sub>s,ov</sub>)</b> 0 <sub>B</sub> <b>NO_OV</b> , No VS overvoltage detected 1 <sub>B</sub> <b>OV_EVENT</b> , VS overvoltage detected (detection is only active when VCC1 is enabled)

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>CP_UV</b>	4	rc	<b>CP_UV</b> $0_B$ <b>NO_UV</b> , No CP undervoltage detected $1_B$ <b>UV_EVENT</b> , CP undervoltage detected
<b>VCC1_SC</b>	3	rc	<b>VCC1 SC</b> $0_B$ <b>NO_SC</b> , No VCC1 short to GND detected $1_B$ <b>SC_EVENT</b> , VCC1 short to GND
<b>VCC1_UV</b>	2	rc	<b>VCC1 UV-Detection (due to Vrtx reset)</b> $0_B$ <b>NO_UV</b> , No VCC1_UV detection $1_B$ <b>UV_EVENT</b> , VCC1 undervoltage detected
<b>VCC1_OV</b>	1	rc	<b>VCC1 Overvoltage Detection</b> $0_B$ <b>NO_OV</b> , No VCC1 overvoltage warning $1_B$ <b>OV_EVENT</b> , VCC1 overvoltage detected
<b>VCC1_WARN</b>	0	rc	<b>VCC1 Undervoltage Prewarning</b> $0_B$ <b>NO_UV</b> , No VCC1 undervoltage prewarning $1_B$ <b>UV_PREWARN</b> , VCC1 undervoltage prewarning detected

**Table 94**    **Reset of SUP\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	y000 0000 0000 0000 <sub>B</sub>			
Restart	x00x xxxx xxxx xxxx <sub>B</sub>			

**Notes**

1. The VCC1 undervoltage prewarning threshold  $V_{PW,f}/V_{PW,r}$  is a fixed threshold and independent of the VCC1 undervoltage reset thresholds.
2. VSINT undervoltage monitoring is not available in Stop Mode due to current consumption saving requirements. Exception: VSINT undervoltage detection is also available in Stop Mode if the VCC1 load current is above the active peak threshold ( $I_{PEAK\_TH}$ ) or if VCC1 is below the VCC1 prewarning threshold (**VCC1\_WARN** is set).
3. The MSB of the POR/Soft Reset value is marked as 'y': the default value of the POR bit is set after Power-on reset (POR value = 1000 0000). However it will be cleared after a device Soft Reset command (Soft Reset value = 0000 0000).
4. During Sleep Mode, the bits VCC1\_SC, VCC1\_OV and VCC1\_UV will not be set when VCC1 is off.
5. The VCC1\_UV bit is never updated in Restart Mode, in Init Mode it is only updated after RSTN was released, it is always updated in Normal Mode and Stop Mode, and it is always updated in any device modes in a VCC1\_SC condition (after VCC1\_UV = 1 for > 2 ms).



**Serial Peripheral Interface**

**Thermal Protection Status**

**THERM\_STAT**

**Thermal Protection Status**

**(100 0001<sub>B</sub>)**

**Reset Value: see Table 95**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES												TSD2_SAFE	TSD2	TSD1	TPW
r												rc	rc	rc	rc

Field	Bits	Type	Description
<b>RES</b>	15:4	r	<b>Reserved, always reads as 0</b>
<b>TSD2_SAFE</b>	3	rc	<b>TSD2 Thermal Shut-Down Safe State Detection</b> 0 <sub>B</sub> <b>NO_TSD2_SF</b> , No TSD2 safe state detected 1 <sub>B</sub> <b>TSD2_SF</b> , TSD2 safe state detected: >16 consecutive TSD2 events occurred, next TSD2 waiting time will be 64s
<b>TSD2</b>	2	rc	<b>TSD2 Thermal Shut-Down Detection</b> 0 <sub>B</sub> <b>NO_TSD2</b> , No TSD2 event 1 <sub>B</sub> <b>TSD2_EVENT</b> , TSD2 OT detected - leading to Fail-Safe Mode
<b>TSD1</b>	1	rc	<b>TSD1 Thermal Shut-Down Detection</b> 0 <sub>B</sub> <b>NO_TSD1</b> , No TSD1 fail 1 <sub>B</sub> <b>TSD1_EVENT</b> , TSD1 OT detected (affected module is disabled)
<b>TPW</b>	0	rc	<b>Thermal Pre Warning</b> 0 <sub>B</sub> <b>NO_TPW</b> , No Thermal Pre warning 1 <sub>B</sub> <b>TPW</b> , Thermal Pre warning detected

**Table 95 Reset of THERM\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0000 xxxx <sub>B</sub>			

*Note: Temperature warning and shutdown bits are not reset automatically, even if the temperature pre warning or the TSD condition is not present anymore.*

## Serial Peripheral Interface

### Device Information Status

#### DEV\_STAT

#### Device Information Status

(100 0010<sub>B</sub>)

Reset Value: see [Table 96](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES						CRC_STAT	CRC_FAIL	DEV_STAT		RES	SW_DEV	WD_FAIL		SPI_FAIL	FAILURE
r						r	rc	rc		r	rh	rh		rc	rc

Field	Bits	Type	Description
RES	15:10	r	<b>Reserved, always read as 0</b>
CRC_STAT	9	r	<b>CRC STAT Information</b> 0 <sub>B</sub> <b>DISABLED</b> , CRC disabled 1 <sub>B</sub> <b>ENABLED</b> , CRC enabled
CRC_FAIL	8	rc	<b>CRC Fail Information<sup>1)</sup></b> 0 <sub>B</sub> <b>NO_FAIL</b> , No CRC Failure 1 <sub>B</sub> <b>FAIL</b> , CRC Failure detected
DEV_STAT	7:6	rc	<b>Device Status before Restart Mode</b> 00 <sub>B</sub> <b>CLEARED</b> , Cleared (Register must be actively cleared) 01 <sub>B</sub> <b>RESTART</b> , Restart due to failure (WD fail, TSD2, VCC1_UV, trial to access Sleep Mode without any wake source activated); also after a wake from Fail-Safe Mode 10 <sub>B</sub> <b>SLEEP</b> , Sleep Mode 11 <sub>B</sub> , reserved
RES	5	r	<b>Reserved, always reads 0</b>
SW_DEV	4	rh	<b>Status of Operating Mode</b> 0 <sub>B</sub> <b>NORMAL</b> , Normal operation 1 <sub>B</sub> <b>SW_DEV</b> , Software Development Mode is enabled
WD_FAIL	3:2	rh	<b>Number of WD-Failure Events</b> 00 <sub>B</sub> <b>NO_FAIL</b> , No WD Fail 01 <sub>B</sub> <b>1x</b> , 1x WD Fail, 10 <sub>B</sub> <b>2x</b> , 2x WD Fail 11 <sub>B</sub> <b>3x</b> , more than 3xWD Fail
SPI_FAIL	1	rc	<b>SPI Fail Information</b> 0 <sub>B</sub> <b>NO_FAIL</b> , No SPI fail 1 <sub>B</sub> <b>INVALID</b> , Invalid SPI command detected
FAILURE	0	rc	<b>Failure detection</b> 0 <sub>B</sub> <b>NO_FAIL</b> , No Failure 1 <sub>B</sub> <b>FAIL</b> , Failure occurred

1) The CRC\_FAIL bit will not be set in case the static CRC enabling / disabling sequence is sent (see [Chapter 5.2](#)).

**Table 96**    **Reset of DEV\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 00xx xx0x xxxx <sub>B</sub>			

**Notes**

1. The bits **DEV\_STAT** show the status of the device before exiting Restart Mode. Either the device came from regular Sleep Mode or a failure (Restart Mode or Fail-Safe Mode) occurred. Coming from Sleep Mode will also be shown if there was a trial to enter Sleep Mode without having cleared all wake flags before.
2. The **WD\_FAIL** bits are implemented as a counter and are the only status bits, which are cleared automatically by the device.
3. The **SPI\_FAIL** bit can only be cleared via SPI command.
4. The bit **CRC\_STAT** and **CRC\_FAIL** can be read regardless the CRC setting. The SPI read command on **DEV\_STAT** ignores the CRC field.

## Serial Peripheral Interface

### Bus Communication Status

#### BUS\_STAT

##### Bus Communication Status

(100 0011<sub>B</sub>)

Reset Value: see [Table 97](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								RES		CANT O	SYSER R	CAN_FAIL		VCAN_ UV	
r								r		rc	rc	rc		rc	

Field	Bits	Type	Description
RES	15:7	r	Reserved, always reads as 0
RES	6:5	r	Reserved, always reads as 0
CANTO	4	rc	<b>CAN Time Out Detection</b> 0 <sub>B</sub> <b>NO_FAIL</b> , Normal operation 1 <sub>B</sub> <b>TIME_OUT</b> , CAN Time Out detected
SYSERR	3	rc	<b>SWK System Error</b> 0 <sub>B</sub> <b>NO_FAIL</b> , Selective Wake Mode is possible 1 <sub>B</sub> <b>FAIL</b> , System Error detected, SWK enabling not possible
CAN_FAIL	2:1	rc	<b>CAN failure status</b> 00 <sub>B</sub> <b>NO_ERR</b> , No error 01 <sub>B</sub> <b>CAN_TSD</b> , CAN Thermal shutdown 10 <sub>B</sub> <b>CAN_TXD_DOM_TO</b> , CAN_TXD_DOM: TXD dominant time out detected 11 <sub>B</sub> <b>CAN_BUS_DOM_TO</b> , CAN_BUS_DOM: BUS dominant time out detected
VCAN_UV	0	rc	<b>Under Voltage CAN Bus Supply</b> 0 <sub>B</sub> <b>NORMAL</b> , Normal operation 1 <sub>B</sub> <b>UNDERVOLTAGE</b> , CAN Supply undervoltage detected. Transmitter disabled

**Table 97** Reset of **BUS\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0xxx xxxx <sub>B</sub>			

#### Notes

1. The VCAN\_UV comparator is enabled if CAN Normal or CAN Receive Only Mode.
2. CAN Recovery Conditions:
  - 1.) TXD Time Out: TXD goes HIGH or transmitter is set to wake capable or switched off.
  - 2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
  - 3.) Supply under voltage: as soon as the threshold is crossed again, i.e. VCAN > VCAN\_UV for CAN.
  - 4.) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXD needs to be HIGH (recessive) for a certain time (transmitter enable time).

## **Serial Peripheral Interface**

3. *CANTO will be set only if CAN2 = 1 (=SWK Mode enabled). It will be set as soon as CANSIL was set and will stay set even in CANSIL it is reset. An interrupt is issued in Stop Mode and Normal Mode as soon as CANTO is set and the interrupt is not masked out, i.e. CANTO\_MASK must be set to 1.*
4. *The SYSERR Flag is set in case of a configuration error and in case of an error counter overflow ( $n > 32$ ) It is only updated if SWK is enabled (CAN\_2 = '1'). See also chapter x.*
5. *CANTO is set asynchronously to the INTN pulse. In order to prevent undesired clearing of CANTO and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INTN.*

## Serial Peripheral Interface

### Wake-up Source and Information Status

#### WK\_STAT

#### Wake-up Source and Information Status

(100 0100<sub>B</sub>)

Reset Value: see [Table 98](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES					RES	CAN_WU	TIMER2_WU	TIMER1_WU	RES		WK5_WU	WK4_WU	RES	RES	RES
r					r	rc	rc	rc	r		rc	rc	r	r	r

Field	Bits	Type	Description
RES	15:11	r	Reserved, always reads as 0
RES	10	r	Reserved, always reads as 0
CAN_WU	9	rc	Wake up via CAN Bus 0 <sub>B</sub> NO_WU, No Wake up 1 <sub>B</sub> WU, Wake up detected
TIMER2_WU	8	rc	Wake up via Timer2 0 <sub>B</sub> NO_WU, No Wake up 1 <sub>B</sub> WU, Wake up detected
TIMER1_WU	7	rc	Wake up via Timer1 0 <sub>B</sub> NO_WU, No Wake up 1 <sub>B</sub> WU, Wake up detected
RES	6:5	r	Reserved, always reads as 0
WK5_WU	4	rc	Wake up via WK5 0 <sub>B</sub> NO_WU, No Wake up 1 <sub>B</sub> WU, Wake up detected
WK4_WU	3	rc	Wake up via WK4 0 <sub>B</sub> NO_WU, No Wake up 1 <sub>B</sub> WU, Wake up detected
RES	2	r	Reserved, always reads as 0
RES	1	r	Reserved, always reads as 0
RES	0	r	Reserved, always reads as 0

**Table 98** Reset of **WK\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0xxx x000 00x0 <sub>B</sub>			

**Note:** At Fail-Safe Mode entry, the **WK\_STAT** register is automatically cleared by the device.

**Serial Peripheral Interface**

**WK Input Level**

**WK\_LVL\_STAT**

**WK Input Level**

(100 0101<sub>B</sub>)

Reset Value: see [Table 99](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES											WK5_LVL	WK4_LVL	RES	RES	RES
r											r	r	r	r	r

Field	Bits	Type	Description
RES	15:5	r	Reserved, always reads as 0
WK5_LVL	4	r	<b>Status of WK5</b> 0 <sub>B</sub> <b>LOW</b> , Low Level (=0) 1 <sub>B</sub> <b>HIGH</b> , High Level (=1)
WK4_LVL	3	r	<b>Status of WK4</b> 0 <sub>B</sub> <b>LOW</b> , Low Level (=0) 1 <sub>B</sub> <b>HIGH</b> , High Level (=1)
RES	2	r	Reserved, always reads as 0
RES	1	r	Reserved, always reads as 0
RES	0	r	Reserved, always reads as 0

**Table 99** Reset of [WK\\_LVL\\_STAT](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 00x0 <sub>B</sub>			
Restart	0000 0000 0000 00x0 <sub>B</sub>			

*Note:* WK\_LVL\_STAT is updated in Normal Mode and Stop Mode and also in Init and Restart Mode. In cyclic sense or wake mode, the registers contain the sampled level, i.e. the registers are updated after every sampling.

**Serial Peripheral Interface**

**High-Side Switch Status**

**HS\_OL\_OC\_OT\_STAT**

**High-Side Switch Status**

**(100 0110<sub>B</sub>)**

**Reset Value: see Table 100**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	RES	HS3_OT	HS2_OT	HS1_OT	RES	RES	HS3_OL	HS2_OL	HS1_OL	RES	RES	HS3_OC	HS2_OC	HS1_OC	
r	r	rc	rc	rc	r	r	rc	rc	rc	r	r	rc	rc	rc	

Field	Bits	Type	Description
RES	15:14	r	<b>Reserved, always reads as 0</b>
RES	13	r	<b>Reserved, always reads as 0</b>
HS3_OT	12	rc	<b>Overtemperature Detection on HS3</b> 0 <sub>B</sub> NO_OT, No OT 1 <sub>B</sub> OT, OT detected
HS2_OT	11	rc	<b>Overtemperature Detection on HS2</b> 0 <sub>B</sub> NO_OT, No OT 1 <sub>B</sub> OT, OT detected
HS1_OT	10	rc	<b>Overtemperature Detection on HS1</b> 0 <sub>B</sub> NO_OT, No OT 1 <sub>B</sub> OT, OT detected
RES	9	r	<b>Reserved, always reads as 0</b>
RES	8	r	<b>Reserved, always reads as 0</b>
HS3_OL	7	rc	<b>Open-Load Detection on HS3</b> 0 <sub>B</sub> NO_OL, No OL 1 <sub>B</sub> OL, OL detected
HS2_OL	6	rc	<b>Open-Load Detection on HS2</b> 0 <sub>B</sub> NO_OL, No OL 1 <sub>B</sub> OL, OL detected
HS1_OL	5	rc	<b>Open-Load Detection on HS1</b> 0 <sub>B</sub> NO_OL, No OL 1 <sub>B</sub> OL, OL detected
RES	4	r	<b>Reserved, always reads as 0</b>
RES	3	r	<b>Reserved, always reads as 0</b>
HS3_OC	2	rc	<b>Overcurrent Detection on HS3</b> 0 <sub>B</sub> NO_OC, No OC 1 <sub>B</sub> OC, OC detected
HS2_OC	1	rc	<b>Overcurrent Detection on HS2</b> 0 <sub>B</sub> NO_OC, No OC 1 <sub>B</sub> OC, OC detected
HS1_OC	0	rc	<b>Overcurrent Detection on HS1</b> 0 <sub>B</sub> NO_OC, No OC 1 <sub>B</sub> OC, OC detected



**Table 100** Reset of **HS\_OL\_OC\_OT\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx xxxx xxxx <sub>B</sub>			

### 13.6.2 Status registers bridge driver

#### General Status register

##### GEN\_STAT

##### General Status register

(101 0000<sub>B</sub>)

Reset Value: see [Table 101](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES						RES	HB3V OUT	HB2V OUT	HB1V OUT	PWM6 STAT	PWM5 STAT	PWM4 STAT	PWM3 STAT	PWM2 STAT	PWM1 STAT
						r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RES	15:10	r	Reserved, always reads as 0
RES	9	r	Reserved, always reads as 0
HB3VOUT	8	r	Voltage level at VSH3 when HB3MODE[1:0] = 11 and CPEN=1 <sup>1)</sup> 0 <sub>B</sub> LOW, VSH3 = Low : VS - VSH3 > V <sub>HS3VDSTHx</sub> 1 <sub>B</sub> HIGH, VSH3 = High: VS - VSH3 ≤ V <sub>HS3VDSTHx</sub>
HB2VOUT	7	r	Voltage level at VSH2 when HB2MODE[1:0] = 11 and CPEN=1 <sup>1)</sup> 0 <sub>B</sub> LOW, VSH2 = Low : VS - VSH2 > V <sub>HS2VDSTHx</sub> 1 <sub>B</sub> HIGH, VSH2 = High: VS - VSH2 ≤ V <sub>HS2VDSTHx</sub>
HB1VOUT	6	r	Voltage level at VSH1 when HB1MODE[1:0] = 11 and CPEN=1 <sup>1)</sup> 0 <sub>B</sub> LOW, VSH1 = Low : VS - VSH1 > V <sub>HS1VDSTHx</sub> 1 <sub>B</sub> HIGH, VSH1 = High: VS - VSH1 ≤ V <sub>HS1VDSTHx</sub>
PWM6STAT	5	r	PWM6 status 0 <sub>B</sub> LOW, PWM6 is Low 1 <sub>B</sub> HIGH, PWM6 is High
PWM5STAT	4	r	PWM5 status 0 <sub>B</sub> LOW, PWM5 is Low 1 <sub>B</sub> HIGH, PWM5 is High
PWM4STAT	3	r	PWM4 Status 0 <sub>B</sub> LOW, PWM4 is Low 1 <sub>B</sub> HIGH, PWM4 is High
PWM3STAT	2	r	PWM3 status 0 <sub>B</sub> LOW, PWM3 is Low 1 <sub>B</sub> HIGH, PWM3 is High
PWM2STAT	1	r	PWM2 Status 0 <sub>B</sub> LOW, PWM2 is Low 1 <sub>B</sub> HIGH, PWM2 is High
PWM1STAT	0	r	PWM1/CRC status 0 <sub>B</sub> LOW, PWM1/CRC is Low 1 <sub>B</sub> HIGH, PWM1/CRC is High

1) HBxVOUT = 0 if (CPEN=1 and HBxMODE ≠ 11) or CPEN=0.

**Table 101** Reset of **GEN\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 xx00 000x <sub>B</sub>			

Serial Peripheral Interface

Turn-on/off delay regulation register

TDREG

Turn-on/off delay regulation register

(101 0001<sub>B</sub>)

Reset Value: see [Table 102](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				RES	IPDCH G3_ST	IPDCH G2_ST	IPDCH G1_ST	RES	IPCHG 3_ST	IPCHG 2_ST	IPCHG 1_ST	RES	TDRE G3	TDRE G2	TDRE G1
r				r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RES	15:12	r	<b>Reserved, always reads as 0</b>
RES	11	r	<b>Reserved, always reads as 0</b>
IPDCHG3_ST	10	r	<b>HB3 predischage status</b> $0_B$ <b>CLAMP</b> , the predischage current is equal to 0.5 mA typ. or ICHGMAX3 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HB3_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < predischage current < ICHGMAX3 <sup>1)</sup>
IPDCHG2_ST	9	r	<b>HB2 predischage status</b> $0_B$ <b>CLAMP</b> , the predischage current is equal to 0.5 mA typ. or ICHGMAX2 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HB2_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < predischage current < ICHGMAX2 <sup>1)</sup>
IPDCHG1_ST	8	r	<b>HB1 predischage status</b> $0_B$ <b>CLAMP</b> , the predischage current is equal to the 0.5 mA typ. or ICHGMAX1 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HBx_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < predischage current < ICHGMAX1 <sup>1)</sup>
RES	7	r	<b>Reserved, always reads as 0</b>
IPCHG3_ST	6	r	<b>HB3 precharge status</b> $0_B$ <b>CLAMP</b> , the precharge current is equal to 0.5 mA typ. or ICHGMAX3 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HB3_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < precharge current < ICHGMAX3 <sup>1)</sup>
IPCHG2_ST	5	r	<b>HB2 precharge status</b> $0_B$ <b>CLAMP</b> , the precharge current is equal to 0.5 mA typ. or ICHGMAX2 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HB2_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < precharge current < ICHGMAX2 <sup>1)</sup>

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>IPCHG1_ST</b>	4	r	<b>HB1 precharge status</b> $0_B$ <b>CLAMP</b> , the precharge current is equal to the 0.5 mA typ. or ICHGMAX1 if AGC[1:0] = 10 <sub>B</sub> or 11 <sub>B</sub> , and HB1_PWM_EN = 1 <sup>1)</sup> $1_B$ <b>NO_CLAMP</b> , 0.5 mA < precharge current < ICHGMAX1 <sup>1)</sup>
<b>RES</b>	3	r	<b>Reserved, always reads as 0</b>
<b>TDREG3</b>	2	r	<b>HB3 Regulation of turn-on/off delay</b> $0_B$ <b>NO_REG</b> , tDON3 and tDOFF3 are not in regulation $1_B$ <b>REG</b> , tDON3 and/or tDOFF3 are in regulation
<b>TDREG2</b>	1	r	<b>HB2 Regulation of turn-on/off delay</b> $0_B$ <b>NO_REG</b> , tDON2 and tDOFF2 are not in regulation $1_B$ <b>REG</b> , tDON2 and/or tDOFF2 are in regulation
<b>TDREG1</b>	0	r	<b>HB1 Regulation of turn-on/off delay</b> $0_B$ <b>NO_REG</b> , tDON and tDOFF are not in regulation $1_B$ <b>REG</b> , tDON and/or tDOFF are in regulation

1) IPCHGx\_ST = 1 otherwise (PWM disabled, HB in high impedance or AGC[1:0] = 00<sub>B</sub> or 01<sub>B</sub>).

**Table 102 Reset of TDREG**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 xx00 000x <sub>B</sub>			

**Serial Peripheral Interface**

**Drain-source overvoltage status**

**DSOV**

**Drain-source overvoltage**

**(101 0010<sub>B</sub>)**

**Reset Value: see [Table 103](#)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>RES</b>	<b>OC_CSA</b>	<b>VSINT OVBRAKE_ST</b>	<b>VSOV BRAKE_ST</b>	<b>RES</b>	<b>LS3DS OV_BRK</b>	<b>LS2DS OV_BRK</b>	<b>LS1DS OV_BRK</b>	<b>RES</b>	<b>RES</b>	<b>LS3DS OV</b>	<b>HS3D SOV</b>	<b>LS2DS OV</b>	<b>HS2D SOV</b>	<b>LS1DS OV</b>	<b>HS1D SOV</b>
r	rc	rc	rc	r	rc	rc	rc	r	r	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
<b>RES</b>	15	r	<b>Reserved, always reads as 0</b>
<b>OC_CSA</b>	14	rc	<b>CSA Overcurrent detection</b> 0 <sub>B</sub> <b>NO_OC</b> , No overcurrent detected 1 <sub>B</sub> <b>OC</b> , Overcurrent detected
<b>VSINTOVBRAKE_ST</b>	13	rc	<b>VSINT Brake status</b> 0 <sub>B</sub> <b>NOT_DETECT</b> , VSINT overvoltage brake condition is not detected 1 <sub>B</sub> <b>DETECT</b> , VSINT overvoltage brake conditions is detected
<b>VSOVBRAKE_ST</b>	12	rc	<b>VS Brake status</b> 0 <sub>B</sub> <b>NOT_DETECT</b> , VS overvoltage brake conditions is not detected 1 <sub>B</sub> <b>DETECT</b> , VS overvoltage brake conditions is detected
<b>RES</b>	11	r	<b>Reserved, always reads as 0</b>
<b>LS3DSOV_BRK</b>	10	rc	<b>Drain-source overvoltage on low-side 3 during braking</b> 0 <sub>B</sub> <b>NO_OV</b> , No drain-source overvoltage on LS3 1 <sub>B</sub> <b>OV</b> , Drain-source overvoltage on LS3
<b>LS2DSOV_BRK</b>	9	rc	<b>Drain-source overvoltage on low-side 2 during braking</b> 0 <sub>B</sub> <b>NO_OV</b> , No drain-source overvoltage on LS2 1 <sub>B</sub> <b>OV</b> , Drain-source overvoltage on LS2
<b>LS1DSOV_BRK</b>	8	rc	<b>Drain-source overvoltage on low-side 1 during braking</b> 0 <sub>B</sub> <b>NO_OV</b> , No drain-source overvoltage on LS1 1 <sub>B</sub> <b>OV</b> , Drain-source overvoltage on LS1
<b>RES</b>	7	r	<b>Reserved, always reads as 0</b>
<b>RES</b>	6	r	<b>Reserved, always reads as 0</b>
<b>LS3DSOV</b>	5	rc	<b>Drain-source overvoltage on low-side 3</b> 0 <sub>B</sub> <b>NO_OV</b> , No drain-source overvoltage on LS3 1 <sub>B</sub> <b>OV</b> , Drain-source overvoltage on LS3

**Serial Peripheral Interface**

Field	Bits	Type	Description
<b>HS3DSOV</b>	4	rc	<b>Drain-source overvoltage on high-side 3</b> $0_B$ <b>NO_OV</b> , No drain-source overvoltage on HS3 $1_B$ <b>OV</b> , Drain-source overvoltage on HS3
<b>LS2DSOV</b>	3	rc	<b>Drain-source overvoltage on low-side 2</b> $0_B$ <b>NO_OV</b> , No drain-source overvoltage on LS2 $1_B$ <b>OV</b> , Drain-source overvoltage on LS2
<b>HS2DSOV</b>	2	rc	<b>Drain-source overvoltage on high-side 2</b> $0_B$ <b>NO_OV</b> , No drain-source overvoltage on HS2 $1_B$ <b>OV</b> , Drain-source overvoltage on HS2
<b>LS1DSOV</b>	1	rc	<b>Drain-source overvoltage on low-side 1</b> $0_B$ <b>NO_OV</b> , No drain-source overvoltage on LS1 $1_B$ <b>OV</b> , Drain-source overvoltage on LS1
<b>HS1DSOV</b>	0	rc	<b>Drain-source overvoltage on high-side 1</b> $0_B$ <b>NO_OV</b> , No drain-source overvoltage on HS1 $1_B$ <b>OV</b> , Drain-source overvoltage on HS1

**Table 103 Reset of DSOV**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0xxx 0xxx 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

Effective MOSFET turn.on/off delay - PWM half-bridge 1

EFF\_TDON\_OFF1

Effective MOSFET turn.on/off delay - HB1 (101 0011<sub>B</sub>)

Reset Value: see [Table 104](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TDOFF1EFF						RES		TDON1EFF					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TDOFF1EFF	13:8	r	Effective active MOSFET turn-off delay HB1 Nominal effective tDOFF1 = 53.3 ns x TDOFF1EFF[13:8] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TDON1EFF	5:0	r	Effective active MOSFET turn-on delay HB1 Nominal effective tDON1 = 53.3 ns x TDON1EFF[5:0] <sub>D</sub>

Table 104 Reset of [EFF\\_TDON\\_OFF1](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			



Serial Peripheral Interface

Effective MOSFET turn.on/off delay - PWM half-bridge 2

EFF\_TDON\_OFF2

Effective MOSFET turn.on/off delay - HB 2 (101 0100<sub>B</sub>)

Reset Value: see [Table 105](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TDOFF2EFF						RES		TDON2EFF					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TDOFF2EFF	13:8	r	Effective active MOSFET turn-off delay HB2 Nominal effective tDOFF2 = 53.3 ns x TDOFF2EFF[13:8] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TDON2EFF	5:0	r	Effective active MOSFET turn-on delay HB2 Nominal effective tDON2 = 53.3 ns x TDON2EFF[5:0] <sub>D</sub>

Table 105 Reset of [EFF\\_TDON\\_OFF2](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

Effective MOSFET turn.on/off delay - PWM half-bridge 3

EFF\_TDON\_OFF3

Effective MOSFET turn.on/off delay - HB3 (101 0101<sub>B</sub>)

Reset Value: see [Table 106](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TDOFF3EFF						RES		TDON3EFF					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TDOFF3EFF	13:8	r	Effective active MOSFET turn-off delay HB3 Nominal effective tDOFF3 = 53.3 ns x TDO3EFF[13:8] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TDON3EFF	5:0	r	Effective active MOSFET turn-on delay HB3 Nominal effective tDON3 = 53.3 ns x TDON3EFF[5:0] <sub>D</sub>

Table 106 Reset of [EFF\\_TDON\\_OFF3](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

MOSFET rise/fall time - PWM half-bridge 1

TRISE\_FALL1

MOSFET rise/fall time - HB1

(101 0111<sub>B</sub>)

Reset Value: see [Table 107](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TFALL1						RES		TRISE1					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TFALL1	13:8	r	Active MOSFET fall time HB1 Nominal tFALL1 = 53.3 ns x TFALL1[5:0] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TRISE1	5:0	r	Active MOSFET rise time HB1 Nominal tRISE1 = 53.3 ns x TRISE1[5:0] <sub>D</sub>

Table 107 Reset of [TRISE\\_FALL1](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

MOSFET rise/fall time - PWM half-bridge 2

TRISE\_FALL2

MOSFET rise/fall time - HB2

(101 1000<sub>B</sub>)

Reset Value: see [Table 108](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TFALL2						RES		TRISE2					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TFALL2	13:8	r	Active MOSFET fall time HB2 Nominal tFALL2 = 53.3 ns x TFALL2[5:0] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TRISE2	5:0	r	Active MOSFET rise time HB2 Nominal tRISE2 = 53.3 ns x TRISE2[5:0] <sub>D</sub>

Table 108 Reset of [TRISE\\_FALL2](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			

Serial Peripheral Interface

MOSFET rise/fall time - PWM half-bridge 3

TRISE\_FALL3

MOSFET rise/fall time - HB3

(101 1001<sub>B</sub>)

Reset Value: see [Table 109](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TFALL3						RES		TRISE3					
r		r						r		r					

Field	Bits	Type	Description
RES	15:14	r	Reserved, always reads as 0
TFALL3	13:8	r	Active MOSFET fall time HB3 Nominal tFALL3 = 53.3 ns x TFALL3[5:0] <sub>D</sub>
RES	7:6	r	Reserved, always reads as 0
TRISE3	5:0	r	Active MOSFET rise time HB3 Nominal tRISE3 = 53.3 ns x TRISE3[5:0] <sub>D</sub>

Table 109 Reset of [TRISE\\_FALL3](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	00xx xxxx 00xx xxxx <sub>B</sub>			

### 13.6.3 Selective wake status registers

#### Selective Wake Status

##### SWK\_STAT

##### Selective Wake Status

(110 0000<sub>B</sub>)

Reset Value: see [Table 110](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES									SYNC	WUP	WUF	CANSI L	SWK_ SET	RES	
r									r	rc	rc	r	r	r	

Field	Bits	Type	Description
RES	15:7	r	Reserved, always reads as 0
SYNC	6	r	<b>Synchronisation (at least one CAN frame without fail must have been received)</b> 0 <sub>B</sub> <b>NO_SYNC</b> , SWK function not working or not synchronous to CAN bus 1 <sub>B</sub> <b>SYNC</b> , Valid CAN frame received, SWK function is synchronous to CAN bus
WUP	5	rc	<b>Wake-up Pattern Detection</b> 0 <sub>B</sub> <b>NO_WUP</b> , No WUP 1 <sub>B</sub> <b>WUP_DETECTED</b> , WUP detected
WUF	4	rc	<b>SWK Wake-up Frame Detection</b> 0 <sub>B</sub> <b>NO_WUF</b> , No WUF 1 <sub>B</sub> <b>WUF_DETECTED</b> , WUF detected
CANSIL	3	r	<b>CAN Silent Time during SWK operation</b> 0 <sub>B</sub> <b>NO_SIL</b> , tsilence not exceeded 1 <sub>B</sub> <b>SIL_EXCEEDED</b> , set if tsilence is exceeded.
SWK_SET	2	r	<b>Selective Wake Activity</b> 0 <sub>B</sub> <b>INACTIVE</b> , Selective Wake is not active 1 <sub>B</sub> <b>ACTIVE</b> , Selective Wake is activated
RES	1:0	r	Reserved, always reads as 0

**Table 110** Reset of **SWK\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 0xxx xx00 <sub>B</sub>			

*Note:* **SWK\_SET** is set to flag that the selective wake functionality is activated (**SYSERR** = 0, **CFG\_VAL** = 1, **CAN\_2** = 1). The selective wake function is activated via a CAN mode change, except if **CAN** = '100'.

## Serial Peripheral Interface

### Selective Wake ECNT Status

#### SWK\_ECNT\_STAT

##### Selective Wake ECNT Status

(110 0001<sub>B</sub>)

Reset Value: see [Table 111](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES										ECNT					
r										r					

Field	Bits	Type	Description
RES	15:6	r	Reserved, always reads as 0
ECNT	5:0	r	<b>SWK CAN Frame Error Counter</b> 00 0000 <sub>B</sub> <b>NO_ERR</b> , No Frame Error 01 1111 <sub>B</sub> <b>31</b> , 31 Frame Errors have been counted 10 0000 <sub>B</sub> <b>OVERFLOW</b> , Error counter overflow - SWK function will be disabled

**Table 111** Reset of [SWK\\_ECNT\\_STAT](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0000 0000 0000 <sub>B</sub>			
Restart	0000 0000 00xx xxxx <sub>B</sub>			

**Note:** If a frame has been received that is valid according to ISO11898-2:2016 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR shall be set and CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

**Serial Peripheral Interface**

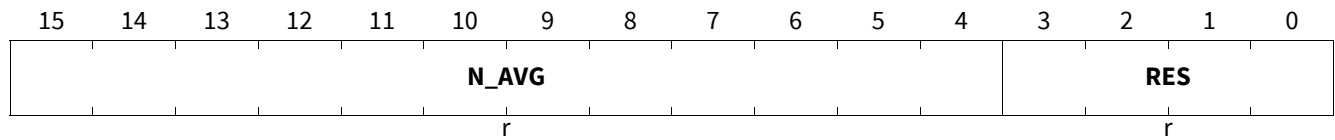
**Selective Wake CDR Status**

**SWK\_CDR\_STAT**

**Selective Wake CDR Status**

**(110 0011<sub>B</sub>)**

**Reset Value: see Table 112**



Field	Bits	Type	Description
<b>N_AVG</b>	15:4	r	<b>Output Value from Filter Block</b> N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit.
<b>RES</b>	3:0	r	<b>Reserved, always reads as 0</b>

**Table 112 Reset of SWK\_CDR\_STAT**

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	1010 0000 0000 0000 <sub>B</sub>			
Restart	xxxx xxxx xxxx 0000 <sub>B</sub>			



### 13.6.4 Family and product information register

#### Family and Product Identification Register

##### FAM\_PROD\_STAT

Family and Product Identification Register (111 0000<sub>B</sub>)

Reset Value: see [Table 113](#)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES					FAM					PROD					
r					r					r					

Field	Bits	Type	Description
RES	15:11	r	Reserved, always reads as 0
FAM	10:7	r	<b>Device Family Identifier</b> 1000 <sub>B</sub> , BLDC Motor System IC
PROD	6:0	r	<b>Device Product Identifier</b> 000 0000 <sub>B</sub> <b>TLE9562-3QX/QX</b> , TLE9562-3QX/-3QXJ/QX 000 0001 <sub>B</sub> <b>TLE9561-3QX/QX</b> , TLE9561-3QX/-3QXJ/QX 000 0010 <sub>B</sub> <b>TLE9563-3QX</b> , TLE9563-3QX/-3QXJ 000 0011 <sub>B</sub> <b>TLE9564QX</b> , TLE9564QX, TLE9185QX 001 0000 <sub>B</sub> <b>TLE9562-3QX V33</b> , TLE9562-3QX V33 001 0010 <sub>B</sub> <b>TLE9563-3QX V33</b> , TLE9563-3QX V33 001 0011 <sub>B</sub> <b>TLE9564QX V33</b> , TLE9564QX V33, TLE9185QX V33 001 1000 <sub>B</sub> <b>TLE9560QX</b> , TLE9560-3QX/-3QXJ

**Table 113** Reset of [FAM\\_PROD\\_STAT](#)

Register Reset Type	Reset Values	Reset Short Name	Reset Mode	Note
POR/Soft reset	0000 0100 0000 0010 <sub>B</sub>			
Restart	0000 0100 0000 0010 <sub>B</sub>			

## 13.7 Electrical Characteristics

**Table 114 Electrical Characteristics: Power Stage**

$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			

### SPI frequency

Maximum SPI frequency	$f_{SPI,max}$	–	–	6.0	MHz	<sup>1)</sup> $V_{CC1} > 3 \text{ V}$	P_14.7.1
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### SPI Interface; Logic Inputs SDI, CLK and CSN

H-input Voltage Threshold	$V_{IH}$	–	–	$0.7 \times V_{CC1}$	V	–	P_14.7.2
L-input Voltage Threshold	$V_{IL}$	$0.3 \times V_{CC1}$	–	–	V	–	P_14.7.3
Hysteresis of input Voltage	$V_{IHY}$	–	$0.12 \times V_{CC1}$	–	V	<sup>1)</sup>	P_14.7.4
Pull-up Resistance at pin CSN	$R_{ICSN}$	20	40	80	k $\Omega$	–	P_14.7.5
Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	k $\Omega$	$V_{SDI/CLK} = 0.2 \times V_{CC1}$	P_14.7.6
Input Capacitance at pin CSN, SDI or CLK	$C_I$	–	10	–	pF	<sup>1)</sup> $V_{CSN}, V_{SDI}, V_{CLK} = V_{CC1}$	P_14.7.7

### Logic Output SDO

H-output Voltage Level	$V_{SDOH}$	$0.8 \times V_{CC1}$	–	–	V	$I_{DOH} = -2 \text{ mA}$	P_14.7.8
L-output Voltage Level	$V_{SDOL}$	–	–	$0.2 \times V_{CC1}$	V	$I_{DOL} = 2 \text{ mA}$	P_14.7.9
‘Tri-state Input Capacitance	$C_{SDO}$	–	10	15	pF	<sup>1)</sup> $V_{CSN}, V_{SDI}, V_{CLK} = V_{CC1}$	P_14.7.11
Tri-state Leakage Current	$I_{SDOLK}$	–10	–	10	$\mu\text{A}$	<sup>1)</sup> $V_{CSN} = V_{CC1}$ , $0\text{V} < V_{SDO} < V_{CC1}$	P_14.7.38

### Data Input Timing<sup>1)</sup>

Clock Period	$t_{pCLK}$	160	–	–	ns	–	P_14.7.12
Clock HIGH Time	$t_{CLKH}$	70	–	–	ns	–	P_14.7.13
Clock LOW Time	$t_{CLKL}$	70	–	–	ns	–	P_14.7.14
Clock LOW before CSN LOW	$t_{bef}$	70	–	–	ns	–	P_14.7.15
CSN Setup Time	$t_{lead}$	160	–	–	ns	–	P_14.7.16
CLK Setup Time	$t_{lag}$	160	–	–	ns	–	P_14.7.17
Clock LOW after CSN HIGH	$t_{beh}$	70	–	–	ns	–	P_14.7.18
SDI Setup Time	$t_{DISU}$	60	–	–	ns	–	P_14.7.19
SDI Hold Time	$t_{DIHO}$	40	–	–	ns	–	P_14.7.20

**Serial Peripheral Interface**

**Table 114 Electrical Characteristics: Power Stage** (cont'd)

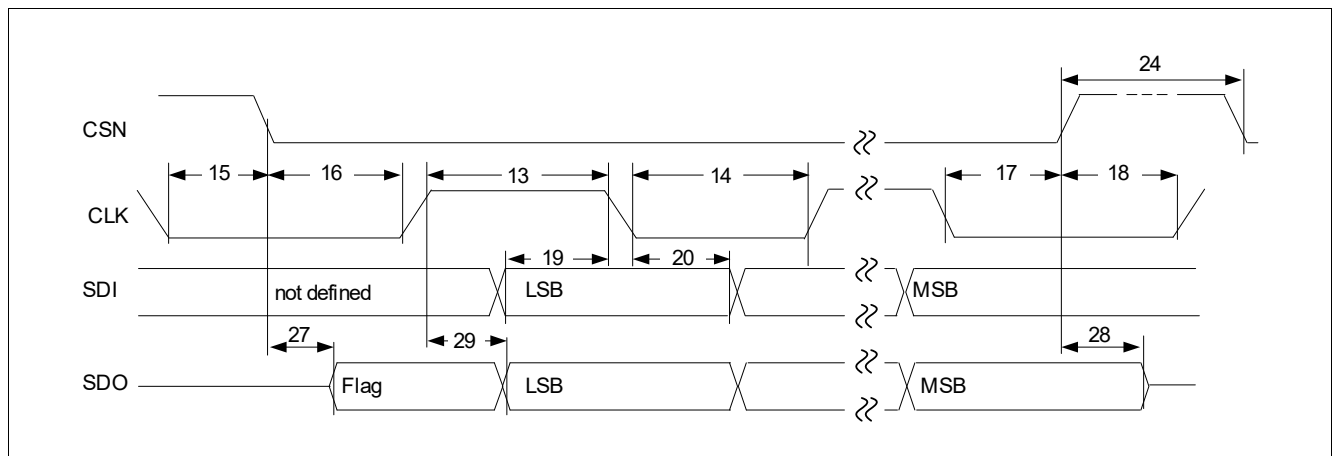
$V_{SINT} = 5.5 \text{ V to } 28 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Signal Rise Time at pin SDI, CLK and CSN	$t_{rIN}$	–	–	20	ns	–	P_14.7.21
Input Signal Fall Time at pin SDI, CLK and CSN	$t_{fIN}$	–	–	20	ns	–	P_14.7.22
Delay Time for Mode Changes <sup>2)</sup>	$t_{Del, Mode}$	–	–	5	$\mu\text{s}$	<sup>3)</sup>	P_14.7.23
CSN HIGH Time	$t_{CSN(high)}$	3	–	–	$\mu\text{s}$	–	P_14.7.24

**Data Output Timing<sup>1)</sup>**

SDO Rise Time	$t_{rSDO}$	–	30	40	ns	$C_L = 50 \text{ pF}$ , $0.2 \times V_{CC1}$ to $0.8 \times V_{CC1}$	P_14.7.25
SDO Fall Time	$t_{fSDO}$	–	30	40	ns	$C_L = 50 \text{ pF}$ , $0.8 \times V_{CC1}$ to $0.2 \times V_{CC1}$	P_14.7.26
SDO Enable Time	$t_{ENSDO}$	–	–	40	ns	LOW impedance	P_14.7.27
SDO Disable Time	$t_{DISSDO}$	–	–	40	ns	HIGH impedance	P_14.7.28
SDO Valid Time	$t_{VASDO}$	–	–	40	ns	$C_L = 50 \text{ pF}$	P_14.7.29

- 1) Not subject to production test; specified by design.
- 2) Applies to all mode changes triggered via SPI commands.
- 3) Guaranteed by design.



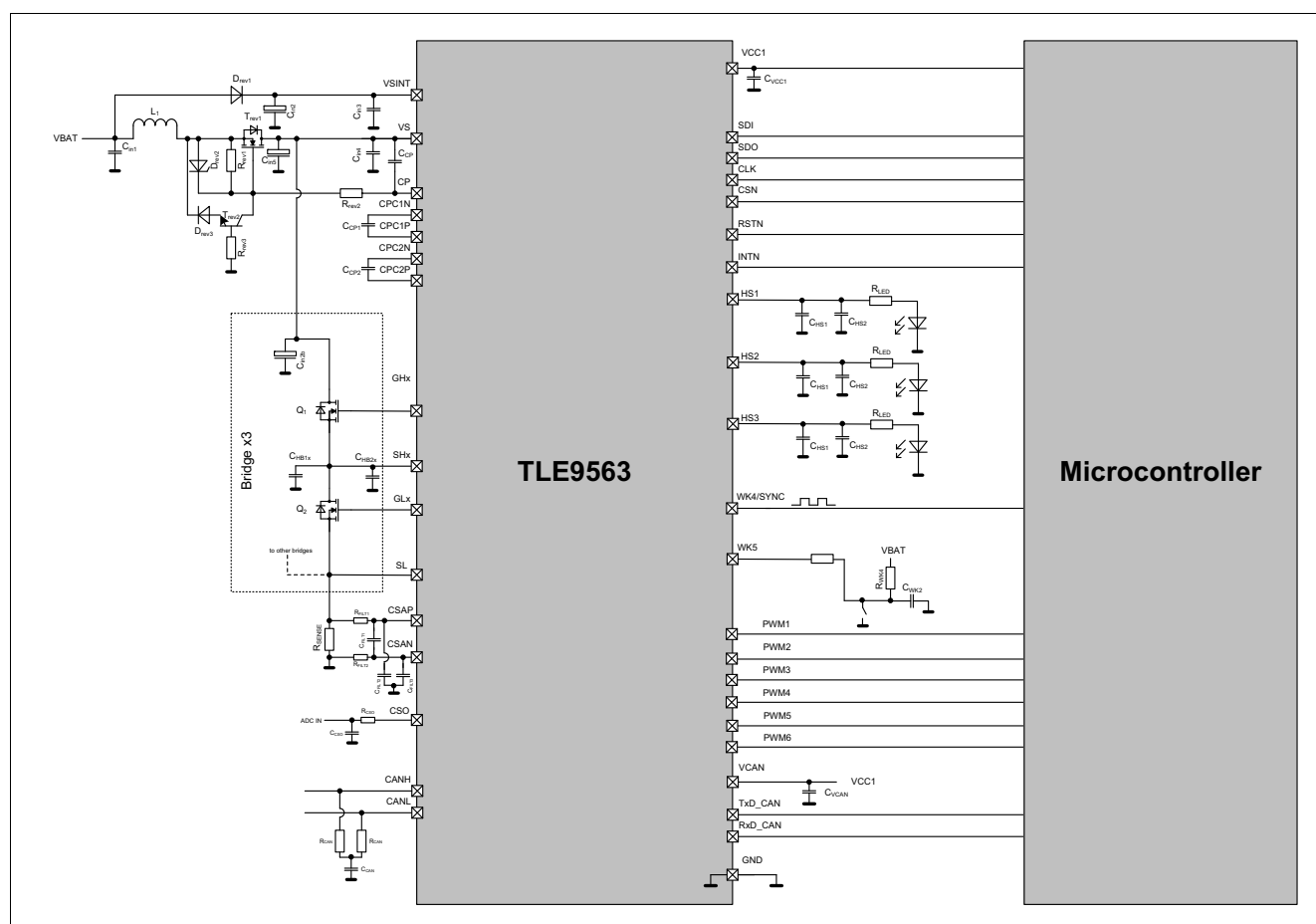
**Figure 80 SPI Timing Diagram**

**Note:** Numbers in drawing correlate with the last 2 digits of the Number field in the Electrical Characteristics table.

## 14 Application Information

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

### 14.1 Application Diagrams



**Figure 81 TLE9563-3QX Application Diagram**

**Note:** This is a very simplified example of an application circuit. The function must be always verified in the real application.

**Application Information**

**Table 115 Bill of Material**

Ref.	Typical Value	Purpose / Comment
<b>Capacitances</b>		
C <sub>in1</sub>	100 nF ±20% ceramic	Input filter battery capacitor for optimum EMC behavior
C <sub>in2</sub>	100 µF ±20%, 50 V Electrolytic	Buffering capacitor to cut off battery spikes, depending on the application
C <sub>in2b</sub>	470 µF ±20%, 50 V Electrolytic	Buffering capacitor for bridges. Cut off battery spikes, depending on the application
C <sub>in3</sub>	100 nF ±20%, 50 V Ceramic	Input capacitor
C <sub>in4</sub>	100 nF ±20%, 50 V Ceramic	Input capacitor
C <sub>in5</sub>	470 µF ±20%, 50 V Electrolytic	Buffering capacitor for bridges. Cut off battery spikes, depending on the application
C <sub>CP</sub>	470 nF ±20%, 50 V Ceramic	Charge-Pump buffering capacitor
C <sub>CP1</sub> / C <sub>CP2</sub>	220 nF ±20%, 50 V Ceramic	Charge-Pump flying capacitor to be placed as closed as possible to the device pins, in order to minimize the length of the PCB tracks
C <sub>FILT1</sub>	1.5 nF ±20%, 16 V Ceramic	Current-sense filtering
C <sub>FILT2</sub> / C <sub>FILT3</sub>	22 nF ±20%, 16 V Ceramic	Current-sense filtering
C <sub>CSO</sub>	16 V Ceramic	CSO buffering cap for a stable ADC voltage. Max 400 pF in case no resistor is used. With 50 Ω resistor up to 2.2 nF. (See CSA configuration register)
C <sub>CAN</sub>	4.7 nF / OEM dependent	Split termination stability
C <sub>VCC1</sub>	2.2 µF ±20%, 16 V	Blocking capacitor. Low ESR. Minimum 1 µF effective capacitance
C <sub>VCAN</sub>	1 µF ... 4.7 µF	Input filter CAN supply. The capacitor must be placed close to the VCAN pin. For optimum EMC and CAN FD performances, the capacitor has to be ≥ 2.2 µF
C <sub>HB1x</sub>	10 nF ±20%, 50 V Ceramic	Half-Bridge EME (electromagnetic emission) and ESD suppression filter to be placed close to the connector. Other capacitance values might be needed depending on application
C <sub>HB2x</sub>	560 pF ±20%, 50 V Ceramic	Optional filter for EMI immunity to be placed close to the SHx pin (PCB footprints highly recommended). Other capacitance values might be needed depending on application
C <sub>HS1</sub>	47 pF / OEM dependent	Only required on case of off-board connection to optimize EMC behavior, place close to pin
C <sub>HS2</sub>	33 nF / OEM dependent	As required by application, mandatory protection for off-board connection

**Application Information**

**Table 115 Bill of Material** (cont'd)

Ref.	Typical Value	Purpose / Comment
$C_{WK1} / C_{WK2}$	47 nF / OEM dependent	Spike filtering, as required by application, mandatory protection for off-board connections
<b>Inductances</b>		
$L_1$	4 uH ... 6 uH	Input filter for power stage - consider high current rating (application dependent)
<b>Resistances</b>		
$R_{REV1}$	100 k $\Omega$ $\pm$ 5%	Other values needed depending on application
$R_{REV2}$	10 k $\Omega$ $\pm$ 5%	Device protection against reverse battery
$R_{REV3}$	10 k $\Omega$ $\pm$ 5%	
$R_{SENSE}$	5 m $\Omega$ $\pm$ 1%	Current-sense resistor
$R_{FILT1} / R_{FILT2}$	4.7 $\Omega$ $\pm$ 5%	Current-sense filtering
$R_{CSO}$	50 $\Omega$ $\pm$ 5%	Compensation for internal opamp. Depending on SPI configuration
$R_{CAN}$	60 $\Omega$ / OEM dependent	CAN bus termination
$R_{LED}$	1 k	Limit LED-current
$R_{WK1} / R_{WK2} / R_{WK3} / R_{WK4}$	10 k $\Omega$ $\pm$ 5%	
<b>Active Components</b>		
$D_{REV1}$	RR268MM600	Reverse polarity protection
$D_{REV2}$	BZX84C16	Gate protection. Limit $V_{GS}$
$D_{REV3}$	BAS21	
$T_{REV1}$	IPZ40N04S5L-2R8	Reverse battery protection, N-MOS
$T_{REV2}$	BC846	
$Q_1 / Q_2$	IPZ40N04S5-3R1	Main power switches

## Application Information

### 14.2 ESD Tests

#### 14.2.1 ESD according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “GUN test” (150 pF, 330  $\Omega$ ) have been performed. The results and test condition are available in a test report. The values for the test are listed below.

**Table 116 ESD “GUN test”<sup>1)2)</sup>**

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, HSx, VS, VSINT, VS, WKx versus GND	> 6	kV	positive pulse
ESD at pin CANH, CANL, HSx, VS, VSINT, VS, WKx versus GND	< -6	kV	negative pulse

- 1) ESD susceptibility “ESD GUN” according to EMC 1.3 Test specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau, EMC Test report Nr. 20.12.20).
- 2) ESD Test “Gun Test” is specified with external components for pins VS, VSINT, VS, WKx, HSx. See the application diagram in [Chapter 14.1](#) for more information.

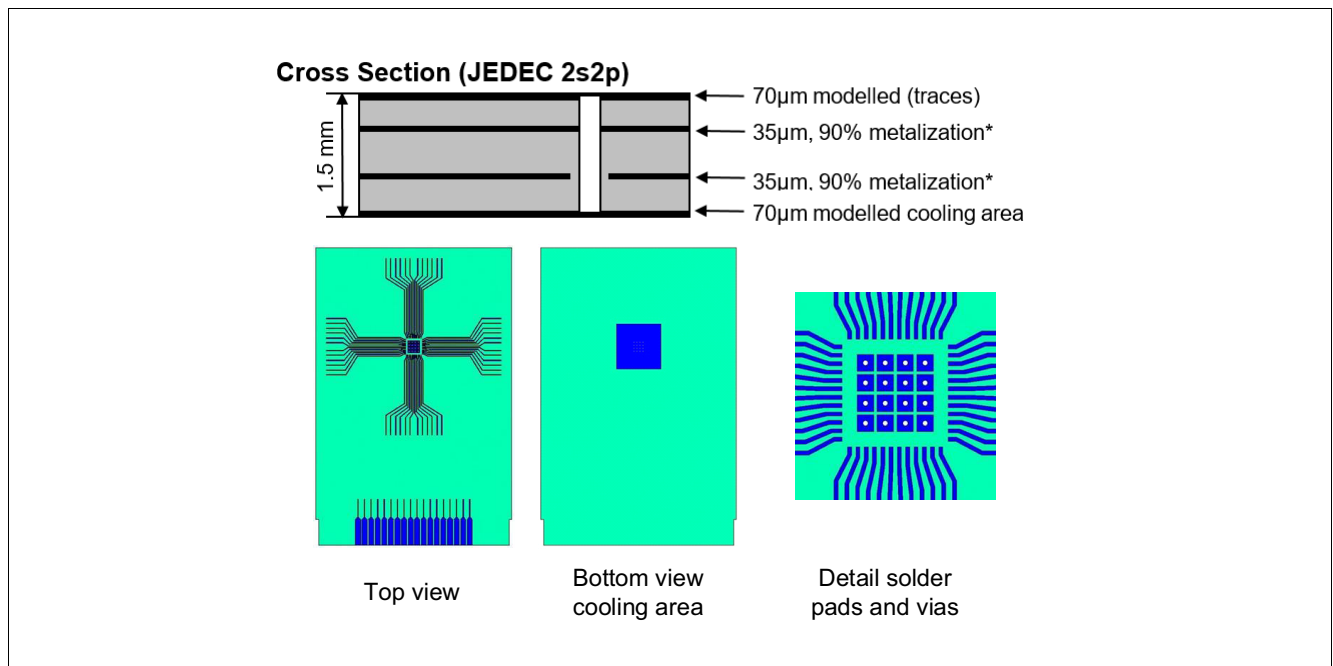
#### 14.2.2 ESD according to SAE J2962

Tests for ESD robustness according to SAE J2962 have been performed.

**Table 117 ESD according to SAE J2962**

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, versus GND	$\pm 4$	kV	Unpowered, contact discharge
ESD at pin CANH, CANL versus GND	$\pm 8$	kV	Powered, contact discharge
ESD at pin CANH, CANL versus GND	$\pm 15$	kV	Powered, air discharge

### 14.3 Thermal Behavior of Package



**Figure 82 Board Setup**

Board setup is defined according JESD 51-2, -5, -7.

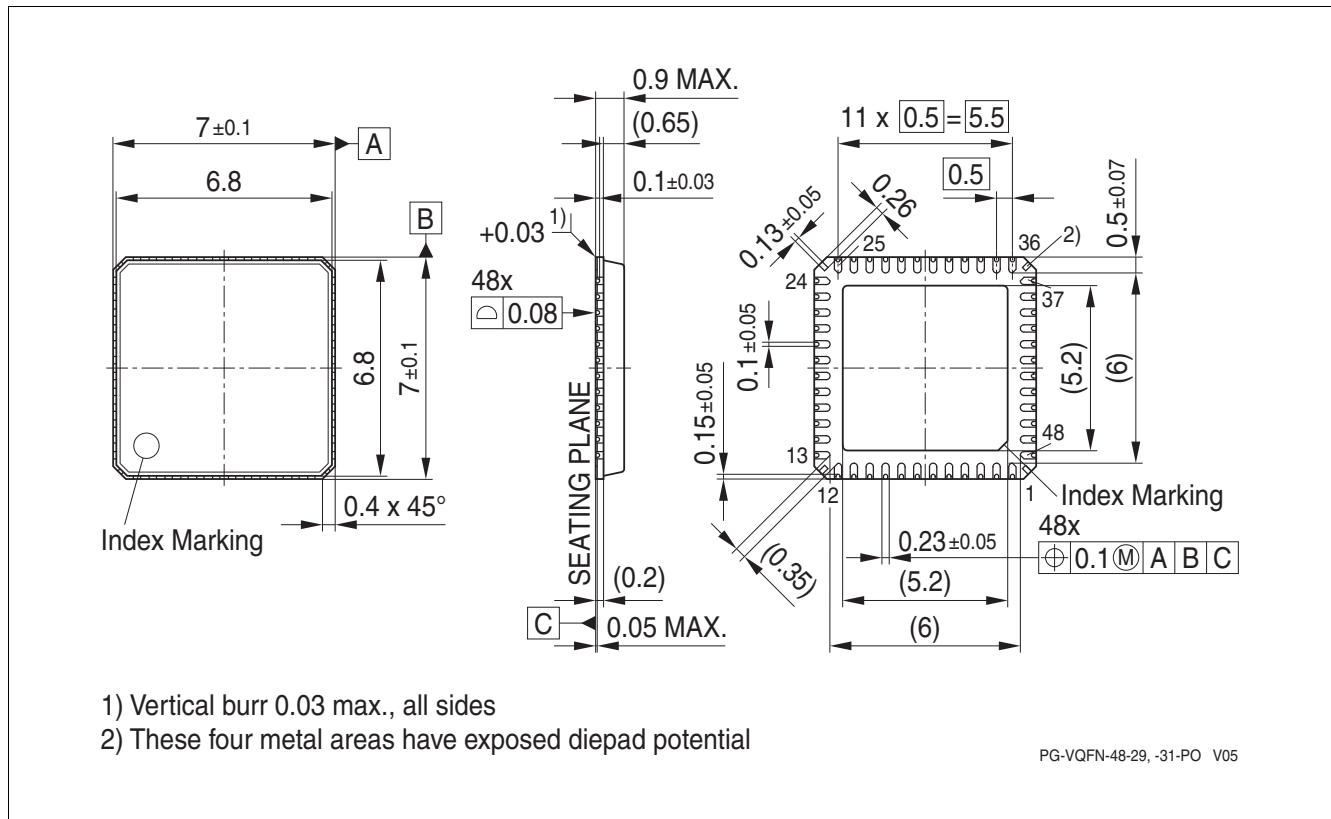
Board:  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  with 2 inner copper layers (35 μm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300 mm<sup>2</sup> cooling area on the bottom layer (70 μm).

### 14.4 Further Application Information

- The VS pin supplies the bridge driver and the charge pump, and is the sense pin for the high-side MOSFETs drain voltage. It is therefore highly recommended to connect a 100 nF / 50V ceramic by-pass capacitor as close as possible to the VS pin with a short PCB trace to GND.
- Please contact us for information regarding the FMEA pin
- For further information you may contact <http://www.infineon.com/>



## 15 Package Outlines



**Figure 83 PG-VQFN-48<sup>1)</sup>**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision History**

## **16 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2021-01-21	First release

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