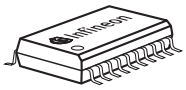
Dual Low-Drop Voltage Regulator

TLE 4470

Features

- Stand-by output 180 mA; 5 V ± 2%
- Adjustable reset switching threshold
- Main output 350 mA; tracked to the stand-by output
- Low quiescent current consumption in standby mode
- Disable function for main output
- Wide operation range: up to 45 V
- Very low dropout
- Power-On-Reset circuit sensing the stand-by voltage
- Early warning comparator for supply undervoltage
- Output protected against short circuit
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection
- Green Product (RoHS compliant)
- AEC Qualified

PG-DSO-14



PG-DSO-20

Functional Description

The TLE 4470 is a monolithic integrated voltage regulator with two very low-drop outputs, a main output Q2 for loads up to 350 mA and a stand by output Q1 providing a maximum of 180 mA. The device is available in two packages the PG-DSO-14 and PG-DSO-20. It is designed to supply microprocessor systems under the severe conditions of automotive applications and is therefore equipped with additional protection functions against overload, short circuit and overtemperature. Of course the TLE 4470 can also be used in other applications where two stabilized voltages are required.

The device operates in the wide junction temperature range of -40 °C to 150 °C.

The stand-by regulator transforms an input voltage V_I in the range of 5.6 V ≤ V_I ≤ 45 V to $V_{Q1,nom}$ = 5 V within an accuracy of 2%, whereas the main regulator is adjustable. By

Type	Package
TLE 4470 GS	PG-DSO-14
TLE 4470 G	PG-DSO-20

use of an external voltage divider the main output voltage can be set to $V_{Q2} \geq 5$ V for the TLE 4470 G type (PG-DSO-20 package). V_{Q1} is compared to the voltage at pin ADJ2, which is proportional to the output voltage V_{Q2}. A control amplifier drives the base of the series PNP transistor via a buffer.

The main output voltage V_{Q2} is tracked to the accuracy of the stand-by output.

For the TLE 4470 GS (PG-DSO-14 package) the output voltage is fixed to 5 V.

To save energy e.g. in battery powered body electronic applications, the main regulator can be switched off via the disable input, which causes the current consumption to drop to 180 µA typical.

Two additional features of the TLE 4470 are an early warning comparator (can be used e.g. to monitor the supply voltage V_I) and reset generator with an adjustable reset delay time. The TLE 4470 G (PG-DSO-20 package) has in addition an adjustable reset switching threshold. This feature is useful with microprocessors which guarantee a safe operation down to voltages below the internally set reset threshold of 4.65 V typical.

Two functions are included in the reset generator, a power-on-reset and an under-voltage reset. The power-on-reset feature is necessary for a defined start of the microprocessor when switching on the application. The reset signal is kept low for a certain delay time after the output voltage V_{Q1} of the regulator has surpassed the reset threshold. An external delay capacitor sets this delay time. The under voltage reset circuit supervises the stand-by output voltage. In case V_{Q1} falls below the reset switching threshold the reset output is set LOW after a short reaction time. The reset LOW signal is generated down to an output voltage V_{Q1} of 1 V.

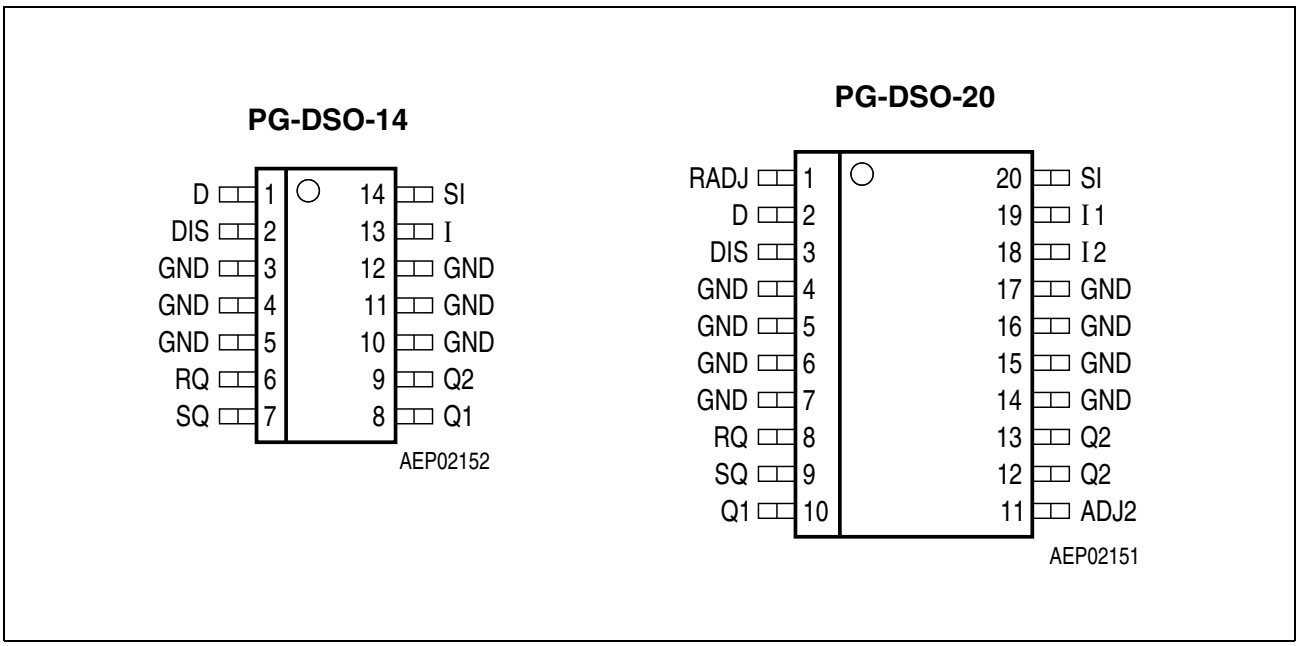


Figure 1 **Pin Configuration** (top view)

Pin Definitions and Functions

Table 1 PG-DSO-20

Pin No.	Symbol	Function
1	RADJ	**Reset switching threshold adjust;** for setting the reset switching threshold connect to a voltage divider from Q1 to GND. If this input is connected to GND, the reset is triggered at the internal threshold.
2	D	**Reset delay;** connect a capacitor C_D to GND for delay time adjustment
3	DIS	**Disable input main regulator;** Q2 disabled with high signal
4, 5, 6, 7	GND	**Ground**
8	RQ	**Reset output;** the open collector output is connected to Q1 via an integrated 30 kΩ resistor
9	SQ	**Sense output;** the open collector output is connected to Q1 via an integrated 30 kΩ resistor
10	Q1	**Stand-by regulator output voltage;** block to GND with a capacitor $C_{Q1} \geq 6$ µF, ESR < 10 Ω at 10 kHz
11	ADJ2	**Main regulator adjust input;** Q2 can be set to higher values than 5 V by an external voltage divider from Q2 to GND
12, 13	Q2	**Main regulator output voltage;** block to GND with a capacitor $C_{Q2} \geq 10$ µF, ESR < 10 Ω at 10 kHz
14, 15, 16, 17	GND	**Ground**
18	I2	**Main regulator input voltage;** block to GND directly at the IC with a ceramic capacitor
19	I1	**Stand-by regulator input voltage;** block to GND directly at the IC with a ceramic capacitor
20	SI	**Sense comparator input**

Table 2 PG-DSO-14

Pin No.	Symbol	Function
1	D	**Reset delay;** connect a capacitor C_D to GND for delay time adjustment
2	DIS	**Disable input main regulator;** Q2 disabled with high signal
3, 4, 5	GND	**Ground**
6	RQ	**Reset output;** the open collector output is connected to Q1 via an integrated 30 kΩ resistor
7	SQ	**Sense output;** the open collector output is connected to Q1 via an integrated 30 kΩ resistor
8	Q1	**Stand-by regulator output voltage;** block to GND with a capacitor, $C_{Q1} \geq 6$ µF, ESR < 10 Ω at 10 kHz
9	Q2	**Main regulator output voltage;** 5 V output tracking to Q1, block to GND with a capacitor $C_{Q2} \geq 10$ µF, ESR < 10 Ω at 10 kHz
10, 11, 12	GND	**Ground**
13	I	**Main and stand-by regulator input voltage;** block to GND directly at the IC with a ceramic capacitor
14	SI	**Sense comparator input**

RADJ: Adjustable reset switching threshold is not available in the PG-DSO-14 package. Reset is always triggered at the internal threshold.

ADJ2: Main regulator adjust input is internally connected to V_{Q2}.

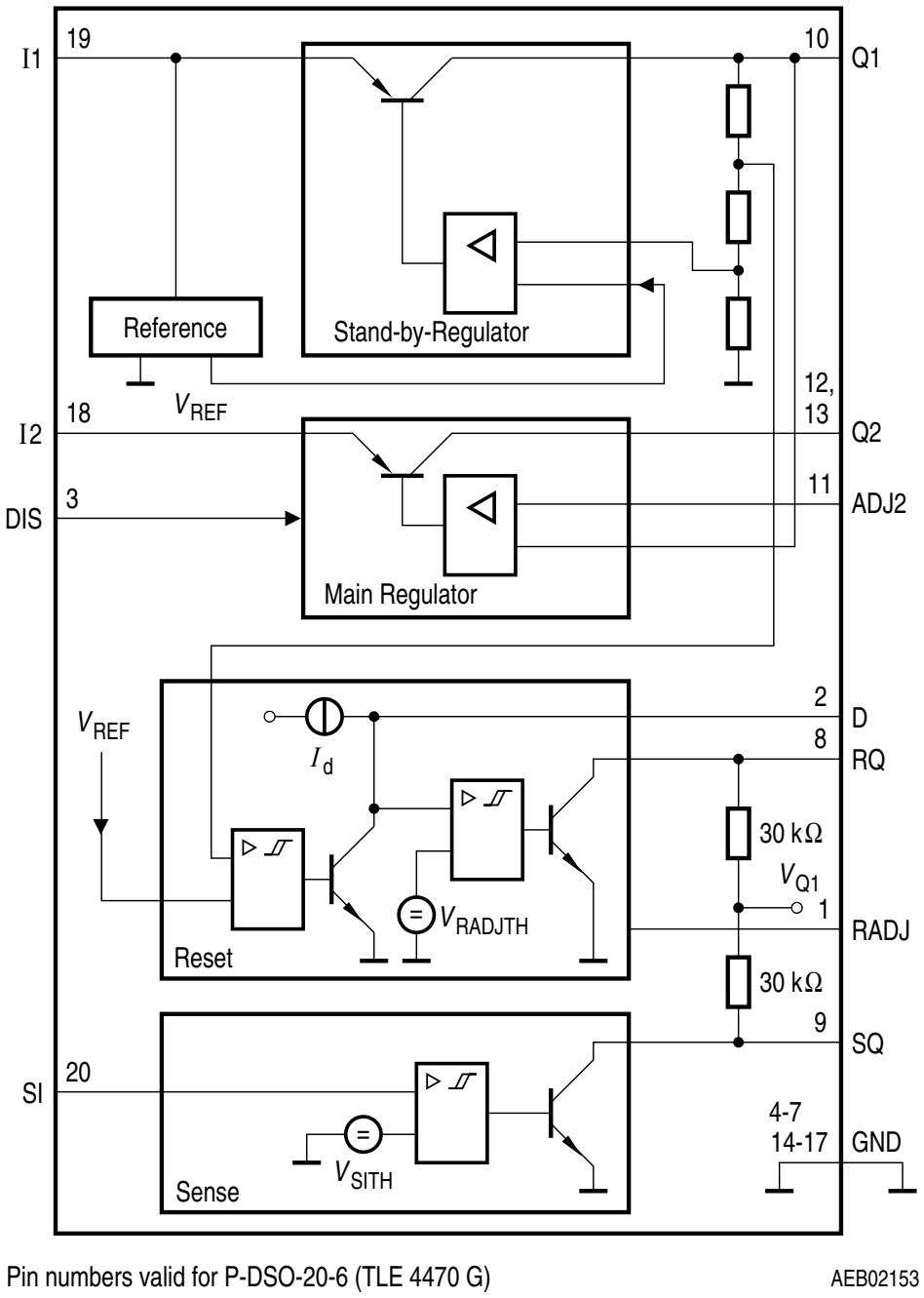


Figure 2 Block Diagram

Table 3 Absolute Maximum Ratings

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Stand-by Regulator Input I1					
Voltage	V_{I1}	-42	45	V	–
Current	I_{I1}	–	–	mA	Internally limited
Main Regulator Input I2					
Voltage	V_{I2}	-42	45	V	–
Current	I_{I2}	–	–	mA	Internally limited
Stand-by Output Q1					
Voltage	V_{Q1}	-1	7	V	–
Current	I_{Q1}	–	–	mA	Internally limited
Main Output Q2					
Voltage	V_{Q2}	-1	36	V	–
Current	I_{Q2}	–	–	mA	Internally limited
Main Regulator Adjust Input ADJ2					
Voltage	V_{ADJ2}	-0.3	18	V	–
Current	I_{ADJ2}	–	–	mA	Internally limited
Sense Output SQ					
Voltage	V_{SQ}	-0.3	25	V	–
Current	I_{SQ}	-5	5	mA	–
Reset Output RQ					
Voltage	V_{RQ}	-0.3	25	V	–
Current	I_{RQ}	-5	5	mA	–
Disable Input DIS					
Voltage	V_{DIS}	-42	45	V	–
Current	I_{DIS}	-2	2	mA	–
Sense Input SI					
Voltage	V_{SI}	-25	18	V	–
Current	I_{SI}	-2	2	mA	–

Table 3 Absolute Maximum Ratings (cont'd)

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Reset Delay D					
Voltage	V_D	-0.3	7	V	–
Current	I_D	-2	2	mA	–
Reset Switching Threshold Adjust RADJ					
Voltage	V_{RADJ}	-0.3	7	V	–
Current	I_{RADJ}	–	–	mA	Internally limited
Temperatures					
Junction temperature	T_j	-50	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Note: ESD-Protection according to MIL Std. 883: ±2 kV.
Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Stand-by regulator input voltage	V_{I1}	5.6	45	V	–
Main regulator input voltage	V_{I2}	$V_{Q2,nom}$ + 0.6 V	45	V	–
Stand-by regulator output current	I_{Q1}	0	180	mA	–
Main regulator output current	I_{Q2}	0	350	mA	–
Disable input voltage	V_{DIS}	-0.3	45	V	–
Sense input voltage	V_{SI}	-0.3	17	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances PG-DSO-14					
Junction pin	$R_{thj\text{-}pin}$	–	32	K/W	Measured to pin 4
Junction ambient	$R_{thj\text{-}a}$	–	112	K/W	1)
Thermal Resistances PG-DSO-20					
Junction pin	$R_{thj\text{-}pin}$	–	23	K/W	Measured to pin 4
Junction ambient	$R_{thj\text{-}a}$	–	100	K/W	1)

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35 µ Cu; 5 µ Sn; Footprint only; zero airflow.

Note: In the operating range the functions given in the circuit description are fulfilled.

Table 5 Electrical Characteristics

$V_{I1} = V_{I2}$ = 14 V; $V_{DIS} < V_{DISL}$; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Stand-by Regulator						
Output 1						
Output voltage	V_{Q1}	4.90	5.0	5.10	V	1 mA < I_{Q1} < 100 mA
Output current limitation	I_{Q1}	180	280	–	mA	[1]
Output drop voltage; $V_{DRQ1} = V_{I1} - V_{Q1}$	V_{DRQ1}	–	300	500	mV	I_{Q1} = 100 mA[1]
Current Consumption						
Quiescent current; stand-by $I_q = I_{I1} - I_{Q1}$	I_q	–	180	250	µA	I_{Q1} = 300 µA; T_j = 25 °C $V_{DIS} > V_{DISH}$ (Q2 = OFF)
		–	180	300	µA	I_{Q1} = 300 µA; $V_{DIS} > V_{DISH}$ (Q2 = OFF)
Quiescent current $I_q = I_{I1} - I_{Q1}$	I_q	–	4	6	mA	I_{Q1} = 100 mA; $V_{DIS} > V_{DISH}$ (Q2 = OFF)
Regulator Performance						
Load regulation	$\Delta V_{Q1,Lo}$	–	15	50	mV	1 mA < I_{Q1} < 150 mA
Load regulation	$\Delta V_{Q1,Lo}$	–	5	25	mV	1 mA < I_{Q1} < 100 mA
Line regulation	$\Delta V_{Q1,Li}$	–	5	20	mV	I_{Q1} = 1 mA; 6 V < V_{I1} < 28 V
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	20 Hz < f_r < 20 kHz; V_r = 5 Vpp
Temperature output voltage drift	$\Delta V_{Q1}/\Delta T$	–	0.3	–	mV/K	–
dV_{I1}/dt stability	V_{Q1}	4.5	–	5.5	V	no reset occurs[2]
Value of output capacitance	C_{Q1}	6	–	–	µF	–
ESR of output capacitance	ESR_{CQ1}	–	–	10	Ω	at 10 kHz

Table 5 Electrical Characteristics (cont'd)

$V_{I1} = V_{I2} = 14$ V; $V_{DIS} < V_{DISL}$; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Main-Regulator						
Output 2						
Output voltage tracking accuracy	$\Delta V_{Q2} = V_{Q2} - V_{Q1}$	-25	5	25	mV	5 mA < I_{Q2} < 100 mA; 6 V < V_{I2} < 40 V[3]
Output voltage tracking accuracy	$\Delta V_{Q2} = V_{Q2} - V_{Q1}$	-25	5	25	mV	5 mA < I_{Q2} < 250 mA; 7 V < V_{I2} < 28 V[3]
Adjust input current	I_{ADJ2}	-1	–	1	µA	–
Output current limitation	I_{Q2}	350	500	–	mA	[1]
Output drop voltage $V_{DRQ2} = V_{I2} - V_{Q2}$	V_{DRQ2}	–	300	600	mV	I_{Q2} = 200 mA[1]
Current Consumption						
Quiescent current; $I_q = I_I - I_Q$	I_q	–	7	15	mA	I_{Q2} = 200 mA; I_{Q1} = 300 µA
Quiescent current; $I_q = I_I - I_Q$	I_q	–	250	500	µA	$I_{Q2} = I_{Q1}$ = 300 µA; T_j = 25 °C
Regulator Performance						
Load regulation	$\Delta V_{Q2,Lo}$	–	5	25	mV	5 mA < I_{Q2} < 200 mA;
Line regulation	$\Delta V_{Q2,Li}$	–	5	20	mV	I_{Q2} = 5 mA; 6 V < V_{I2} < 28 V
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	20 Hz < f_r < 20 kHz; V_r = 5 Vpp
Temperature output voltage drift	$\Delta V_{Q2}/\Delta T$	–	0.5	–	mV/K	–
dV_{I2}/dt stability	V_{Q2}	4.5	–	5.5	V	no reset occurs[3]
Value of output capacitance	C_{Q2}	10	–	–	µF	–
ESR of output capacitance	ESR_{CQ2}	–	–	10	Ω	at 10 kHz

Table 5 Electrical Characteristics (cont'd)

$V_{I1} = V_{I2} = 14$ V; $V_{DIS} < V_{DISL}$; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Disable Input DIS						
H-input voltage threshold	V_{DISH}	2.3	–	–	V	–
L-input voltage threshold	V_{DISL}	–	–	1.4	V	Output 2 active
H-input current	I_{DISH}	-2	-1	1	µA	2.3 V < V_{DIS} < 7 V
L-input current	I_{DISL}	-6	-2	-0.5	µA	0 V < V_{DIS} < 1.4 V
Reset Timing D and Output RQ						
Reset switching threshold	$V_{Q, rt}$	4.5	4.65	4.8	V	RADJ connected to GND
Reset adjust threshold	V_{RADJTH}	1.25	1.35	1.45	V	V_{Q1} > 3.5 V
Reset output low voltage	V_{RQL}	–	0.15	0.3	V	R_{RQ} = 10 kΩ externally connected to Q1; $V_{Q1} \geq 1$ V
Reset high voltage	V_{RQH}	4.5	–	–	V	–
Reset pull-up resistor	R_{RQ}	20	30	45	kΩ	Internally connected to Q1
Reset charging current	$I_{D,c}$	3	5	9	µA	V_D = 1 V
Upper timing threshold	V_{DU}	1.5	1.8	2.2	V	–
Lower timing threshold	V_{DL}	0.3	0.4	0.55	V	–
Reset delay time	t_{rd}	12	15	20	ms	C_D = 47 nF
Reset reaction time	t_{rr}	–	0.5	2.0	µs	C_D = 47 nF

Table 5 Electrical Characteristics (cont'd)

$V_{I1} = V_{I2} = 14$ V; $V_{DIS} < V_{DISL}$; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Sense Input SI and Output SQ						
Sense threshold voltage	V_{SITH}	1.28	1.35	1.45	V	V_{SI} decreasing
Sense threshold hysteresis	V_{SIHY}	25	60	100	mV	–
Sense output low voltage	V_{SQL}	–	0.15	0.4	V	R_{SQ} = 10 kΩ externally connected to Q1; V_{SI} < 1.1 V; V_{I1} > 4.5 V
Sense output high voltage	V_{SQH}	4.5	–	–	V	–
Sense pull-up resistor	R_{SQ}	20	30	45	kΩ	Internally connected to Q1

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value.

2) Square wave at V_I: 8 V to 18 V; f = 10 kHz; $t_r = t_f \leq 100$ ns.

3) V_{Q2} connected to ADJ2.

Application Information

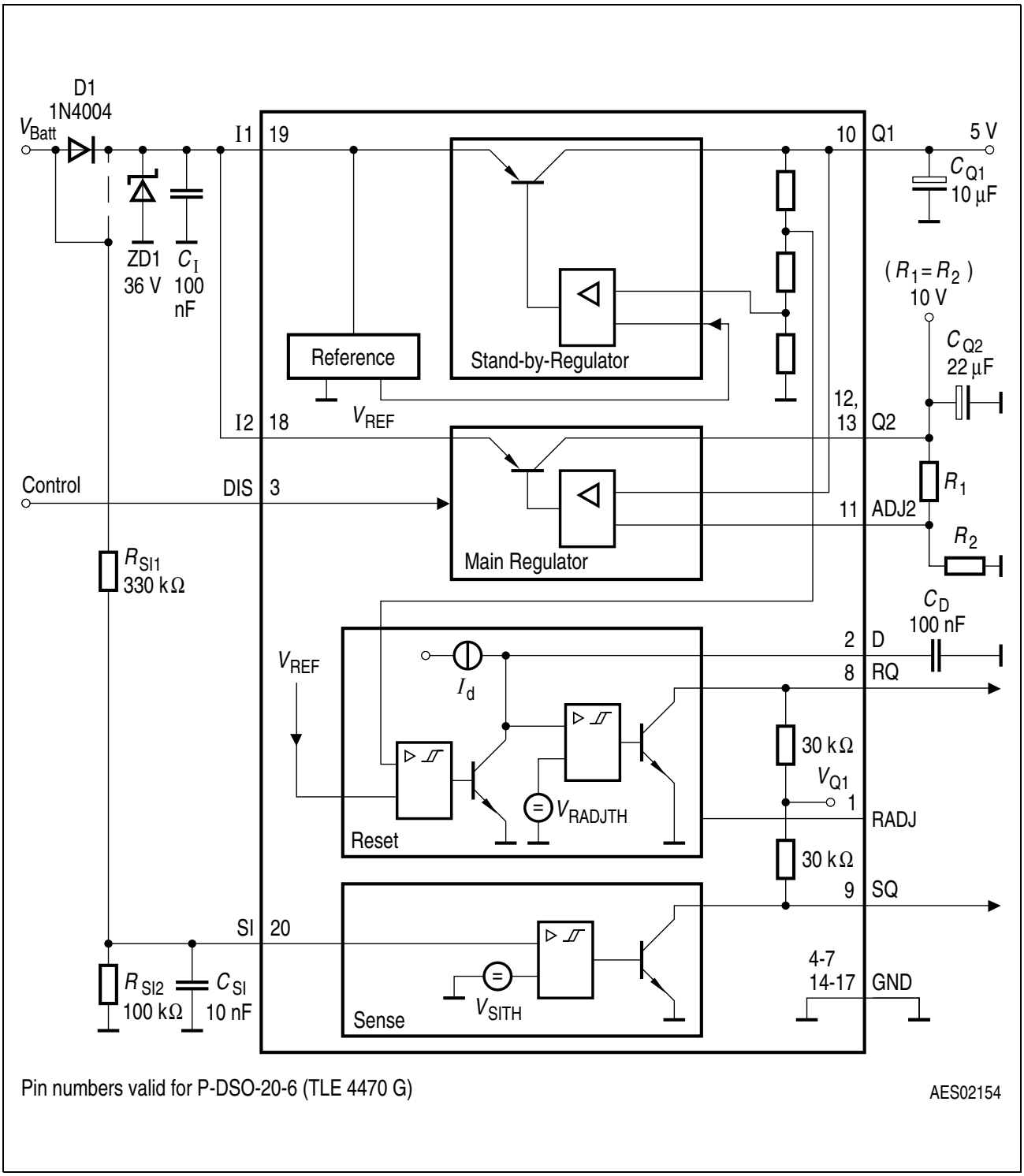


Figure 3 Application Circuit

Input, Output

The input capacitor C_I is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_I, the LC circuit of input inductivity and input capacitance can be damped. To stabilize the regulation circuits of the stand-by and main regulator, output capacitors C_{Q1} and C_{Q2} are necessary. Stability is guaranteed at values $C_{Q1} \geq 6$ µF and $C_{Q2} \geq 10$ µF, both with an ESR ≤ 10 Ω within the operating temperature range.

For the TLE 4470 G (PG-DSO-20) the output voltage V_{Q2} of the main regulator can be adjusted to 5 V ≤ $V_{Q2,nom}$ ≤ 20 V by connecting an external voltage divider to the voltage adjust pin ADJ2. For V_{Q2} = 5 V the voltage adjust pin has to be connected directly to the main output.

For calculating V_{Q2} or R_1 and R_2 respectively the following equations can be used:

$$V_{Q2} = V_{Q1} \times (1 + R_1 / R_2) \quad (1)$$

or

$$R_1 = R_2 \times (V_{Q2} / V_{Q1} - 1) \quad (2)$$

Disable

The main regulator of the TLE 4470 can be switched OFF by a voltage above 2.3 V at pin DIS. Reducing this voltage below 1.4 V will switch ON the main regulator again.

Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (\Delta t \times I_{D,c}) / \Delta V \quad (3)$$

Definitions:

- C_D = delay capacitor
- Δt = reset delay time
- $I_{D,c}$ = charge current, typical 5 µA
- $\Delta V = V_{DU}$, typical 1.8 V
- V_{DU} = upper delay switching threshold at C_D for reset delay time

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 2 µs for delay capacitor of 100 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20 \text{ s/F} \times C_D \quad (4)$$

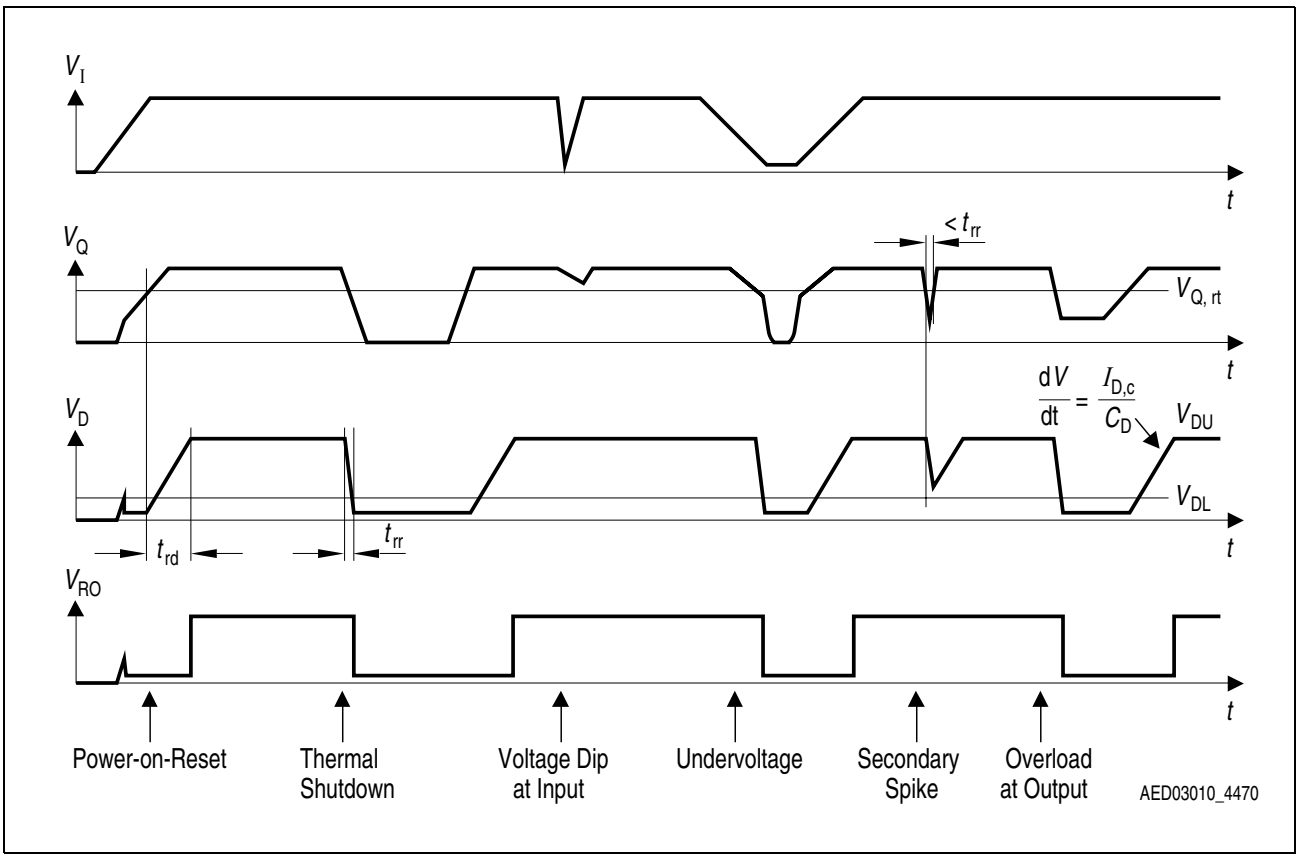


Figure 4 Reset Timing

Reset Switching Threshold

The internally set reset threshold is 4.65 V. When using the TLE 4470 G (PG-DSO-20) this threshold can be adjusted to 3.5 V < $V_{Q, rt}$ < 4.6 V by connecting an external voltage divider to pin RADJ. If this pin is not needed, it can be left open or even better connected to GND.

$$R_1 = R_2 \times (V_{Q, rt} - V_{ref}) / V_{ref} \text{ or } V_{Q, rt} = V_{ref} (1 + R_1 / R_2) \quad (5)$$

Definitions:

- $V_{Q, rt}$ = Reset threshold
- V_{ref} = comparator reference voltage, typical 1.35 V
  (Reset adjust input current ≈ 50 nA)

The reset output pin is internally connected to the stand-by output Q1 via a 30 kΩ pull-up resistor. The reset LOW signal at pin RQ is guaranteed down to an output voltage V_{Q1} of 1 V typical.

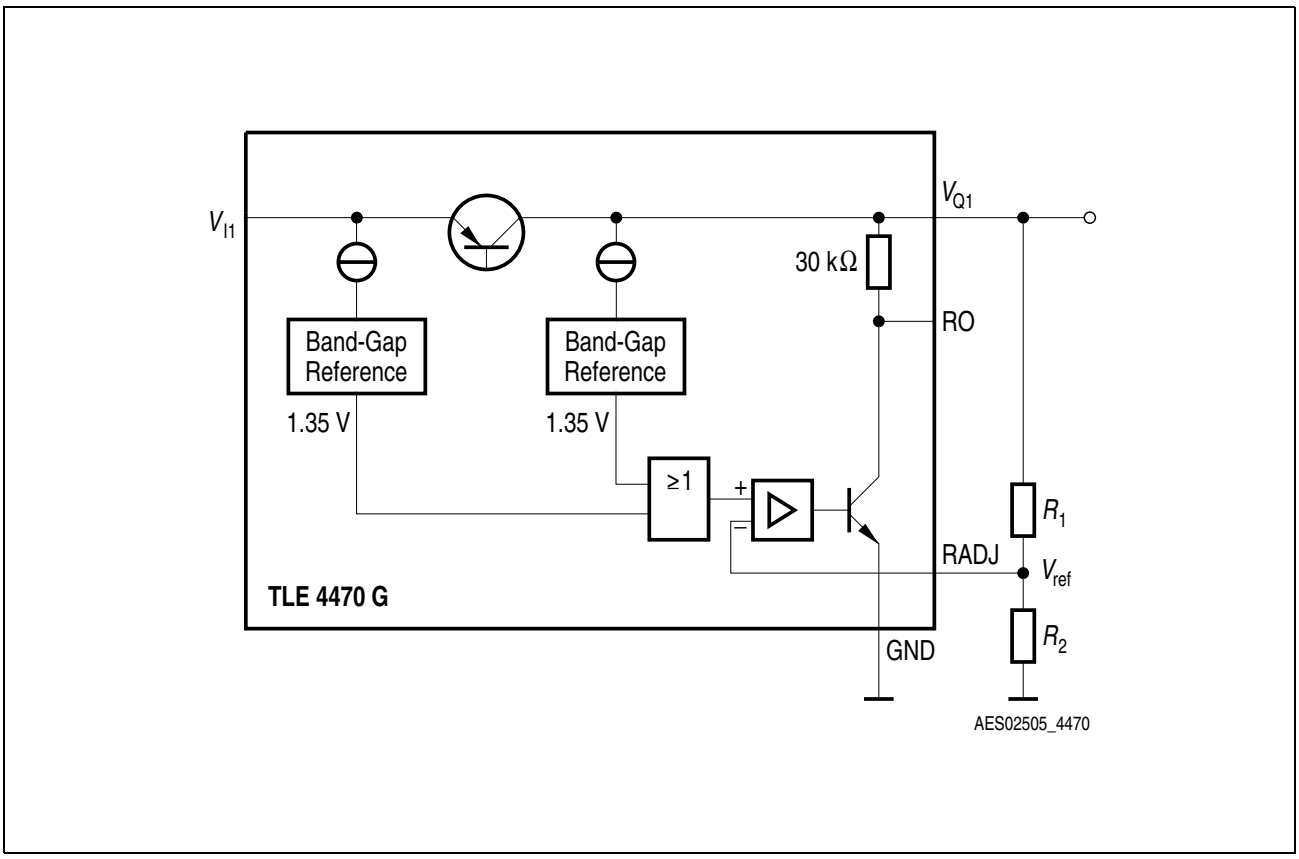


Figure 5

Early Warning

The early warning function compares a voltage defined by the user to an internal reference voltage. Therefore the voltage to be supervised has to be scaled down by an external voltage divider in order to compare it to internal sense threshold (reference voltage) which is typically 1.35 V. The sense out pin is set to low when the user defined voltage falls below this threshold.

A typical example where this circuit can be used is to supervise the input voltage V_I to give the microprocessor a prewarning of a low battery condition.

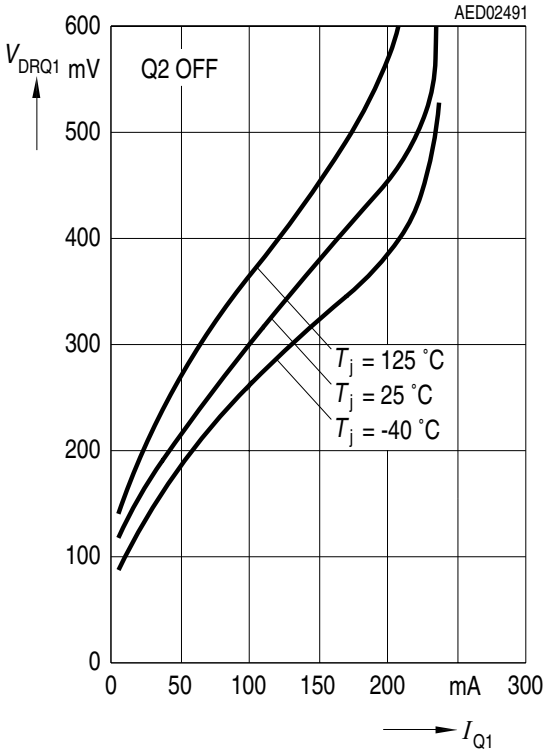
Calculation of the voltage divider can be easily done since the sense input current can be neglected. The equations needed for calculation are identical to the previously given ones.

To minimize transient influences the use of a capacitor in parallel to R_2 is recommended.

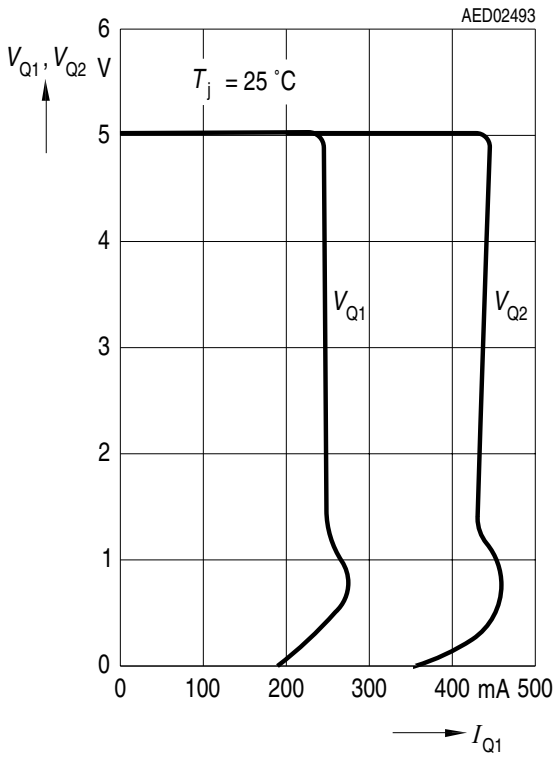
Like the reset output pin, the sense out pin SQ is internally connected to the stand-by output Q1 via a 30 kΩ pull-up resistor. The sense out LOW signal at pin SQ is generated down to an input voltage V_{I1} of 3 V typical.

Typical Performance Characteristics

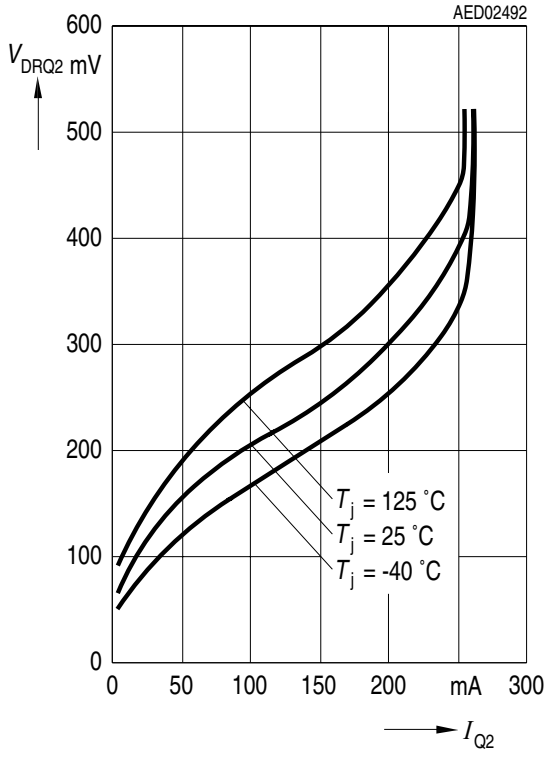
Drop Voltage V_{DRQ1} versus Output Current I_{Q1}



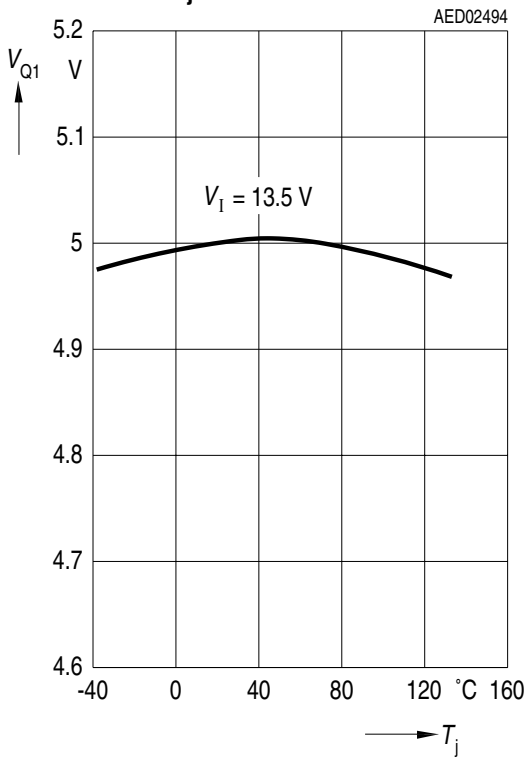
Output Voltage V_{Q1}, V_{Q2} versus Output Current I_{Q1}



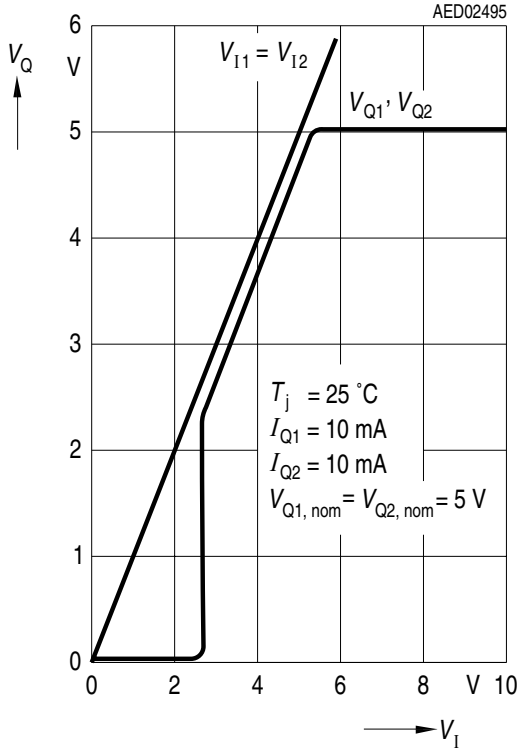
Drop Voltage V_{DRQ2} versus Output Current I_{Q2}



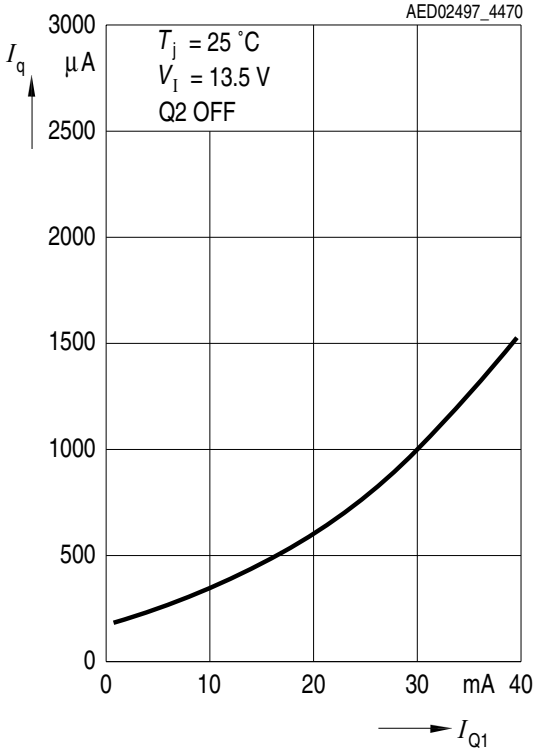
Output Voltage V_{Q1} versus Temperature T_j



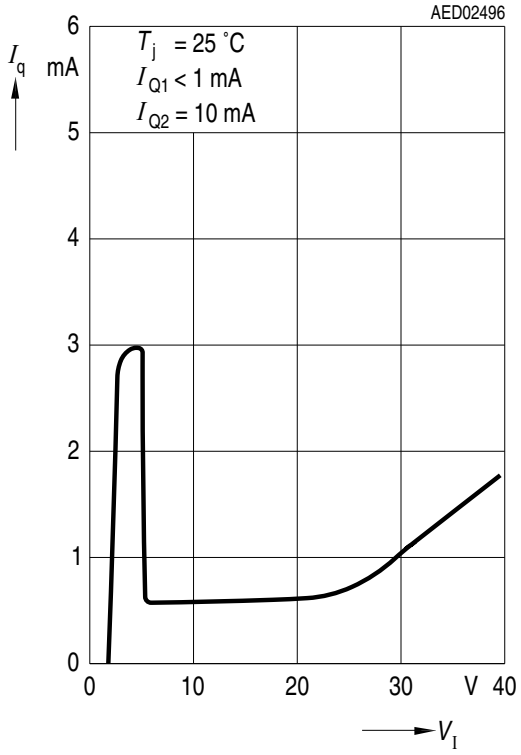
Output Voltage V_{Q1}, V_{Q2} versus Input Voltage V_I ($V_{I1} = V_{I2}$)



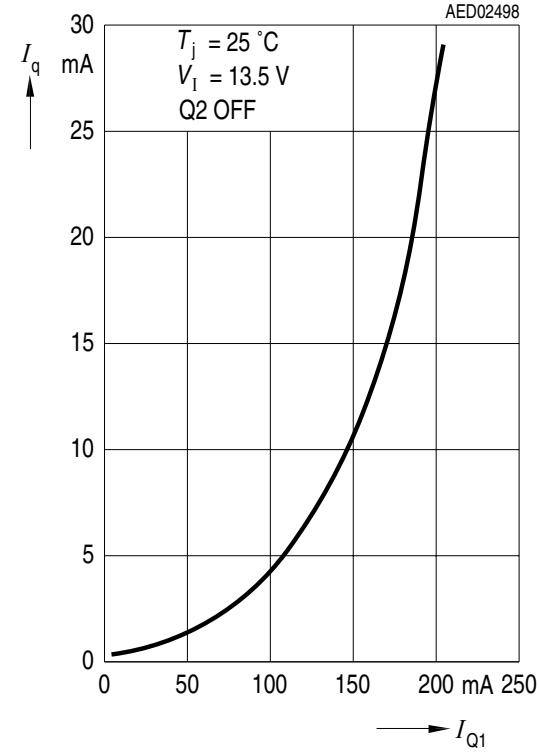
Current Consumption I_q versus Output Current I_{Q1} (low load)



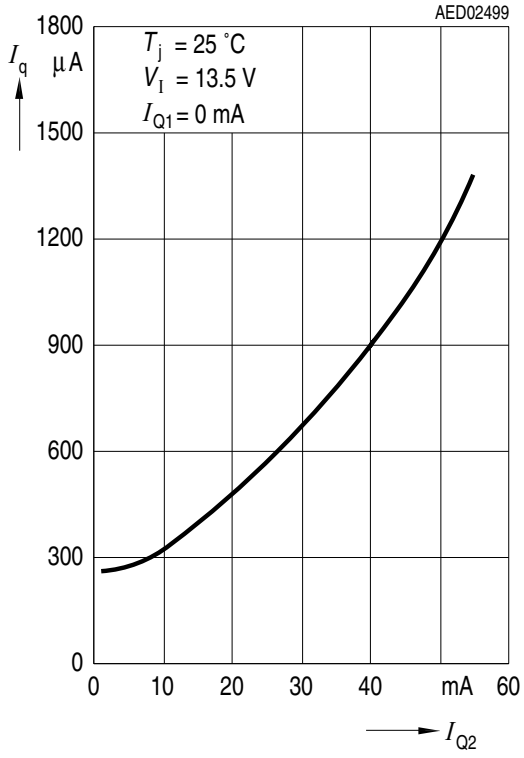
Current Consumption I_q versus Input Voltage V_I



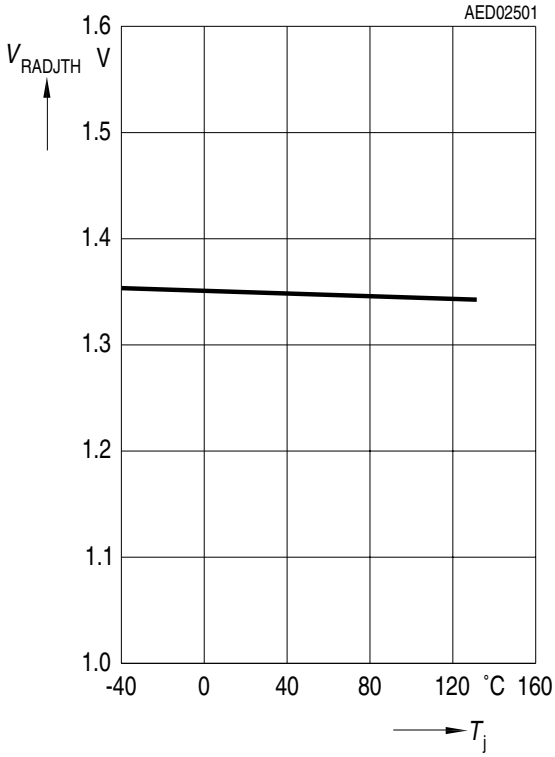
Current Consumption I_q versus Output Current I_{Q1} (high load)



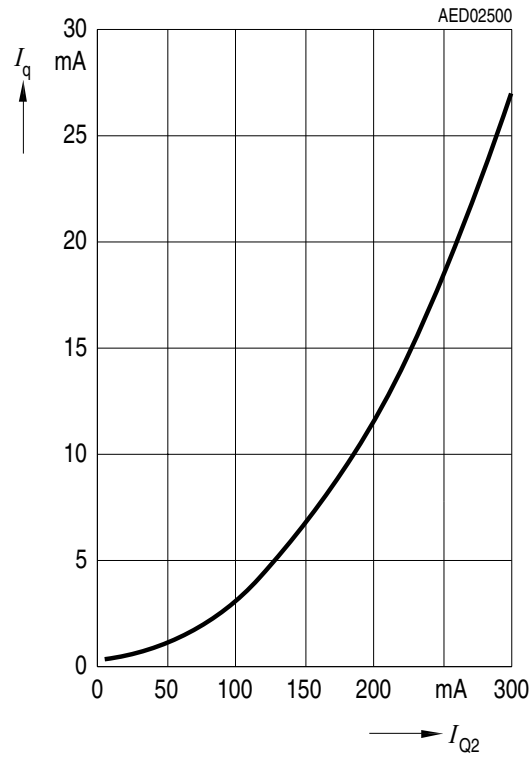
Current Consumption I_q versus Output Current I_{Q2} (low load)



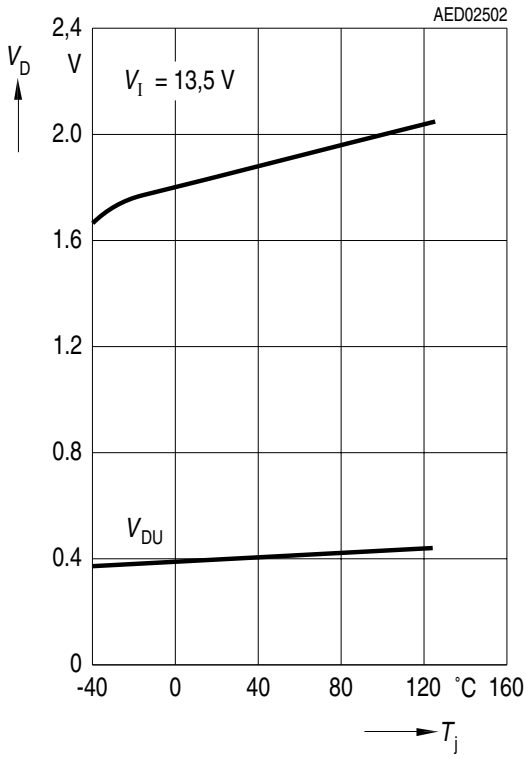
Reset Adjust Threshold V_{RADJTH} versus Temperature T_j



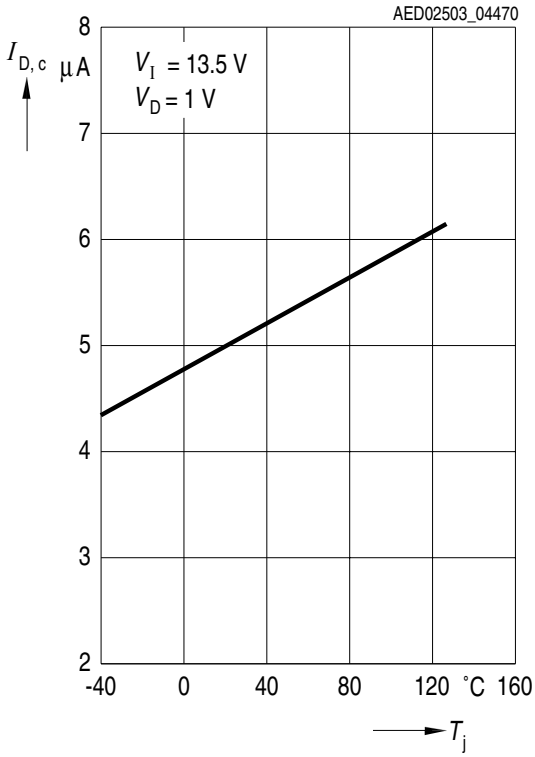
Current Consumption I_q versus Output Current I_{Q2} (high load)



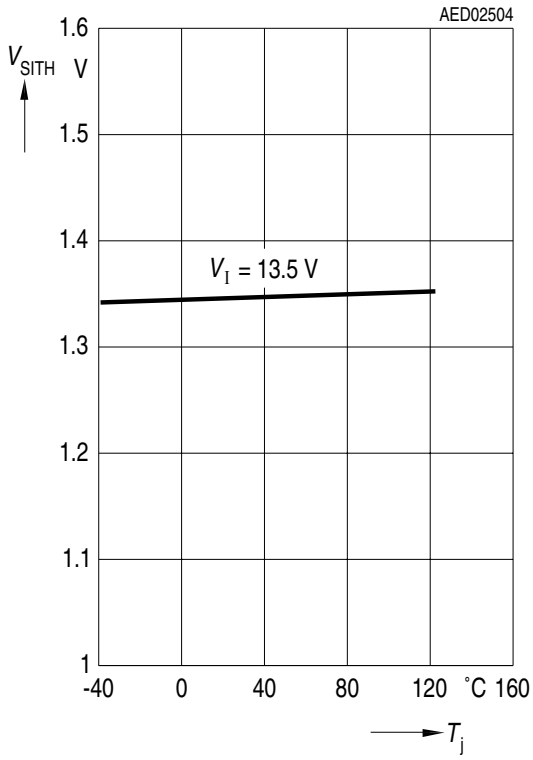
Switching Voltage V_{DU}, V_{DL} versus Temperature T_j



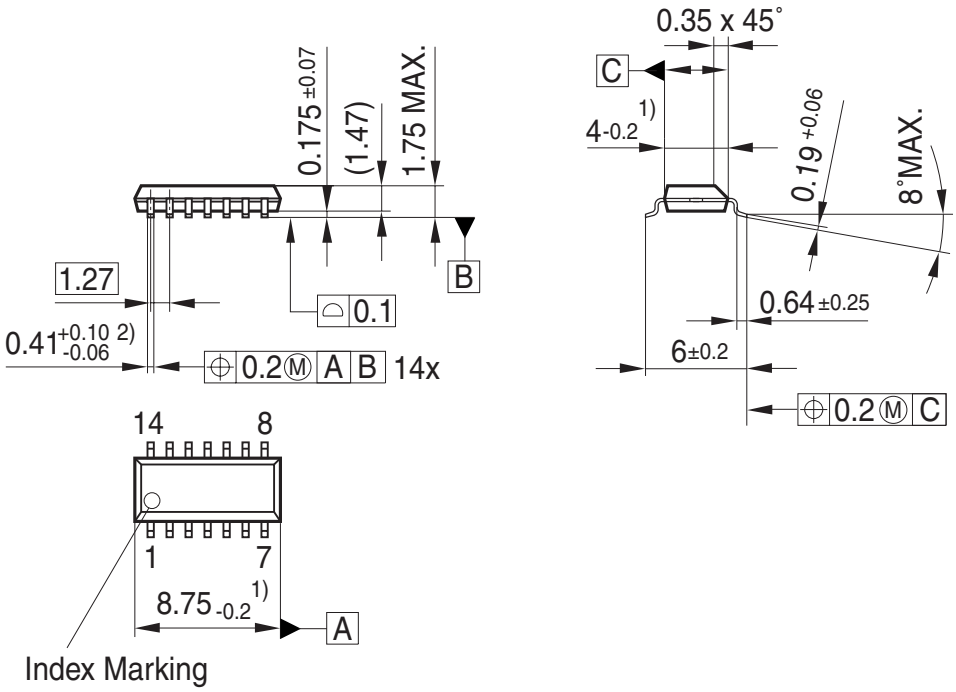
Charge Current $I_{D,c}$ versus Temperature T_j



Sense Threshold V_{SITH} versus Temperature T_j



Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Lead width can be 0.61 max. in dambar area

GPS01230

Figure 6 **PG-DSO-14** (Plastic Green Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm

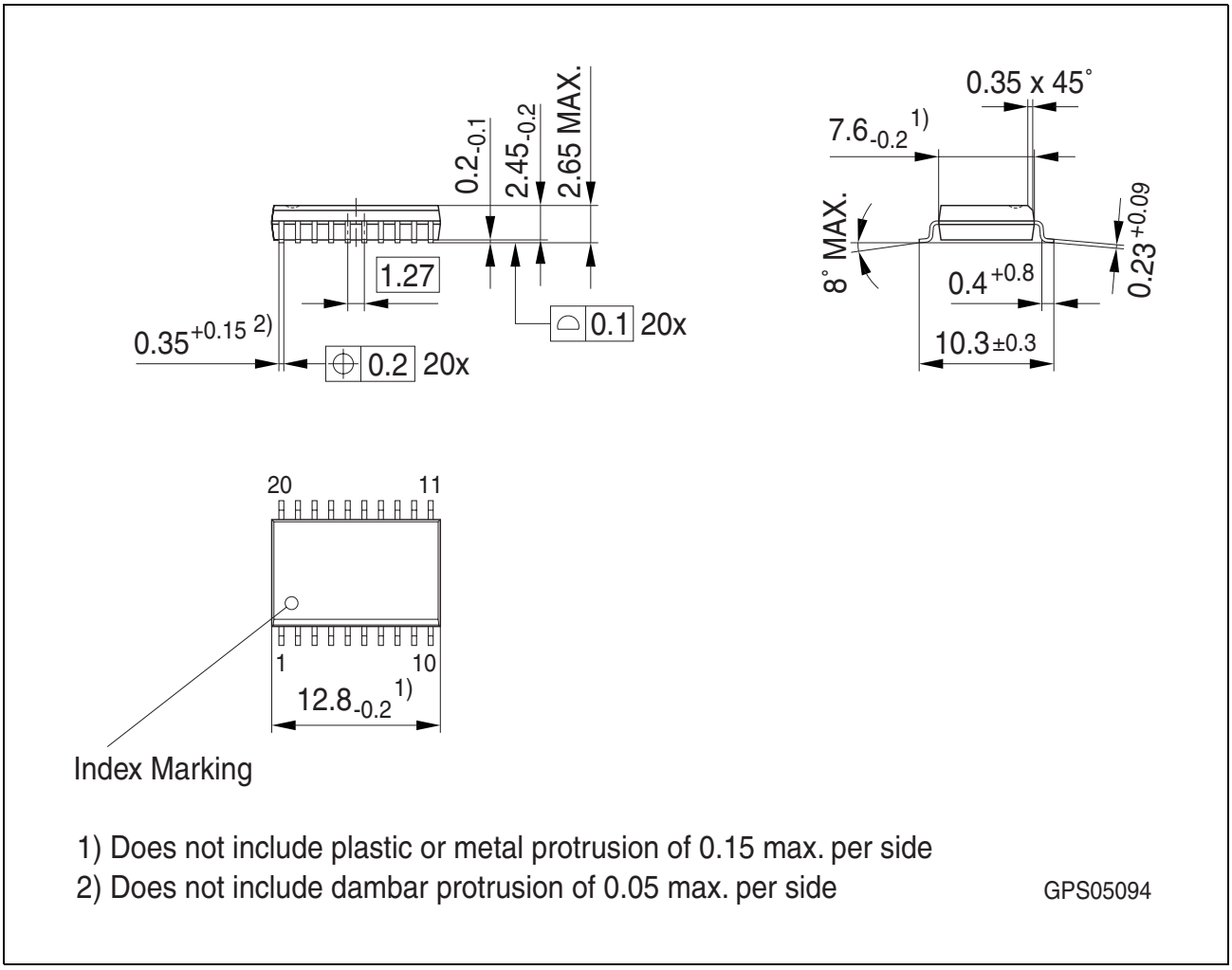

Figure 7 **PG-DSO-20** (Plastic Green Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 1.2	2008-03-20	Initial version of RoHS-compliant derivate of TLE 4470 **Page 1**: AEC certified statement added **Page 1** and **Page 21**f: RoHS compliance statement and Green product feature added **Page 1** and **Page 21**f: Package changed to RoHS compliant version Legal Disclaimer updated

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