

# 45 W power supply using CoolSET™ SiP ICE184LM

REF\_45W1\_ZVS\_184LM

## About this document

### Scope and purpose

This application note describes a reference design for a high-efficiency 45 W power supply using Infineon's latest CoolSET™ System in Package (SiP) ICE184LM. The power supply is designed with a universal input AC line voltage and single output (isolated +12 V/3.75 A).

Highlights of this power supply:

- Overall high efficiency to meet energy efficiency requirements
- Simplified circuitry with high-level integration of power control and protection features
- Auto-restart protection scheme to minimize interruption to enhance end user experience
- Zero voltage switching (ZVS) technology to boost efficiency performance

### Intended audience

This document is intended for power supply design, application engineers, or others who want to design efficient and reliable auxiliary power supplies.

### CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching schemes offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- [SMPS](#)
- [Home appliances](#)
- [Server](#)
- [Telecom](#)

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### Introduction

## 1 Introduction

This document describes a 12 V / 3.75 A power supply using Infineon's latest CoolSET™ SiP ICE184LM. This reference design demonstrates high efficiency and cost-effectiveness, made possible by the high-level integration capabilities of CoolSET™ SiP.

This general-purpose design is engineered to address the diverse needs of different applications. Whether it's a high-performance computing system, a smart home device, or an industrial control system, this design provides a solid foundation for development. By leveraging this single output design, developers can focus on their core competencies, rather than worrying about the underlying technology.

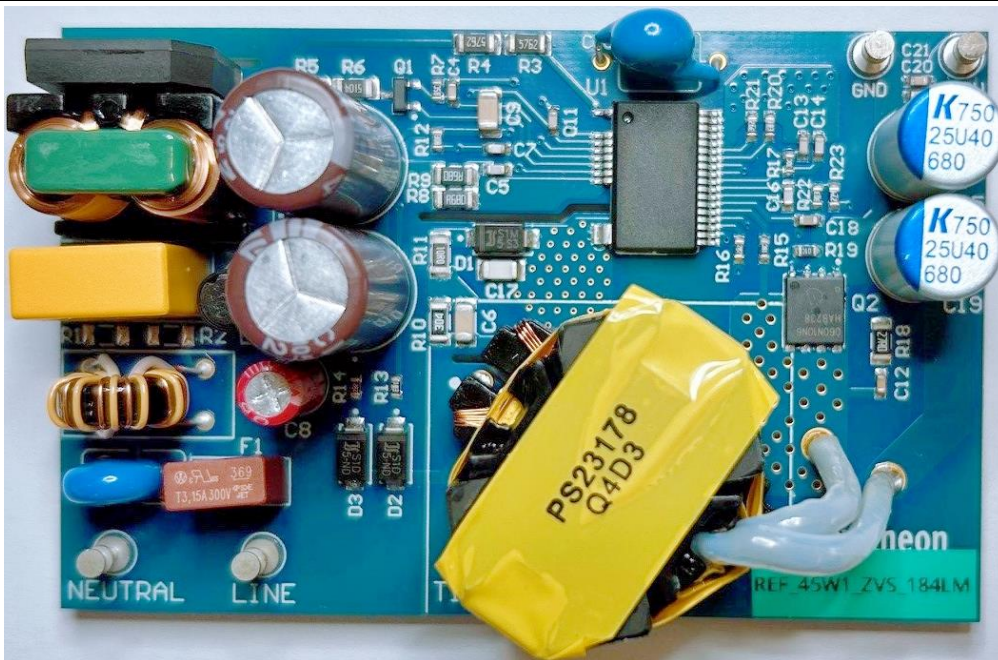
[Table 1](#) lists the general system requirement for a power supply, and the corresponding Infineon solution by ICE184LM.

**Table 1** General system requirement and reference design solution

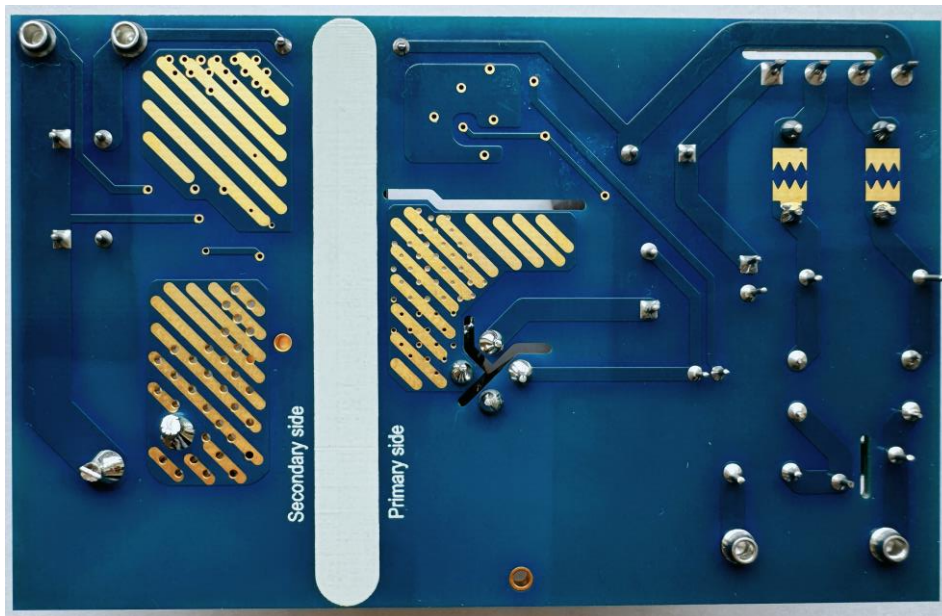
	<b>General system requirement</b>	<b>Reference design solution – ICE184LM</b>
1	High efficiency to meet energy efficiency requirements	Primary zero voltage switching and secondary optimal synchronous rectifier control
2	Simplified circuitry with high-level integration	Primary 800 V MOSFET, primary and secondary controller, and communication integrated in a DSO-27 package
3	Minimize interruption to enhance end user experience	All protections are defined to enter auto-restart mode

## 2 Reference board

This document provides complete design details including power supply specifications, schematics, bill of materials, PCB layout, transformer specification, and performance data.



Top side of the board



Bottom side of the board

Figure 1 Photograph of REF\_45W1\_ZVS\_184LM

## Board specifications

### 3 Board specifications

The following table represents the minimum acceptance performance of the design. The actual performance is listed in the [Measurement data and graphs](#) Section.

**Table 2 Specifications of REF\_45W1\_ZVS\_184LM**

Description	Symbol	Min.	Typ.	Max.	Units	Comments
<b>Input</b>						
Voltage	$V_{IN}$	90	–	264	V AC	Two wires (no P.E.)
Frequency	$f_{LINE}$	47	50/60	64	Hz	–
No-load input power	$P_{stby}$	–	–	20	mW	Measured at 230 V AC
Line Overvoltage	$V_{IN\_OVP}$	–	277	–	V AC	–
<b>Output</b>						
Output voltage	$V_{OUT}$	–	12	–	V	±5 percent
Output current	$I_{OUT}$	3.75	–	–	A	–
Output voltage ripple	$V_{RIPPLE}$	–	–	240	mV	–
Overcurrent protection	$I_{OCP}$	–	–	5.6	A	–
<b>Efficiency</b>						
Maximum load efficiency	$\eta$	–	92.5	–	%	Measured at 230 V AC
<b>Environmental</b>						
Conducted EMI	–	6			dB	Margin, CISPR 22 class B
<b>ESD</b>						
Contact discharge	–	±8			kV	–
Air discharge	–	±15			kV	–
<b>Surge immunity</b>						
Differential mode	–	±2			kV	–
Common mode	–	±4			kV	–
PCB size	–	80 x 50			mm <sup>2</sup>	L x W
Ambient temperature	$T_a$	–	–	50	°C	Convection cool

Circuit diagram

4 Circuit diagram

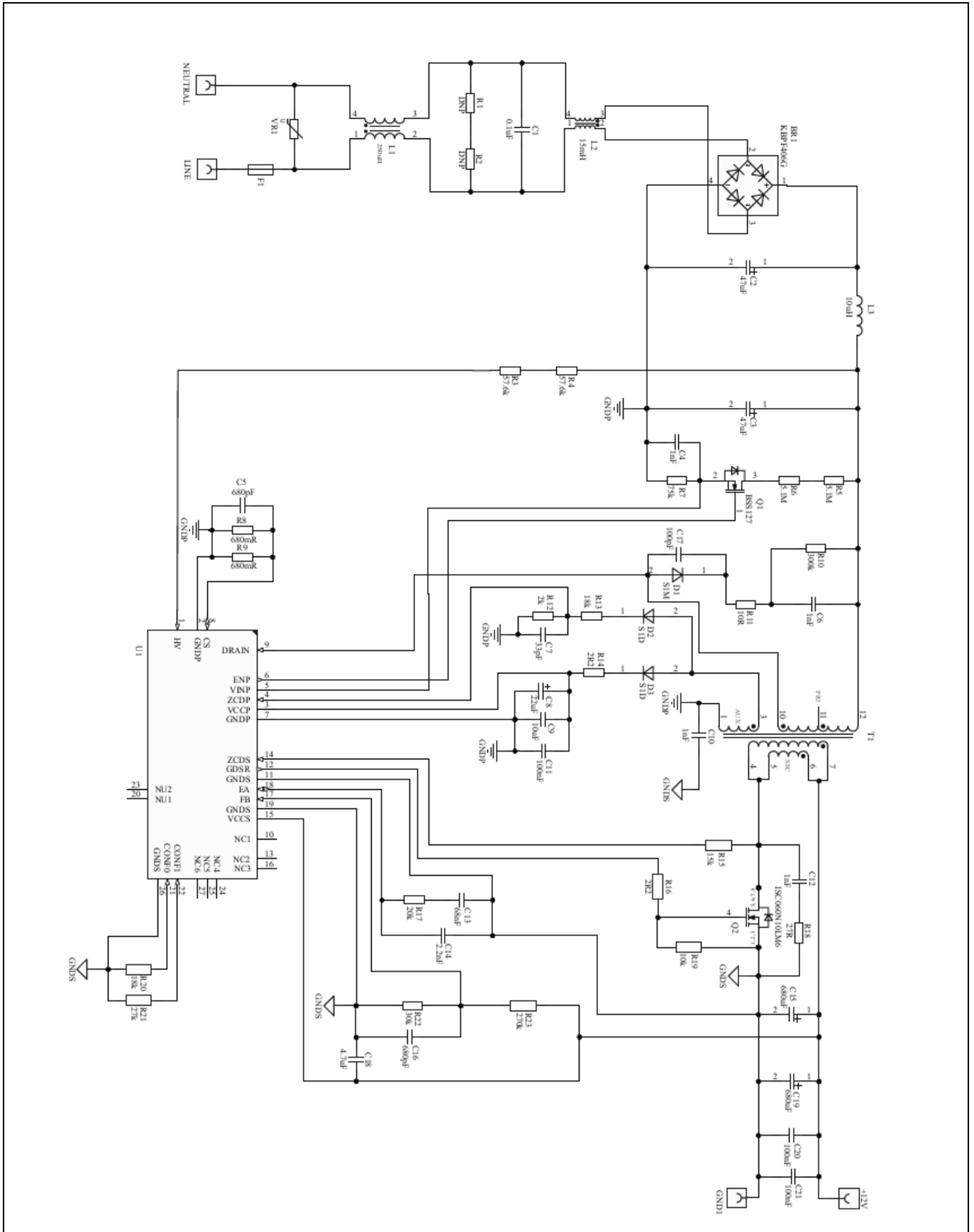


Figure 2 Schematic of REF\_45W1\_ZVS\_184LM

## 5 Circuit description

This section briefly describes the reference design circuit by different functional blocks. For details of the design procedure and component selection for the flyback circuitry, check the IC datasheet [2] and design guide [1].

### 5.1 EMI filtering and line rectification

The input of the power supply is taken from the AC power grid, which is in the 90 V AC ~ 264 V AC range. The F1 fuse is right at the entrance to protect the system in case of excess current entering the system circuit due to a fault. Following is the varistor VR1, which is connected across L and N to absorb the line surge transient. Common mode chokes L1 and L2 and the X-capacitor C1 form a basic filter to reduce the DM- and CM-conducted EMI noise. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the  $\pi$  filter (capacitor C2, C3, and L3).

### 5.2 CoolSET™ SiP power stage

The flyback converter power stage consists of a power transformer, primary power MOSFET, secondary synchronous rectifier (SR) MOSFET, secondary output capacitors, and filtering component if necessary. Primary and secondary side power management are separated for isolated power supply domains ( $V_{CCP}$ , GNDP and VCCS, GNDS). ICE184LM provides reinforced and safe isolated communication between primary and secondary sides.

#### 5.2.1 CoolSET™ SiP primary side

CoolSET™ SiP ICE184LM integrates a 950 V startup cell and 800 V power MOSFET together at the primary side. The IC is self-starting through the startup resistor  $R_{HV}$  (R3, R4) in series with the HV pin – to charge the  $V_{CCP}$  pin capacitor (C8) when AC is applied. These startup resistors (R3, R4), together with ZCDP pin external configuration resistor  $R_{ZCDPL}$  (R12), determine the brown-in and brown-out protections, as shown in Table 3.

**Table 3 Primary side configuration options**

Option	$R_{ZCDPL}(\min); R_{ZCDPL}(\max)$	Brown in current threshold $I_{HV\_BI}$	Brown out current threshold $I_{HV\_BO}$	Internal shunt resistor $R_{HVshunt}$
1	[1.00 k $\Omega$ ; 1.05 k $\Omega$ ]	2.00 mA	1.40 mA	0.5 k $\Omega$
2	[1.87 k $\Omega$ ; 2.70 k $\Omega$ ]	1.00 mA	0.70 mA	1.0 k $\Omega$
3	[4.30 k $\Omega$ ; 5.00 k $\Omega$ ]	0.67 mA	0.47 mA	1.5 k $\Omega$
4	[9.20 k $\Omega$ ; 9.50 k $\Omega$ ]	0.50 mA	0.35 mA	2.0 k $\Omega$

Select Option 2 with  $R_{ZCDPL}$  (R12) = 2 k $\Omega$ , then the brown-in voltage can be estimated as:

$$V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BI} = (115 \text{ k}\Omega + 1 \text{ k}\Omega) \times 1 \text{ mA} = 116 \text{ V}$$

#### Equation 1

and the brown-out voltage can be estimated as:

$$V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BO} = (115 \text{ k}\Omega + 1 \text{ k}\Omega) \times 0.7 \text{ mA} = 81 \text{ V}$$

#### Equation 2

Moreover, R13 and R14 resistors offer zero crossing detection during the soft-start period and primary-sensed output overvoltage protection (OVP).

### Circuit description

$$V_{OUT\_OVP} = \left( \frac{(R_{ZCDPH} + R_{ZCDPL}) \times V_{ZCDP\_OVP\_min}}{R_{ZCDPL}} + V_{Daux} \right) \times \frac{N_{SEC}}{N_{AUX}} - V_{Dsec}$$

$$= \left( \frac{(2 \text{ k}\Omega + 18 \text{ k}\Omega) \times 2.05 \text{ V}}{2 \text{ k}\Omega} + 0.3 \text{ V} \right) \times \frac{4}{5} - 0.1 \text{ V} \approx 16 \text{ V}$$

#### Equation 3

Where,

$N_{MAIN}$  : Number of primary turns

$N_{SEC}$  : Number of secondary turns

$N_{AUX}$  : Number of auxiliary turns

$V_{Daux}$  : Diode forward voltage drop at auxiliary winding

$V_{Dsec}$  : Voltage drop across SR MOSFET  $V_{ZCDP\_OVP\_min}$  : Minimum voltage of the output overvoltage threshold

$V_{OUT\_OVP}$  : User-defined output overvoltage level

C7 is chosen to adjust the delay time, which starts when the drain-source voltage falls below the bus voltage until the ZCDP voltage falls to  $V_{ZCDPthr}$  (typical 100 mV). Therefore, the power switch can be turned on at the valley point of the drain-source voltage. This is normally done through experimentation.

A 33 uF capacitor for C8 is applied to ensure stable system operation and enough break time for auto-restart protection. The  $V_{CCP}$  resistor R14 is treated as noise attenuation in case of a severe voltage spike coupling from the transformer during the surge test.

The AC line overvoltage protection is detected by sensing the bus capacitor voltage through the  $V_{INP}$  pin via the divider resistors R5, R6, and R7. Once the  $V_{INP}$  pin voltage is higher than the line overvoltage threshold  $V_{VINP\_LOVP}$ , the controller enters the line overvoltage protection and releases the protection mode after the  $V_{INP}$  pin voltage is lower than  $V_{VINP\_LOVP}$ .

Estimated  $L_{OVP}$  voltage is calculated:

$$V_{BUS\_OVP} = V_{VINP\_LOVP} \times \frac{R8+R6+R7}{R8} = 2.80 \text{ V} \times \frac{75 \text{ k}\Omega + 5100 \text{ k}\Omega + 5100 \text{ k}\Omega}{75 \text{ k}\Omega} = 383 \text{ V}$$

#### Equation 4

A low-cost RCD clamp consisting of the D1 diode, R10 and R11 resistors, and the C6 capacitor is implemented to suppress the peak drain voltage when turning off the power switch inside U1. This passive snubber helps dissipate the energy stored in the transformer leakage inductance. The C17 capacitor is to further reduce high-frequency emissions.

### 5.2.2 CoolSET™ SiP secondary side

The secondary side of CoolSET™ SiP ICE184LM starts to take over the PWM control when output voltage reaches 95% of its regulation target. The ICE184LM PWM control is based on sensing the reflected voltage from the primary side via the ZCDS pin and the error amplifier output EA voltage. ICE184LM-integrated PWM and SR control ensures that the timing of the SR power switch (Q2) and the primary side power switch is well-synchronized, which avoids the cross conduction of the two switches and provides reliable synchronous rectification. In addition, the current injection function via the SR power switch Q2 enables for zero voltage switching operation on the primary side.



### Circuit description

R20 is connected to CONF0 and serves as  $R_{SET0}$ . The value of R20 is determined by the transformer turns ratio, which is a critical parameter in the design. According to [Table 4](#), the transformer turns ratio is specified as 8. Based on this value, R20 is set as 18 k $\Omega$ .

**Table 4 Resistance for  $R_{SET0}$**

Turns ratio $N_{MAIN} / N_{SEC}$	$R_{SET0}$
5	3.9 k $\Omega$
6	6.8 k $\Omega$
7	12.0 k $\Omega$
8	18.0 k $\Omega$
9	27.0 k $\Omega$
10	39.0 k $\Omega$

R21 is connected to CONF1 and serves as  $R_{SET1}$  to preset the operation-relevant parameters. Select Option 5 in [Table 5](#), set R22 as 27 k $\Omega$  to achieve <20 mW no load input power at input 230 VAC. These four parameters associated with  $R_{SET1}$  can be adjusted to optimize the hysteretic mode performance. By selecting different  $V_{EA\_EHM}$  values, the user can tune the power level of hysteretic mode; higher  $V_{EA\_EHM}$  values enable higher hysteretic power. In hysteretic mode, precise control over the pulse width and timing is crucial to achieving optimal standby power. The pulse width is determined by the  $V_{EA\_PWM\_HM}$  value, while the pulse starting and ending points are controlled by  $V_{EA\_HMon}$  and  $V_{EA\_HMOff}$ . By carefully adjusting these values, the hysteretic power can be fine-tuned to achieve the lowest standby power consumption.

**Table 5 Resistance for  $R_{SET1}$**

Option	1	2	3	4	5	6
$R_{SET1}$	3.9 k $\Omega$	6.8 k $\Omega$	12.0 k $\Omega$	18.0 k $\Omega$	27.0 k $\Omega$	39.0 k $\Omega$
EA voltage threshold for entering hysteretic mode ( $V_{EA\_EHM}$ )	0.586 V	0.586 V	0.605 V	0.605 V	0.624 V	0.624 V
EA voltage for pulses during hysteretic mode ( $V_{EA\_PWM\_HM}$ )	800 mV	900 mV	900 mV	800 mV	900 mV	800 mV
EA voltage hysteretic mode on threshold ( $V_{EA\_HMon}$ )	1.2 V	1.2 V	1.2 V	1.25 V	1.2 V	1.25 V
EA voltage hysteretic mode off threshold ( $V_{EA\_HMOff}$ )	0.9 V	0.9 V	0.9 V	0.8 V	0.9 V	0.8 V

A compensation network consisting of C13, C14, and R17 is implemented to stabilize the output voltage regulation. This network is carefully designed to ensure that the power supply's output voltage remains stable and within the desired range. For a detailed understanding of the compensation network's calculation, see the design guide [\[1\]](#). This resource provides a comprehensive explanation of the calculations.

To minimize ripple voltage, the choice of output capacitors is crucial. For C15 and C19, low equivalent series resistance (ESR)-type capacitors are recommended. In addition, capacitors C20 and C21 are added to suppress high frequency noise.

## 6 PCB layout

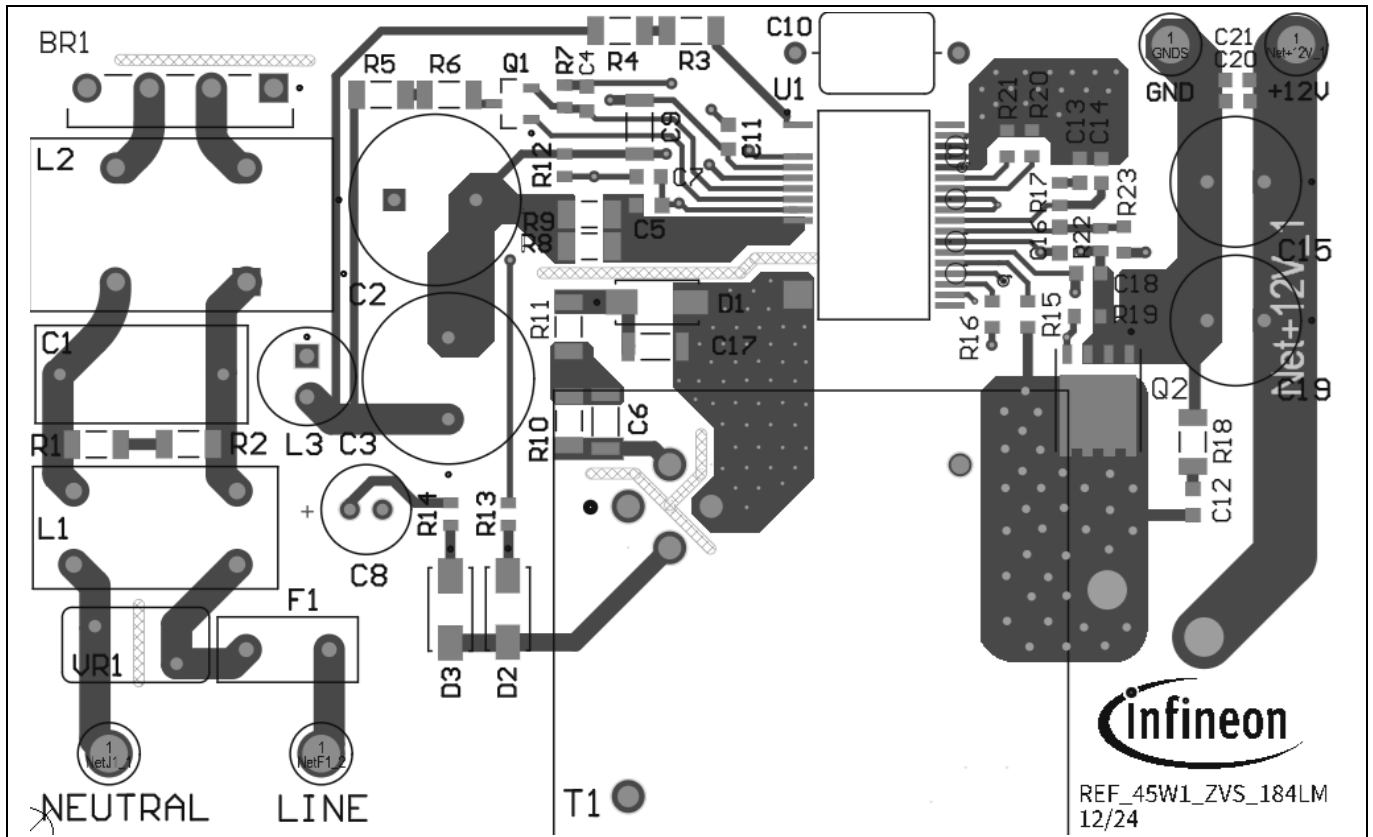


Figure 3 Top-side PCB

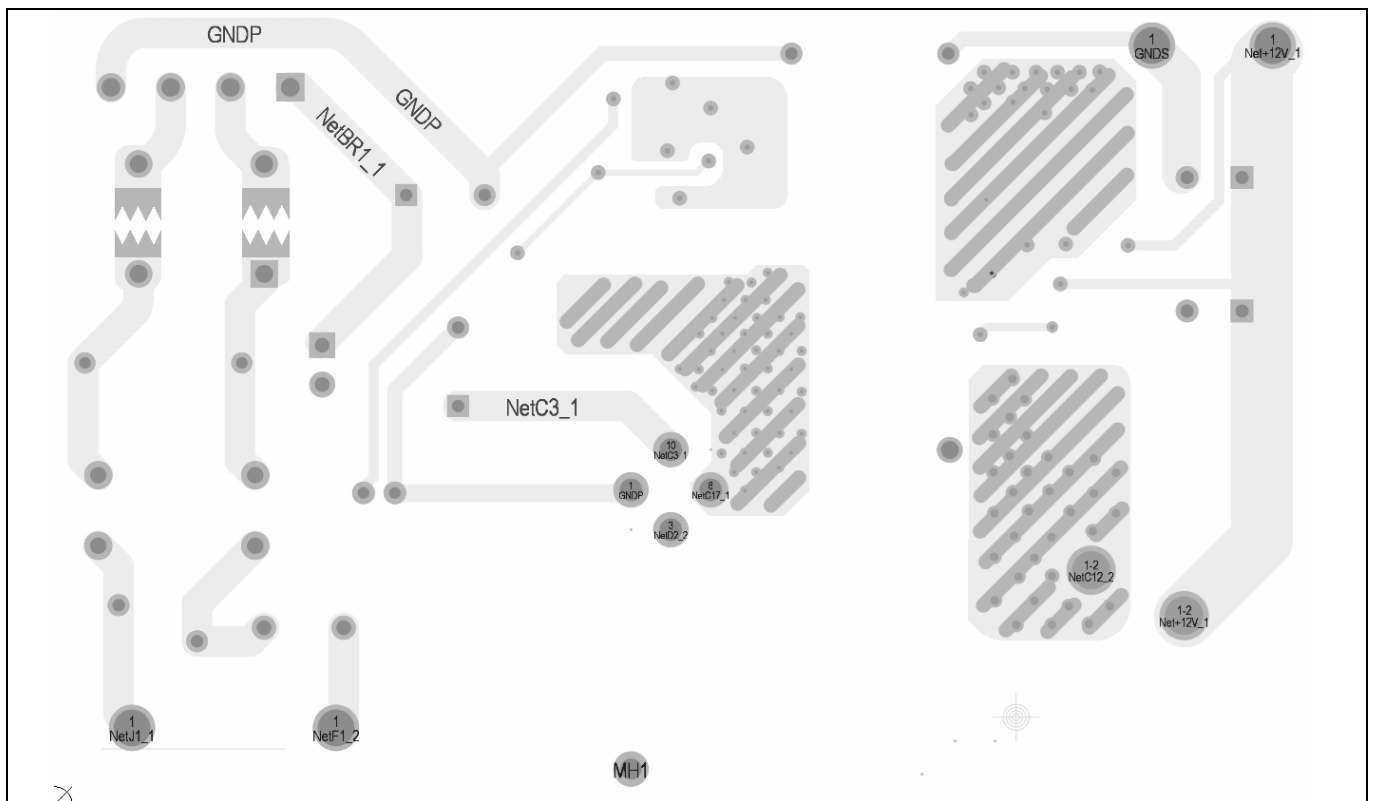


Figure 4 Bottom-side PCB

### PCB layout

PCB layout is crucial to a successful design. Following are some recommendations:

1. Minimize the loop with pulse shape current or voltage, such as the loop formed by the bus voltage source, primary winding, main power switch, and current sense resistor or the loop consisting of the secondary winding, output diode and output capacitor, or the loop of the VCCP and VCCS power supply
2. Star the ground at the bulk capacitor: all primary grounds should be connected to the ground of the bulk capacitor separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ SiP device. The primary star ground can be split into several groups:
  - i. Combine signal (all small-signal grounds connecting to the controller GNDP pin such as the filter capacitor C4, C5, and C7) and power ground (current sense resistor R8 and R9)
  - ii. VCCP ground includes the VCCP capacitor C8 ground and the auxiliary winding ground, pin 1 of the power transformer
  - iii. EMI return ground includes the Y capacitor for isolated flyback application
  - iv. DC ground from the bridge rectifier BR1
  - v. CoolSET™ SiP primary side GNDP pin 2 and pin 7 are recommended to jointly connected to a PCB copper plate, and then star connected to Bulk Cap Ground
3. CoolSET™ SiP secondary side GNDS pin 11, pin 19, and pin 26 are recommended to jointly connected to a PCB copper plate, and then star connected to the SR MOSFET source pin
4. Place the filter capacitor (C11, C18) close to the controller ground (GNDP and GNDS): Filter capacitors C4, C5, C7 and C13, C14, C16 should be placed as close to the controller ground and the controller pin as possible to reduce the switching noise coupled into the controller
5. High voltage (HV) trace clearance: HV traces like startup and drain traces should maintain sufficient spacing to the nearby traces to avoid arcing
6. Keep a minimum of 232 mm<sup>2</sup> copper area at both the primary drain pin and secondary GNDS each for enhanced thermal performance of the CoolSET™ SiP

## Bill of materials

## 7 Bill of materials

Table 6 BOM

No.	Designator	Description	Manufacturer	Part number	Qty
1	BR1	BRIDGE RECT 1PHASE 800 V 4 A GBL	Taiwan Semi	KBPF406G	1
2	C1	CAP FILM 0.1 UF 10% 310 VAC RAD	DG CX	MX2104KQ3C30GB20	1
3	C2, C3	CAP ALUM 47 UF 20% 400 V RADIAL	YMIN	KCME2002G470MF	2
4	C4, C12	MLCC - SMD/SMT 1nF 100 V 10% 0603			2
5	C5, C16	MLCC - SMD/SMT 680 pF 100 V 10% 0603			2
6	C6	MLCC - SMD/SMT 1000 PF 1 KV 10% 1206	MuRata	GRM31BR72H102KW01	1
7	C7	MLCC - SMD/SMT 25 V 33 pF C0G 0603 10%			1
8	C8	CAP ALUM 22UF 20% 50 V RADIAL TH	WE	860020672011	1
9	C9	MLCC - SMD/SMT 50 V 10 uF X7R 1206 10%			1
10	C10	CAP CER 1NF X1/Y1 440 V/400 V	Kemet	C721U102MSVDBA7317	1
11	C11, C20, C21	MLCC - SMD/SMT 100 nF 50 V 10% 0603			3
12	C13	MLCC - SMD/SMT 50 V 68 nF X7R 0603 10%			1
13	C14	MLCC - SMD/SMT 2.2 nF 50 V 10% 0603			1
14	C15, C19	Polymer Capacitors 25 Vol 680 uF RAD 2 KHR	Kemet	A750KW687M1EAAE016	2
15	C17	MLCC - SMD/SMT 100 PF 1 KV 10% 1206	Kemet	C1206C101KDGACTU	1
16	C18	MLCC - SMD/SMT 25V 4.7 uF X5R 0603 10%			1
17	D1	DIODE GEN PURP 1 KV 1A SMA	Diotec	S1M	1
18	D2, D3	DIODE GEN PURP 200 V 1A SMA	Diotec	S1D	2
19	F1	Time Lag Fuse, 300 V, 3.15 A	Littelfuse	36913150000	1
20	L1	Common Mode Standard 4 Pins, 250 uH	Endela	L-10-0179	1
21	L2	Common Mode Standard 4 Pins, 15 mH	lucky-tenda	TD1212-15.0mH, vertical	1
22	L3	FIXED IND 10UH 2.5A TH	WE	7447462100	1
23	Q1	MOSFET, 21 mA, 600 V Depletion, 3-Pin SOT-23	Infineon	BSS127IXTSA1	1
24	Q2	MOSFET Transistor, 97 A, 100 V, 8-Pin TDSO	Infineon	ISC060N10NM6ATMA1	1
25	R3, R4	Thick Film Resistors - SMD 1/4 watt 57.6 KOhm 1206 1%			2
26	R5, R6	Thick Film Resistors - SMD 5.1 M 1206 5%			2
27	R7	Thick Film Resistors - SMD 75 KOhm 100 mW 0603 1%			1
28	R8, R9	Thick Film Resistors - SMD 1/4 watt 0.68 Ohm 1206 1%			2
29	R10	Thick Film Resistors - SMD 2/3 watt 300 KOhm 1206 5%	Panasonic	ERJ-P08J304V	1
30	R11	Thick Film Resistors - SMD 1/4 watt 10 Ohm 1206 1%			1
31	R12	Thick Film Resistors - SMD 2 KOhm 100 mW 0603 1%			1
32	R13, R20	Thick Film Resistors - SMD 18 kOhm 100 mW 0603 1%			2
33	R14, R16	Thick Film Resistors - SMD 2.2 Ohm 100 mW 0603 1%			2
34	R15	Thick Film Resistors - SMD 15 kOhm 100 mW 0603 1%			1
35	R17	Thick Film Resistors - SMD 20 KOhm 100 mW 0603 1%			1
36	R18	Thick Film Resistors - SMD 1/4 watt 27 Ohm 1206 1%			1
37	R19	Thick Film Resistors - SMD 10 KOhm 100 mW 0603 1%			1
38	R21	Thick Film Resistors - SMD 27 k Ohm 100 mW 0603 1%			1
39	R22	Thick Film Resistors - SMD 30 k Ohm 100 mW 0603 1%			1
40	R23	Thick Film Resistors - SMD 270 kOhm 100 mW 0603 1%			1
41	T1	RM10 10-Terminal EXT, 360 uH	Sumida	PS23-178	1
42	U1	CoolSET™ SiP	Infineon	ICE184LM	1
43	VR1	VARISTOR 510 V 1.75 KA DISC 7 MM	Epcos	B72207S2321K101	1
44	NEUTRAL, LINE, GND, 12V	Solder Terminal, Double Turret, .109 Long	Keystone	1502-2	4

Transformer specification

## 8 Transformer specification

### 8.1 Electrical diagram and coil build

Manufacturer and part number: Sumida (PS23-178)

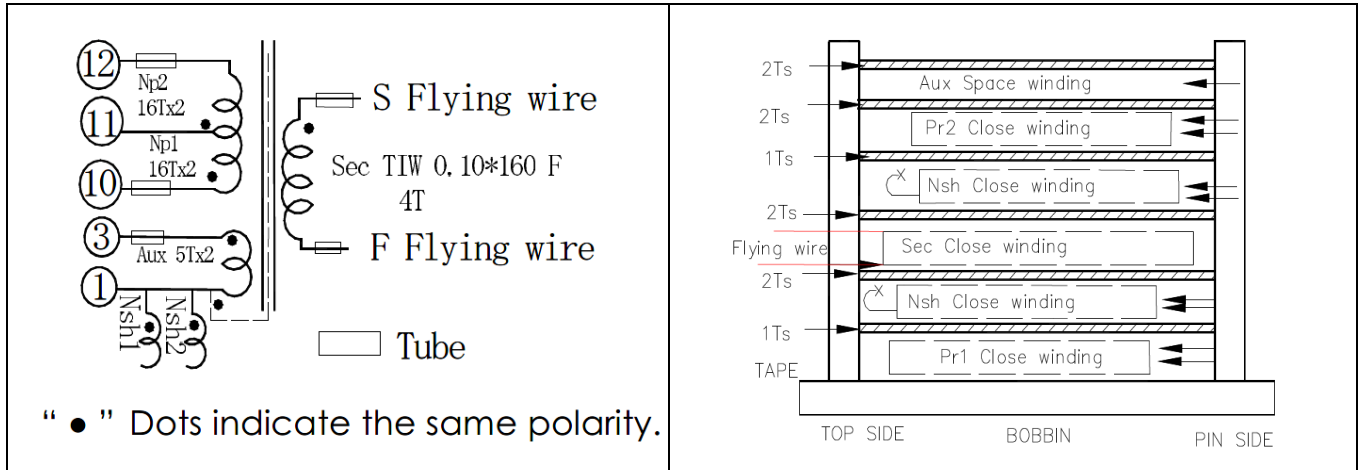


Figure 5 Electrical diagram and coil build

### 8.2 Electrical specifications

Electrical characteristic (at 25°C, unless of otherwise specified)

Items	Specification	Measuring conditions
Inductance (10-12)	360μH±5% Within	100kHz/0.1V
DCR (1-3)	Max. 280mΩ	
DCR (S Fly wire-F Fly wire)	Max. 4.5mΩ	
DCR (10-12)	Max. 120mΩ	
Hi top (1,3,10,11,12)-(S Fly wire, F Fly wire)	AC 3000Vrms	50/60Hz, 1mA, 2s
Hi top (1,3)-(10,11,12)	AC 1000Vrms	50/60Hz, 1mA, 2s
Turns ratio (10-12):(S Fly wire-F Fly wire):(1-3)	32:4:5 ±3%	

Figure 6 Electrical specifications

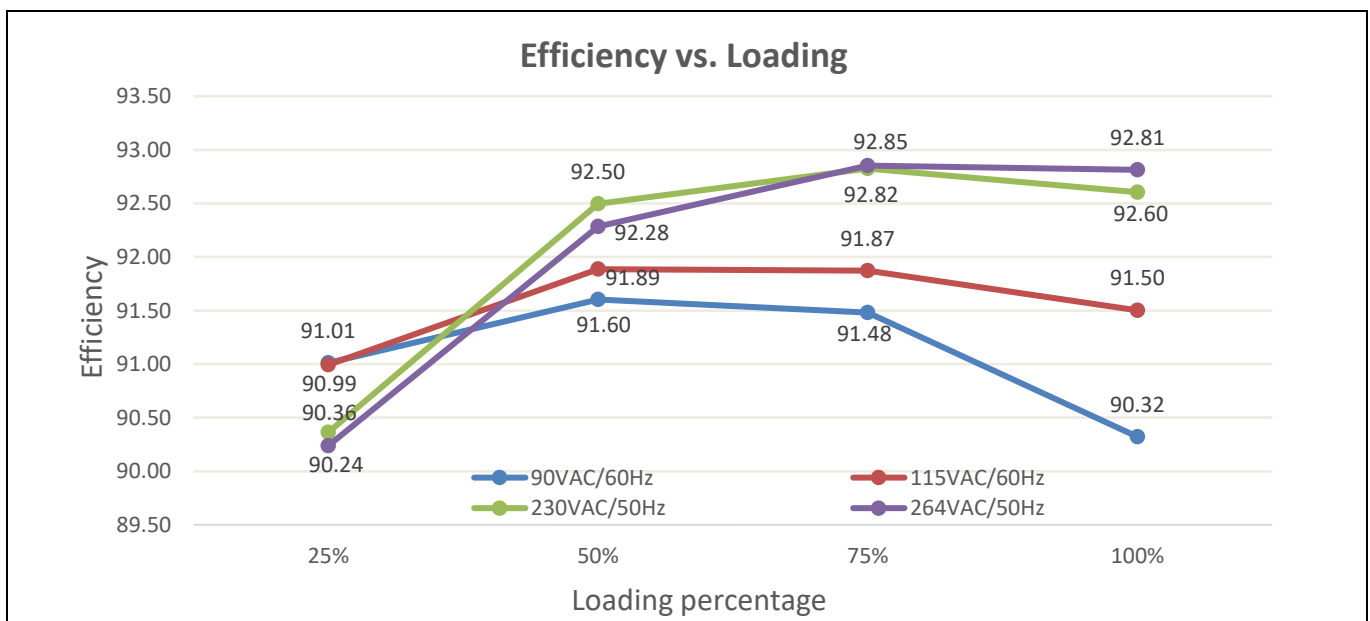
## 9 Measurement data and graphs

All performance data is measured at room temperature  $T_a = 25^\circ\text{C}$  unless otherwise specifically mentioned.

### 9.1 Efficiency result

**Table 7** Efficiency data

Input (V AC/Hz)	Load percentage	$P_{IN}$ (W)	$V_o$ (V)	$I_o$ (A)	$P_o$ (W)	Efficiency (%)	Average efficiency (%)
90 V AC/60 Hz	25%	12.44	12.06	0.94	11.32	91.01	91.11
	50%	24.75	12.06	1.88	22.67	91.60	
	75%	36.99	12.06	2.81	33.84	91.48	
	100%	50.00	12.05	3.75	45.16	90.32	
115 V AC/60 Hz	25%	12.44	12.06	0.94	11.32	90.99	91.56
	50%	24.67	12.06	1.88	22.67	91.89	
	75%	36.81	12.05	2.81	33.82	91.87	
	100%	49.34	12.05	3.75	45.15	91.50	
230 V AC/50 Hz	25%	12.53	12.06	0.94	11.33	90.36	92.07
	50%	24.50	12.05	1.88	22.66	92.50	
	75%	36.43	12.05	2.81	33.81	92.82	
	100%	48.72	12.04	3.75	45.12	92.60	
264 V AC/50 Hz	25%	12.55	12.06	0.94	11.33	90.24	92.05
	50%	24.56	12.05	1.88	22.66	92.28	
	75%	36.43	12.05	2.81	33.82	92.85	
	100%	48.64	12.04	3.75	45.14	92.81	



**Figure 7** Efficiency vs Loading

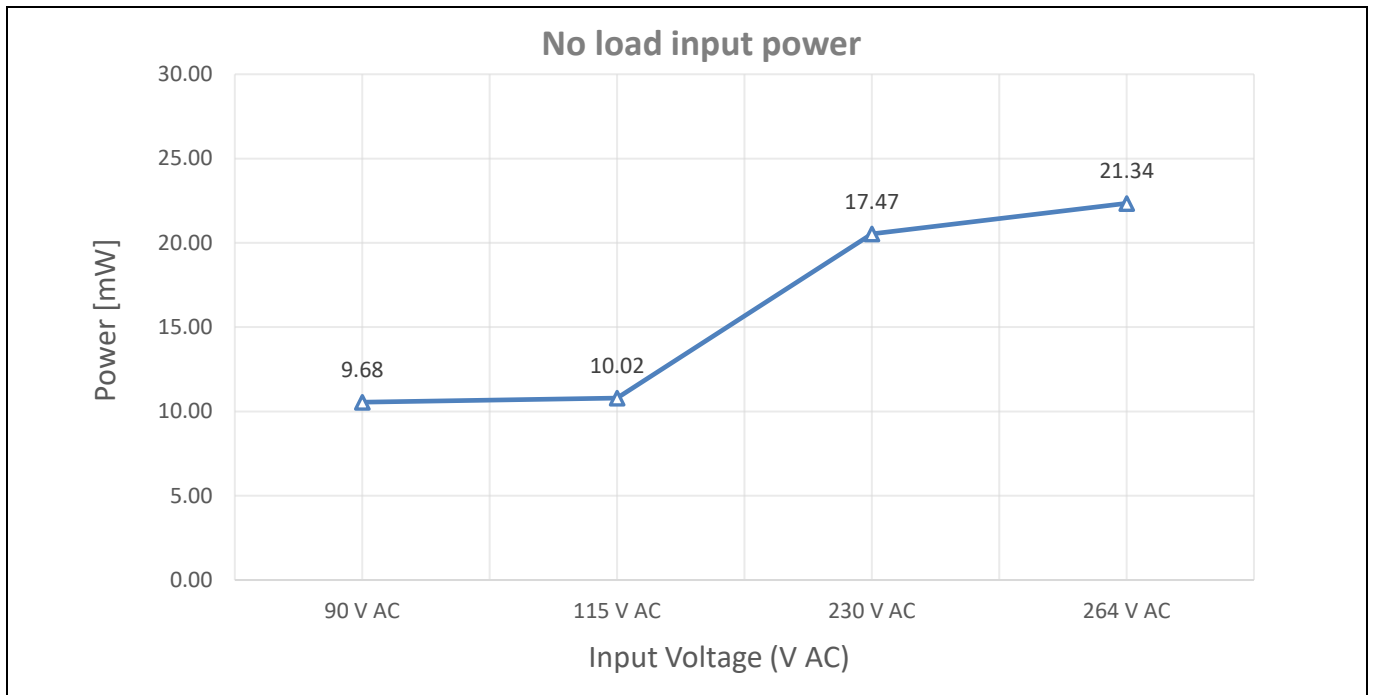


Figure 8 Standby power vs AC-line input voltage

### 9.2 ESD immunity (EN 61000-4-2)

The reference board was subjected to ESD testing according to EN 61000-4-2 level 4 ( $\pm 8$  kV contact and  $\pm 15$  kV air discharge). It was tested at full load (resistive load) and met criteria A (normal performance within the specification limits).

Table 8 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			V <sub>OUT1</sub>	GNDS	
230 V AC, 45 W	Contact	$\pm 8$ kV	10	10	Pass
	Air	$\pm 15$ kV	10	10	Pass

### 9.3 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test according to EN 61000-4-5 level 4 ( $\pm 2$  kV DM and  $\pm 4$  kV CM). It was tested at full load (resistive load) and met criteria A (normal performance within the specification limits).

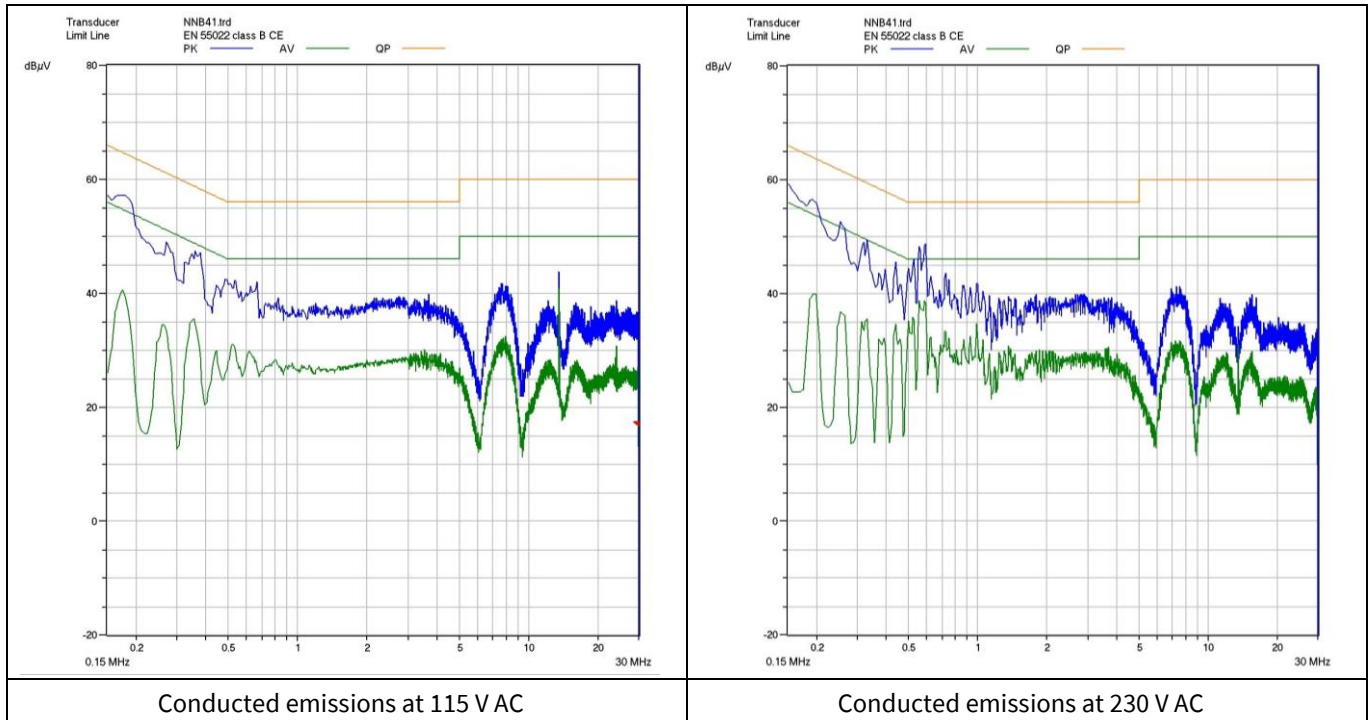
Disable input line OVP to avoid mistriggering while testing  $\pm 4$  kV CM.

Table 9 System lightning surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 V AC, 45 W	DM	$\pm 2$ kV	L → N	3	3	3	3	Pass
		$\pm 4$ kV	L → G	3	3	3	3	Pass
	CM	$\pm 4$ kV	N → G	3	3	3	3	Pass

## 9.4 Conducted emissions (EN 55022 Class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) Class B. The reference board was tested at full load (resistive load) at input voltages of 115 V AC and 230 V AC.



**Figure 9** Conducted emissions

## 9.5 Thermal measurement

The thermal testing of the reference board was executed in open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of critical components. The measurements were taken at the maximum load running for one hour. The tested input voltages were 90 V AC and 264 V AC.

**Table 10** Component temperature at full load under  $T_a = 25^\circ\text{C}$

Circuit code	Major component	Input voltage 90 V AC	Input voltage 264 V AC
		Temperature (°C)	Temperature (°C)
TR1	Main transformer	60.3	62.9
BR1	Bridge diode	83.5	51.9
U1	ICE184LM	87.7	67.8
Q1	SR MOSFET	59.6	62.1
RCD	Primary side RCD snubber	82.3	75.3



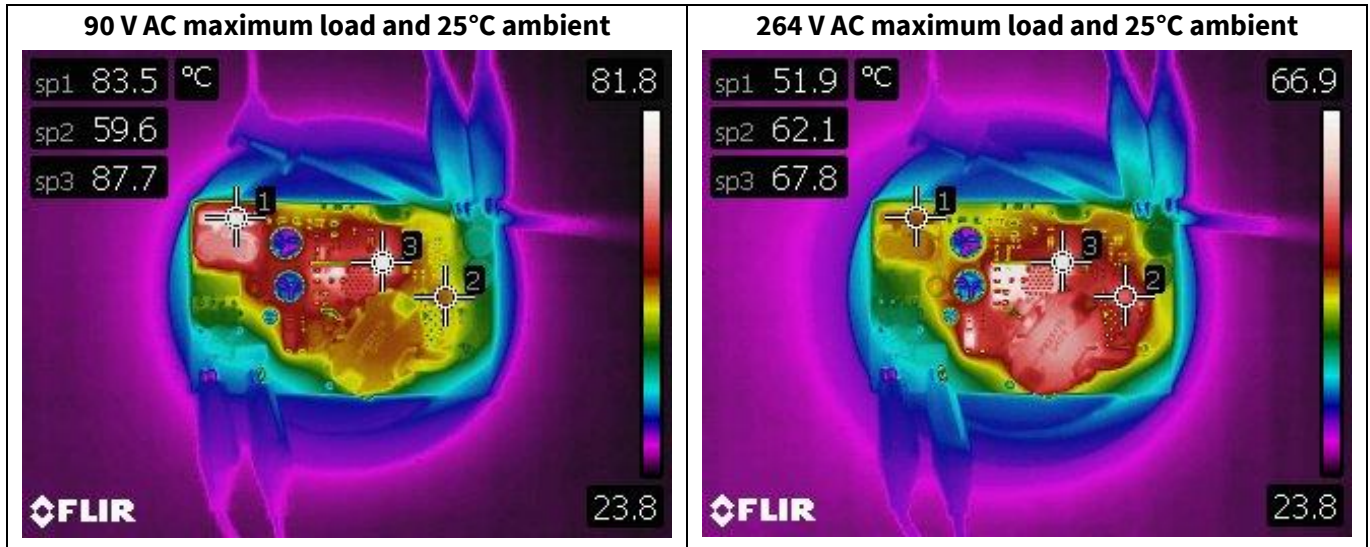


Figure 10 Thermal image of REF\_45W1\_ZVS\_184LM

Waveforms and scope plots

## 10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy oscilloscope.

### 10.1 Startup at full load

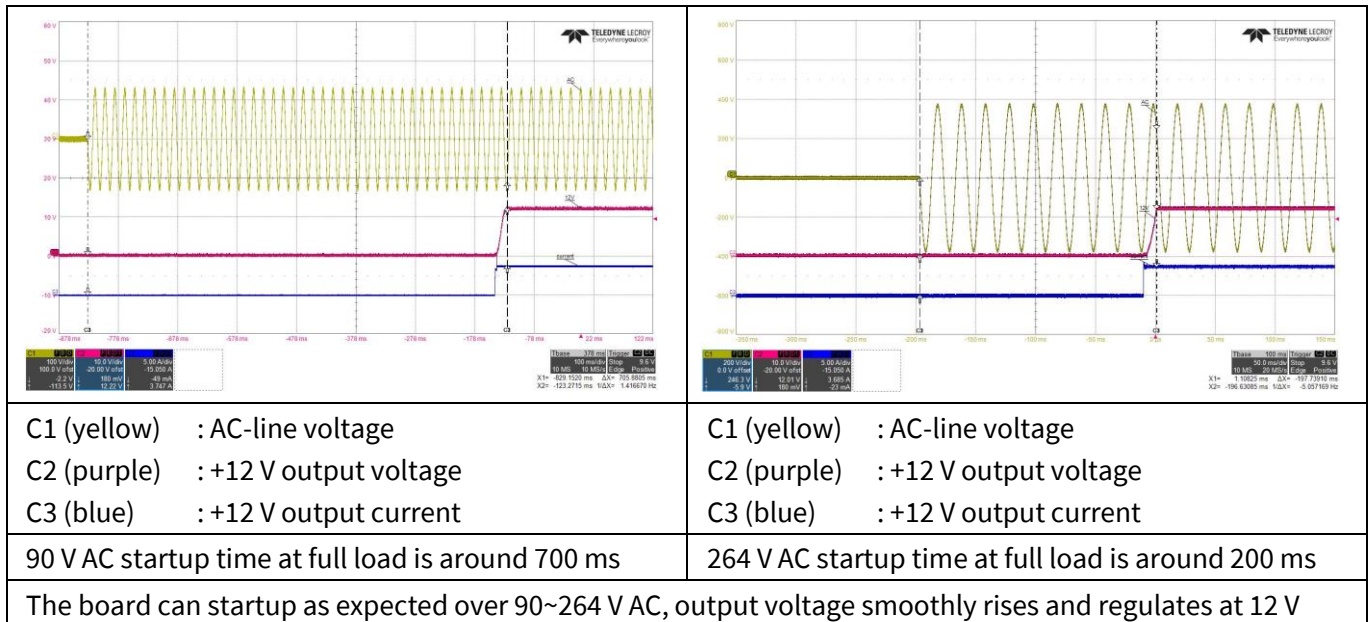


Figure 11 Startup at full load

### 10.2 Switching waveform at full load

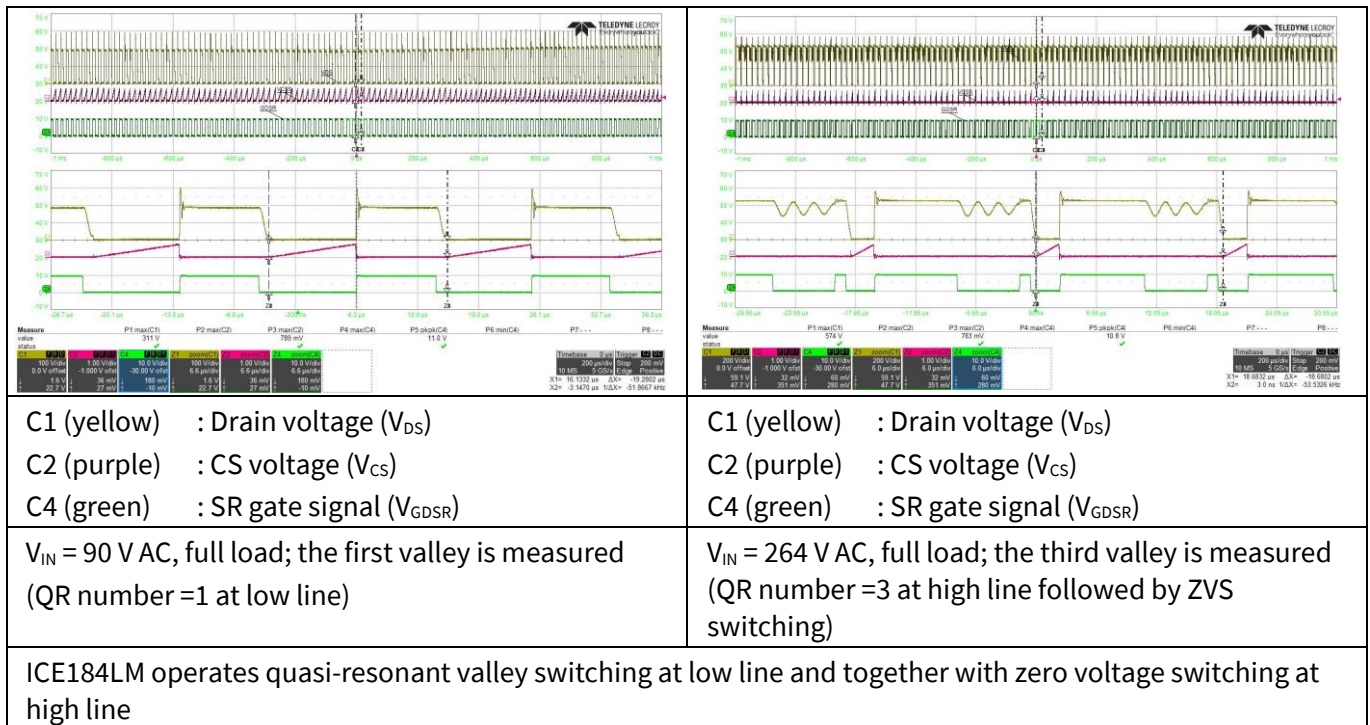


Figure 12 Switching waveform at full load

### 10.3 SR FET voltage at full load

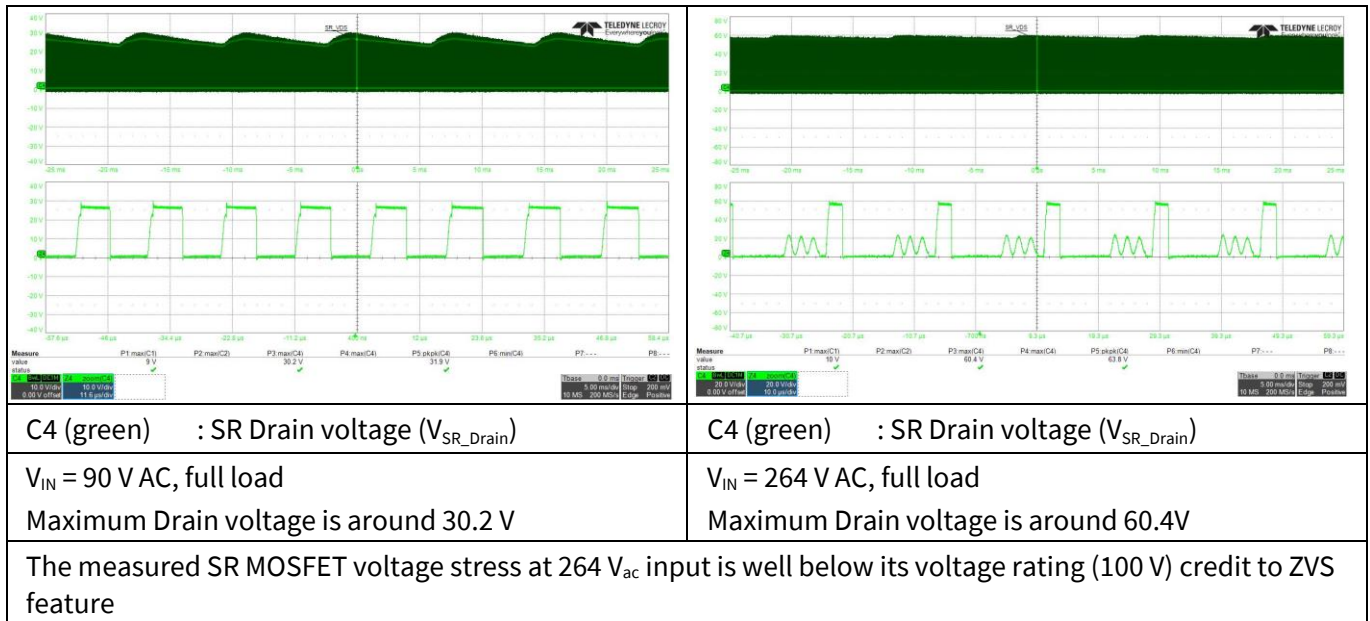


Figure 13 SR FET voltage

### 10.4 Output ripple voltage at full load

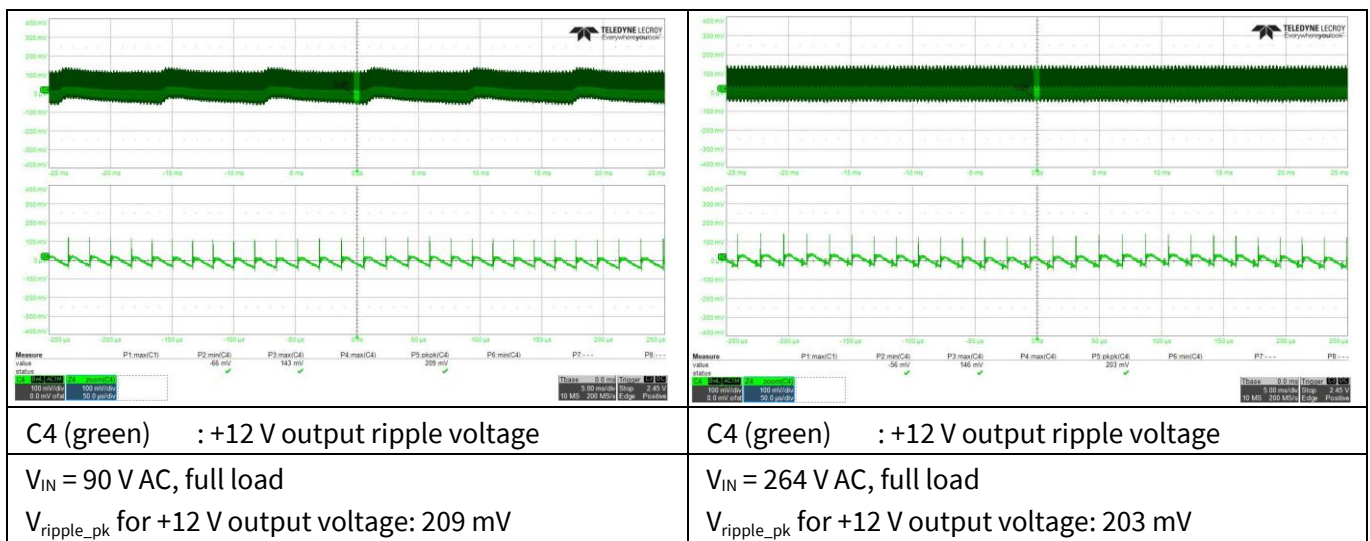
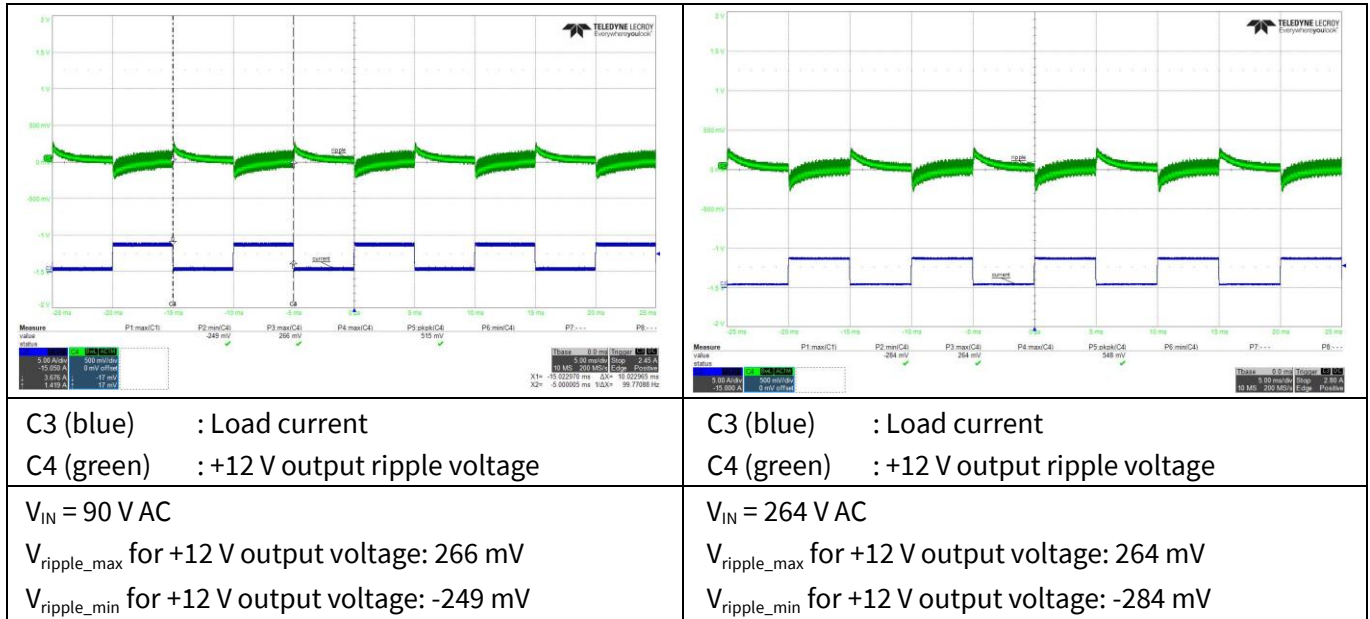


Figure 14 Output ripple voltage at full load (20 MHz bandwidth and 47 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

### 10.5 Load transient response



**Figure 15** Load transient response (+12 V output load change from 10 percent to 100 percent at 0.4 A/ $\mu\text{s}$  slew rate, 100 Hz; 20 MHz bandwidth and 47  $\mu\text{F}$  electrolytic capacitor in parallel with 0.1  $\mu\text{F}$  ceramic capacitor)

## 11 Appendix: Transformer design spreadsheet

**Table 11 Transformer design spreadsheet**

Input parameters			Unit	Value
Input	Minimum AC input voltage	$V_{ACMin}$	[V]	90
Input	Maximum AC input voltage	$V_{ACMax}$	[V]	264
Input	Line frequency	$f_{AC}$	[Hz]	60
Input	DC ripple voltage	$V_{DC\ Ripple}$	[V]	35
Input	Output voltage	$V_{OUT}$	[V]	12
Input	Output current	$I_{OUT}$	[A]	3.75
Input	Maximum output power for over-load protection	$P_{OUTMax}$	[W]	54
Result	Nominal output power	$P_{OUTNor}$	[W]	45
Input	Voltage drop across SR MOSFET(Qs)	$V_{F\ SR}$	[V]	0.1
Input	Estimated efficiency under low line and full load condition	$\eta$		0.9
Result	Estimated total capacitance on drain pin	$C_{Drain}$	[pF]	200
Input	Select transformer turns ratio	$n$		8
Result	Reflection voltage	$V_R$	[V]	96.8
Input	$V_{VCCP}$ voltage	$V_{VCCP}$	[V]	15
Input	Forward voltage of $V_{CC}$ diode	$V_{Daux}$	[V]	0.3
Input	CoolSET™ SiP		ICE184LM	
Input	Low line min. switching frequency	$f_s$	[Hz]	48000
<b>Input parameter calculation</b>				
Result	Max. input power	$P_{INMax}$	[W]	60.00
Result	Input RMS current	$I_{AC\_RMS}$	[A]	1.111
Result	Max. DC input voltage	$V_{DCMax\_Pk}$	[V]	373.35
Result	Min. peak input voltage (with ripple voltage)	$V_{DCmin\_Pk}$	[V]	127.28
Result	Min. DC input voltage	$V_{DCmin}$	[V]	90.19
Result	Discharging time for half line cycle	$T_D$	[ms]	6.32
Result	Required energy during discharging time	$W_{IN}$	[Ws]	0.38
Result	Max. duty cycle	$D_{Max}$		0.5177
<b>Post calculation with input capacitor</b>				
Result	Calculated input capacitance	$C_{IN\_cal}$	[ $\mu$ F]	98.66
Input	Select input capacitor	$C_{IN}$	[ $\mu$ F]	94
<b>Transformer parameter calculation</b>				
Result	Primary inductance	$L_P$	[H]	3.572E-04
Result	Average input current of primary inductance	$I_{AV}$	[A]	1.29
Result	Ripple current of primary inductance	$\Delta I$	[A]	2.723
Result	Peak current of primary inductance	$I_{P\_Max}$	[A]	2.65
Result	Min. current of primary inductance	$I_{Valley}$	[A]	0.0
Result	RMS current of primary inductance	$I_{P\_RMS}$	[A]	1.08
<b>Select core type</b>				
Input	Core information	Core type		RM10
		Core material		TPW33

# 45 W power supply using CoolSET™ SiP ICE184LM

REF\_45W1\_ZVS\_184LM



## Appendix: Transformer design spreadsheet

	Maximum flux density	$B_{Max}$	[T]	0.35
	Minimum magnetic cross-section	$A_{min}$	[mm <sup>2</sup> ]	98
	Bobbin width	BW	[mm]	10.49
	Winding cross-section	$A_N$	[mm <sup>2</sup> ]	45
	Average length of turn	$l_N$	[mm]	38.61

### Winding calculation

Result	Number of primary turns	$N_{MAIN}$	Turns	27.56
Input	Choose number of primary turns	$N_{MAIN}$	Turns	32
Result	Number of secondary turns	$N_{SEC}$	Turns	4.00
Input	Choose number of secondary turns	$N_{SEC}$	Turns	4.0
Result	Number of $V_{VCCP}$ turns	$N_{AUX}$	Turns	5.06
Input	Choose number of auxiliary turns	$N_{AUX}$	Turns	5
Result	$V_{VCCP}$ voltage	$V_{VCCP}$	[V]	14.83

### Post calculation

Result	Post calculation for reflection voltage	$V_R$	[V]	96.80
Result	Post calculation for max. duty cycle	$D_{Max}$		0.50
Result	Post calculation for max. flux density	$B_{Max}$	[T]	0.301
Result	Post calculation for max. turn-on time	$T_{ON\_MAX\_CAL}$	[us]	10.48
Result	Max. turn-on time controlled by IC (system config)	$T_{ON\_MAX\_POWER}$	[us]	11.17

### Transformer winding design

Input	Margin according to safety standard	M	[mm]	0
Input	Copper space factor	$f_{Cu}$		0.3
Input	Primary winding area factor	$AF_{NP}$		0.6
Input	Secondary winding area factor	$AF_{NS}$		0.35
Input	Auxiliary winding area factor	$AF_{NVCC}$		0.05

### Primary winding

Input	Insulation thickness	INS	[mm]	0.02
Result	Area of primary wire	$A_p$	[mm <sup>2</sup> ]	0.25
Result	Diameter of primary wire	Dia.	[mm]	0.57
Result	Wire size	AWG		23
Input	selected wire size	AWG		28
Input	Number of parallel wire	$N_p$		2
Result	Diameter of selected primary wire	Dia.	[mm]	0.32
Result	Effective copper area of primary		[mm <sup>2</sup> ]	0.1642
Result	Primary current density	$S_p$	[A/mm <sup>2</sup> ]	6.60
Result	Effective bobbin width	$BW_e$	[mm]	10.5
Result	Diameter of primary wire including insulation	$Od_p$	[mm]	0.36
Result	Max. primary turns/layers	$NL_P$	Turns/layer	14
Result	Primary layers	$Ln_P$	Layers	3

### Secondary winding

Input	Insulation thickness	INS	[mm]	0.2
Result	Area of secondary wire	$A_s$	[mm <sup>2</sup> ]	1.18
Result	Diameter of secondary wire	Dia.	[mm]	1.23

### Appendix: Transformer design spreadsheet

Result	Wire size	AWG		16
Input	Selected wire size	AWG		38
Input	Number of parallel wires	$N_p$		160
Result	Diameter of secondary wires	Dia.	[mm]	0.10
Result	Effective copper area of secondary		[mm <sup>2</sup> ]	1.3046
Result	Secondary current density	$S_s$	[A/mm <sup>2</sup> ]	6.61
Result	Effective bobbin width	$BW_E$	[mm]	10.5
Result	Diameter of secondary wire including insulation	$Od_s$	[mm]	1.69
Result	Max. secondary turns/layer	$NL_s$	Turns/layer	6
Result	Secondary layers	$Ln_s$	Layers	1

### References

### References

- [1] Infineon Technologies AG: Datasheet – *CoolSET™ SiP*
- [2] Infineon Technologies AG: Application note – *Design Guide for ZVS QR flyback using CoolSET™ SiP*
- [3] Infineon Technologies AG: *Calculation Tool for CoolSET™ SiP*



Revision history

Revision history

Document version	Date of release	Description of changes
V 1.0	2025-04-11	Initial release

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