PSOC™ Control Low-Voltage PFC Development Expansion Kit user guide

About this document

Scope and purpose

This document describes hardware details of the Low-Voltage Power Factor Correction (LV PFC) Development Expansion Board. The board provides an evaluation platform for digital-control applications with PSOC™ Control, Arm® Cortex®-M33 based MCU. This board forms part of Infineon's digital-power evaluation platform kits.

Intended audience

This document targets KIT_PSC3_PFC1 users. Use this board under laboratory conditions with additional items listed in the Getting started section.

Evaluation board

This board is designed to evaluate the performance of Infineon's PSOC™ Control family of MCUs and to help users become familiar with its peripherals and features.

Important notice

“Evaluation Boards and Reference Boards” shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as “Reference Board”).

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Safety precautions

***Note**: Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

Infineon's PSOC™ Control Low-Voltage PFC Development Expansion Kit provides a safe and flexible platform for developing and testing digital power-conversion control on the PSOC™ Control MCU family. It includes the complete power stage, current and voltage-sensing circuits, configurable auxiliary supplies, and independent hardware-protection features. A 120-pin connector links the board to the control card, giving access to all required analog, digital, and PWM signals for PFC control.

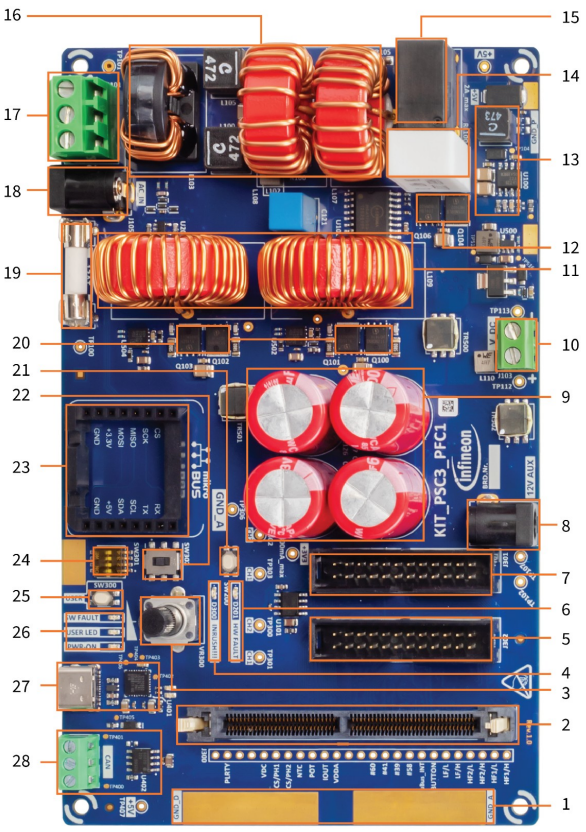
Multiple interfaces, including USB-UART, CAN, and mikroBUS, support communication and system expansion. Dedicated test points simplify measurement, debugging, and validation of control-loop behavior. This platform enables rapid evaluation of totem-pole PFC operation and serves as a starting point for firmware development using ModusToolbox™.

1.1 Features

This section describes the major hardware elements, functional interfaces, and protection features integrated into the PFC evaluation board.

- **Hardware features**:
  - **Input filter**: The board includes an input filter designed to mitigate EMI noise
  - **Inrush-current limiter**: An inrush-current limiter lowers instantaneous peak current when bulk capacitors are in a discharged state
  - **Interleaved totem-pole PFC stage**: The power stage consists of an interleaved totem-pole PFC featuring:
    - Two interleaved high-frequency half-bridge legs
    - One slow half-bridge leg
  - **Control Card connector**: A dedicated connector enables the user to plug in the selected Control Card
  - **Master-slave connection**: A master-slave interface allows the Control Card installed on the PFC board to control a second evaluation board, such as:
    - A dual buck board
    - A low-voltage LLC board
  - **Test points**: Multiple test points are available for convenient measurement access and detailed converter analysis
- **User-machine interface**:
  - **General-purpose press button**: Used for basic user interaction
  - **LED indicators**: The board provides multiple LEDs to display system status:
    - Power ON indication
    - User LED and SW FAULT indicators for control regulation and fault status
  - **Communication interfaces**: Available communication options include:
    - CAN interface
    - Dual-port serial interface
    - mikroBUS header
- **Auxiliary power supply**: An independent 12 V DC auxiliary-supply input is provided to bias the IC and enable signal generation even when no input voltage is applied
- **Hardware protection**: Hardware-protection circuits operate independently of the MCU. These circuits serve as the final safety barrier to protect the board from damage caused by incorrect PWM-signal sequences

***Note**: Not all failures combinations are covered by this protection circuit.*



1 Analog and Digital test points with related ground planes
2 120-pin connector for hosting KIT_PSC3Mx_CC1 (J300)
3 Potentiometer for analog voltage generation to MCU input pin.
4 Red LED to signal inrush resistor is still active (D300)
5 SLAVE IN daisy chain connector (J302)
6 Red LED to signal a fault event not handled by MCU happened (D201)
7 MASTER OUT daisy chain connector (J301)
8 Auxiliary DC input supply, 12 V for independent usage from AC side
9 Auxiliary DC input supply, 12 V for independent usage from AC side
10 DC output voltage connector (J103)
11 PFC boost inductors phase 1 and phase 2 (L109, L112)
12 Low Frequency half bridges switches (Q104, Q106)
13 Step down voltage regulator (VAUX/VOUT to 5 V) and circuitry
14 Inrush current limiter resistance (4.7R)
15 Relay (RL100)
16 Input Filter
17 AC Input Connector (J101)
18 AC Input barrel jack for AC-AC Adapter (J105)
19 Input Fuse. 12A slow (F100)
20 Phase 1 & Phase 2 half bridge switches (Q100, Q103)
21 hardware fault switch, to reset the ext. fault event (SW200)
22 Switch to select SPI lines according to CC1 used (SW302)
23 mikroBUS connector
24 Switch to select between SPI lines and second UART (SW301)
25 User switch, routed to MCU input pin (SW300)
26 LEDs:
– MCU driven RED LED (SW FAULT)
– MCU driven GREEN LED (USER LED)
– Green LED to signal presence of 3.3 V (PWR ON)
27 USB to dual UART converter
28 CAN interface connection

Figure 1 Low-voltage PFC Evaluation Board hardware details

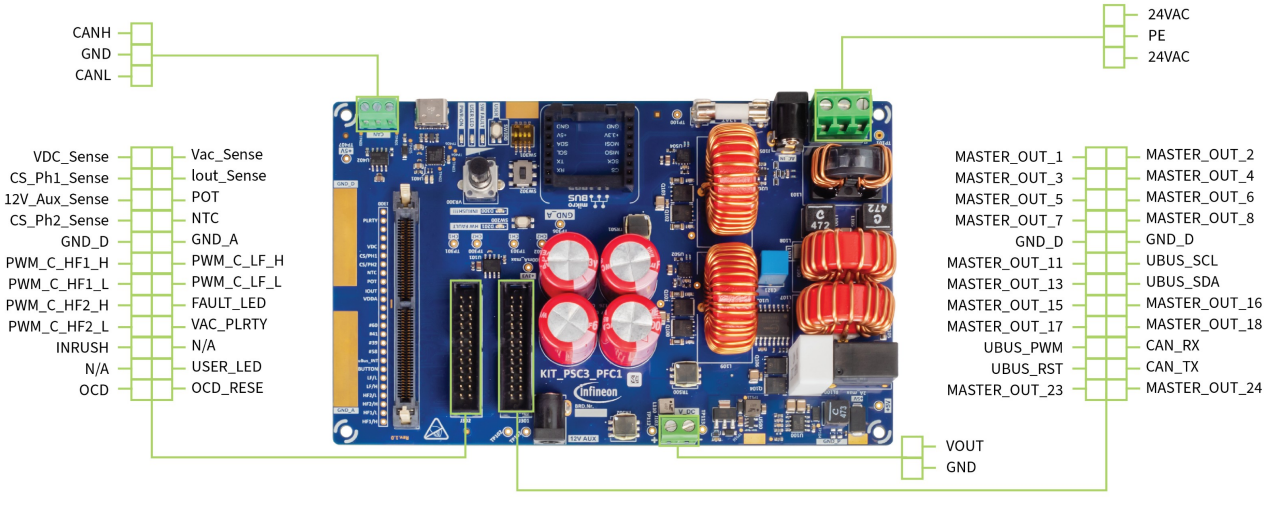


Figure 2 Low-voltage PFC Evaluation Board pinout details

1.2 Kit contents

Kit contents include:

- PFC evaluation board
- AC-AC power adapter

Table 2 AC-AC adapter usage information

		• *The AC-AC power adapter includes a selector switch with default position set to '0' or disconnected. Adjust the position to correct AC supply voltage for your working location (110 V or 230 V applicable)* • *Selecting the wrong range causes permanent damage and renders transformer unusable* ***Warning:*** ***Do not use non-galvanic isolated supply sources. Using a non-isolated AC input can cause injury to the user/permanent damage to the evaluation board***

Note: *The AC-AC adapter terminates with Europlug Type-C. Purchase a universal adapter to match your plug standard.*

1.3 Completing the evaluation kit

To operate the kit, additional items must be ordered separately.

1.3.1 Minimal hardware setup in standalone LV PFC testing

For minimal hardware setup in standalone LV PFC testing, the following components are required:

- **PSOC™ Control Card**: The PSOC™ Control Card options and offerings are as follows:
  - **KIT_PSC3M5_CC1**: Active and preferred
  - **KIT_PSC3M8_CC1**: Does not have supported application firmware as of March 2026, firmware support is planned for the second half of 2026
- **DC load**: The load shall be greater than or equal to the output electrical quantities specified in Hardware specifications. Use a resistive load (rheostat) or a DC electronic load, such as KORAD KEL102
- **Output cables**: Cables should be suitable for connecting the PFC board output to the DC load

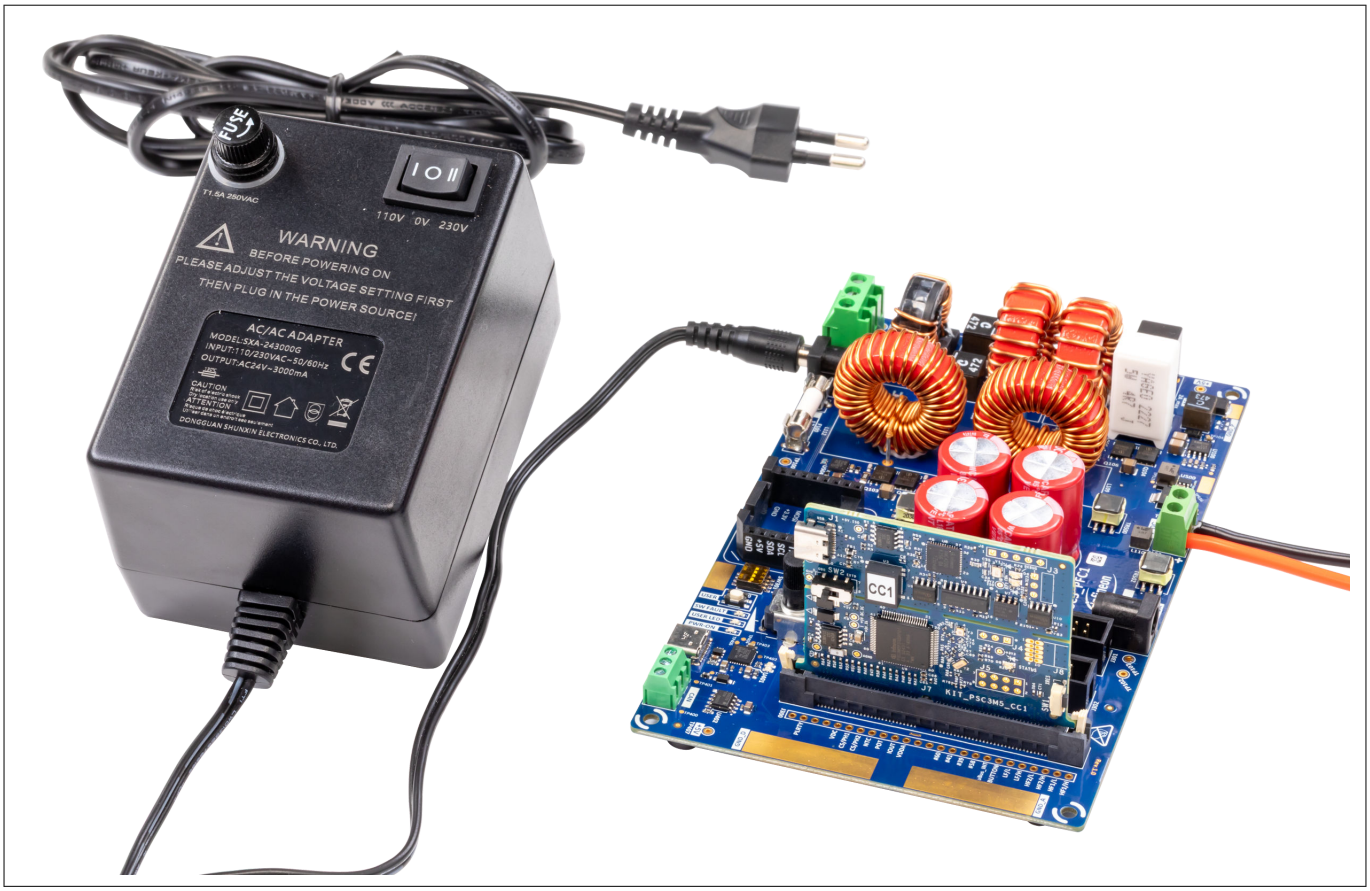


Figure 3 Overview of the minimal hardware setup

1.3.2 Full hardware setup in standalone LV PFC testing

System functionality can be extended by adding the following optional components:

- **PMBus dongle**: The PMBus dongle enables use of the graphical user interface available in the Power Suite package. As of March 2026, the firmware has been tested with the PMBus dongle, USB0008. The latest USB dongle (for example USB0010) may also be used
- **AC-DC auxiliary supply**: Enables system debugging when input voltage is absent, for example SMI6B-12-4-P6 available on DigiKey. However, the system includes an on-board auxiliary supply that operates on the output DC bus voltage starting at 10 V DC

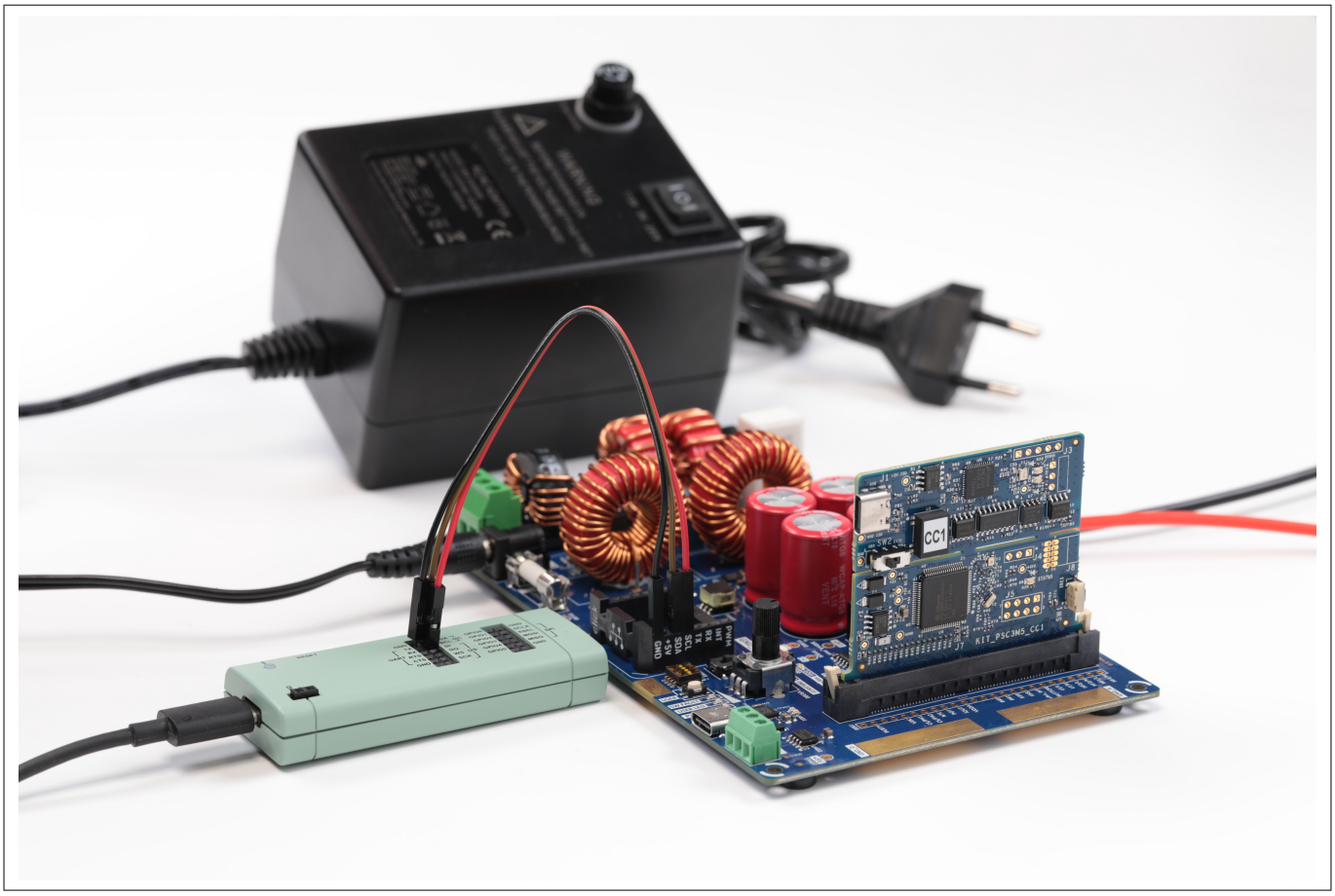


Figure 4 Overview of the full hardware setup

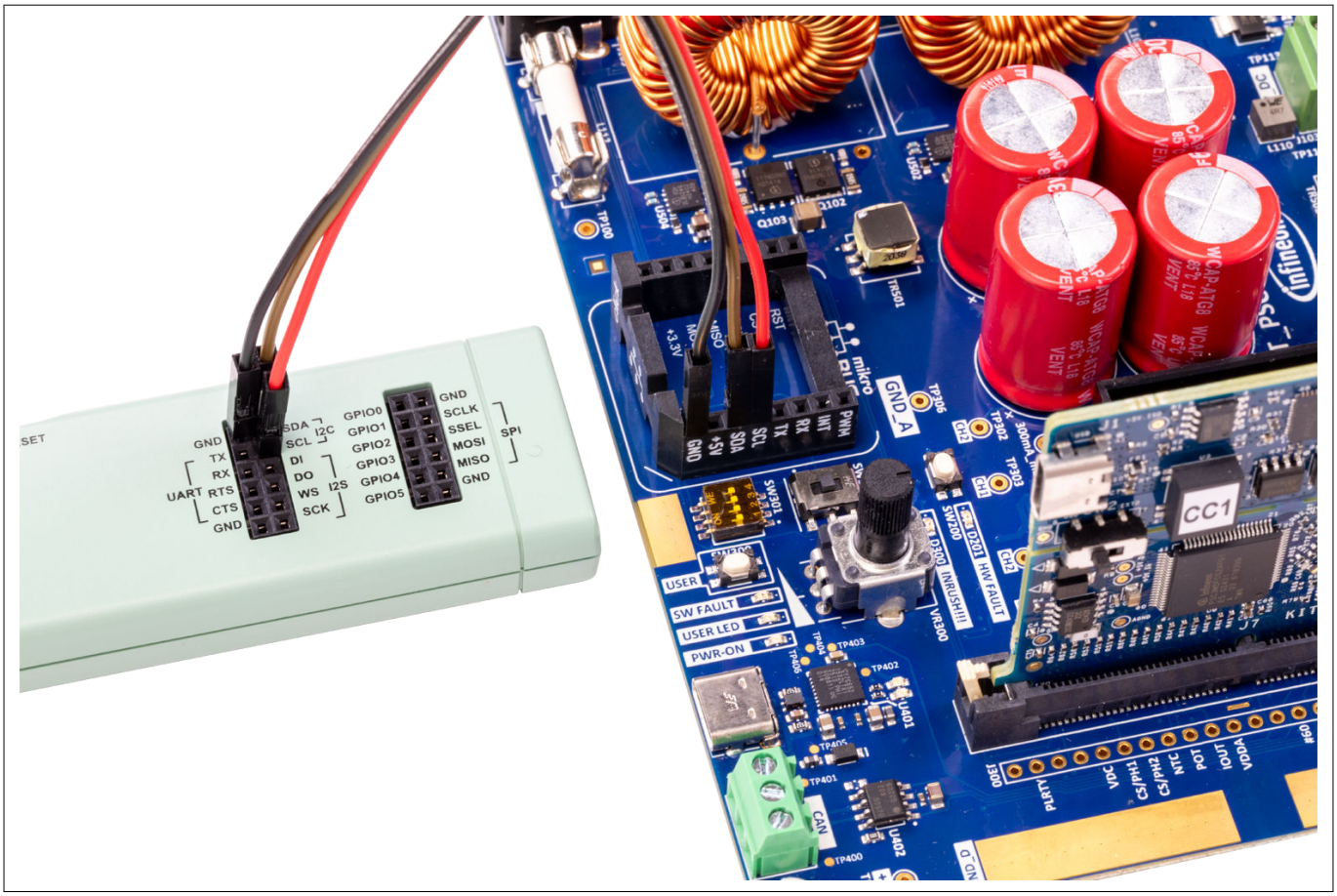


Figure 5 **PMBus connection detail**

1.4 Hardware specifications

Table 3 **Hardware specifications**

Parameter	Unit	Values			Remarks
		Min.	Nominal.	Max.	
Input voltage	V_{ac}	12	23	26	AC-AC adapter generates only 23 V_{ac}.
Input current	A_{ac}	-	-	10	-
Output voltage	VDC	-	40	50	-
Output current	ADC	-	-	2.5	-
Output power	W	-	-	78	Total power when supplied by the AC-AC adapter or programmable bench power supply is limited by the current sensor that measures peak current up to 5 A.
Switching frequency	kHz	-	100	500	Maximum limit is theoretical but not tested.

2 Kit operation

The Low-Voltage PFC evaluation board is a scaled-down implementation of a real totem-pole PFC stage, with operating parameters reduced by approximately a factor of ten compared to a high-voltage design. Its main goal is to provide a realistic and functional system prototype, offering greater fidelity than a simulated digital twin. It closely resembles the high-voltage TP-PFC in architecture and behavior while operating in a safe low-voltage environment.

The board can be used directly on a standard laboratory desk without requiring specialized high-voltage equipment. By keeping the regulated DC output voltage below 50 V, the system remains below hazardous-voltage limits defined by safety standards.

The platform enables users to learn how to use the differentiating MCU peripherals of the PSOC™ Control family through direct interaction with a multi-phase totem-pole PFC system. Eventually, users can extend the system by interconnecting an additional expansion board in a daisy-chain configuration.

2.1 Getting started

The Low-Voltage PFC Development Expansion Kit must be used with the PSOC™ Control C3M5 Digital Power Control Card, KIT_PSC3M5_CC1, which is supported in ModusToolbox™. Using ModusToolbox™, you can enable and configure PSOC™ Control C3M5 MCU resources and middleware libraries, write source code for the control-loop implementation, and program and debug the MCU.

A code example is available for evaluating the PFC evaluation board using the PSOC™ Control C3M5 Digital Power Control Card. This example helps you become familiar with the PFC Evaluation Board and the PSOC™ Control C3M5 MCU and provides a foundation for creating your own design. You can access it through the ModusToolbox™ New Application, with the appropriate BSP selected in the tool. Alternatively, you can visit Infineon's code examples for the ModusToolbox™ software page to access these examples.

Similar support will also extend to future products within the PSOC™ Control family.

2.1.1 Setting up the hardware assembly

To assemble the hardware, do the following:

1. Ensure that the selector switch on the AC-AC power adapter is set to the correct AC supply voltage as shown in Figure 6

Figure 6 Selector-switch setting on the AC-AC power adapter

2. Insert the PSOC™ C3 Control Card into the control-card slot, as shown in Figure 7

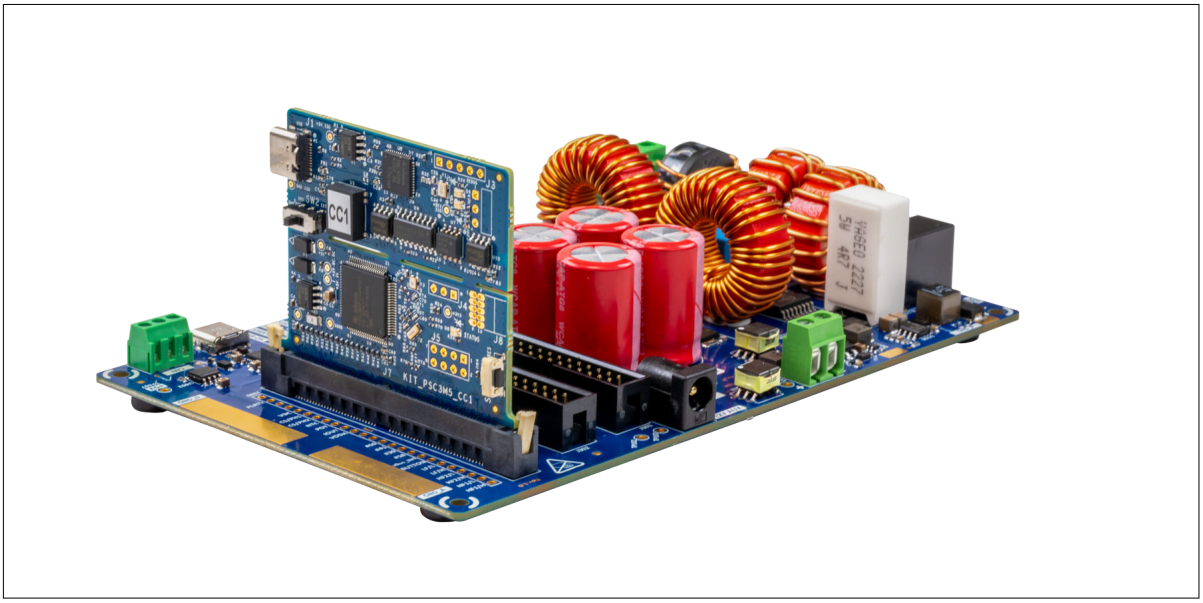


Figure 7 Control-card installation

3. Connect the USB-C cable to the control card, as shown in Figure 8, and program the control card with the associated code example as described on the kit website

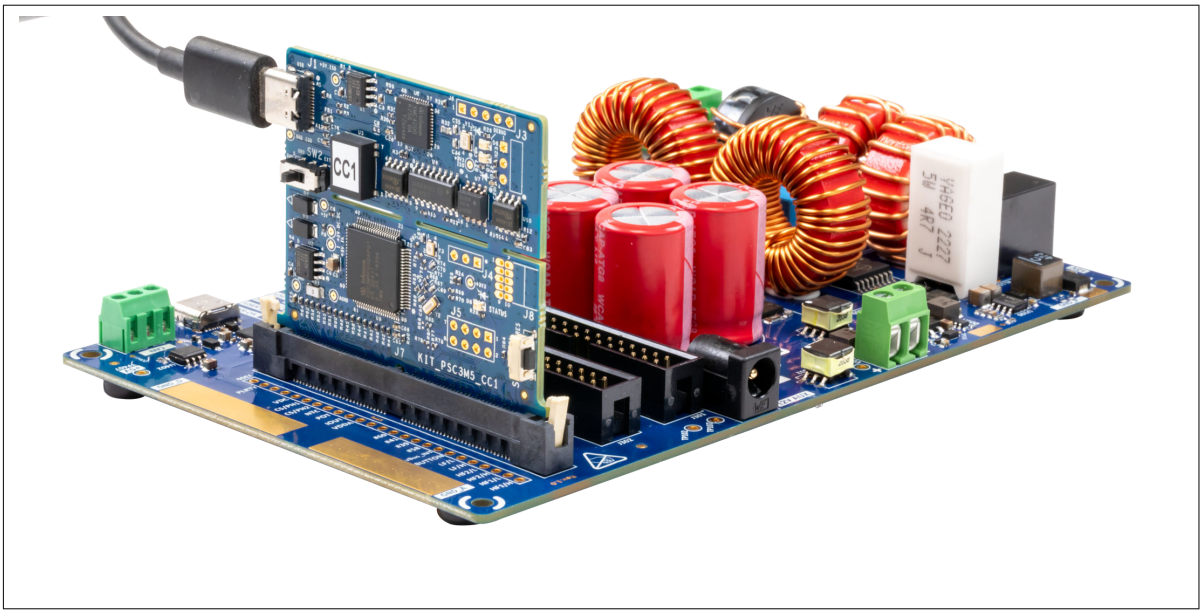


Figure 8 USB-C cable setup for programming the PSOC™ C3 Control Card

2.2 Creating, programming, and debugging a project in ModusToolbox™

The PSOC™ Control C3M5 Control Card can be programmed and debugged using the onboard J-Link debugger. The onboard J-Link programmer and debugger support USB-UART bridge functionality. An XMC4200 device is used to implement the J-Link functionality.

***Note**: To use J-Link, ensure that you have downloaded and installed the latest J-Link drivers.*

The following steps briefly introduce project creation, programming, and debugging using ModusToolbox™ software. For detailed instructions, go to **Help** > **ModusToolbox™ General Documentation** > **ModusToolbox™ user guide**.

1. Connect the KIT_PSC3M5_CC1 board to the PC using the provided USB cable through the J-Link USB connector, as shown in Figure 8. If you are connecting it for the first time, it enumerates as a USB composite device

   ***Note**: For additional details, see the KIT_PSC3M5_CC1 Quick Start Guide or user guide*

2. The debugger on this kit uses J-Link and one UART. The COM LED (green) remains ON when the USB is connected

   ***Note**: Programming can be performed using the onboard J-Link debugger or by attaching an external debugger to connector J8 on the control card. It is recommended to use the onboard J-Link debugger*

3. In the Eclipse IDE for ModusToolbox™ software, import the code example (application) into a new workspace

   a. In the Quick Panel, click **New Application** from the **Start** section

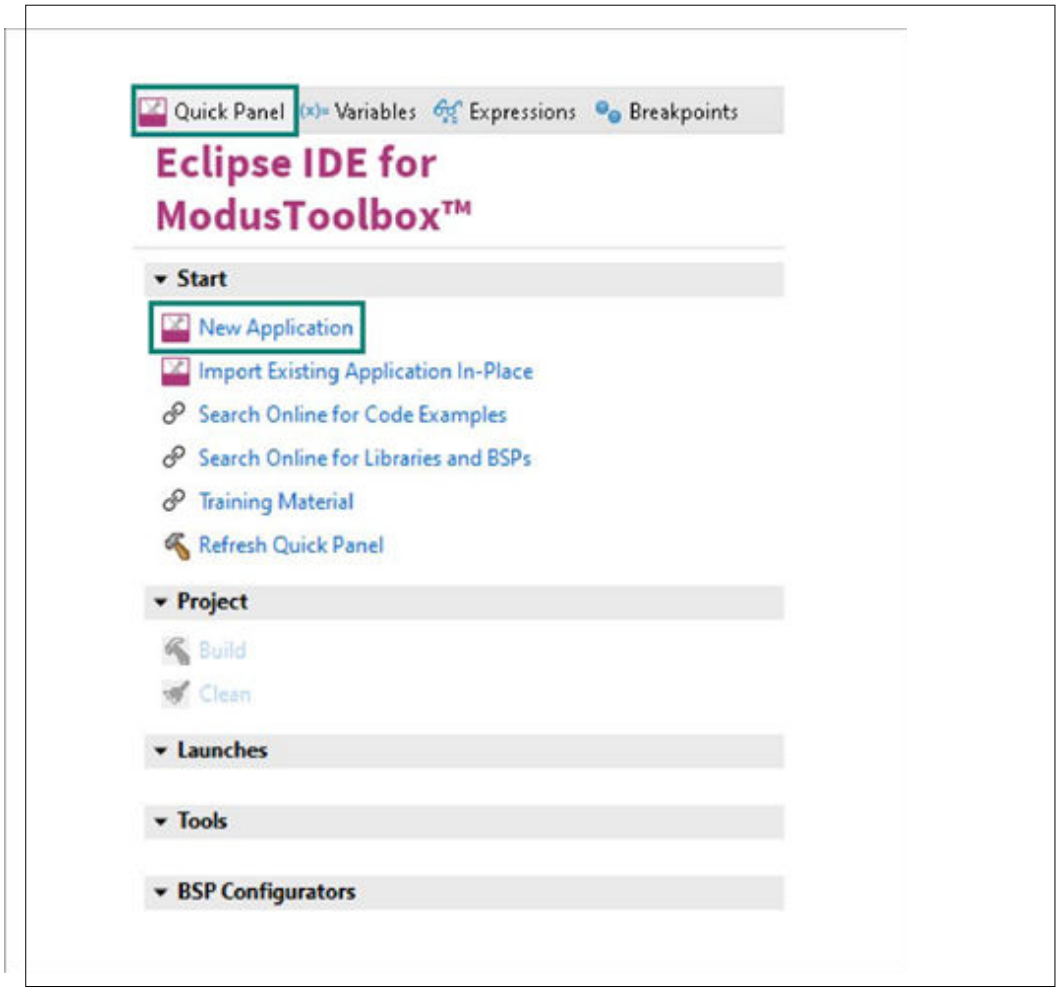


Figure 9 Creating a New Application

b. In the **Choose Board Support Package** window, select the BSP **KIT_PSC3M5_CC1** and click **Next**

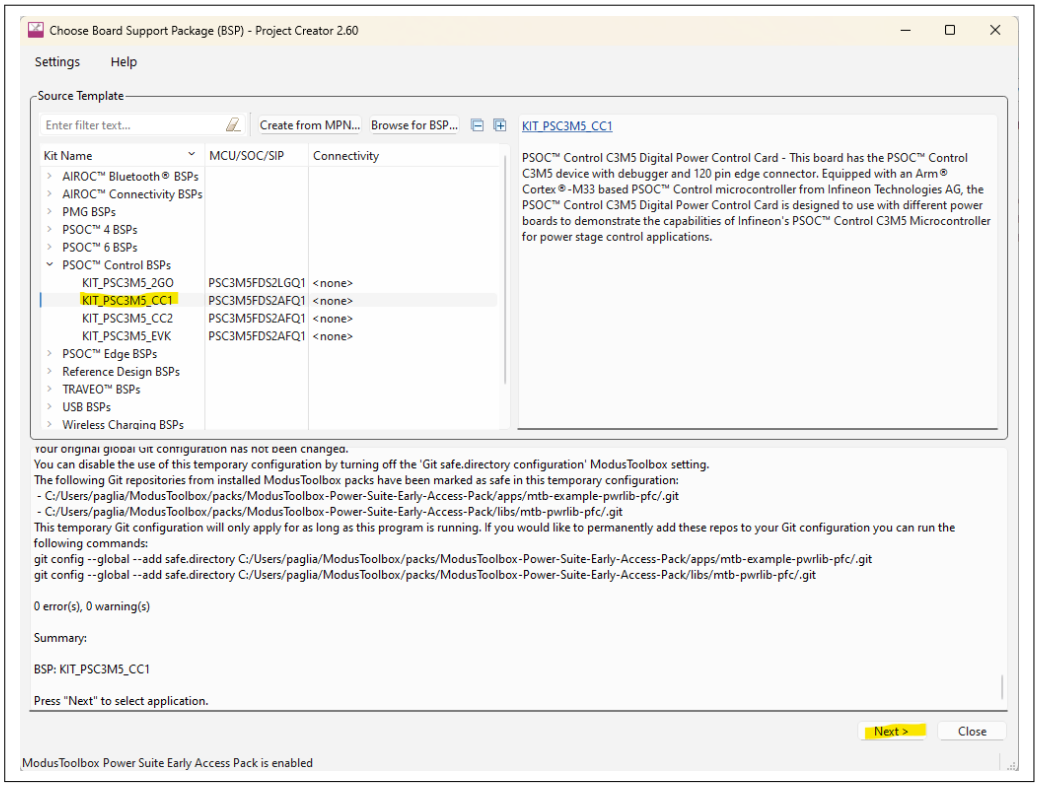


Figure 10 Choose Board Support Package

c. In the **Select Application** window, choose the application and click **Create**

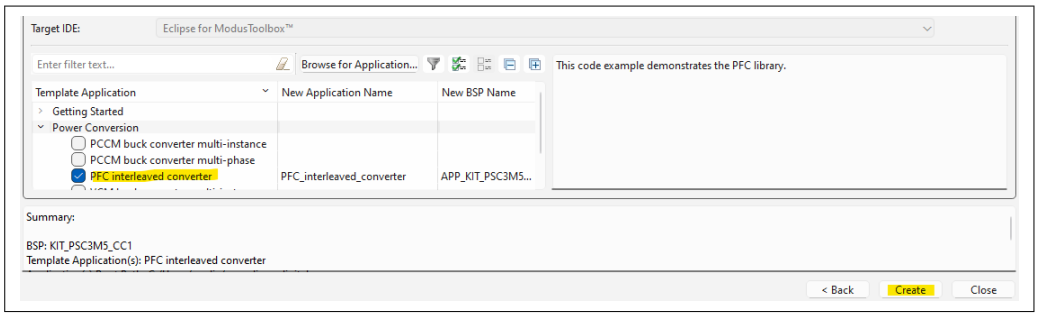


Figure 11 Create the application

4. To build and program the PSOC™ Control C3M5 MCU application:

a. In the **Project Explorer**, select the **<App_Name>** project

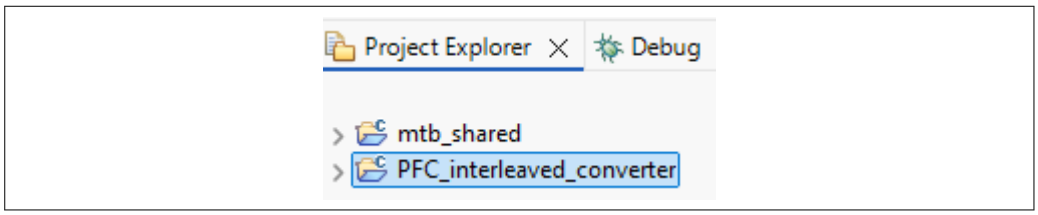


Figure 12 Programming in ModusToolbox™

b. ModusToolbox™ includes an integrated debugger. In the Quick Panel, click the **<App_Name> Program (J-Link)** configuration from the **Launches** section, as shown in Figure 13

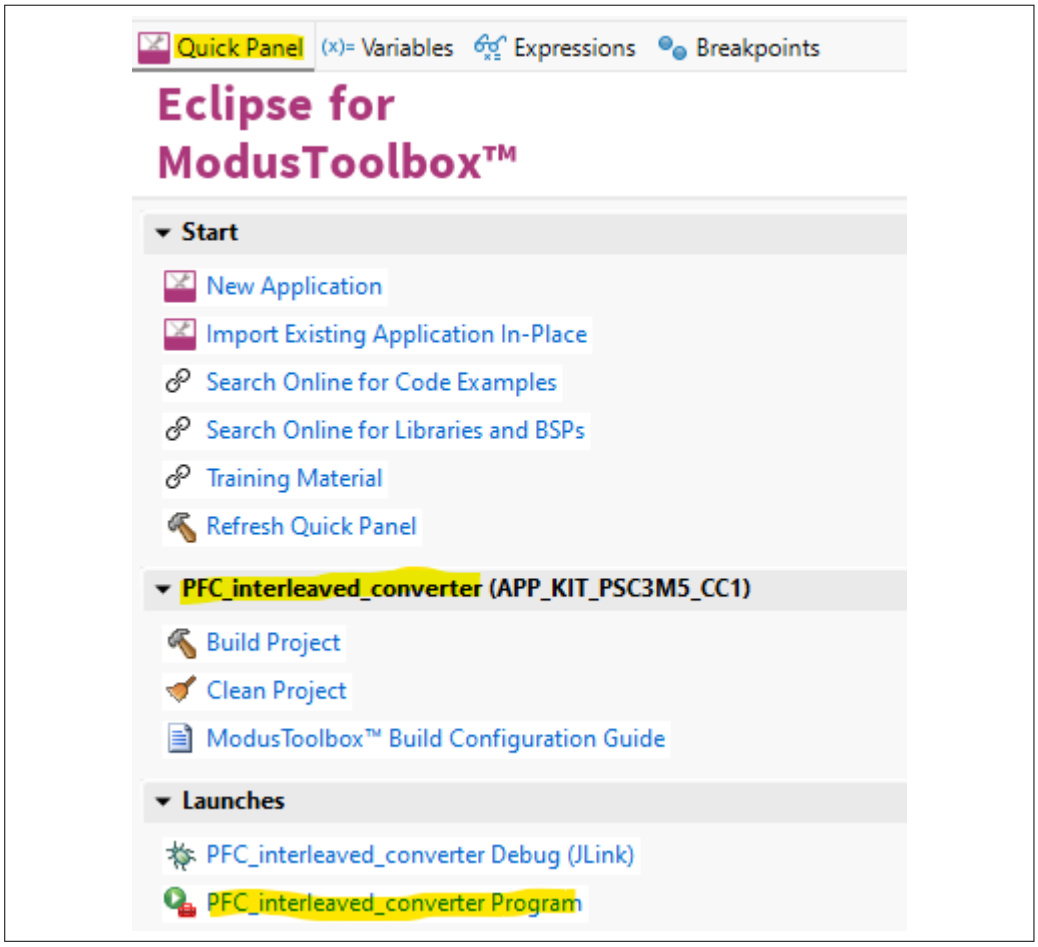


Figure 13 Programming the application

5. To debug the application, choose the `<App_Name> Debug (J-Link)` configuration from the **Launches** section

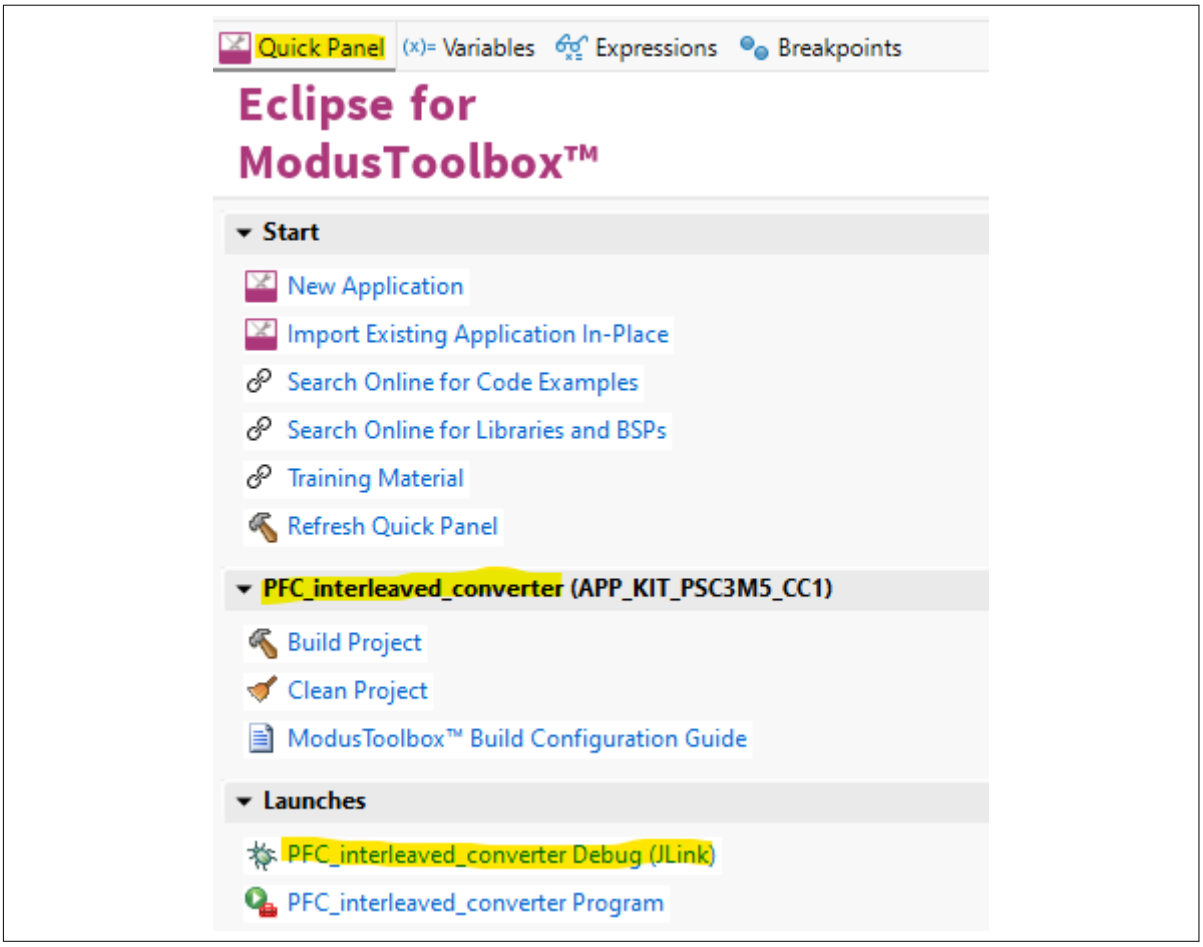


Figure 14 Debugging in ModusToolbox™

For additional details, see the Program and Debug section in the Eclipse IDE for ModusToolbox™ user guide.

3 Hardware

3.1 Block diagram

The Low-Voltage PFC evaluation board consists of two phases with high-frequency half-bridge legs and a low-frequency half-bridge. Each phase has a dedicated current sensor to support current-based algorithm development. The input and output voltages are sensed and routed to the 120-pin connector to provide the required analog quantities for completing a software-based PFC algorithm. A polarity signal is also generated from the AC input to increase robustness in firmware development and to counter line-cycle dropout events.

Figure 15 shows the high-level LV PFC block diagram, emphasizing the topology and the essential quantities required for control-based algorithm development.

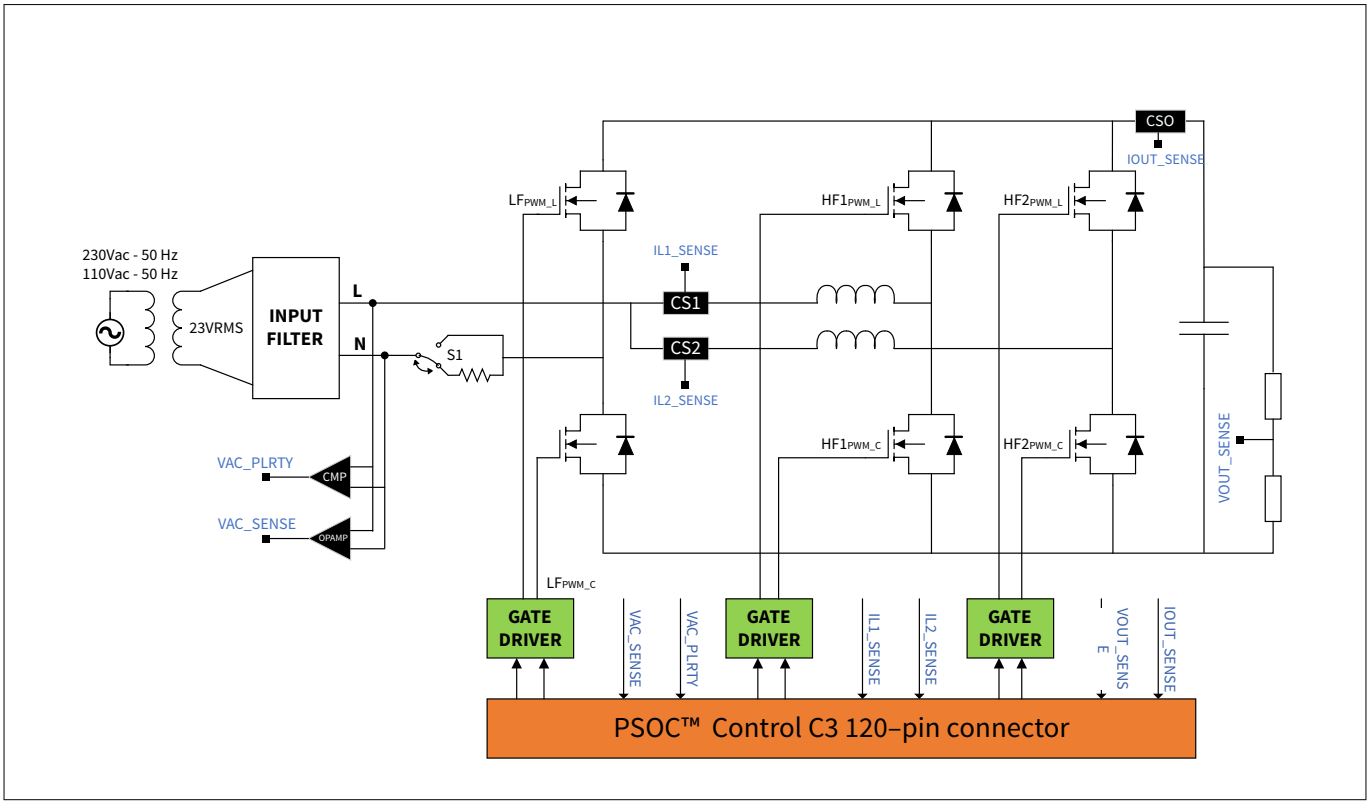


Figure 15 High-level LV PFC block diagram

3.1.1 Functional blocks

The Low-Voltage PFC evaluation board consists of five main functional domains:

1. **Input stage**: This domain manages all voltage-generation functions such as:
   - AC input to DC-bus voltage output
   - Auxiliary-supply voltage concept
2. **Protection**: This domain provides onboard active protection that acts in parallel as the ultimate safeguard against potential electrical overstress caused by misuse of PWM signals
3. **Gate driver**: This domain handles level-shifting of logic PWM signals to gate-drive signals
4. **Controller**: This domain covers pin assignment for the control-card 120-pin connector, the signal-conditioning circuits, and simple HMI features such as LEDs, a push button, and a potentiometer
5. **Communication**: This domain includes the communication layers added to the board to interface with the algorithm, including a dual serial port, a CAN port, and a standard mikroBUS interface for external click-board devices

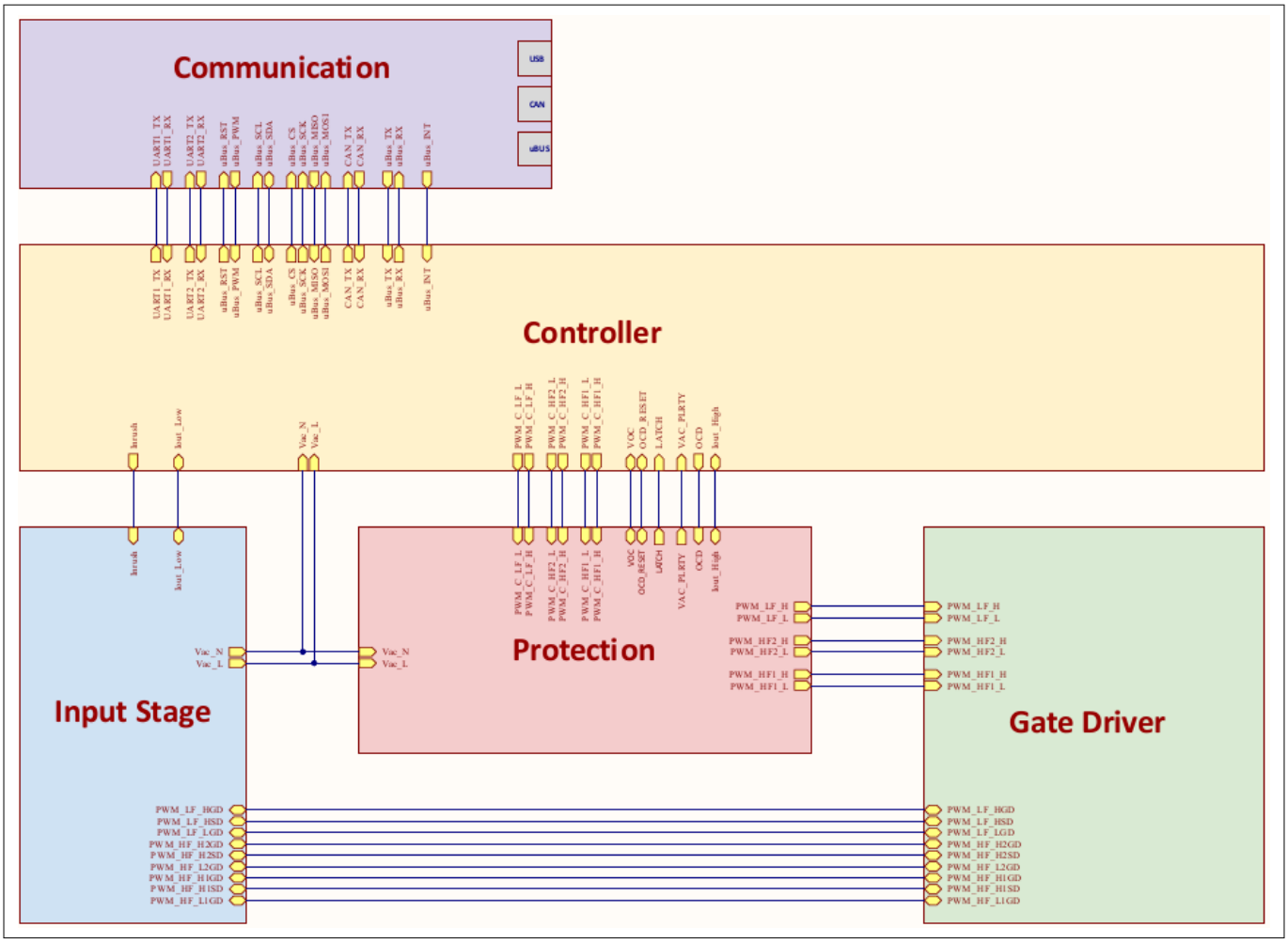


Figure 16 Functional blocks of the LV PFC evaluation board hardware

3.1.2 Power flow and supply strategy

Figure 17 provides a high-level overview of the strategy used to generate the different voltage rails required to power the system. The following sections provide a more detailed description for the same.

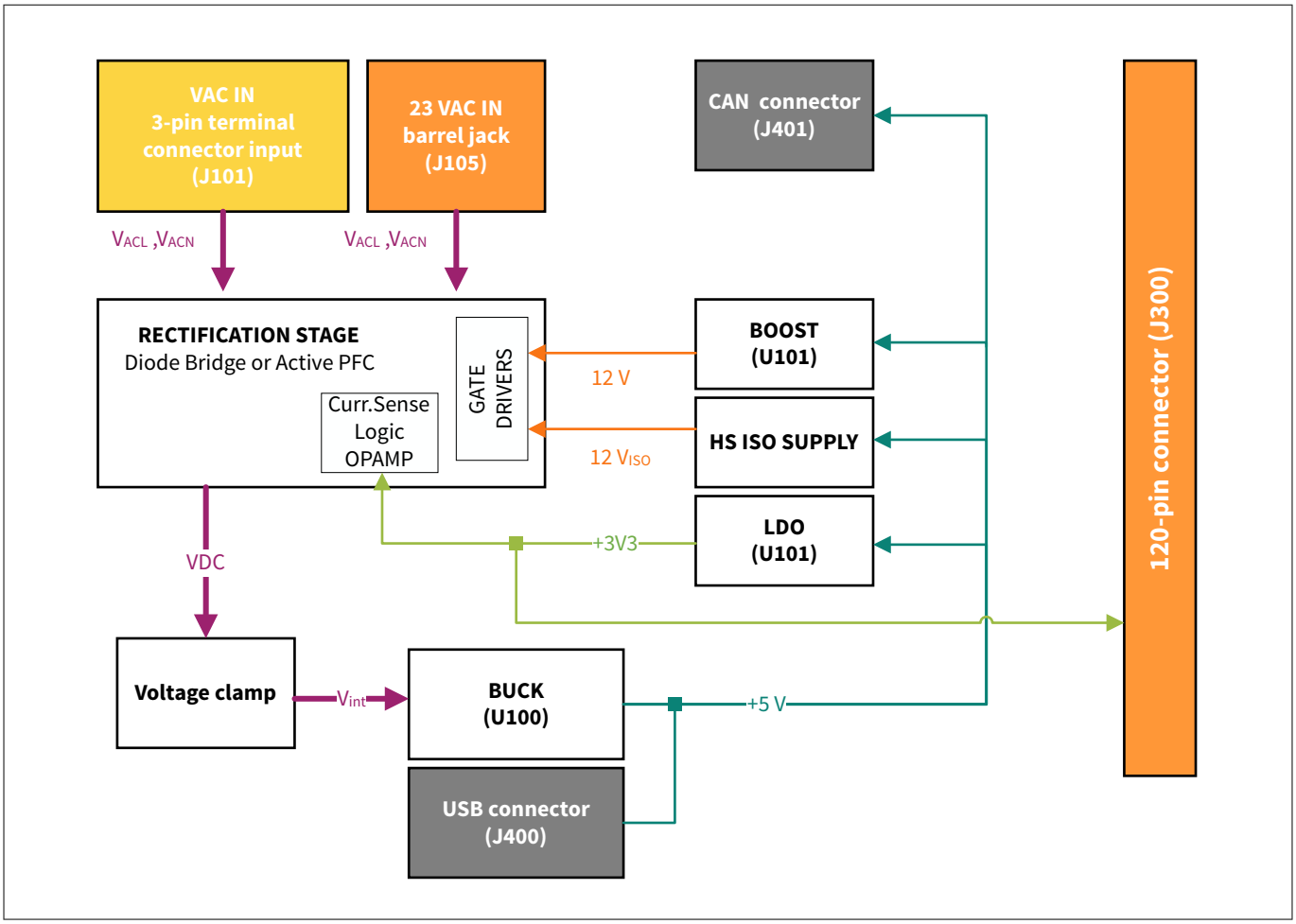


Figure 17 **Voltage-rail generation strategy for system power-up**

3.1.3 Input stage

The Low-Voltage totem-pole PFC evaluation board is intended for low-voltage operation. Its main specifications are listed in Table 3. Operating the board above its rated voltage limits will cause permanent hardware damage.

When used with the PFC code example introduced in the Getting started section, the default regulated output voltage is 40 V. The maximum output current is limited by the current sensor on each phase inductor, with a peak current limit of 5 A. Exceeding this limit in an attempt to increase output power results in a distorted current waveform, typically appearing as a trapezoid or a clipped sine wave due to sensor saturation.

***Note**: A different output voltage can be configured either by modifying the default target value in the firmware (minimal setup), or by sending an appropriate PMBus command using the dongle and the GUI provided with Power Suite (full setup). For detailed instructions, see the GUI user manual.*

Hardware limits also apply. Independent protection activates at 55 V, and the output bulk capacitors are rated for 63 V. Exceeding this voltage causes permanent board damage.

The minimum DC output voltage is determined by the rectified AC input voltage. For boost-type PFC stages, a general rule of thumb is:

$$V_{OUT\_MIN} = V_{AC\_RMS} * \sqrt{2} \quad (1)$$

.

Using the provided transformer, this results in a minimum output of approximately 32.6 V.

Figure 18 shows a schematic view of the input stage.

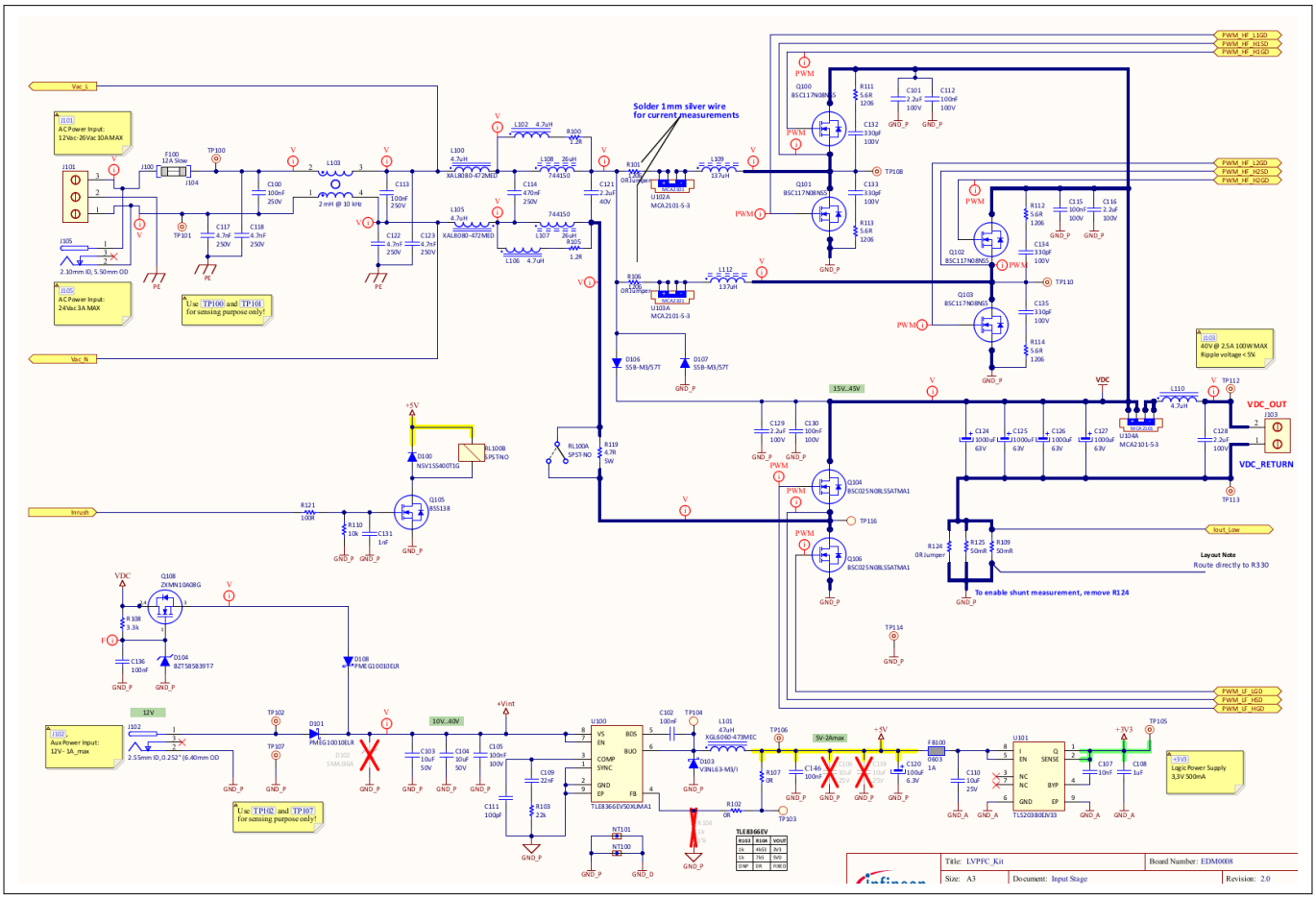


Figure 18 Input stage overview

Two input connectors are available: J101 and J105.

- **AC-AC adapter connection**:
  - When using the provided transformer with a barrel plug, connect it to J105
  - This connection is rated for a maximum continuous current of 3 A RMS
- **Programmable power-supply connection**:
  - When laboratory equipment is available, use J101, which supports up to 10 A RMS
  - The current-sensing circuitry on the input inductor limits the peak current to 5 A

Warning: ***Do not use non-galvanic isolated supply sources. Using a non-isolated AC input can cause injury to the user/permanent damage to the evaluation board***

A slow 12 A fuse protects the circuit against high inrush currents during startup.

The input stage includes an EMI filter composed of X-capacitors, Y-capacitors, a common-mode choke, and a differential-mode choke. This network reduces harmonic content fed back into the AC line that results from the high switching frequency and the hard-switching characteristics of the totem-pole PFC topology. Two test points, TP100 and TP101, are located next to the input connectors for voltage sensing only. They must not be used as current-supply terminals. When monitoring the AC input with an oscilloscope, use a differential probe for safe measurement.

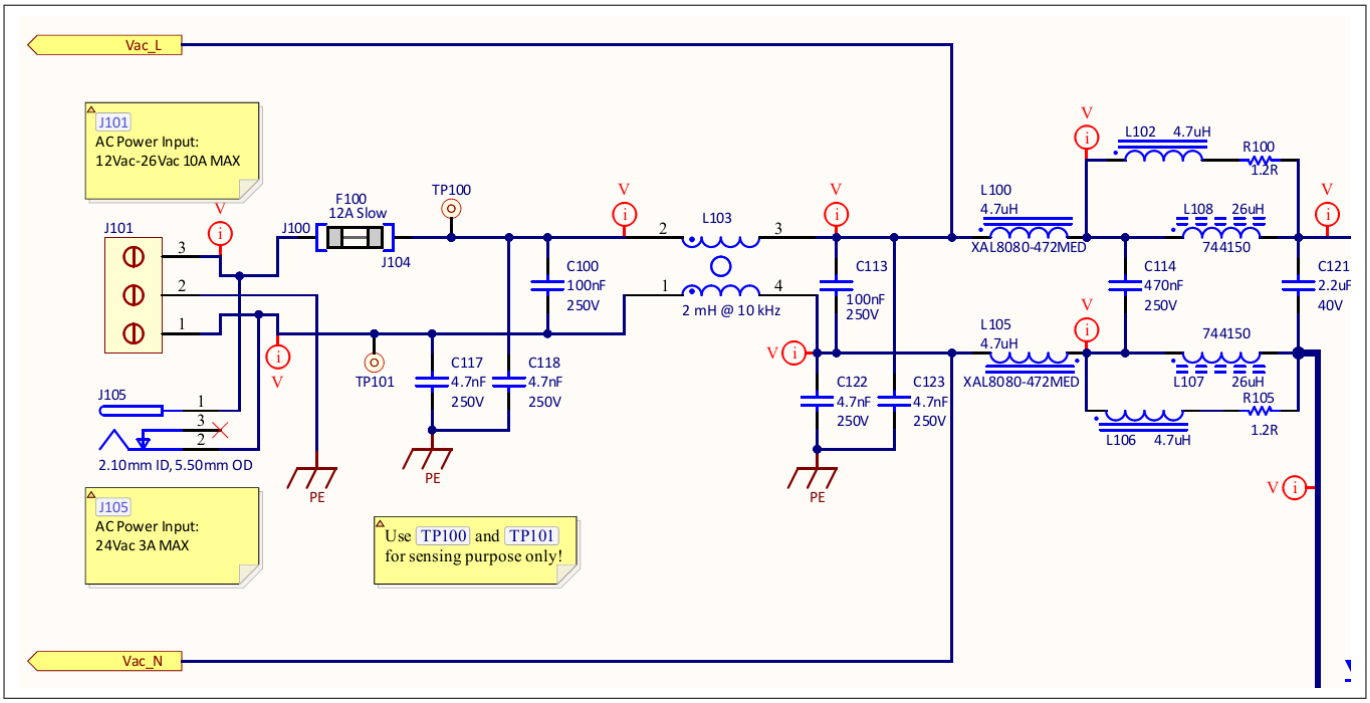


Figure 19 Input stage: AC input and input filter

3.1.3.1 High-frequency and low-frequency power stages

The two high-frequency (HF) phases each consist of:

- A 5 A current sensor
- A 137 µH boost inductor
- An OptiMOS™ Gen 5 BSC117N08NS5 MOSFET (80 V, 49 A nominal at 25 °C, low gate charge) half-bridge

The return path from the bulk capacitor terminates at the low-frequency (LF) half-bridge, where a different OptiMOS™ Gen 5 BSC025N08LS5 MOSFET is used (80 V, 187 A nominal, ultra-low $R_{DS(on)}$).

Both MOSFETs are rated for 80 V, but they differ in nominal continuous drain current and key performance characteristics:

- **HF side**: Selected for low gate charge to reduce switching losses at high frequency
- **LF side**: Selected for very low conduction $R_{DS(on)}$ to reduce conduction losses

These high-current MOSFETs are selected to ensure low thermal stress without heatsinks, enabling a compact board layout. Each transistor is paralleled with an RC snubber to damp voltage ringing during hard-switching transients.

3.1.3.2 Switching node test points

The performance of each switching node can be monitored through test points TP108, TP110, and TP116.

3.1.4 Output stage

The total output capacitance is 4 mF, selected as a trade-off between transient performance and board footprint, and optimized for operation with the provided transformer. The output connector is J103. Use appropriate wires to connect J103 to an external load.

Voltage at the output can be measured using TP112 and TP113; a standard single-ended oscilloscope probe is sufficient.

3.1.4.1 Output current sensing options

Two sensing methods are available for output-current monitoring:

- **Default: Hall-effect current sensor**
  - MCA2101-5-3, gain 230 mV/A
  - Identical to the input-stage sensor
- **Alternative: Shunt-based measurement**
  - Amplified by an operational amplifier
  - Gain 172.5 mV/A

***Note**: Switching from the default option to the shunt-based measurement requires a PCB rework:*

- *Remove R124 and R337 (0 Ω)*
- *Populate R338 (0 Ω)*

This modification does not affect analog routing to the MCU. However, the different gain and voltage offset require adjusting the current-sensing parameters in software.

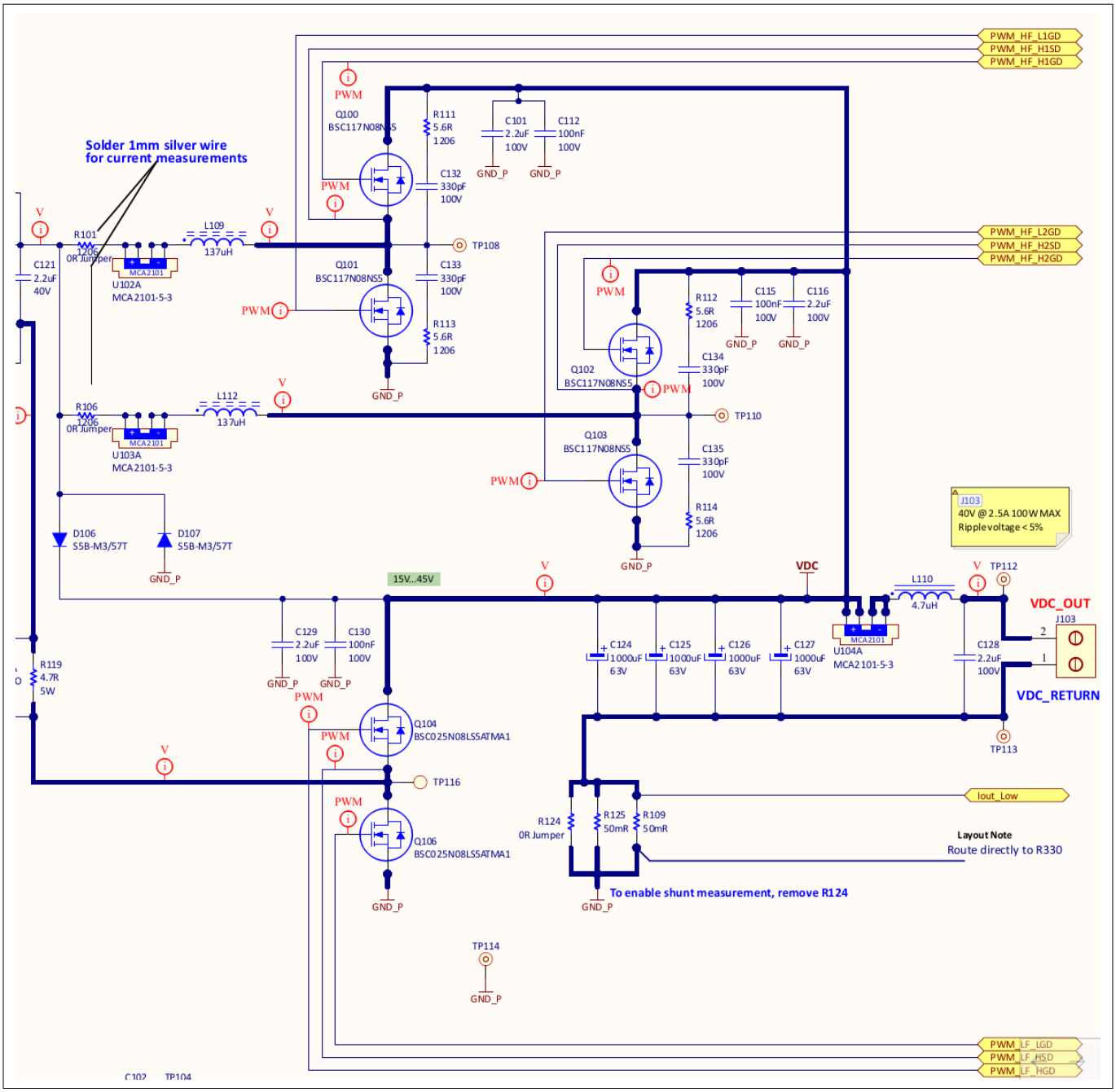


Figure 20 Input stage: High-frequency and low- frequency half bridges and output capacitor

3.1.4.2 Inrush current limiting circuit

At power-up, an inrush-current limiter is required to protect the board components.

In a standard totem-pole PFC topology, current can flow from the AC input to the DC output stage due to the forward conduction of the MOSFET body diodes. This occurs whenever the bulk output capacitors are discharged or when their voltage is below the rectified AC input.

The highest electrical stress on the power components typically occurs during the first power-on event. To reduce the peak inrush current, a 4.7 Ω series resistor (R119) is inserted in the AC-input path.

Once the output bulk capacitors are charged to the nominal level, the resistor must be bypassed to prevent continuous power dissipation and overheating of R119.

A relay is used for this purpose. When activated, it shorts the resistor. The relay coil is driven by the digital signal inrush, which is controlled by the MCU according to a dedicated start-up sequence.

Figure 21 shows the implemented inrush-limiting and bypass circuit.

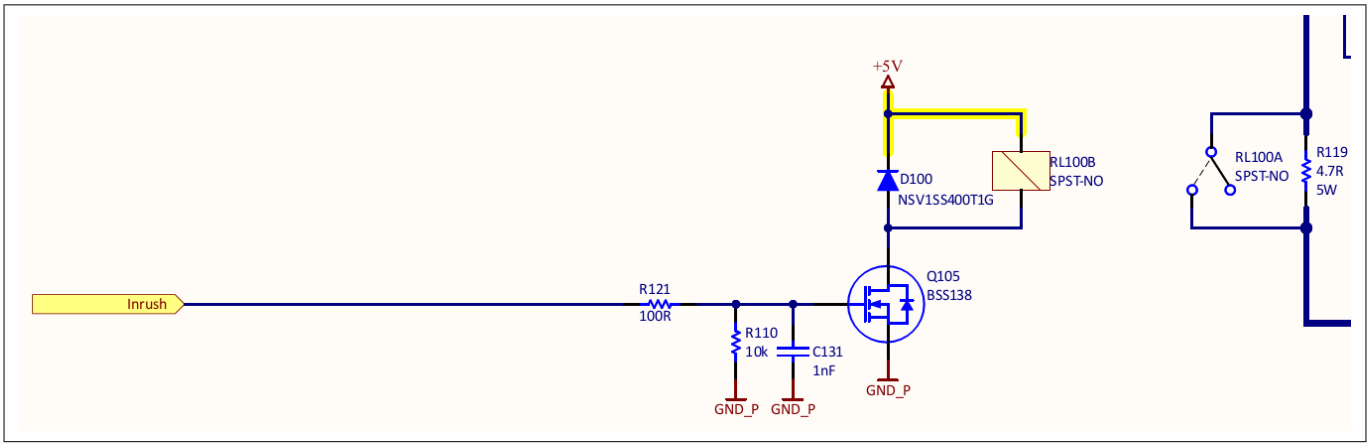


Figure 21 Input stage: Inrush current limiter circuit

3.1.5 Auxiliary supply strategy

The board provides three alternative methods to generate the bias voltages required for the onboard ICs and the control card:

1. **AUX_DC input (J102)**: A barrel jack where an external AC-DC power supply can be connected. A suitable product is suggested in the Introduction section. This method is recommended when:
   - Debugging with no AC input voltage applied
   - Operating without the provided firmware example
   - Learning MCU behavior and the PFC topology starting from a safe low-voltage condition
2. **USB Type-A to Type-C connection (J400)**: This is an alternative to the method based on the AUX_DC input
3. **VDC from the bulk capacitor**: The rectified DC bus obtained from the AC input stage. This source is always available when AC mains are present at the input. This method is intended for normal operation

3.1.5.1 Power sequence

From the selected auxiliary input (1 or 3), the U100 (TLE8366) step-down regulator generates a regulated +5 V rail with a maximum continuous current capability of 2 A.

Attention**: **The maximum input voltage tolerated by U100 is 40 V.

When VDC is used as the source and exceeds the Zener threshold, the protection circuit formed by Q108 (MOSFET), D104 (39 V Zener), R108, and C136 limits the voltage applied to U100.

The RC network provides a controlled turn-on, and the Zener diode clamps the voltage to approximately 39 V, ensuring safe, simple, and effective protection for U100. The +3.3 V rail for the microcontroller is derived from U101 (TLS203B0EJ low-noise LDO), which is supplied by the +5 V rail.

Table 4 Warning note

	*Do not insert the AC barrel jack into the AUX_DC connector, as this results in permanent damage to the board.*

3.1.5.2 Test points

The following test points are provided for monitoring the auxiliary-supply rails:

- **TP102**: Auxiliary input voltage (AUX_DC)
- **TP106**: +5 V rail
- **TP105**: +3.3 V rail

For the detailed schematic of the auxiliary-supply circuitry, see Figure 22 and Figure 23.

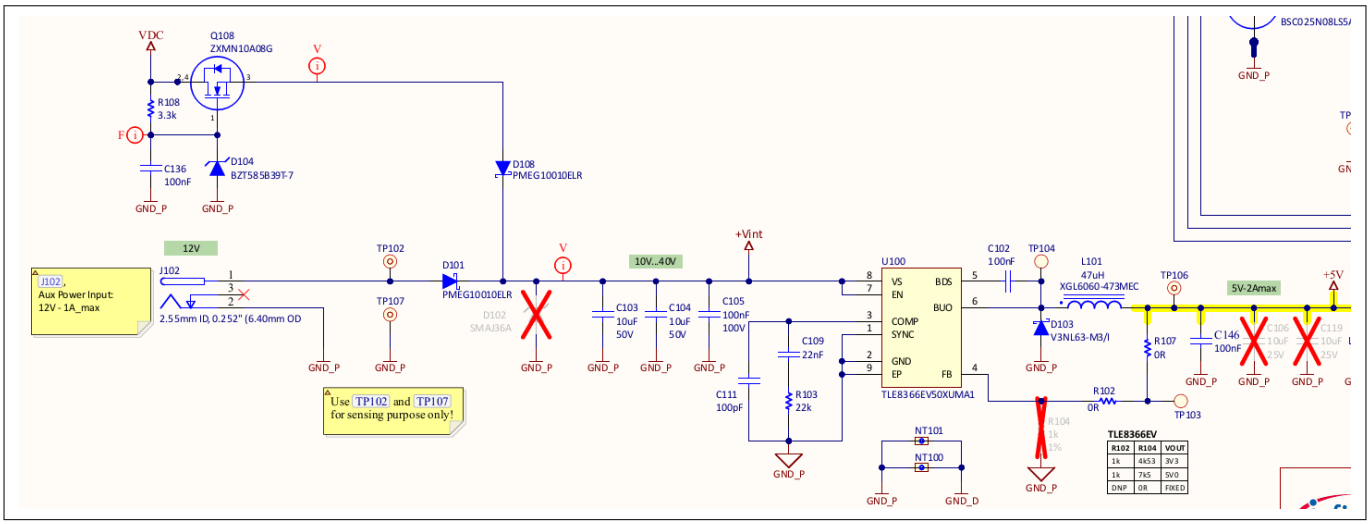


Figure 22 Input stage: Auxiliary supply from VDC to 5 V

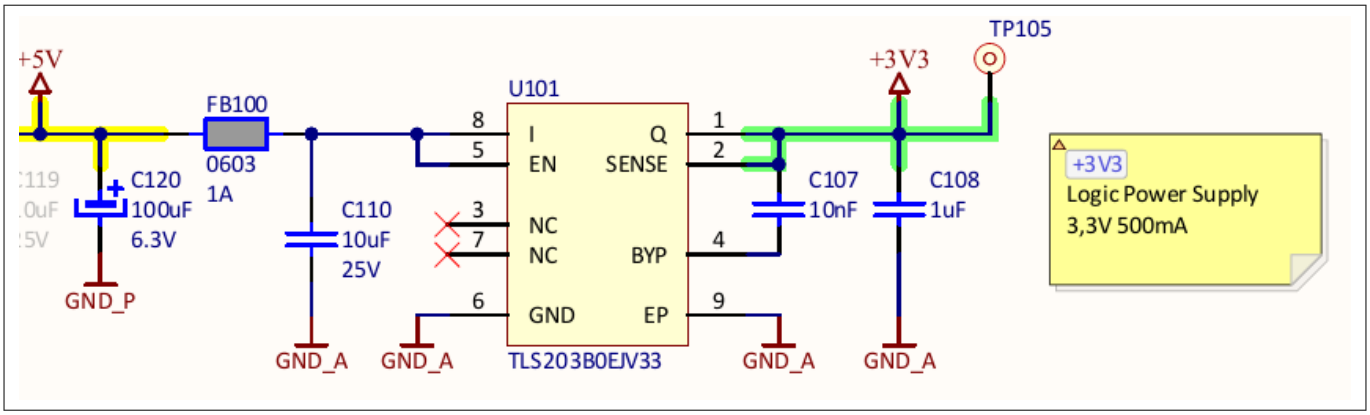


Figure 23 Input stage: Auxiliary supply from 5 V to 3.3 V

3.1.6 Hardware protection circuit

The board is equipped with a hardware-protection circuit that operates independently from the MCU. Its purpose is to prevent permanent damage if an incorrect PWM sequence is generated, for example due to firmware malfunction or incorrect configuration.

Protection functions

Two protection functions are implemented:

1. **Output-voltage protection**:
   - A comparator continuously monitors the VDC bus voltage
   - The signal is scaled down by a gain of 0.055 via a resistive divider

- When the scaled voltage exceeds 3 V (approximately 54.5 V at the bus), the comparator output transitions low
- This event latches a fault condition in hardware

2. **Overcurrent detection (OCD)**:
   - The OCD input is generated by the wired-OR combination of the three current-sensor OC outputs
   - Each current sensor is configured with its OC pin at 0.5 × VCC, corresponding to a trip threshold of approximately 10 A
   - When exceeded, the corresponding sensor pulls its OC pin low, propagating the fault to the combined OCD line

Latch and PWM disable

When a fault is latched, the resulting signal is combined in hardware with the PWM command signals through logic AND gates. As long as the latch is active, all PWM outputs from the MCU (for example, `PWM_C_HF1_H`) are forced low at the gate-driver inputs (U200, U202). This ensures that the power stage remains in a safe state regardless of the MCU output.

Fault indication and reset

The latch status is available to the MCU through the 120-pin connector, enabling software logging or auxiliary actions. If the MCU does not manage the event, a red LED (D201) turns on when a fault occurs. A manual reset is provided through the SW200 push-button.

- On activation, the latch is cleared
- For OCD events, the circuit also triggers the current sensors built-in reset procedure according to the manufacturer specifications

Table 5 Warning note

	*To get the board running, the OCD_RESET pin on the MCU side must be configured as Open Drain, Drives Low, Input Buffer Off, with the initial value set to High.*

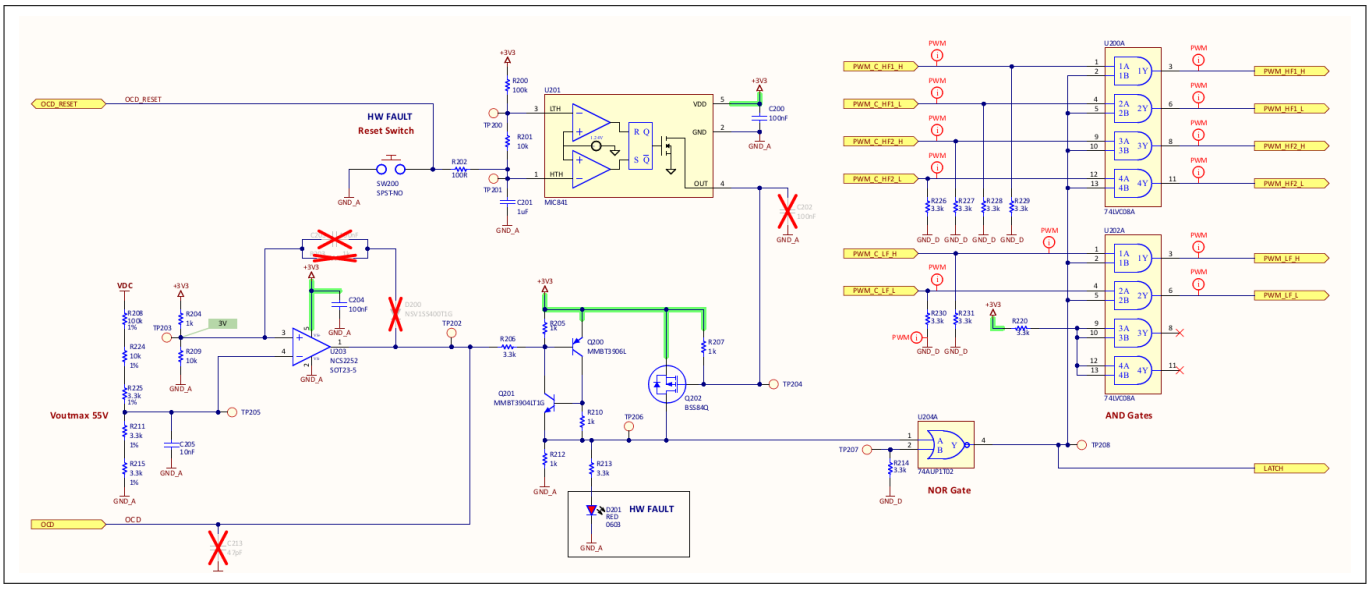


Figure 24 Protection: Detection and reset circuits

3.1.7 Controller

The MCU, as introduced in the Kit contents section, is not included in the KIT_PSC3_PFC1 kit contents. The evaluation board includes a 120-pin connector (J300, HTEC8-160-01-L-DV-A-BL). The KIT_PSC3Mx_CC1 control-card board can be easily plugged into this connector to establish the required digital and analog connections.

Table 6 lists the 120-pin connector pinout details. The table also includes the control-card pin-assignment information. Although the MCU is not part of the evaluation board, a dedicated MCU column is included to make it easier to learn and debug. These limitations can be resolved through PCB rework by de-soldering 0 Ω resistors and re-soldering them to establish the required connections.

Table 6 120-pin connector pinout details

Pin number	Low-Voltage PFC board	KIT_PSC3M5_CC 1	KIT_PSC3M5_CC 1	Low-Voltage PFC board	Pin number
1	-	+3V3	XRES	-	2
3	-	-	P3.0	FAULT_LED	4
5	MASTER_OUT_11	P4.4	P3.1	uBus_INT	6
7	MASTER_OUT_13	P4.5	P9.4	USER_BUTTON	8
9	GND_D	GND	5V0_IN	+5 V	10
11	MASTER_OUT_15	P4.6	-	-	12
13	MASTER_OUT_17	P4.7	P9.0	INRUSH	14
15	uBus_SCL	P7.0	P9.1	ZCD_PH1(*)	16
17	uBus_SDA	P7.1	P9.2	ZCD_PH2(*)	18
19	MASTER_OUT_	P7.2	P9.3	USER_LED	20
21	MASTER_OUT_	P7.3	P9.5(**)	-	22
23	GND_D	GND	5V0_IN	+5 V	24
25	PWM_C_HF1_H	P4.0	-	-	26
27	PWM_C_HF1_L	P4.1	P0.0/ WCO_OUT(**)	-	28
29	PWM_C_HF2_H	P4.2	P0.1/WCO_IN(**)	-	30
31	PWM_C_HF2_L	P4.3	P1.0/ECO_IN(**)	-	32
33	PWM_C_LF_H	P7.4	P1.1/ ECO_OUT(**)	-	34
35	PWM_C_LF_L	P7.5	-	-	36
37	GND_D	GND	5V0_IN	+5 V	38
39	#39	P7.6	-	-	40
41	OCD_RESET	P7.7	P2.2	uBus_MOSI/CLK	42
43	-	-	P2.3	uBus_MISO/MOSI	44
45	uBus_PWM	P6.0	P5.0/SDA(**)	-	46
47	uBus_RST	P6.1	P5.1/SCL(**)	-	48
49	CAN_RX	P6.2	P3.2	UART2_TX	50

(table continues...)

Table 6 (continued) 120-pin connector pinout details

Pin number	Low-Voltage PFC board	KIT_PSC3M5_CC 1	KIT_PSC3M5_CC 1	Low-Voltage PFC board	Pin number
51	CAN_TX	P6.3	P3.3	UART2_RX	52
53			P5.2/ UART_RX(**)	uBus_TX	54
55	GND_D	GND	P5.3/ UART_TX(**)	uBus_RX	56
57	MASTER_OUT_23	P8.0	P8.4	LATCH	58
59	MASTER_OUT_24	P8.1	P8.5	#60	60
61	OCD	P8.2	-	-	62
63	VAC_PLRTY	P8.3	-	-	64
65	MASTER_OUT_1	AN_A0	VDDA_C		66
67	MASTER_OUT_3	AN_A1	AN_A7	MASTER_OUT_2	68
69	MASTER_OUT_5	AN_A5	AN_A6	MASTER_OUT_4	70
71	MASTER_OUT_7	AN_A3	AN_B4	MASTER_OUT_6	72
73	GND_A	AGND	AGND	GND_A	74
75	CS_PH2_Sense	AN_A4	AN_B5	MASTER_OUT_8	76
77		VAREF_EXT_C	AN_B2	Vac_Sense	78
79	CS_PH1_Sense	AN_A2	AN_B3	Iout_Sense	80
81	VDC_Sense	AN_B0	AN_B6	POT	82
83	12V_AUX_Sense	AN_B1	AN_B7	NTC	84
85	-	-	-	-	86
87	GND_A	AGND	AGND	GND_A	88
89	-	-	-	-	90
91	-	-	-	-	92
93	-	-	-	-	94
95	-	-	-	-	96
97	-	-	-	-	98
99	-	-	-	-	100
101	-	-	-	-	102
103	-	-	-	-	104
105	-	-	-	-	106
107	-	-	-	-	108
109	-	-	-	-	110
111	-	-	GND	GND_A	112

(table continues...)

Table 6 (continued) 120-pin connector pinout details

Pin number	Low-Voltage PFC board	KIT_PSC3M5_CC1	KIT_PSC3M5_CC1	Low-Voltage PFC board	Pin number
113	GND_A	GND	P2.0/TDI	uBus_CS	114
115	-	P1.2/TCK(**)	P2.1/TDO	#116	116
117	-	P1.3/TMS(**)	VBACKUP_C	-	118
119	-	+3V3	+3V3	-	120

(*): ZCD_PH1 and ZCD_PH2 are placeholders for future use and are not used on the LV PFC REV20 board.

(**): MCU pins have defined functionality on the control card. Therefore, these pins are not exposed to the 120-pin connector by default. To enable them for use on J300, a KIT_PSC3M5_CC1 PCB rework is required. For more information, see the Control Card user guide.

3.1.8 Analog sensing

3.1.8.1 AC voltage sensing

Input voltage is measured using the operational amplifier U300, configured with an inverting gain and a DC offset set to half of the +3V3 voltage. Figure 25 shows the corresponding hardware implementation.

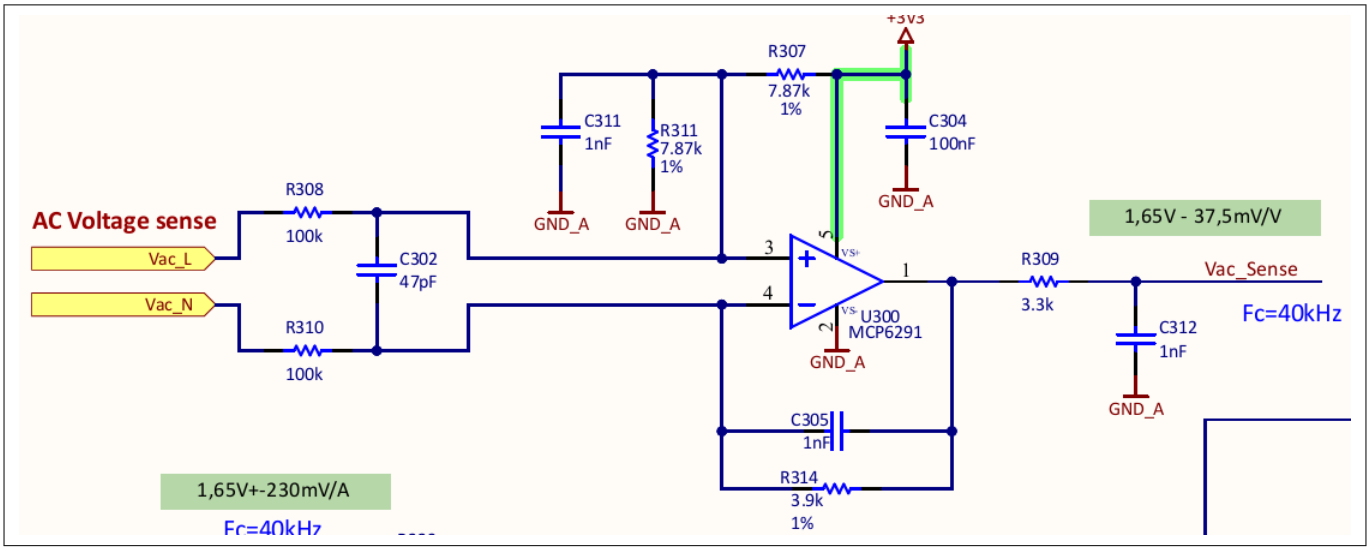


Figure 25 AC input voltage sensing

3.1.8.2 DC output voltage sensing

A simple voltage divider is used for this measurement, and Figure 26 shows the corresponding hardware implementation.

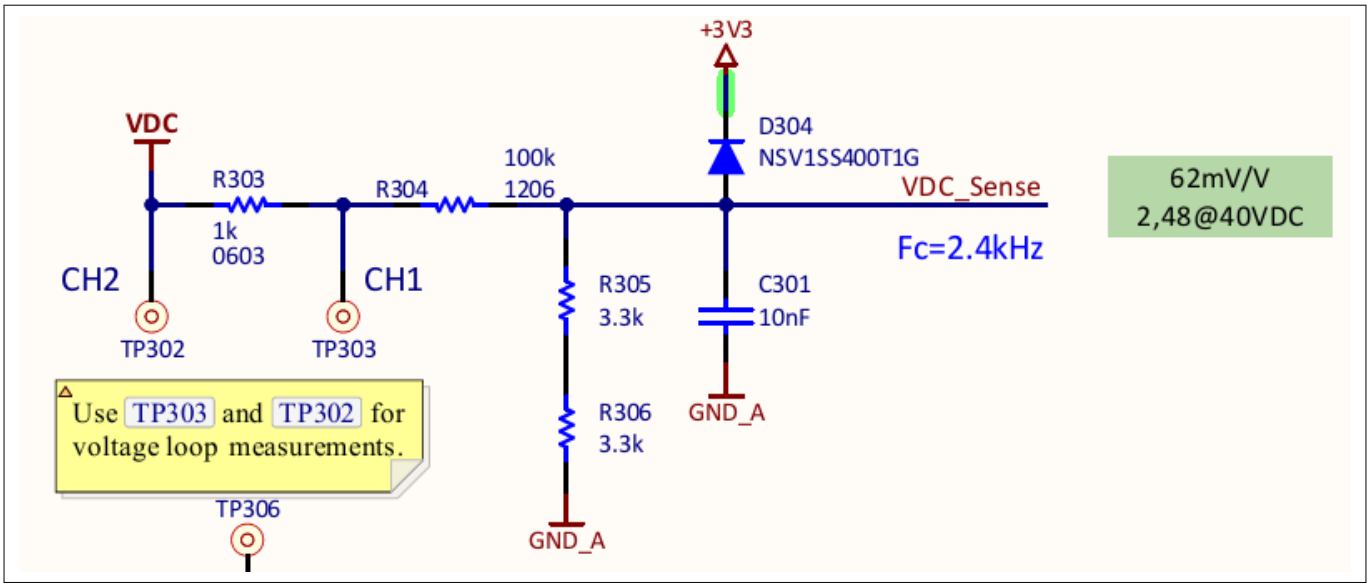


Figure 26 DC output voltage sensing

3.1.8.3 Auxiliary supply voltage sensing

Since the 12 V rail is generated from the 5 V supply, an additional analog input on this rail is included to monitor the auxiliary-voltage status. The analog quantity routed to the MCU is produced by a voltage divider, as shown in Figure 27.

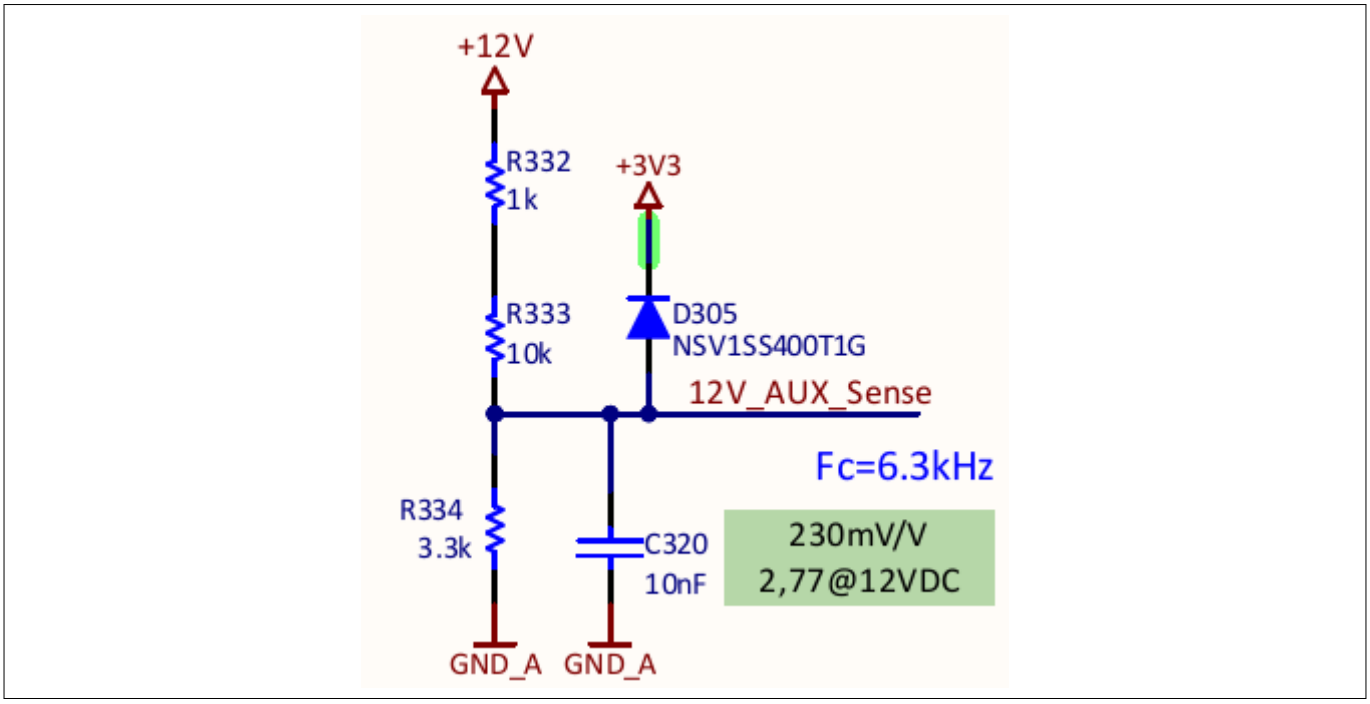


Figure 27 Auxiliary supply voltage sensing

3.1.8.4 Current sensing

The output current and the phase current flowing through the inductors are measured by the MCA2101-5-3 sensor. Figure 28 shows one of the three sensors used in the design. The sensing section is shown in the input

stage with the IC designator U104A, while the low-current and low-voltage side of the circuit is shown below with the designator U104B.

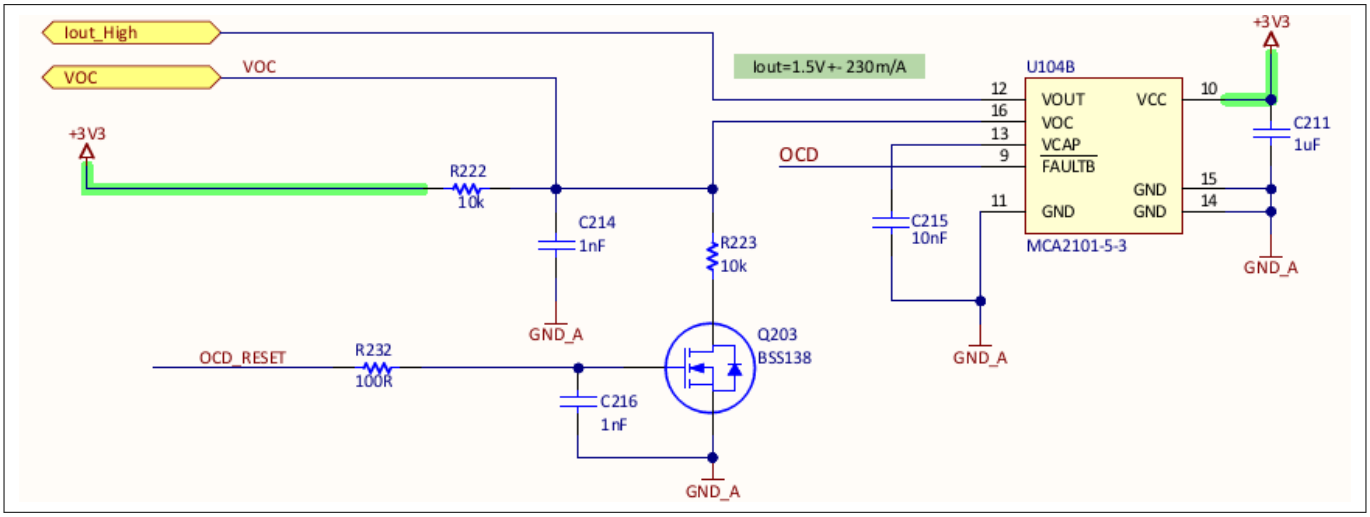


Figure 28 Current-sensor circuit used in the design

3.1.8.5 Temperature sensing

A Negative Thermocouple (NTC) is added to the circuit and is located between the output capacitor and the phase-1 half-bridge. As the temperature increases, the resistance of the sensing element decreases, which lowers the input voltage applied to the MCU pin. Figure 29 shows the implemented circuit. The nominal resistance at 25°C is 10 kΩ.

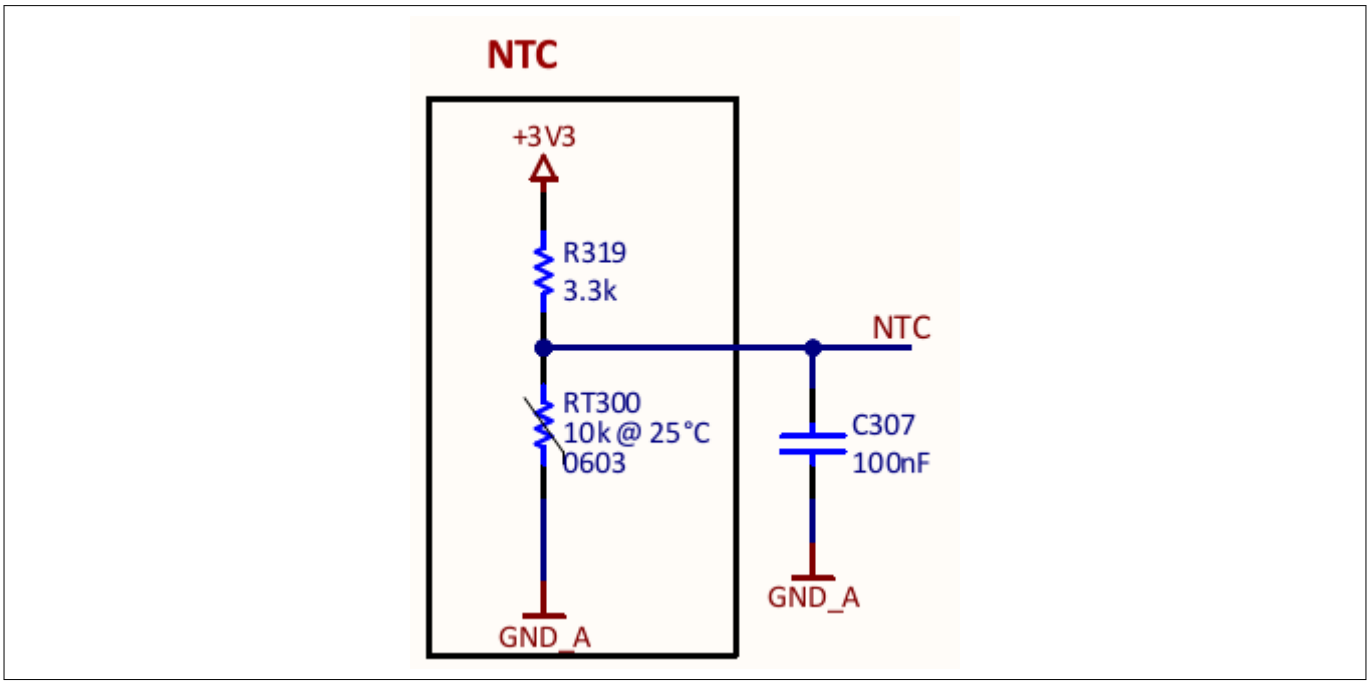


Figure 29 Temperature sensor circuit

Table 7 Analog sensing gain

Parameter	Voltage offset	Gain	Test point	Values		
				Min.	Nominal.	Max.
AC voltage sensing	1.65 V	–37.5 mV/V	J303.15	–44 Vpk	-	+44 Vpk
DC voltage sensing	0 V	62 mV/V	J303.21	0 V	-	53.2 V
Auxiliary supply voltage sensing	0 V	230 mV/V	J302.5		12 V	-
Current sensing (MCA2101-5-3)	1.5 V	230 mV/A	J303.16 (OUT) J303.19 (PH2) J303.20 (PH1)	–5 A	-	+5 A
Current sensing (Alternative)	1.65 V	172.5 mV/A	J303.16 (OUT)	–9.5 A	-	+9.5 A
Temperature sensing	0 V	-	J303.18	-	2,48 V at 25°C	0.2 V at 120°C
Potentiometer (HMI)	0 V	Volt divider	J303.17	0	1,65 V at default	3.3 V

3.1.9 LEDs

Table 8 summarizes the functions of the LEDs available on the board.

Table 8 LED functionality

LED	Designator	Color	Function
INRUSH	D201	Red	Normally ON at power-up. Indicates that the inrush resistor R119 is still engaged. Turns OFF when the MCU drives the *INRUSH* pin.
HW FAULT	D300	Red	Normally OFF. Turns ON when a hardware-failure protection event is detected.
PWR ON	D303	Green	Turns ON when the +3V3 supply is generated. This also implies that the +5 V rail is correctly generated.
USER LED	D301	Green	MCU-driven LED. The user can define when to turn it ON. It turns ON when the MCU pin is set High. A possible usage is to signal that the output voltage is within regulation limits or to blink the LED when the power stage is actively modulating.
SW FAULT	D302	Red	MCU-driven LED. The user can define when to turn it ON. It turns ON when the MCU pin is set High. A possible usage is to signal an abnormal condition detected by the firmware, such as a wrong sensor offset.
UART1 Heart Bit	D402	Green	Driven by U401 when UART1 communication is active.
UART2 Heart Bit	D401	Green	Driven by U401 when UART2 communication is active.

3.1.10 User button

The Low-Voltage PFC evaluation board has one user button, SW300, connected to pin 8 on J300. This general-purpose button allows the user to interact with the hardware. Its normal state is HIGH, and it transitions to LOW when external pressure is applied.

3.1.11 Master–slave configuration

The Low-Voltage PFC evaluation board can be connected to a second evaluation board using a 24-pin ribbon cable to create a master-slave configuration controlled by a single digital power control card. To enable this connection, connect the master connector J302 on the LV PFC board (where the control card is installed) to the slave connector on the chained evaluation board. The master and slave connectors carry only ADC, PWM, and GPIO signals.

When two evaluation boards are connected in daisy-chain mode using a 24-pin ribbon cable, the power interconnection must be completed according to the requirements of the slave board. For example, the output voltage of the PFC must be connected to the input voltage of the chained board. If the master and slave connection is not required, these connectors still provide useful access points to MCU pins in addition to the test-point connector J303. By using jumper wires, you can probe both digital and analog signals.

3.1.12 Test point connector

J303 is added to the board to give the user an easy way to probe, with single-ended oscilloscope probes, the analog and digital signals used for driving a totem-pole PFC. By default, J303 is not populated with a connector, leaving only the vias exposed. Oscilloscope probe tips can be inserted directly into these vias to simplify measurement.

To simplify the grounding scheme, crocodile-clip-friendly ground areas are provided next to the J303 location. For more information on the available signals. see Test points.

3.1.13 Connection to network analyzer

It is possible to analyze the frequency response of the control loop by injecting a variable-frequency signal into a small shunt resistor using an external network analyzer. This tool is used to determine the bandwidth and phase margin of the Low-Voltage PFC converter.

The evaluation board includes the following test points for frequency-response measurements:

- TP302 and TP303, placed across resistor R303, for output-voltage frequency-response determination
- TP300 and TP301, placed across resistor R302, for current-loop frequency-response determination (available only on phase 1)

3.1.14 Communication interfaces

Multiple interfaces are provided to support the development of custom protocols for exchanging information with the MCU.

3.1.14.1 Serial communication interface

The board includes a USB-to-dual-UART bridge (Cypress CY7C65215) that provides multiple communication interfaces between the MCU and an external host, such as a PC. When connected to a computer, this device enumerates as two virtual COM ports. The purpose of offering two independent channels is to support the parallel implementation of different communication protocols.

These two independent channels include:

- **Low-frequency channel**: Intended for slow-rate monitoring protocols, such as exchanging configuration commands, reading fault or status registers, or retrieving low-frequency variables
- **High-frequency channel**: Suitable for streaming internal algorithm variables at high data rates, enabling a virtual-oscilloscope functionality

These examples illustrate representative use cases. Protocols can be defined and implemented according to application requirements.

Connection

Use a USB cable (Type-A to Type-C) to connect the PC to connector J400 on the board. When the USB cable is plugged in, 5 V is supplied to the board, the LDO turns on and generates the 3V3 rail, and the D303 PWR_ON LED illuminates. During serial communication, the green LEDs (D401) and (D402) glow.

***Note**: The USB cable is not supplied with the kit and must be purchased separately.*

For the hardware-implementation diagram, see Figure 30.

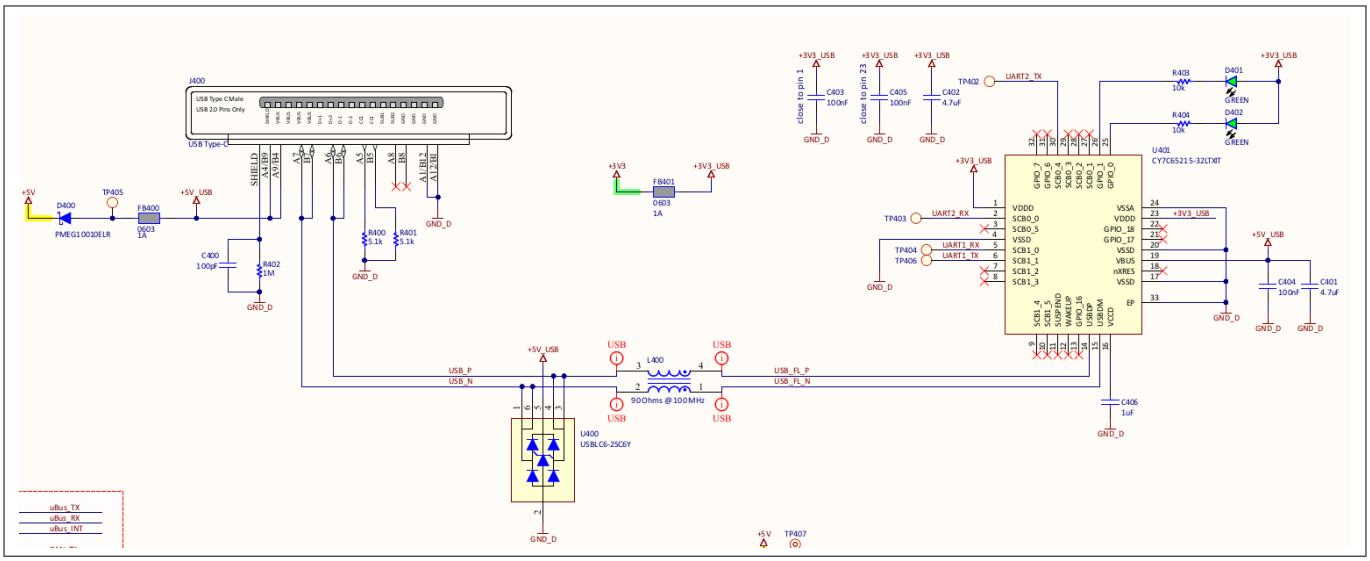


Figure 30 Serial communication interface: USB-to-dual-UART bridge

Dual USB-UART bridge configuration

The U401 device (Cypress CY7C65215 dual-port USB bridge) converts the USB connection into two independent UART interfaces for the MCU. Custom baud rates can be defined by configuring the associated serial communication block (SCB) within the Device Configurator under the baud rate property.

Routing and Port selection:

- **UART2**: Routed directly to the 120-pin connector
- **UART1**: Routed through the SW301 switch block. This configuration allows the same SCB instance to be re-purposed in one of the following ways:
  - As a UART interface connected to the USB bridge
  - As an SPI interface available on the mikroBUS connector (SK400), which requires additional configuration depending on the control card in use

Table 9 provides the SCB-mapping configuration associated with SW301.

Table 9 SW301 options

Mapping configuration	Position			
	1	2	3	4
Not connected	OFF	OFF	OFF	OFF
UART1	OFF	ON	ON	OFF
uBus_SPI	ON	OFF	OFF	ON

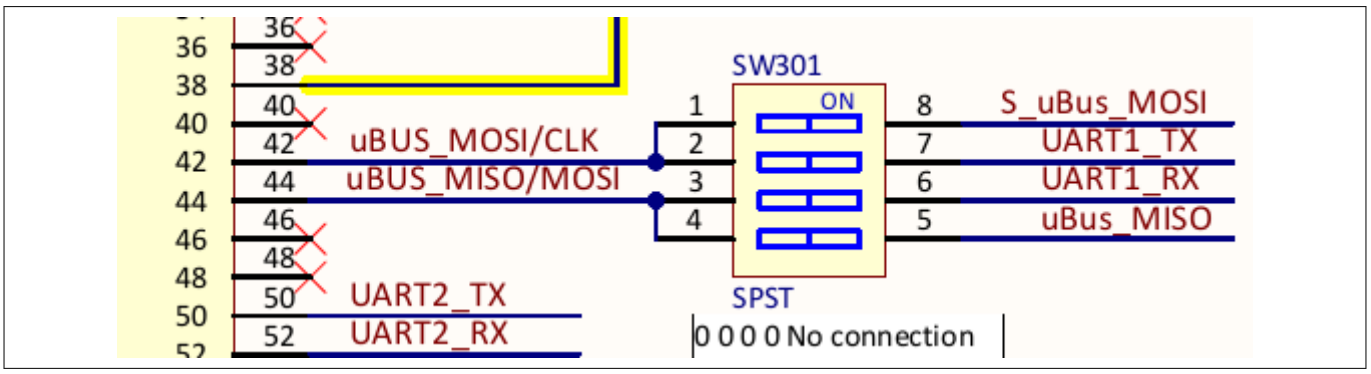


Figure 31 UART routing to the 120-pin connector

3.1.14.2 CAN interface

If an existing CAN slave stack is available and needs to be ported and tested on the PSOC™ Control MCU, the evaluation board supports a CAN interface through connector J401.

Table 10 CAN interface functionality

J401	Functionality
1	CANH
2	GND
3	CANL

A direct connection to the 120-pin connector is provided by using a dedicated SCB.

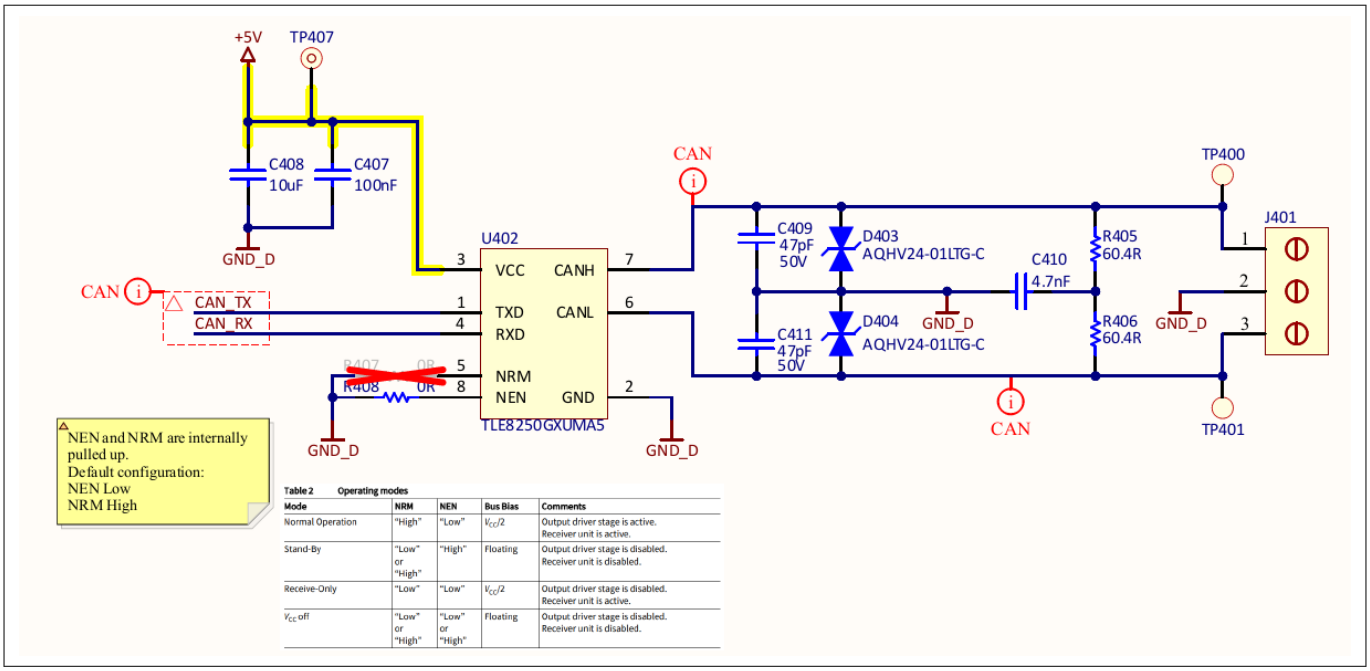


Figure 32 CAN schematic

3.1.14.3 mikroBUS expansion connector

The board is equipped with a mikroBUS connector (SK400) to extend the system capabilities by adding third-party Click boards. This widely used form factor enables easy integration of peripherals such as displays, communication modules, and sensors.

***Note**: No firmware example is provided for mikroBUS peripherals. Custom application code must be developed as required.*

For the pinout details of the mikroBUS interface connector, see Figure 33.

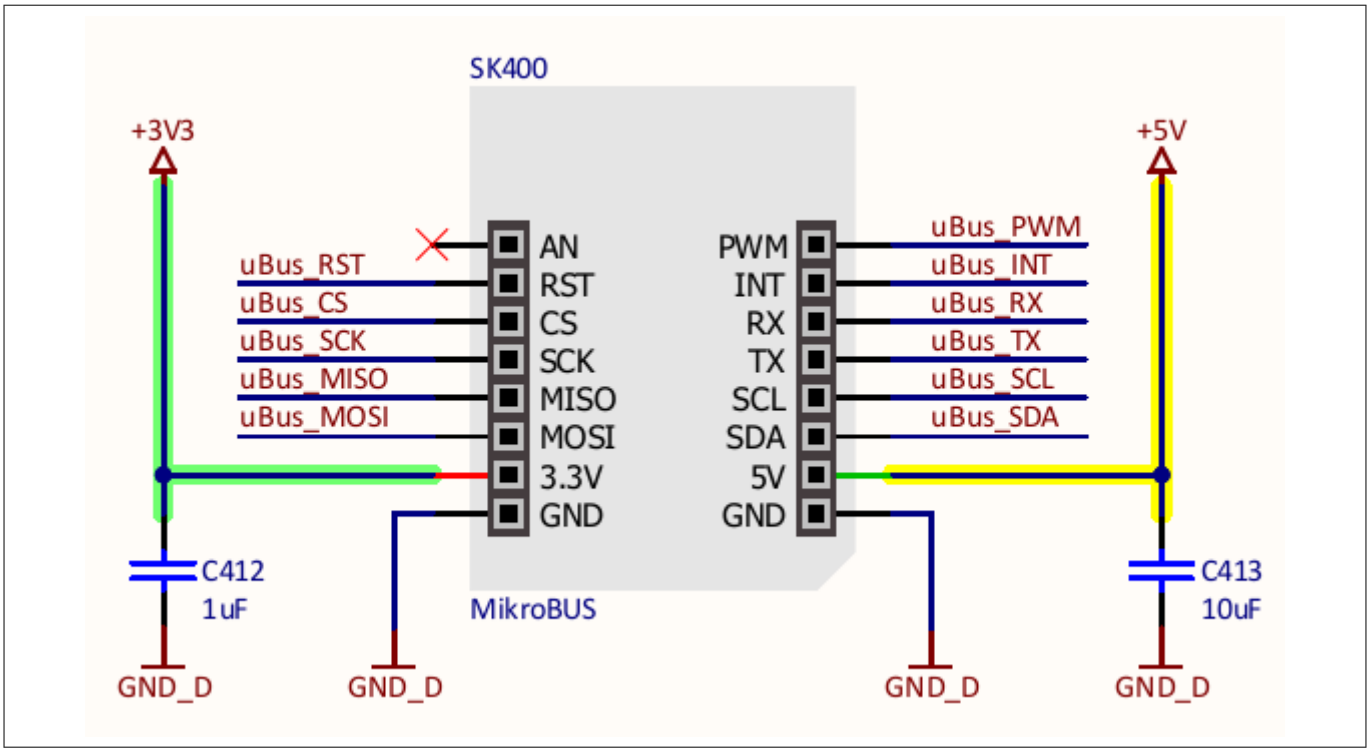


Figure 33 mikroBUS connector

SK400 exposes multiple resources, including I²C, SPI, and GPIOs. Some of these signals, although physically routed to the 120-pin connector, may not be connected on the control card side. See Table 6 to verify whether a PCB rework on the control card is required.

***Notes**:*

1. *Control cards assign certain pins to local functions, which prevents these pins from being exposed on the 120-pin connector. However, 0 Ω resistors are provided to repurpose these pins from local use on the control card to external availability on the 120-pin connector through a PCB rework*
2. *To use I²C correctly on SK400, the default pin initialization in the Device Configurator must be updated. When selecting the I²C protocol, change the SDA and SCK pin settings from Open Drain to Resistive pull-up*

Jumper wires (not supplied) may be connected to these pins for development or test purposes. Most mikroBUS pins are directly connected to the 120-pin connector, with the exception of the SPI signals.

SPI/UART1 shared SCB

As described in the Serial communication interface section, the mikroBUS SPI interface shares the same SCB instance used for UART1 (USB-UART bridge). Therefore, SPI and UART1 cannot operate simultaneously. The selection between these two functions is controlled through SW301.

Table 11 SW301 options

Mapping configuration	Position			
	1	**2**	**3**	**4**
Not connected	OFF	OFF	OFF	OFF
UART1	OFF	ON	ON	OFF
uBus_SPI	ON	OFF	OFF	ON

SW302 configuration

SW302 is a slider switch. Its function is to connect one terminal to one of two possible terminations depending on the slider position. It handles two terminals. The purpose of this switch is to repurpose selected 120-pin connections when the recommended control card, KIT_PSC3M5_CC1, is replaced with future products.

Table 12 SW302 configuration

Control card	Slider position	120-pin connector function
KIT_PSC3M8_CC1	1-2 4-5	J300.42 → uBUS_SCK J300.116 → uBUS_MOSI
KIT_PSC3M5_CC1	3-1 6-5	J300.42 → uBUS_MOSI J300.116 → uBUS_SCK

3.1.15 Gate driver

The logic-level PWM signals generated by the MCU are translated into gate-drive signals by the three onboard 2EDL8124 junction-isolated gate drivers (U502, U504, U505), one per half-bridge. The gate drivers require a 12 V supply. This is generated from the 5 V input by a boost converter (U500), as shown in Figure 34.

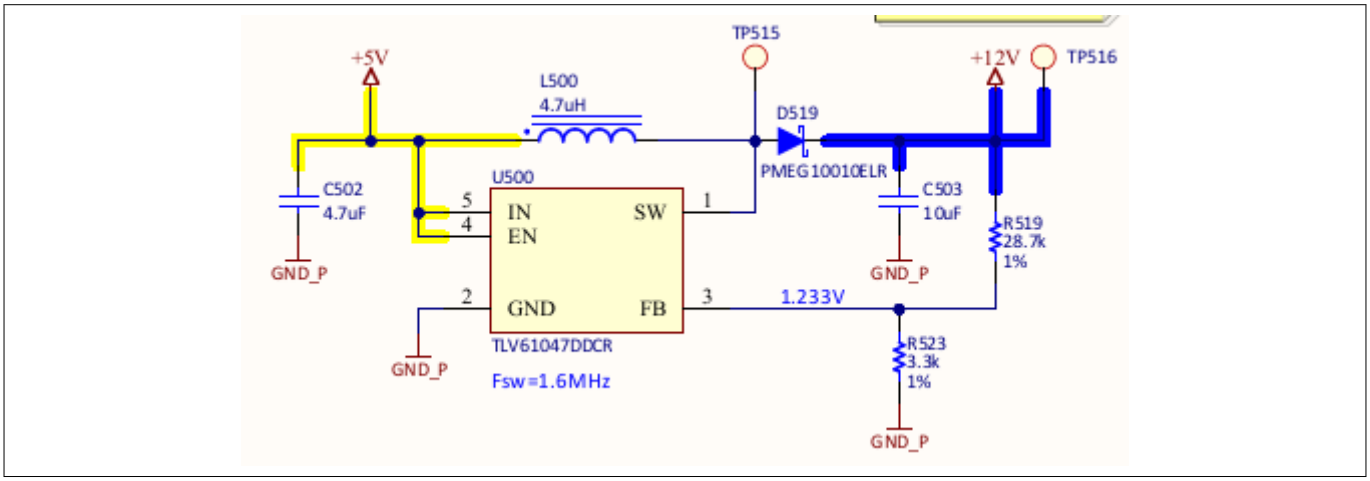


Figure 34 Gate driver supply voltage generation

In a standard configuration, a bootstrap capacitor is used to supply the high-side driver section. However, this method limits the maximum duty cycle and may lead to missed commutation pulses when the AC input is abnormal or during extended on-time.

To avoid these limitations, the board uses a small isolated auxiliary power supply for each high-side. This auxiliary supply consists of:

- An open-loop push-pull IC (U501) operating at approximately 420 kHz, shared across all phases
- A dedicated gate-drive transformer for each phase
- A Zener diode to clamp the gate-supply voltage below 13 V

The bootstrap-voltage-rail generation diagram illustrates this architecture.

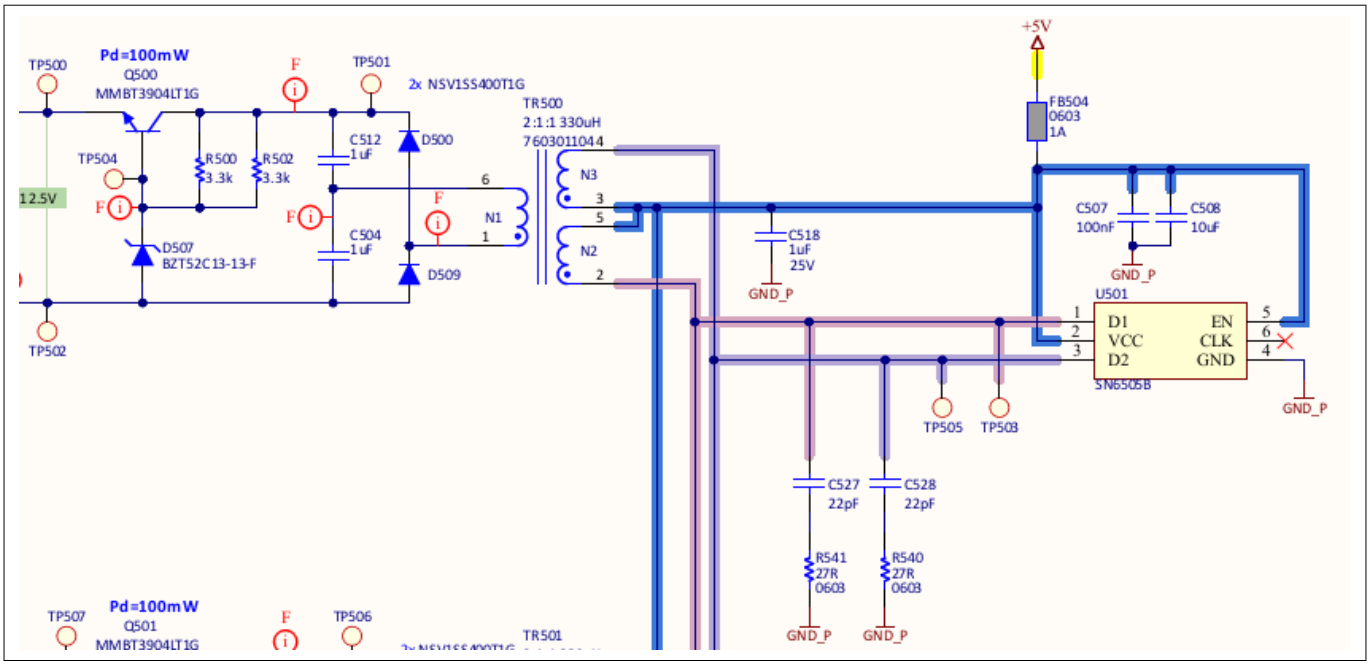


Figure 35 Bootstrap-voltage-rail generation

The following figure shows the complete gate-driver circuit for one half-bridge. This stage is repeated three times, once for each half-bridge (HF1, HF2, and LF). Multiple test points are provided to monitor the different nodes in the gate-driver stage.

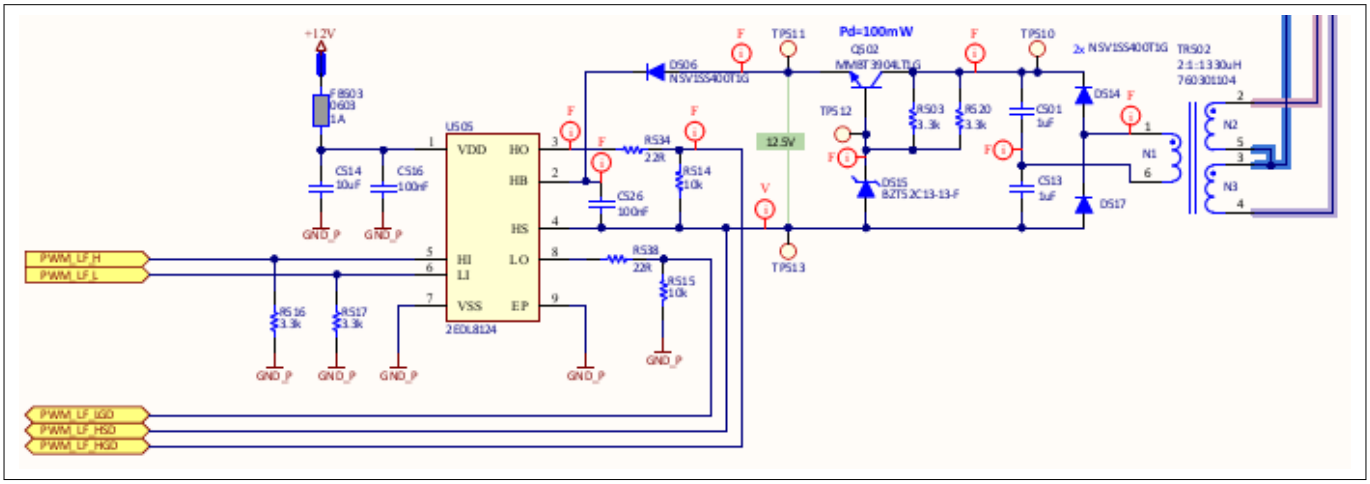


Figure 36 Gate driver circuit (x3, one per each half-bridge)

Table 13 Warning note

	The nominal 12.5 V bootstrap voltage must be measured using an isolated differential probe or an isolated multimeter. Measurement points include: • ***HF phase 1**: TP500, TP502* • ***HF phase 2**: TP507, TP509* • ***LF phase**: TP511, TP513* *Do not use single-ended probes. Using a single-ended probe may create a short circuit to ground due to the floating reference of the bootstrap circuit.*

3.1.16 Test point overview

Table 14 shows a comprehensive list of all test points on the board.

For compactness, the following abbreviations are used:

- **TP**: Test Point
- **DP**: Differential probe
- **SE**: Single-ended probe
- **GD**: Gate driver
- **PH**: High-frequency leg
- **LF**: Low-frequency leg

Table 14 Test points overview

Test points	Circuit	Description	Remarks
GND_A	-	Analog ground plane	TP to be referred to suggested ground plane for best accuracy. All GND tied together
GND_D	-	Digital ground plane	
GND_P	-	Power ground plane	
TP100	Input stage	AC voltage input line	DP 1
TP101	Input stage	AC voltage input neutral	DP 1
TP102	Input stage	External auxiliary supply voltage (+)	SE at GND_P
TP107		Power ground	-
TP106	Aux supply	+5 V voltage rail (+)	SE at GND_P
TP105	Aux supply	+3V3 voltage rail (+)	SE at GND_A
TP104	Aux supply	Buck switch regulator output	SE at GND_P
TP103	Aux supply	Buck switch regulator feedback input	SE at GND_P
TP108	Boost stage	High-frequency PH1 switching node	SE at GND_P
TP114		Power ground	-
TP110	Boost stage	High-frequency PH2 switching node	SE at GND_P
TP112	Boost stage	PFC DC Output voltage (+)	SE at GND_P
TP113	Boost stage	PFC DC Output voltage (-)	SE at GND_P
TP116	Boost stage	Low-frequency switching node	SE at GND_P
TP205	Protection	Output voltage protection circuit, comparator input (-)	SE at GND_A
TP203	Protection	Output voltage protection circuit, comparator input (+)	SE at GND_A
TP202	Protection	Combined protection output	SE at GND_A
TP204	Protection	Output of hysteretic comparator for resetting the latch	SE at GND_A

(table continues...)

Table 14 (continued) Test points overview

Test points	Circuit	Description	Remarks
TP206	Protection	Latched output	SE at GND_A
TP200	Protection	Low voltage threshold for comparator (for latch reset)	SE at GND_A
TP201	Protection	High voltage threshold for comparator (for latch reset)	SE at GND_A
TP208	Protection	Output protection status	SE at GND_D
TP207	Protection	Pulled down to digital ground	SE at GND_D
TP302 – TP303	Loop response	Voltage loop bandwidth test (signal)	SE at GND_A
TP306	Loop response	Analog Ground	Close to signal
TP300 – TP301	Loop response	Current loop bandwidth measurement (signals)	SE at GND_A
TP304 – TP305	Not connected	For future development	-
TP400	Communication	CAN High	SE at GND_D
TP401	Communication	CAN Low	SE at GND_D
TP403	Communication	UART 2 Receive	SE at GND_D
TP402	Communication	UART 2 Transmit	SE at GND_D
TP404	Communication	UART 1 Receive	SE at GND_D
TP406	Communication	UART 1 Transmit	SE at GND_D
TP405	Communication	USB supply voltage	SE at GND_D
TP407	Communication	CAN supply voltage	SE at GND_D
TP503	GD supply	Switching node	SE at GND_P
TP505	GD supply	Complementary switching node	SE at GND_P
TP501	GD supply	PH1: Rectified voltage	DP 2
TP500	GD supply	PH1: Isolated supply voltage (+)	DP 2
TP502	GD supply	PH1: Reference isolated supply voltage (-)	DP 2
TP504	GD supply	PH1: Isolated voltage clamp	DP 2
TP506	GD supply	PH2: Rectified voltage	DP 3
TP507	GD supply	PH2: Isolated supply voltage (+)	DP 3
TP509	GD supply	PH2: Reference isolated supply voltage (-)	DP 3
TP508	GD supply	PH2: Isolated voltage clamp	DP 3
TP510	GD supply	LF: Rectified voltage	DP 4
TP511	GD supply	LF: Isolated supply voltage (+)	DP 4

(table continues...)

Table 14 (continued) Test points overview

Test points	Circuit	Description	Remarks
TP513	GD supply	LF: Reference isolated supply voltage (-)	DP 4
TP512	GD supply	LF: Isolated voltage clamp	DP 4
TP515	GD supply	Boost converter switching node	SE at GND_P
TP516	GD supply	Gate driver supply voltage	SE at GND_P
OCD	J303	Combined overcurrent detection	SE at GND_A
PLRTY	J303	AC polarity digital signal	SE at GND_A
DAC0	J303	MCU generated voltage (not supported by KIT_PSC3M5_CC1)	SE at GND_A
DAC1	J303	MCU generated voltage (not supported by KIT_PSC3M5_CC1)	SE at GND_A
VDC	J303	MCU analog input: PFC out voltage	SE at GND_A
CS/PH1	J303	MCU analog input: PH1 current sense	SE at GND_A
CS/PH2	J303	MCU analog input: PH2 current sense	SE at GND_A
NTC	J303	MCU analog input: Power stage temp	SE at GND_A
POT	J303	MCU analog input: Potentiometer	SE at GND_A
#60	J303	MCU digital: Available debug pin	SE at GND_D
OCD_R	J303	MCU digital: Monitoring reset over current	SE at GND_D
#39	J303	MCU digital: Available debug pin	SE at GND_D
LATCH	J303	MCU digital: Monitoring fault protection events	SE at GND_D
BUTTON	J303	MCU digital: Monitoring on board press button	SE at GND_D
LF/L	J303	MCU digital: MCU PWM command for LF low-switch	SE at GND_D
LF/H	J303	MCU digital: MCU PWM command for LF high-switch	SE at GND_D
HF2/L	J303	MCU digital: MCU PWM command for PH2 low-switch	SE at GND_D
HF2/H	J303	MCU digital: MCU PWM command for PH2 high-switch	SE at GND_D

(table continues...)

Table 14 (continued) Test points overview

Test points	Circuit	Description	Remarks
HF1/L	J303	MCU digital: MCU PWM command for PH1 low-switch	SE at GND_D
HF1/H	J303	MCU digital: MCU PWM command for PH1 high-switch	SE at GND_D

4 Limitations and known issues

- For user safety, use the provided AC-AC power adapter as an isolated AC input for the PFC board. If another AC input source is used, ensure it is also isolated. Using a non-isolated AC input can harm the user or permanently damage the evaluation board
- Before turning ON or turning OFF active PFC operation, ensure that the PFC is at no-load or light-load to avoid large passive-rectification pulses

5 Production data

The board has been designed using Altium Designer. The full PCB design data, including schematics, layout, and the BOM, can be downloaded from the kit webpage.

Revision history

Document version	Date of release	Description of changes
**	2026-02-17	Initial release

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