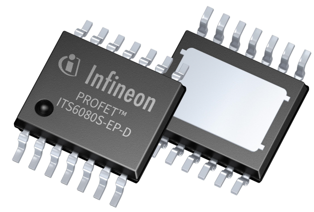
PROFET™ Industrial 75 mΩ single channel smart high-side power switch

Features



- Single channel smart high-side power switch with integrated protection and diagnosis
- Maximum $R_{DS(ON)}$ 75 mΩ at T_j = 25°C
- Overvoltage lockout
- Supply voltage tolerance up to 60 V
- User adjustable current limitation ranging from: 0.85 A to 5.1 A
- Wide output current range
- Open load diagnosis (in ON-state and OFF-state)
- Synchronized discharge functionality
- 24 V control inputs compatible to 3.3 V and 5 V logic levels
- 4 kV electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Very small, thermally enhanced TSDSO-14 package
- Green product (RoHS compliant)

RoHS

Potential applications

- Digital output modules (PLC applications, factory automation)
- Industrial peripheral switches and power distribution
- Switching resistive, inductive and capacitive loads in industrial environments
- Replacement for electromechanical relays, fuses and discrete circuits
- Most suitable for loads that require a flexible but precise current limit

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47J.

Description

The ITS6080S-EP-D is a single channel smart high-side switch providing diagnosis capabilities and enhanced protection functions. The device offers an adjustable current limitation to offer higher reliability for protecting the system. It provides enhanced diagnostic features including a separated status pin for sensing fault conditions. The ITS6080S-EP-D is designed to switch resistive, inductive or capacitive loads in industrial applications. The high voltage IN and DEN pins, can directly be interfaced with an optocoupler.

Type	Package	Marking
ITS6080S-EP-D	PG-TSDSO-14	IT6080SD

Table of contents

1 Product description

More functions are named in detail as follows:

Diagnostic functions

- Short circuit to ground (overload) indication
- Open load detection in OFF and in ON
- Overtemperature switch off indication
- Overvoltage lockout indication
- Stable diagnostic signal during short circuit, overtemperature shutdown

Protection functions

- Overvoltage protection and overvoltage lockout (switch off)
- User adjustable overload- and short circuit protection
- Stable behavior during undervoltage
- Overtemperature protection with restart after cooling down phase
- Reverse polarity / inverse current protection with external components
- Loss of ground protection

The qualification of this product is based on JEDEC JESD47J and may reference to existing qualification results of similar products. Such referring is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications. Infineon Technologies administrates a comprehensive quality management system according to the latest version of the ISO9001 and IATF 16949.

The most updated certificates of the ISO9001 and IATF 16949 are available at https://www.infineon.com/cms/en/product/technology/quality/

2 Block diagram

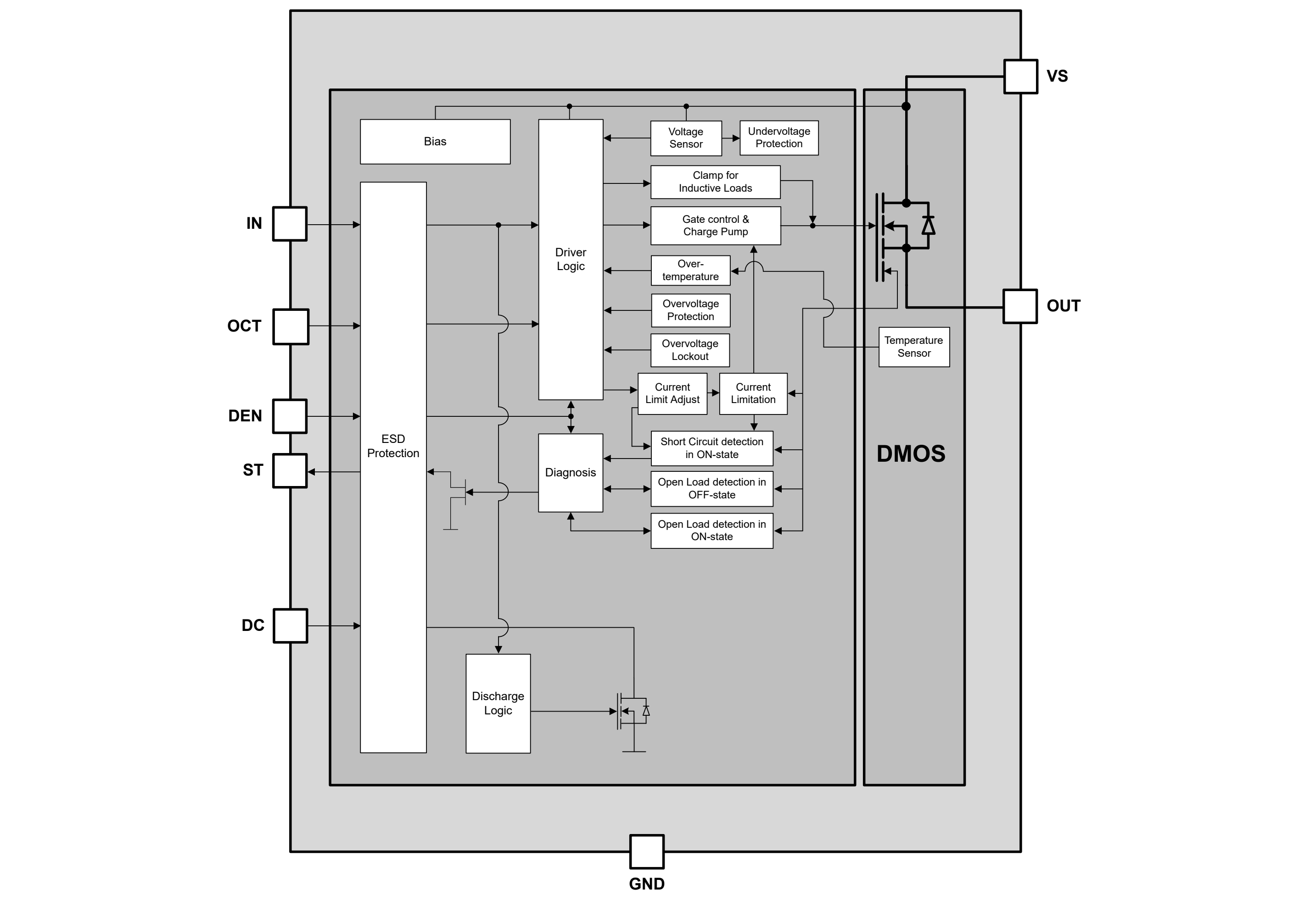


Figure 1 Block diagram ITS6080S-EP-D

3 Pin configuration

3.1 Pin assignment ITS6080S-EP-D (PG-TSDSO-14)

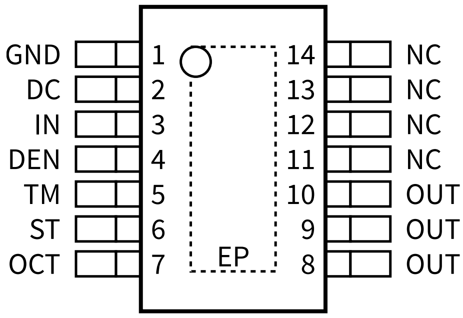


Figure 2 Pin configuration PG-TSDSO-14

3.2 Pin definitions and functions ITS6080S-EP-D (PG-TSDSO-14)

Pin	Symbol	Function
1	GND	**Ground**; Ground connection
2	DC	**Discharge Functionality**; provides a transient discharge path to GND after switching the channel off
3	IN	**Input Channel Control**; digital input signal for channel activation
4	DEN	**Diagnosis Enable**; digital input signal to enable the extended diagnosis features
5	TM	**Test Mode Entry**; must be connected with a series resistor to device ground (pin 1)
6	ST	**Status**; open drain output to provide diagnosis information. Connect ST-pin with external pull-up resistor to high (logic level or V_S)
7	OCT	**Over Current Threshold**; connect with an appropriate external resistor to device GND to adjust the current limitation threshold to the desired value
8, 9, 10	OUT	**Output**; protected high-side power output channel [1)]
11, 12, 13, 14	NC	**Not Connected**
Exposed Pad	VS	**Voltage Supply**

1) All three output pins should be connected to each other on the PCB as close as possible to the corresponding pads in order to avoid non-homogeneous current densities on separated traces

3.3 Voltage and current definitions

Figure 3 shows all terms used in this datasheet, with associated convention for positive values.

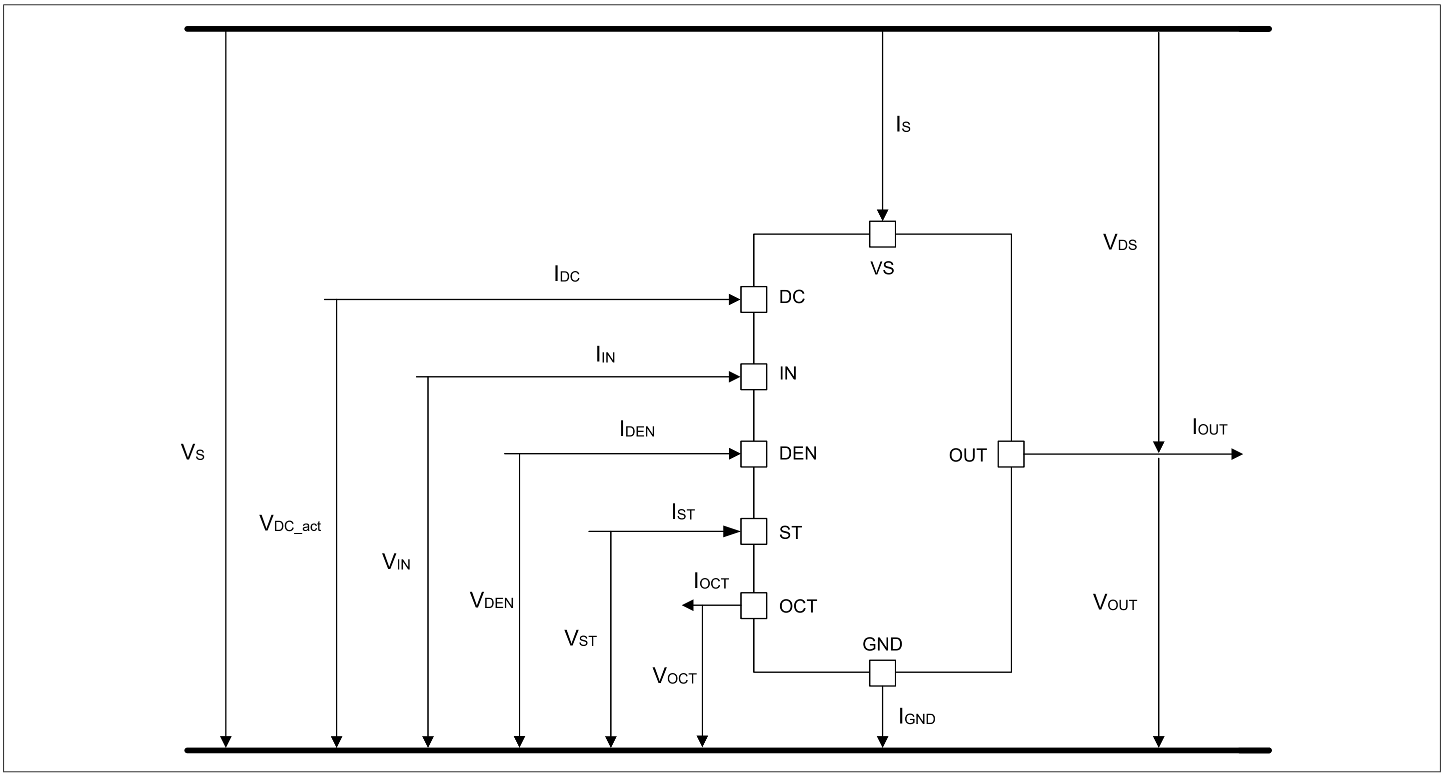


Figure 3 **Voltage and current definitions**

4 General product characteristics

4.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

Tj = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Supply voltage	V_S	-0.3	–	60	V	[1] Qualified for reduced mission profile of up to 125 h over lifetime	P_4.1.2
Supply voltage	V_S	-0.3	–	62	V	[1] [2] t < 2 minutes	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	28	V	[1] [3] t < 2 minutes; T_A = 25°C; $R_L \geq$ 25 Ω; a sufficiently dimensioned ground path protection D_{GND} needs to be foreseen externally	P_4.1.3
Supply voltage for short circuit protection	$V_{S(SC)}$	0	–	36	V	[1]	P_4.1.4
Control input pins (IN, DEN)							
Voltage at control input pins	V_{IN}, V_{DEN}	-0.3	–	V_S	V	[1] $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_4.1.5
Current through control input pins	I_{IN}, I_{DEN}	-2	–	2	mA	[1]	P_4.1.6
OCT-pin							
Voltage at OCT-pin	V_{OCT}	-0.3	–	V_S	V	[1] $V_S \geq V_{OCT}$	P_4.1.7
Current through OCT-pin	I_{OCT}	-2	–	2	mA	[1]	P_4.1.8
DC-pin							
Voltage at DC-pin	V_{DC_inact}	-0.3	–	V_S	V	[1] $V_S \geq V_{DC\_inact}$; I_{DC}= 0	P_4.1.9
Voltage at DC-pin (discharge active)	V_{DC_act}	–	–	20	V	[1] $V_S > V_{DC\_act}$; $I_{DC} \leq I_{DC\_sink}$	P_4.1.28
Current through DC-pin	I_{DC}	-250	–	250	mA	[1] t < 2 minutes	P_4.1.10
ST-pin							

(table continues...)

Table 1 (continued) Absolute maximum ratings

Tj = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage at ST-pin	V_{ST}	-0.3	–	V_S	V	1) $V_S \geq V_{ST}$	P_4.1.12
Current through ST-pin	I_{ST}	-2	–	2	mA	1)	P_4.1.13
Power stage							
Power dissipation (DC)	P_{TOT}	–	–	1.8	W	1) 4) T_A = 85°C T_j < 150°C	P_4.1.16
Maximum energy dissipation Single pulse	E_{AS}	–	–	300	mJ	1) I_L = 0.5 A; T_j = 150°C; V_S = 28 V	P_4.1.17
Voltage at power transistor	V_{DS}	–	–	65	V	1)	P_4.1.19
Ground current							
Current through ground pin	I_{GND}	-20	–	20	mA	1)	P_4.1.20
Temporary current through ground pin	I_{GND}	-250	–	250	mA	1) 5) t < 2 minutes	P_4.1.21
Temperatures							
Junction temperature	T_j	-40	–	150	°C	1)	P_4.1.22
Storage temperature	T_{STG}	-55	–	150	°C	1)	P_4.1.23
ESD susceptibility							
ESD susceptibility (all pins)	V_{ESD_HBM}	-2	–	2	kV	1) 6) HBM	P_4.1.24
ESD susceptibility OUT-pin vs. GND and VS connected	V_{ESD_HBM}	-4	–	4	kV	1) 6) HBM	P_4.1.25
ESD susceptibility	V_{ESD_CDM}	-500	–	500	V	1) 7) CDM	P_4.1.26
ESD susceptibility pin (corner pins)	V_{ESD_CDM}	-750	–	750	V	1) 7) CDM	P_4.1.27

1) Not subject to production test; specified by design
2) Please note that in case of transient voltage spikes exceeding $V_{S(AZ)}$ the resulting GND current must be limited by an external resistor in the ground path in order to ensure I_{GND} remains inside the allowed maximum ratings
3) Reverse polarity protection can only be achieved in combination with external components. For more details please refer to the corresponding chapters Overvoltage protection and Reverse polarity protection
4) This parameter serves as reference for the thermal budget: it illustrates the power dissipation that can be handled by the device in an application under the given boundary conditions before exceeding the maximum rating of T_j when assuming a R_{thJA} value for a thermally well dimensioned PCB connection like given in the JEDEC case RthJA_2s2pvia listed in Table 3 in Chapter 4.3. As R_{thJA} depends strongly on the applied PCB and layout of any individual application the actual achievable values of P_{TOT} can either be lower or higher depending on the given application

5) During Discharge pin operation or during reverse current situations
6) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001(1.5 kΩ, 100 pF)
7) ESD susceptibility, Charged Device Model “CDM” JEDEC JESD22-C101

Notes*:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Please note that fault conditions are not considered as normal operation conditions and the protection functions are neither designed for continuous operation nor for repetitive operation*

4.2 Functional range

Table 2 Functional range

Tj = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(NOM)}$	8	24	36	V	$V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_4.2.1
Extended operating voltage	$V_{S(NOM)}$	5	–	$V_{S(OV)\_LO}$	V	[1] $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$ (parameter deviations possible)	P_4.2.2
Overvoltage tolerance range	$V_{S(OV\_TR)}$	$V_{S(OV)\_RS}$	–	60	V	[1] [2] $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_4.2.3
Minimum functional supply voltage during power-up	$V_{S(OP)\_MIN}$	–	4.3	5	V	V_S increasing IN = high From $V_{DS} = V_S$ to $V_{DS} \leq 0.5$ V	P_4.2.4
Undervoltage shutdown	$V_{S(UV)}$	3	3.5	4.1	V	V_S decreasing IN = high From $V_{DS} \leq 1$ V to $V_{DS} = V_S$	P_4.2.5
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	[1] –	P_4.2.6
Overvoltage lockout threshold	$V_{S(OV)\_LO}$	47	51	55	V	$V_S \geq V_{IN}$; $V_S \geq V_{DEN}$ V_S rising	P_4.2.7
Overvoltage lockout restart voltage	$V_{S(OV)\_RS}$	46	50	54	V	$V_S \geq V_{IN}$; $V_S \geq V_{DEN}$ V_S falling	P_4.2.8
Overvoltage lockout blanking time	t_{OV_BLK}	–	230	–	µs	[1] [3] –	P_4.2.9
Overvoltage lockout hysteresis	$V_{S(OV)\_HYS}$	–	1	–	V	[1] –	P_4.2.10
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.11

1) Not subject to production test; specified by design
2) Reduced mission profile applies
3) This parameter applies for both cases - OVLO standby mode being entered from OFF-state as well as from ON-state

***Note**: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

4.3 Thermal resistance

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to exposed pad soldering point	R_{thJC}	–	4.5	–	K/W	1)	P_4.3.1
Junction to ambient All channels active	$R_{thJA\_2s2pvia}$	–	39	–	K/W	1) 2)	P_4.3.2
Junction to ambient All channels active	R_{thJA_1s0p}	–	126	–	K/W	1) 3)	P_4.3.3
Junction to ambient All channels active	$R_{thJA\_1s0p\_300mm}$	–	61	–	K/W	1) 4)	P_4.3.4
Junction to ambient All channels active	$R_{thJA\_1s0p\_600mm}$	–	49	–	K/W	1) 5)	P_4.3.5

1) Not subject to production test; specified by design
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. $P_{DISSIPATION}$ = 0.1 W
3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, footprint; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu, $P_{DISSIPATION}$ = 0.1 W
4) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 300 mm; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu, $P_{DISSIPATION}$ = 0.1 W
5) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 600 mm; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu, $P_{DISSIPATION}$ = 0.1 W

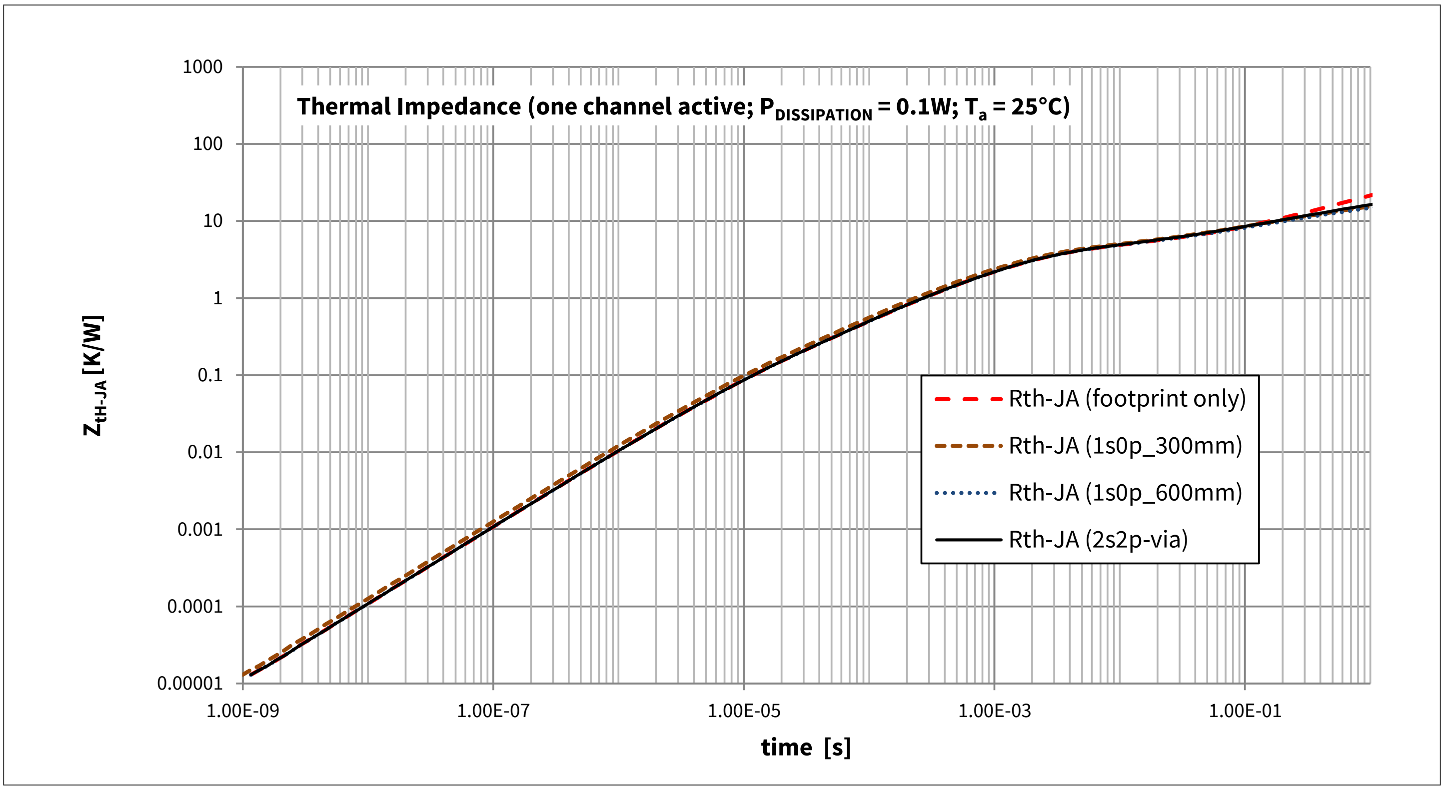


Figure 4 Thermal impedance (short time scale)

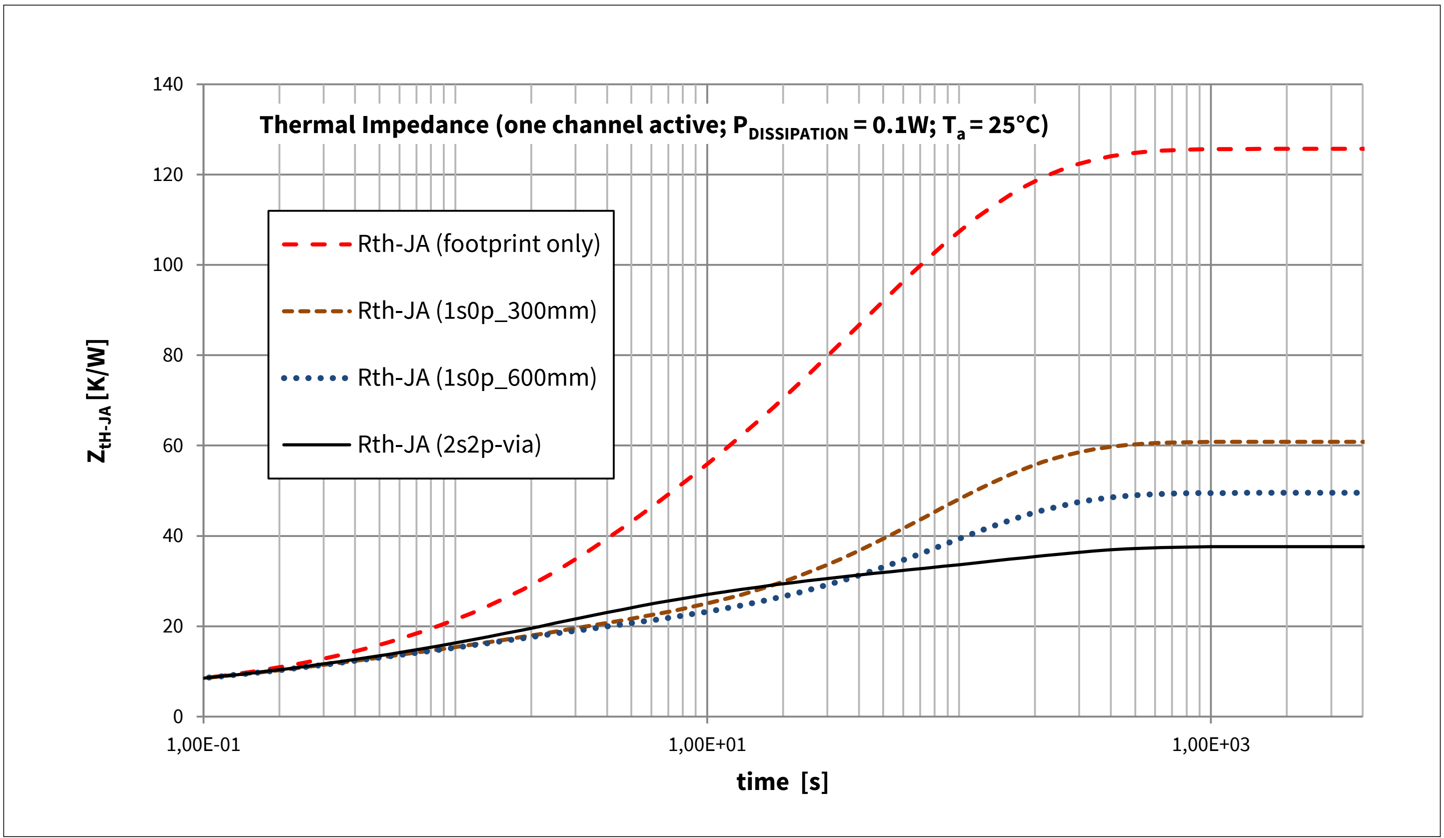


Figure 5 **Thermal impedance (long time scale; one channel active)**

5 Operation and diagnostic modes

5.1 State diagram

Depending on supply voltage V_S, input signals and usage of diagnosis the ITS6080S-EP-D can be in different operation modes. Figure 6 provides an overview of the operation modes and their corresponding operation currents.

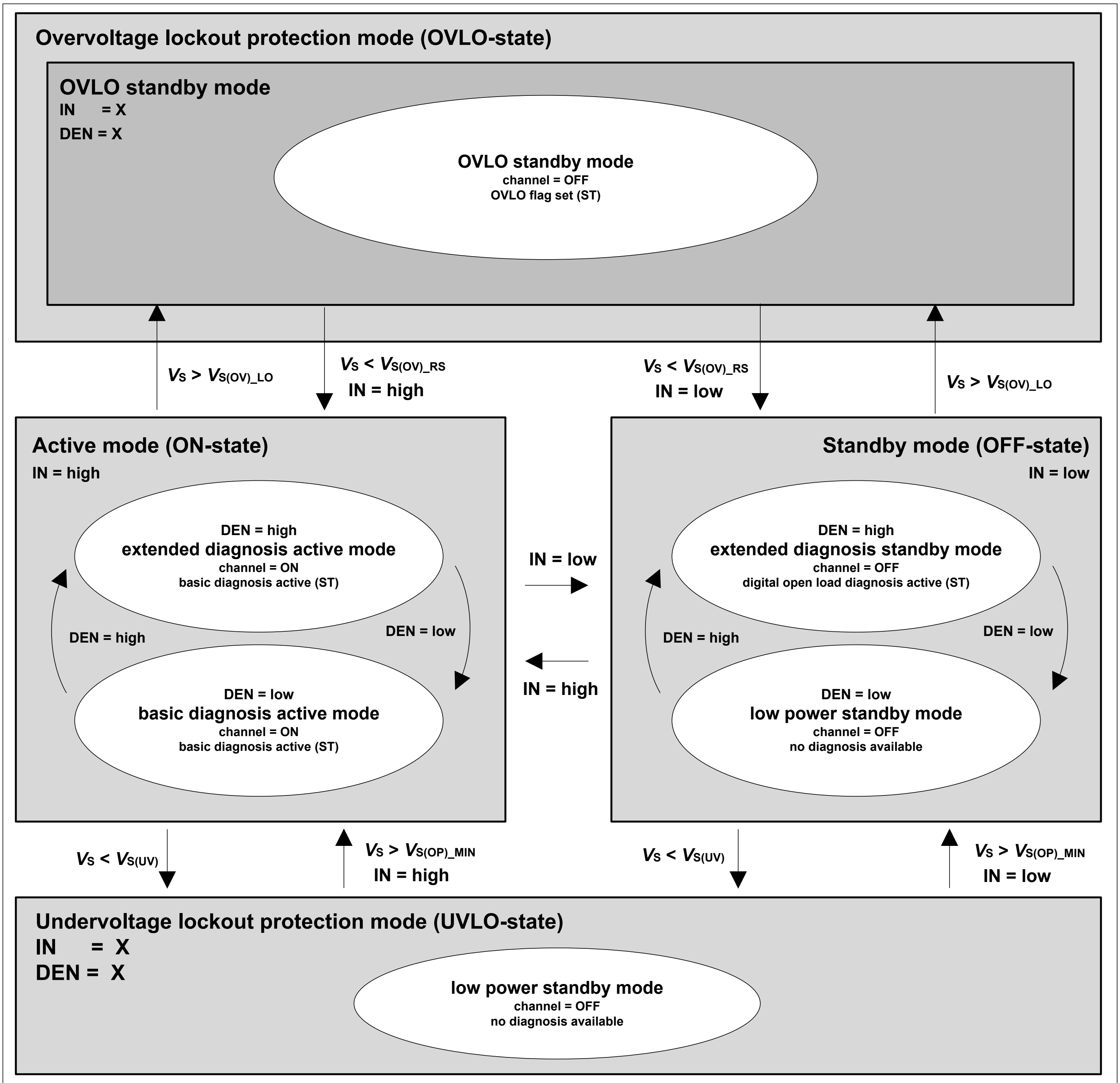


Figure 6 **State diagram ITS6080S-EP-D**

5.2 Electrical characteristics: current consumption

Table 4 Electrical characteristics: current consumption

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Operation currents							
ON - state current at T_J = 25°C (basic diagnosis)	I_{GND_ON}	–	2.3	2.9	mA	1) T_j ≤ 25°C; V_S = 24 V; V_{IN} = high; V_{DEN} = low; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.6
ON - state current at T_J = 150°C (basic diagnosis)	I_{GND_ON}	–	2	2.5	mA	1) T_j = 150°C; V_S = 24 V; V_{IN} = high; V_{DEN} = low; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.1
ON - state current at T_J = 25°C (extended diagnosis)	$I_{GND\_ON\_ed}$	–	2.6	3.2	mA	1) T_j ≤ 25°C; V_S = 24 V; V_{IN} = high; V_{DEN} = high; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.7
ON - state current at T_J = 150°C (extended diagnosis)	$I_{GND\_ON\_ed}$	–	2.3	2.8	mA	1) T_j = 150°C; V_S = 24 V; V_{IN} = high; V_{DEN} = high; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.2
Standby currents (to device GND)							
OFF - state current; (low power standby mode)	I_{GND_OFF}	–	0.1	1	µA	V_S = 24 V; V_{IN} floating; V_{DEN} floating	P_5.2.3

(table continues...)

Table 4 (continued) Electrical characteristics: current consumption

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
OFF - state current (extended diagnosis standby mode)	$I_{GND\_OFF\_ed}$	–	1.3	1.6	mA	[2] V_S = 24 V; V_{IN} = low; V_{DEN} = high	P_5.2.4
Overvoltage lockout mode current							
OVLO standby mode current	I_{GND_OVLO}	–	1.5	–	mA	[2] V_S = 60 V; 0 V ≤ V_{IN} ≤ V_S; 0 V ≤ V_{DEN} ≤ V_S DEN = IN = X	P_5.2.5

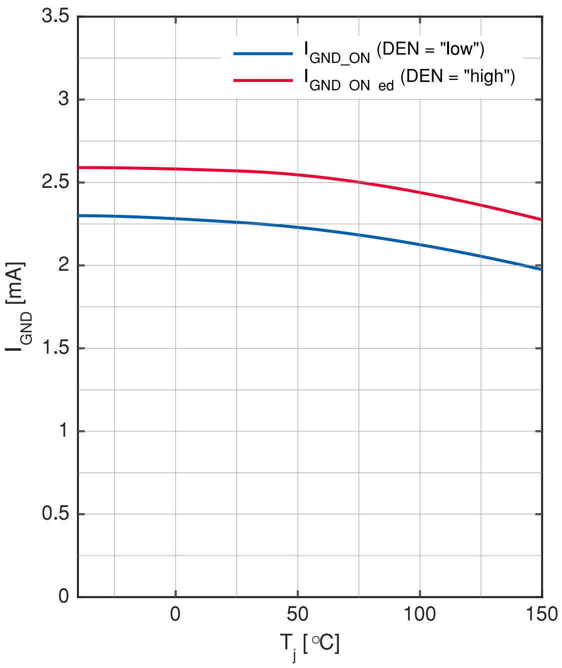
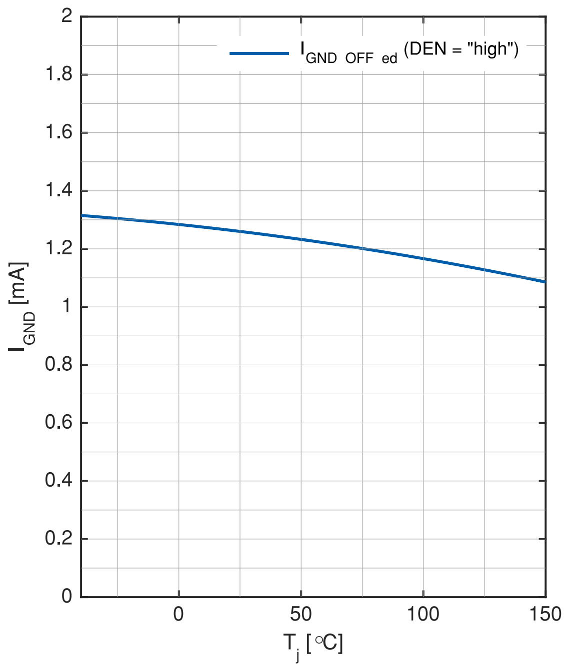
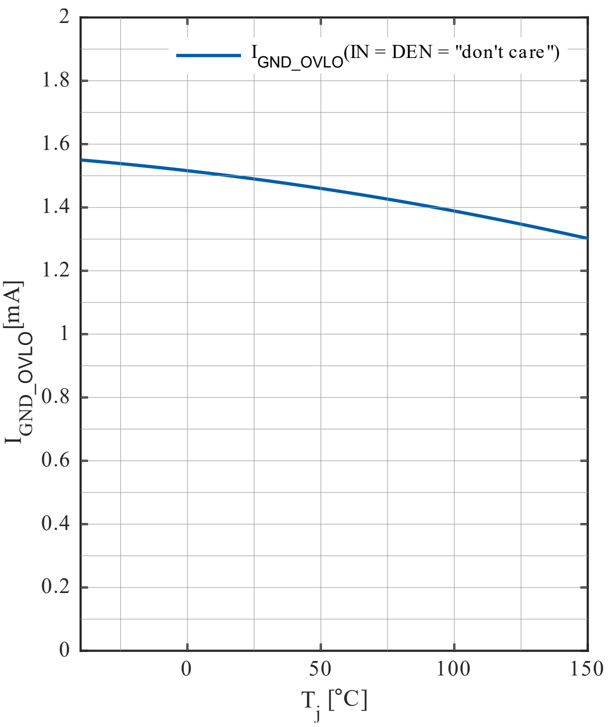
1) The current flowing out of the OCT-pin I_{OCT} depends on the adjusted current limitation value (R_{OCT}) and is not included in this parameter. In case of fault conditions also an additional current may be drawn from the ST-pin to device GND if applied. The ST-pin current - if applicable - is also not included in this parameter

2) The ST-pin current drawn by the ST-pin to device GND if applied is not included in this parameter. The ST-pin current during fault conditions will depend on the external pull-up circuit

5.3 Typical performance characteristics current consumption

Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

Operating current I_{GND_ON} versus junction temperature T_j (IN = high)	Extended diagnosis standby current $I_{GND\_OFF\_ed}$ versus junction temperature T_j (IN = high)
	
Overvoltage lockout mode current I_{GND_OVLO} versus junction temperature T_j	
	

6 Power stage

The power stage is built using an N-channel vertical power MOSFET (DMOS) with charge pump.

6.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ of the power stage depends on supply voltage as well as on junction temperature T_j. Figure 7 shows the influence of temperature on the typical ON-state resistance. The behavior of the power stage in reverse polarity condition is described in Chapter 7.4.

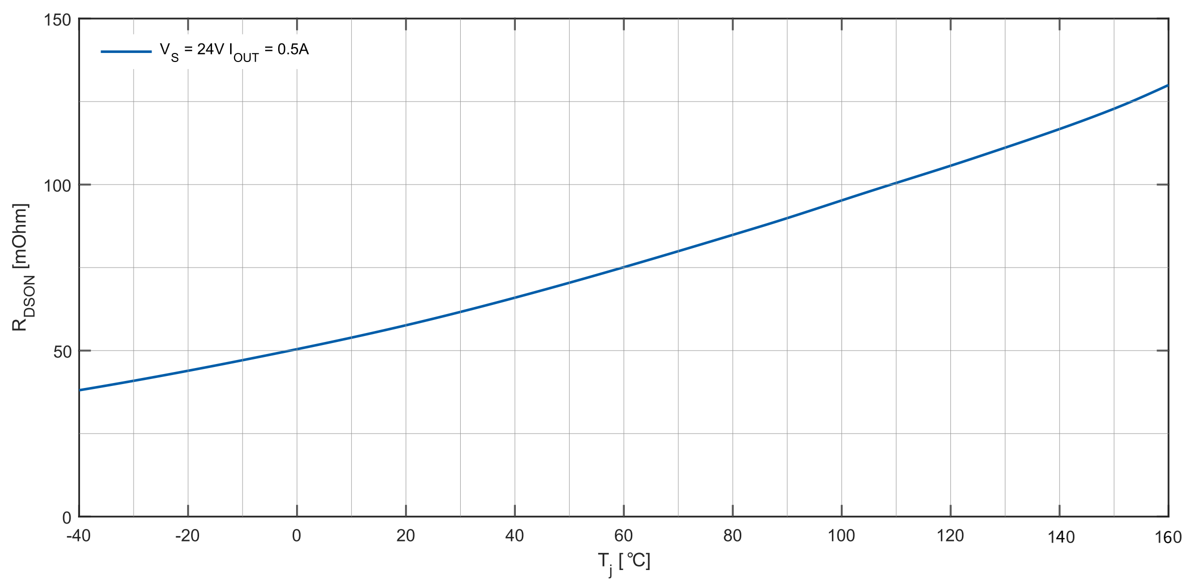


Figure 7 **Typical ON-state resistance**

6.2 Turn on/off characteristics with resistive load

A high signal at the input pin (see Chapter 10) causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission. Figure 8 shows the typical timing when switching a resistive load.

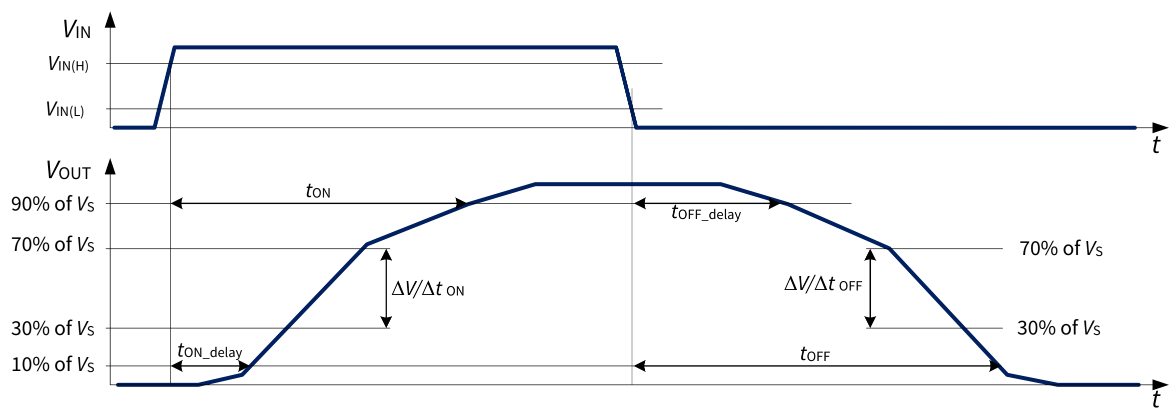


Figure 8 **Switching a resistive load timing**

6.3 Inductive load

6.3.1 Output clamping

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltage drop over the power stage a voltage clamp mechanism $Z_{DS(AZ)}$ is implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). The clamping mechanism allows in addition a fast demagnetization of inductive loads because during the phase of active clamping the power is dissipated to a great extent rapidly inside the switch. On the other hand, the power dissipated inside the switch while switching off inductive loads can cause considerable stress to the device. Therefore, the maximum allowed energy at a given current (and by this also the inductance) is limited. In Figure 9 and Figure 10 the basic principle of active clamping is illustrated as well as simplified waveforms when switching off inductive loads. If the DC-pin is utilized to discharge the output after switching off the channel a blocking diode has to be placed between DC-pin and OUT. In general, the usage of a blocking diode in the DC path is mandatory if the DC pin is at risk of being pulled below device GND. This diode ensures a stable behavior of the output clamp with the DC-pin attached to OUT while switching off inductive loads. Without this diode current would flow from device GND via the DC path to the output OUT bypassing the output clamp structure and potentially overstress or destroy the DC-pin or the GND path. In addition a series resistor has to be placed in the DC path to limit the power dissipation inside the IC. For a more details on the usage of the DC-pin and required external components please refer to Chapter 8.

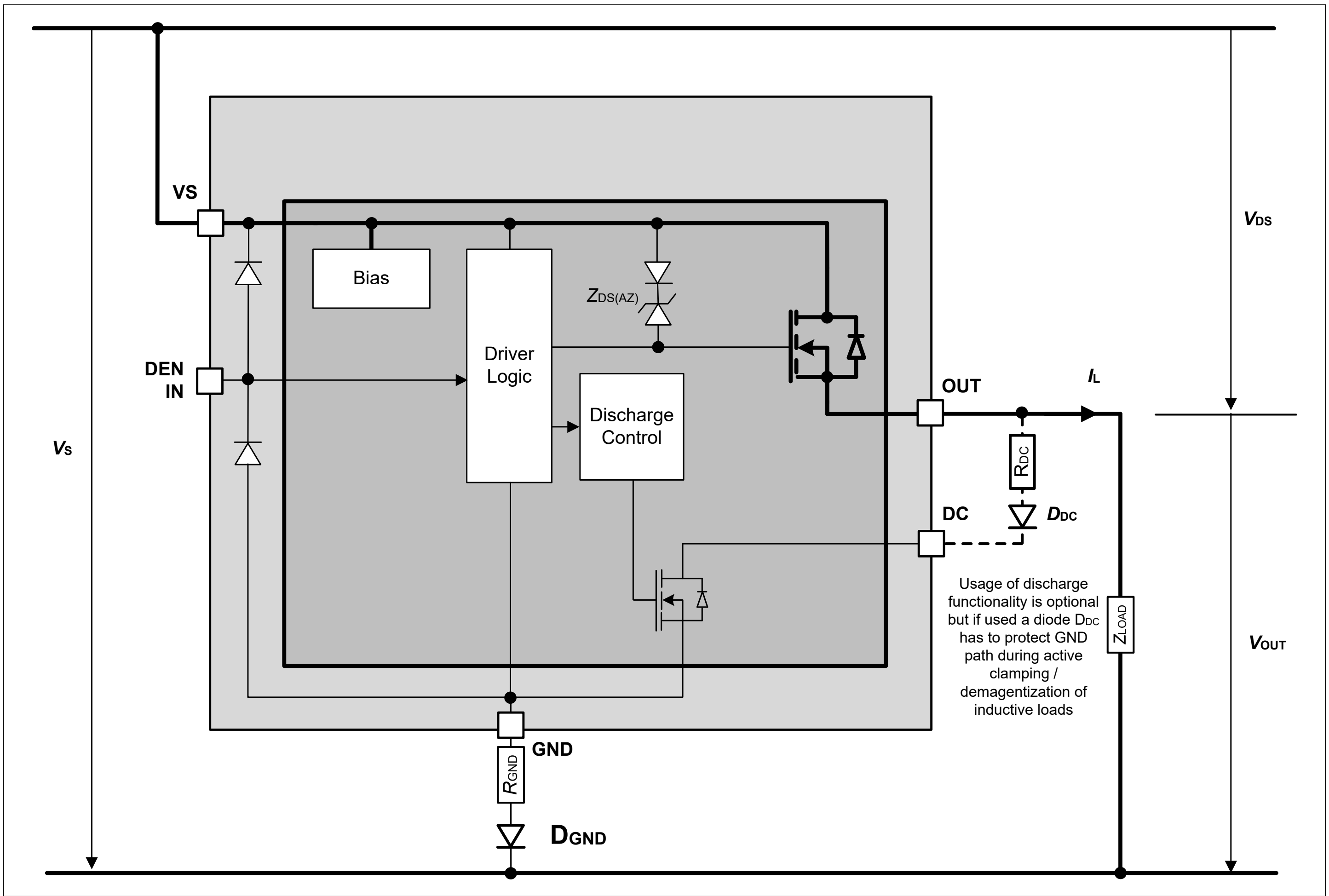


Figure 9 **Output clamp ITS6080S-EP-D**

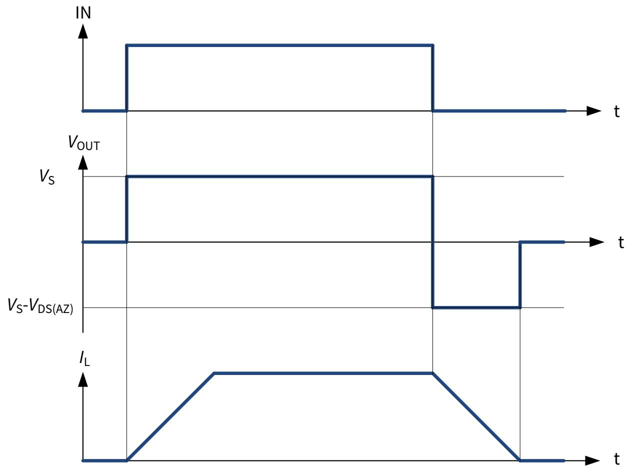


Figure 10 **Switching an Inductive load timing**

6.3.2 Maximum load inductance

During demagnetization of inductive loads, the following energy must be dissipated by the ITS6080S-EP-D. This energy can be calculated by help of the following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right] \quad (1)$$

Following equation gets simplified under the assumption of $R_L = 0\ \Omega$:

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \quad (2)$$

The energy, which may be converted into heat, is limited by the thermal design of the component. See Figure 11 for the maximum allowed energy dissipation as a function of the load current for a singular pulse event on the channel.

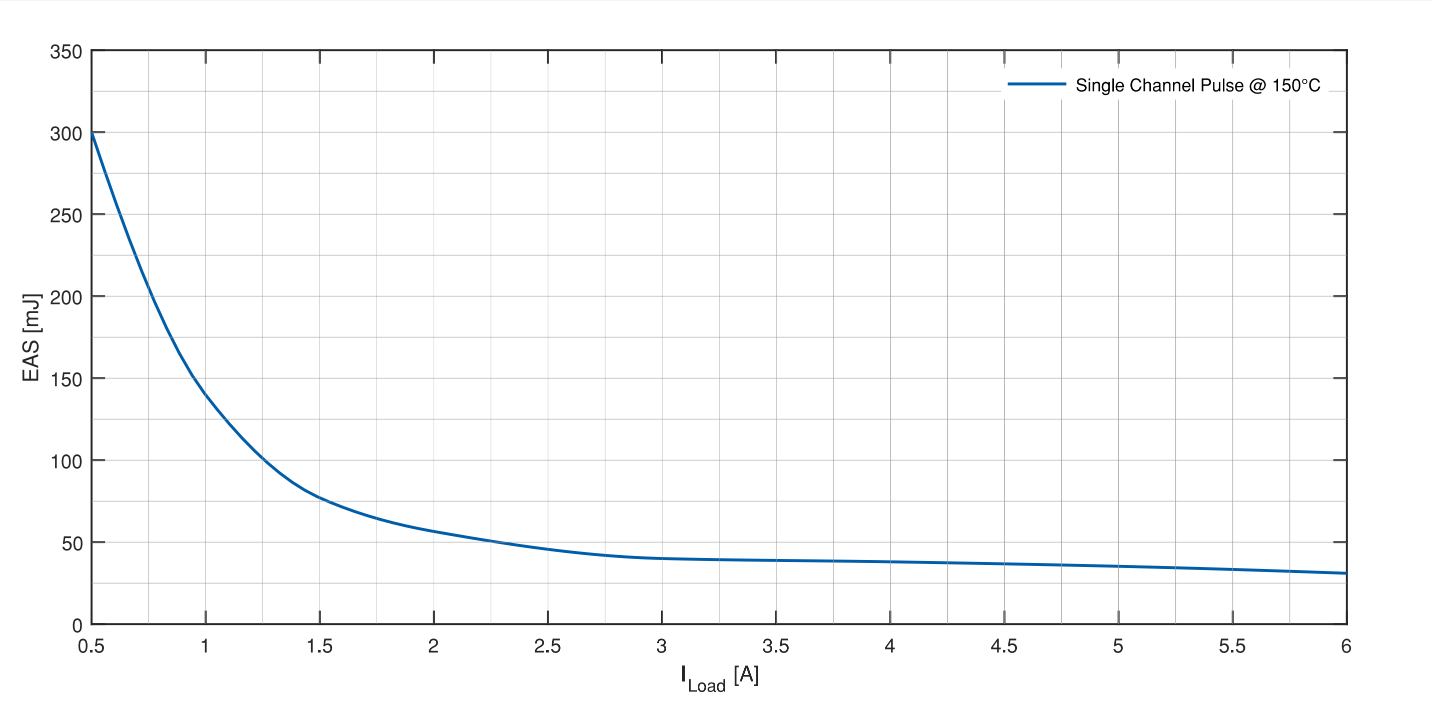


Figure 11 **Maximum energy dissipation single pulse; V_S = 28 V**

6.4 Inverse current capability

In case of inverse current, meaning a voltage V_{INV} at the output higher than the supply voltage V_S, a current $I_{L(INV)}$ will flow from output to VS-pin via the body diode of the power transistor (please refer to Figure 12). If the channel is active (ON-state) by the time when the inverse current condition appears it will remain active and its output stage will follow the state of the corresponding IN-pin, which means that the channel can be switched off during inverse current condition. If the channel is inactive (OFF-state) by the time when the inverse current condition appears it will remain inactive regardless of the state of the IN-pin. If during an inverse current condition the IN-pin is set from low to high in order to activate the channel, the output stage of the channel is kept OFF until the inverse current disappears. For all cases the inverse current should not be higher than $I_{L(INV)}$. Please note that during inverse current condition the protection functions are not available.

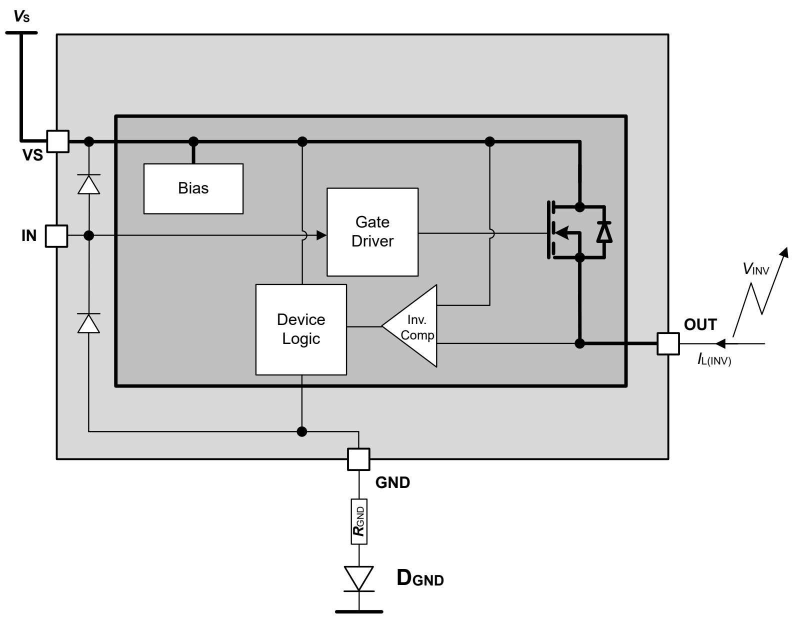


Figure 12 **Inverse current circuitry ITS6080S-EP-D**

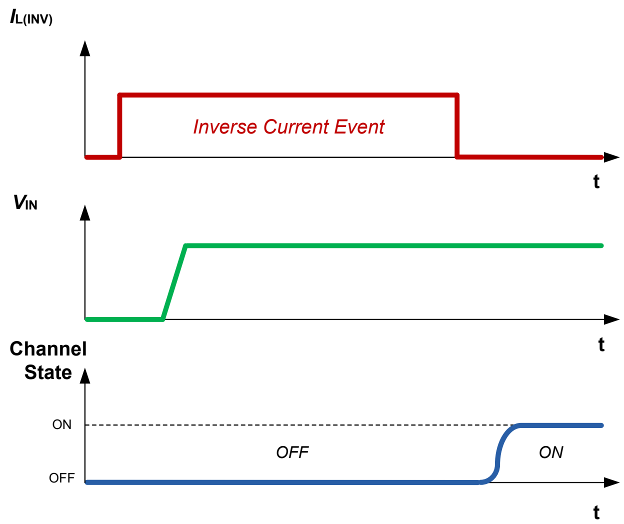


Figure 13 **Inverse current event: channel in OFF-state (channel remains off for duration of inverse current event)**

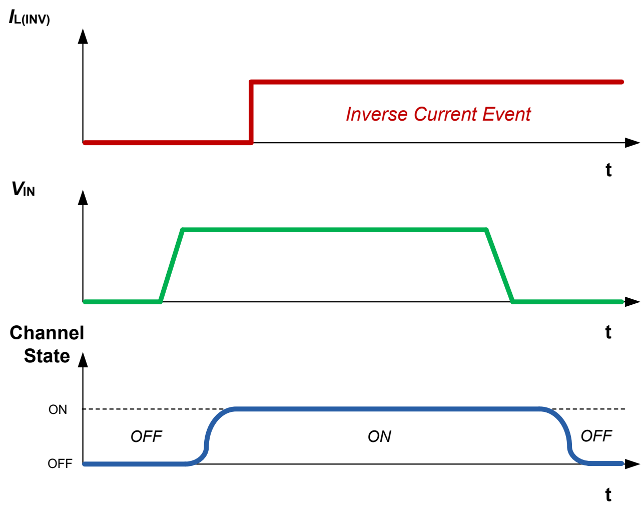


Figure 14 Inverse current event: channel in ON-state (output not influenced and can be switched off)

6.5 Electrical characteristics: Power stage

Table 5 Electrical characteristics: Power stage

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance (T_j = 25°C)	$R_{DS(ON)}$	–	60	75	mΩ	1) I_L = 0.5 A; V_{IN} = high; T_j = 25°C	P_6.5.1
ON-state resistance (T_j =125°C)	$R_{DS(ON)\_125}$	–	110	–	mΩ	1) I_L = 0.5 A; V_{IN} = high; T_j = 125°C	P_6.5.2
ON-state resistance (T_j = 150°C)	$R_{DS(ON)\_150}$	–	125	150	mΩ	I_L= 0.5 A; V_{IN} = high; T_j = 150°C	P_6.5.3
Allowable nominal load current range in conjunction with a selected current limit setting or based on thermal constraints	$I_{L(NOM)}$	–	2.5	–	A	1) 2) T_A = 85°C, T_J < 150°C	P_6.5.4
Output voltage drop limitation at small load currents	$V_{DS(SLC)}$	–	12	25	mV	I_L = 10 mA	P_6.5.20

(table continues...)

Table 5 (continued) Electrical characteristics: Power stage

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	65	70	75	V	I_{DS} = 5 mA	P_6.5.6
Output leakage current (OFF-state)	$I_{L(OFF)}$	–	0.1	0.5	µA	[1] V_{IN} = low; V_{OUT} = 0 V; $T_j \leq$ 85°C	P_6.5.7
Output leakage current (OFF-state)	$I_{L(OFF)\_150}$	–	1.5	5	µA	V_{IN} = low; V_{OUT} = 0 V; T_j = 150°C	P_6.5.8
Output leakage current in overvoltage lockout (OVLO-state)	$I_{L(OVLO)}$	–	5.5	18	µA	[1] [3] V_S = 60 V; $V_{IN} = V_{DEN}$ = X; V_{OUT} = 0 V; $T_j \leq$ 25°C	P_6.5.21
Output leakage current in overvoltage lockout (OVLO-state)	$I_{L(OVLO)\_150}$	–	3	5	µA	[3] V_S = 60 V; $V_{IN} = V_{DEN}$ = X; V_{OUT} = 0 V; T_j = 150°C	P_6.5.22
Inverse current capability	$I_{L(INV)}$	–	2.2	–	A	[1] [4] $V_S < V_{OUT}$; t < 2 minutes	P_6.5.9
Slew rate (switch on) 30% to 70% of V_S	$\Delta V/\Delta t_{ON}$	–	0.7	–	V/µs	R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.10
Slew rate (switch off) 70% to 30% of V_S	$-\Delta V/\Delta t_{OFF}$	–	1.0	–	V/µs	R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.11
Turn on time to V_{OUT} = 90% of V_S	t_{ON}	–	52	85	µs	[5] R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA; V_{DEN} = low	P_6.5.13

(table continues...)

Table 5 (continued) Electrical characteristics: Power stage

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn off time to V_{OUT} = 10% of V_S	t_{OFF}	–	35	70	µs	R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.14
Turn on/off matching t_{OFF} - t_{ON}	Δt_{SW}	-45	0	45	µs	R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.15
Turn on time to V_{OUT} = 10% of V_S	t_{ON_delay}	–	25	40	µs	5) R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA; V_{DEN} = low	P_6.5.16
Turn off time to V_{OUT} = 90% of V_S	t_{OFF_delay}	–	16	40	µs	R_L = 47 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.17

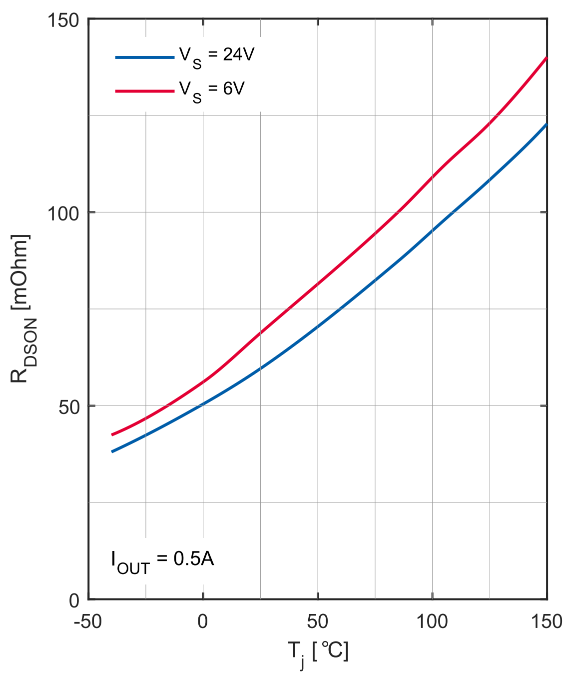
1) Not subject to production test; specified by design
2) The allowable nominal load current can be restricted by two different factors - the magnitude of the adjusted current limitation but as well by thermal constraints. The minimum limit given here corresponds to the limitation by the current limitation when adjusted to its minimum value (I_{OCT} = 6.67 µA) while the maximum limit corresponds to the thermal limitation where the maximum T_j of 150°C is reached assuming T_{AMB} =85°C and $R_{thJA\_2s2pvia}$. In normal operation the minimum required distance of $I_{L(NOM)}$ to the adjusted current limitation has to be maintained. For further details and numbers please refer to Table 13
3) Valid after output is completely switched off
4) Please note that during inverse current condition the protection features are not operational
5) This timing will be faster if device is in extended diagnosis standby mode (DEN = high). For further details see typical performance graphs Turn on time tON to VOUT = 90% versus current limit adjust current IOCT (DEN = low & high) and Turn on delay time tON_delay to VOUT = 10% versus current limit adjust current IOCT (DEN = low & high)

6.6 Typical performance characteristics power stage ITS6080S-EP-D

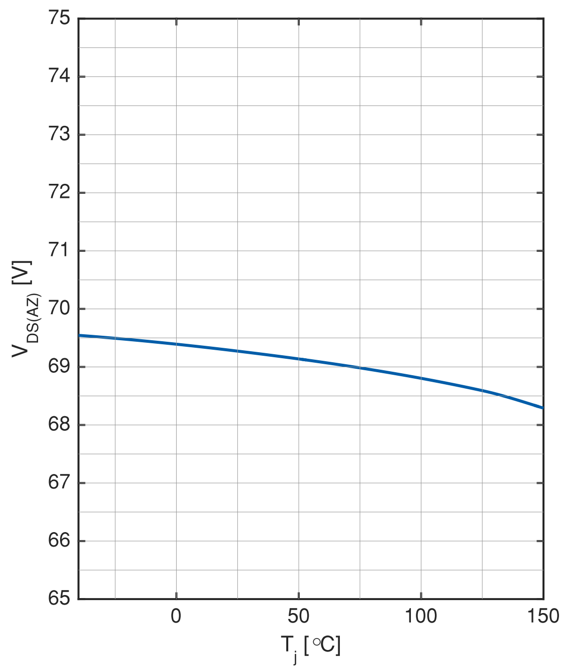
Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

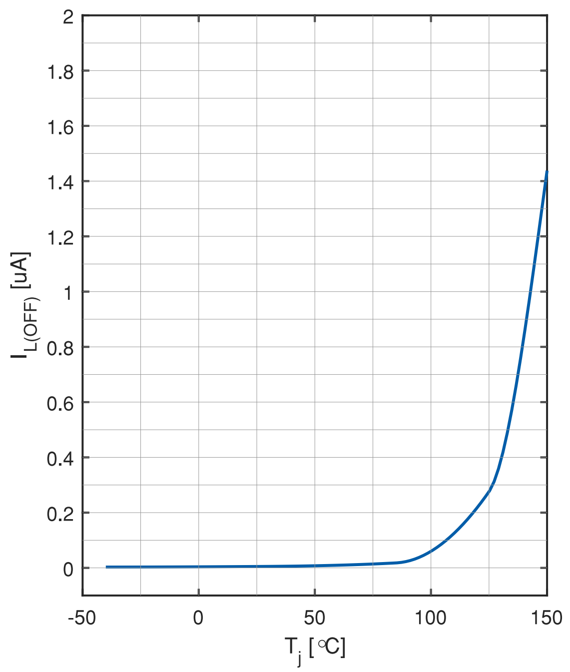
ON-state resistance $R_{DS(ON)}$ versus junction temperature T_j



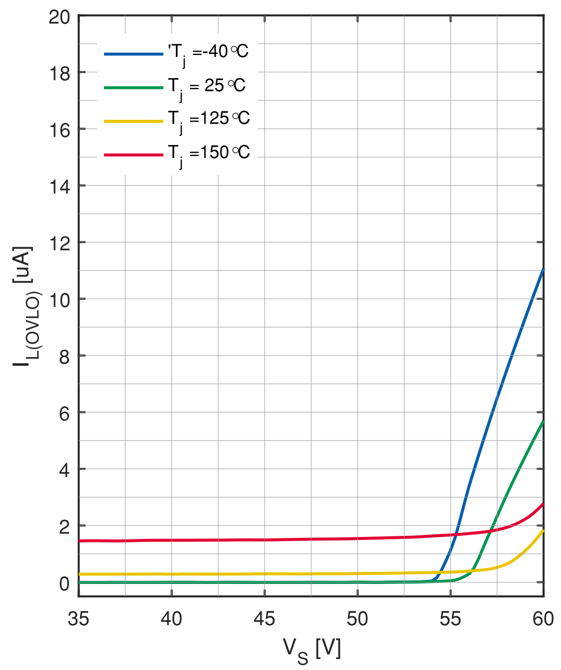
Output clamp voltage $V_{DS(AZ)}$ versus junction temperature T_j

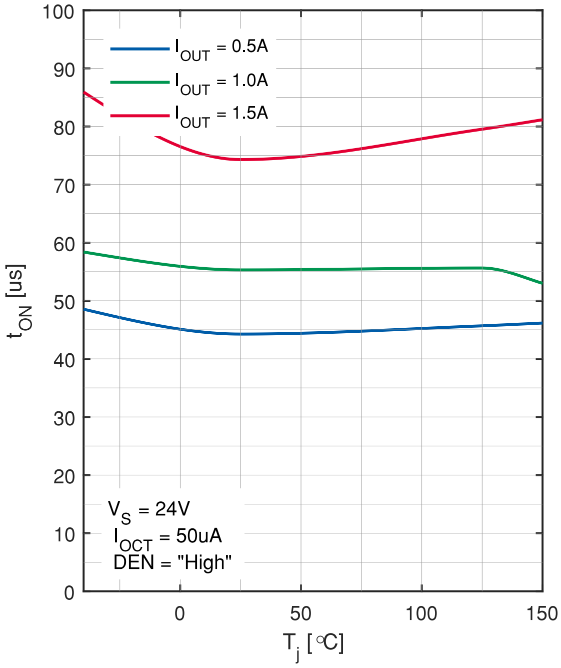
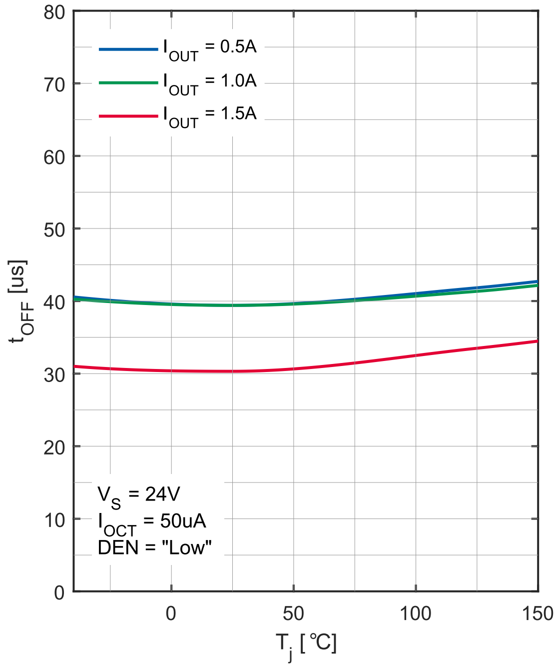
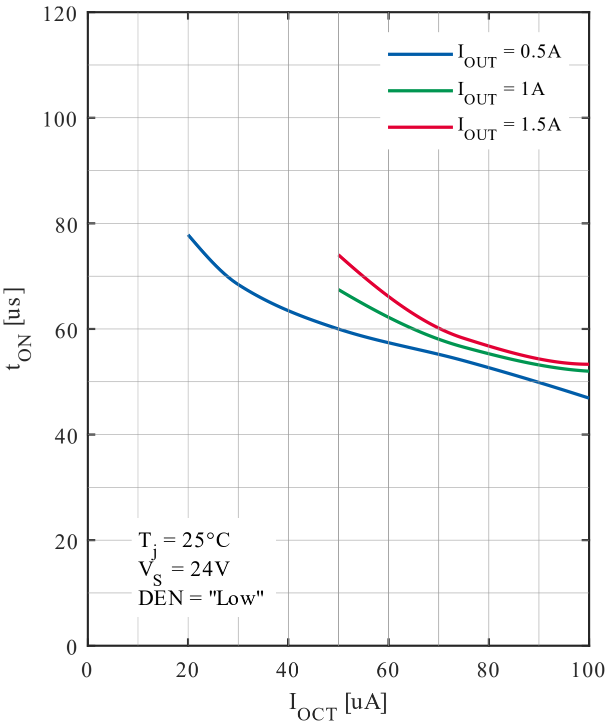
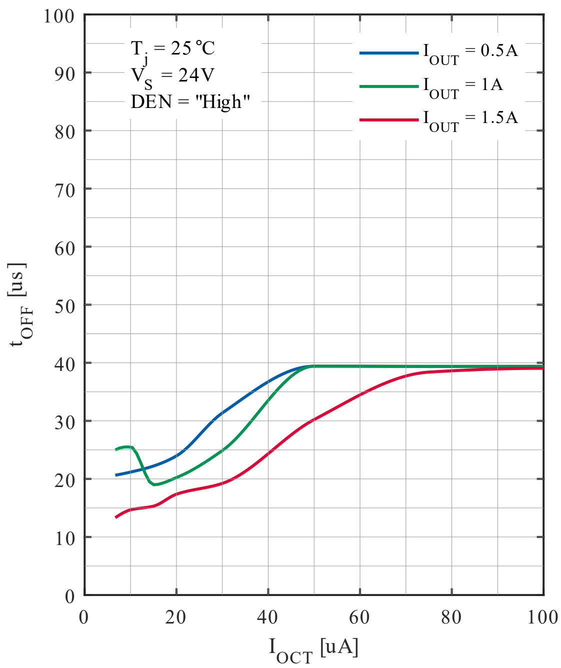


Output leakage current $I_{L(OFF)}$ versus junction temperature T_j



Output leakage current when entering OVLO versus supply voltage V_S



Turn on time t_{ON} to V_{OUT} = 90% versus junction temperature T_j	Turn off time t_{OFF} to V_{OUT} = 10% versus junction temperature T_j
	
Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT}	Turn off time t_{OFF} to V_{OUT} = 10% versus current limit adjust current I_{OCT}
	

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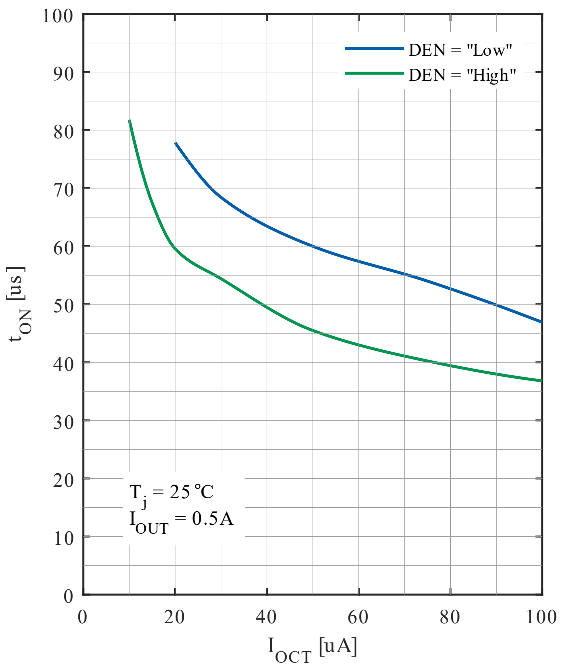
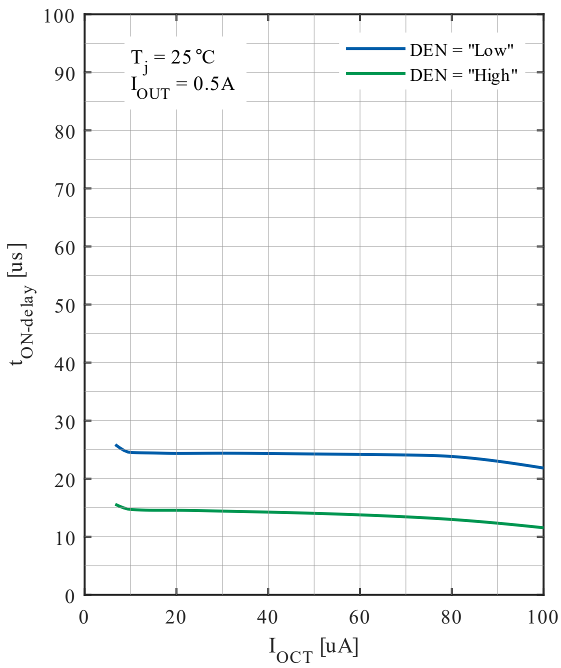
Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT}	Turn on delay time t_{ON_delay} to V_{OUT} = 10% versus current limit adjust current I_{OCT}
	

7 Protection functions

The device provides integrated protection functions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Protection functions are designed to prevent the destruction of the ITS6080S-EP-D due to fault conditions described in the datasheet. Please note that fault conditions are not considered as normal operation conditions and the protection functions are neither designed for continuous operation nor for repetitive operation.

7.1 Loss of ground protection

In case of loss of module ground when the load remains connected to ground, the device protects itself by automatically turning off (when it was previously on) or remaining off, regardless of the voltage applied at the input pin. In an application where the input IN is directly controlled by logic levels < V_S (e.g. by a microcontroller without galvanic isolation), it is recommended to use input resistors between the external control circuit (microcontroller) and the ITS6080S-EP-D to protect also the external control circuit in case of loss of ground. In case of loss of module or device ground, a current $I_{OUT(GND)}$ can flow out of the DMOS as is illustrated in Figure 15, below.

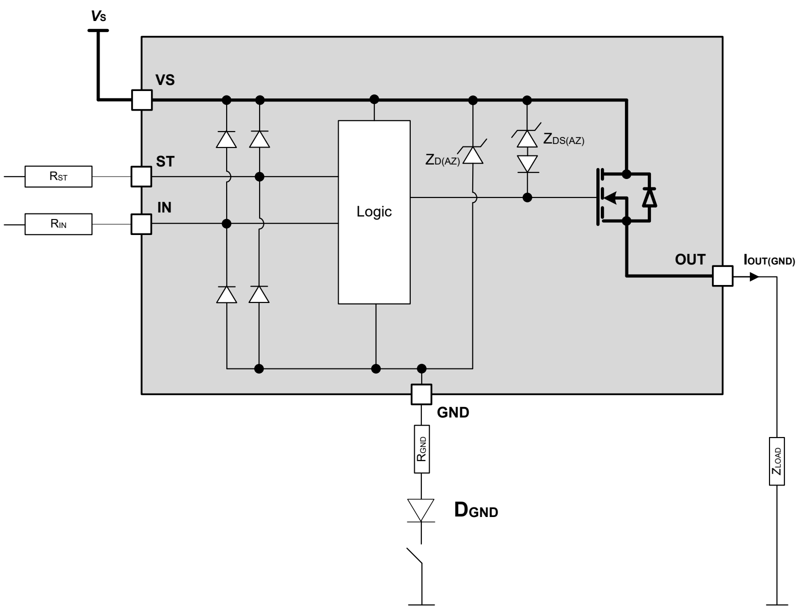


Figure 15 Loss of ground protection with external components

7.2 Undervoltage protection

If the supply voltage falls below $V_{S(UV)}$ the undervoltage protection of the device is triggered. $V_{S(UV)}$ represents hence the minimum voltage for which the switch still can hold ON. Once the device is off $V_{S(OP)\_MIN}$ represents the lowest voltage where the device is turning on again (and thus the channel can be switched again). If the supply voltage is below the undervoltage threshold $V_{S(UV)}$, the channel of the device is off (or turning off). As soon as the supply voltage is recovering and exceeding the threshold of the functional supply voltage $V_{S(OP)\_MIN}$, the device is re-powering and its channel can be switched again. In addition the protection functions as well as diagnosis becomes operational once $V_{S(OP)\_MIN}$ is reached. Figure 16 illustrates the undervoltage mechanism.

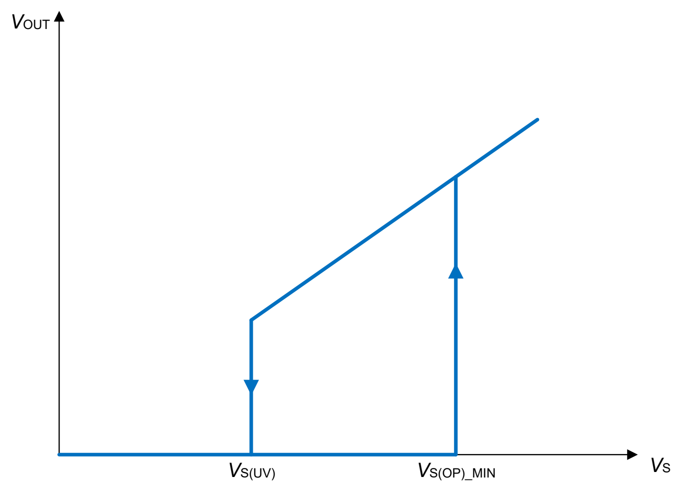


Figure 16 Undervoltage behavior

7.3 Overvoltage protection

The ITS6080S-EP-D provides an overvoltage protection. The overvoltage protection consists of two different sub-functions. First there is an overvoltage lockout mechanism (OVLO) to protect the load in case of permanent overvoltage on the V_S - line above the extended functional range up to a value of 60 V. In addition to the OVLO protection there is an integrated overvoltage clamp mechanism that protects the IC itself in case of short overvoltage pulses above $V_{S(AZ),MIN}$ that may occur on the V_S - line.

7.3.1 Overvoltage lockout

The overvoltage lockout (OVLO) of the ITS6080S-EP-D is defined in the first place to protect the load in case of unwanted voltage excursions on the V_S - line that may occur and persist for longer times (from ms range up multiple days). An OVLO event will be recognized if V_S exceeds a threshold value of $V_{S(OV)\_LO,TYP}$ for a duration longer than the blanking time of $t_{OV\_BLK,TYP}$. If an OVLO event is recognized during active mode the channel will be immediately switched off regardless of the logic state of the IN-pin and remains locked out until the overvoltage situation has cleared. Overvoltage events exceeding the OVLO threshold but not lasting longer than the blanking time will be filtered out by the OVLO circuit in order to avoid unwanted shut-off events. The OVLO circuit has a hysteresis of $V_{S(OV)\_HYS,TYP}$ to ensure a stable behavior. The device will return to normal operation once V_S is falling back below the OVLO restart voltage $V_{S(OV)\_RS}$ and the built-in hysteresis, $V_{S(OV)\_HYS}$. In other words, the output channel will follow the state of the IN-pin again after V_S is in back in its functional range. If the ITS6080S-EP-D faces an OVLO event a diagnosis flag will be set on the ST-pin for the duration of the OVLO event. Once the OVLO circuit has switched off the output channel the ITS6080S-EP-D will remain in OVLO standby mode for the duration of the overvoltage event where it just provides diagnosis information and keeps monitoring V_S . The ITS6080S-EP-D is qualified to remain in the OVLO-state for macroscopic time scales of up to 125 hours over lifetime at $V_{S,MAX}$.

The ITS6080S-EP-D is able to detect OVLO events not only during active mode but also when the device is in standby mode (both - low power standby mode and extended diagnosis standby mode) where the channel is already off. In order to be able to detect an OVLO event during OFF-state the ITS6080S-EP-D has a corresponding wake-up routine implemented. OVLO events during OFF-state will block the input pin circuitry for activation of the channel until the overvoltage situation is cleared while the ST-pin is flagging the OVLO fault situation regardless of the logic state of the DEN-pin. (For further details please refer to the corresponding truth table Table 9 in Chapter 9).

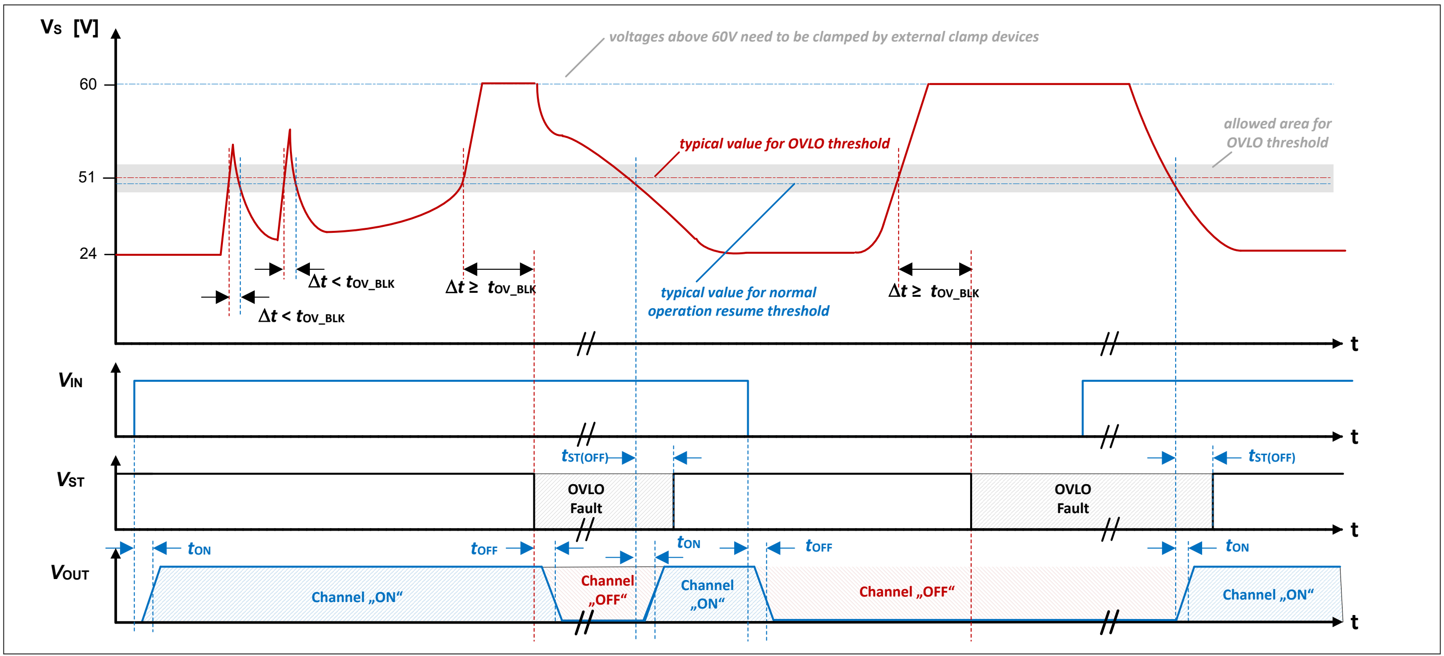


Figure 17 **Exemplary overview of overvoltage lockout and overvoltage clamping**

7.3.2 Overvoltage clamp

In addition to the OVLO feature there is an integrated clamping mechanism for overvoltage protection ($Z_{D(AZ)}$) against transient overvoltage spikes. To ensure this mechanism operates properly within the application, the current in the Zener diode $Z_{D(AZ)}$ must be limited by an external GND protection R_{GND}. Figure 18 shows a typical application to withstand overvoltage events. In case of supply voltage transients higher than $V_{S(AZ)}$, the voltage from supply to device ground is clamped. As a result, the device ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at IN-pin rises almost to that potential, depending on the impedance of the connected circuitry. As a consequence, in case of transient overvoltage events > $V_{S(AZ)}$, external resistors have to be placed at the control pins that limit the current that can flow out of these pins while the device GND potential becomes higher than the voltage level at the control pins. Next to these protection resistors at the control pins also the GND path itself has to be protected against excessive current flow during such pulses by placing a resistor in the GND path. For a more detailed description of external devices for protection under fault conditions please refer to Chapter 11.2.

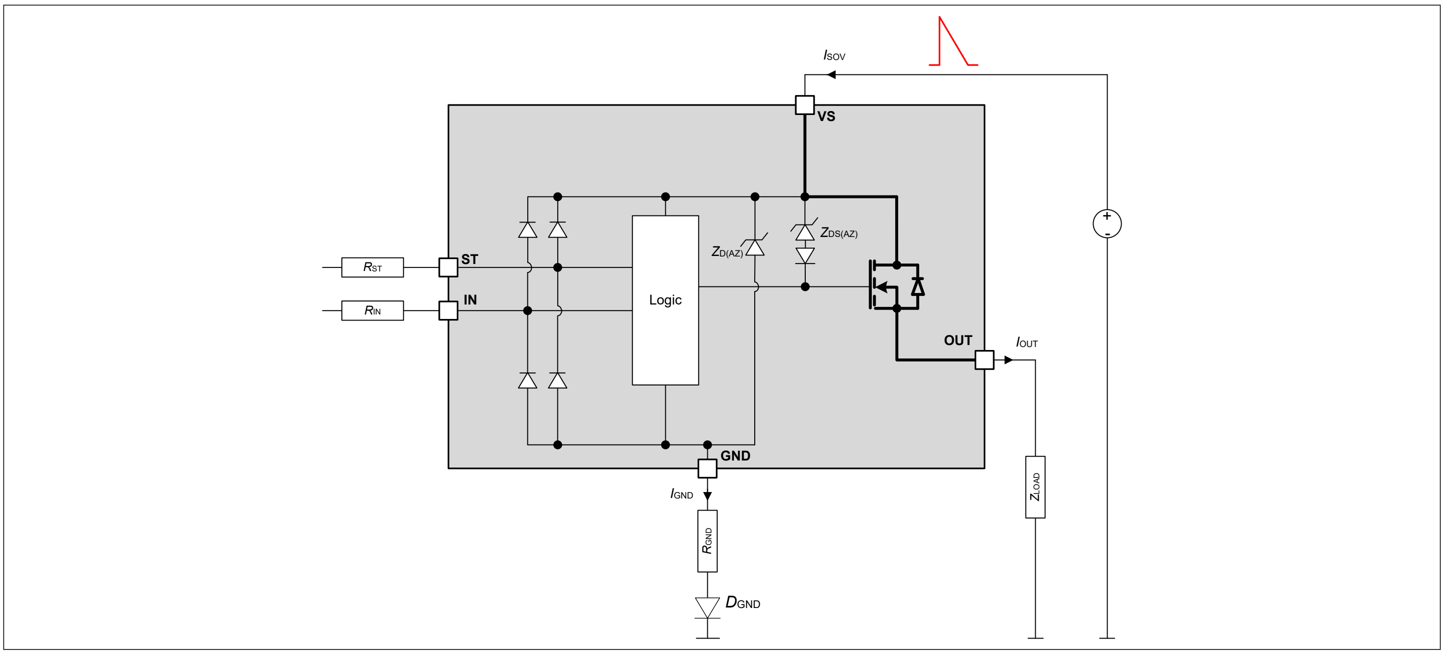


Figure 18 Overvoltage clamp protection with external components

7.4 Reverse polarity protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS will dissipate power. The current flowing through the intrinsic body diode is limited externally by the load itself. But in addition also the current into the ground path and the logic pins must be limited by external components to the maximum allowed current described in Chapter 4.1. Figure 19 shows a typical application. As external protection of the ground path the usage of a diode in the GND-path is recommended. For a more detailed description of external devices for protection please refer to Chapter 11.2. During reverse polarity no protection functions are available.

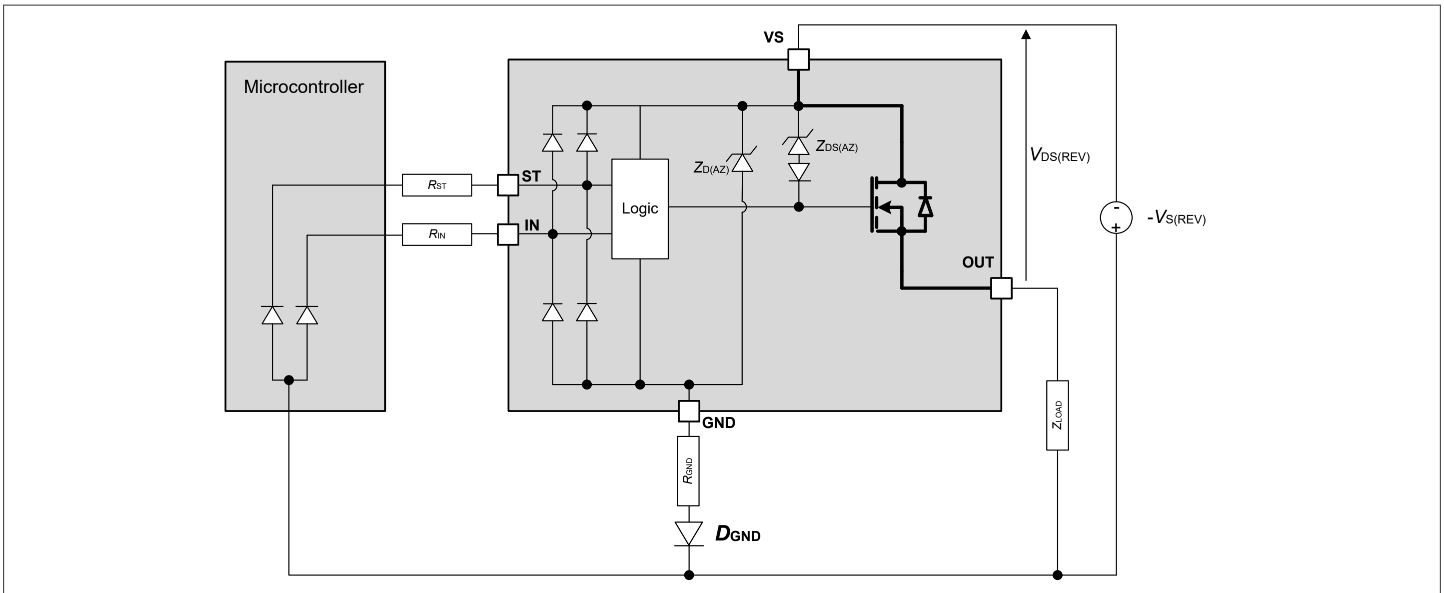


Figure 19 Reverse polarity protection with external components

7.5 Overload protection

In case of overload, such as high inrush currents or short circuit to ground, the ITS6080S-EP-D offers a set of protection mechanisms. As a first step, it comprises an accurate adjustable current limitation. This feature offers protection against overstress for the load as well as for the power output stage. In case of DMOS temperature increase exceeding the device safe operating environment, overtemperature and dynamic temperature protection mechanism will be triggered.

7.5.1 Current limitation

The ITS6080S-EP-D provides a very versatile and user friendly current limitation functionality that can be adjusted externally by the user in a broad range. The adjustment of the current limitation threshold $I_{LIM(th,adj)}$ to the desired value is controlled by the I_{OCT} current that is driven by the overcurrent threshold pin (OCT-pin) out of the device. The OCT-pin thereby is acting as a voltage source providing V_{OCT}. In the most simple and straight forward way the current limit adjustment can hence be achieved by connecting the OCT-pin with an appropriately dimensioned resistor to device ground. Figure 20 illustrates the usage of the adjustable current limitation. Please note that the values for the current limitation threshold $I_{LIM(th,adj)}$ are defined in such a way that they coincide with the typical values of the resulting current limitation at 25°C. The typical values of the current limitation at different temperatures may hence differ from $I_{LIM(th,adj)}$ to a certain degree. Typical values of the current limitation for different temperatures as a function of I_{OCT} are shown in Chapter 11.3.

The adjusted current limit threshold $I_{LIM(th,adj)}$ is a function of the current I_{OCT} driven by the OCT-pin.

The appropriate resistor, R_{OCT} can be derived by the equation:

$$R_{OCT} = \frac{V_{OCT}}{I_{OCT}} \tag{3}$$

The specified range of I_{OCT} that can be used to adjust $I_{LIM(th,adj)}$ allows to vary the current limitation over a wide area. In case of an OCT-pin short to ground with the current exceeding $I_{OCT(short2GND)}$ the device will set the current limit value to $I_{LIMOCT(short2GND)}$. However, due to the maximum rating of the allowed current through OCT-pin I_{OCT}, it is not recommended to shorten the OCT-pin to device GND. In case of reverse battery condition, this could lead to violations of the maximum ratings, therefore the I_{OCT} absolute maximum rating needs to be considered. If I_{OCT} exceeds the threshold $I_{OCT(short2GND)}$ it will be reported as a fault flag on the ST-pin. Please note that this fault flag will be set only during ON-state when DEN is set to low. For more details about diagnosis upon being outside the specified I_{OCT} range please refer to Chapter 9.1.

R_{OCT} values causing the I_{OCT} currents below the specified OCT adjust range are not recommended for usage as the resulting current limitation suffers from limited accuracy and hence is not specified.

The adjustable current limitation feature of the ITS6080S-EP-D offers several advantages and flexibility to the user. When adjusting the device to a specific current limitation threshold LIM(th,adj), ensure that between the adjusted current limitation threshold $I_{LIM(th,ad)}$ and the expected nominal current of the application there is a certain distance in order to avoid unwanted activation of the current limitation circuit during normal operation. Table 13 defines the maximum allowable load current for a certain OCT resistor setting.

Please note that when the load current of the device gets close(r) to the adjusted current limitation threshold, the turn on slew rate gets slower, resulting in longer t_{ON} timing, while at the same time corresponding turn off slew rate may become faster leading to shorter t_{OFF} timings.

Keeping the above-mentioned distance ensures that the influence of the current limitation threshold on switching timings is moderate. It is illustrated in Figure 31.

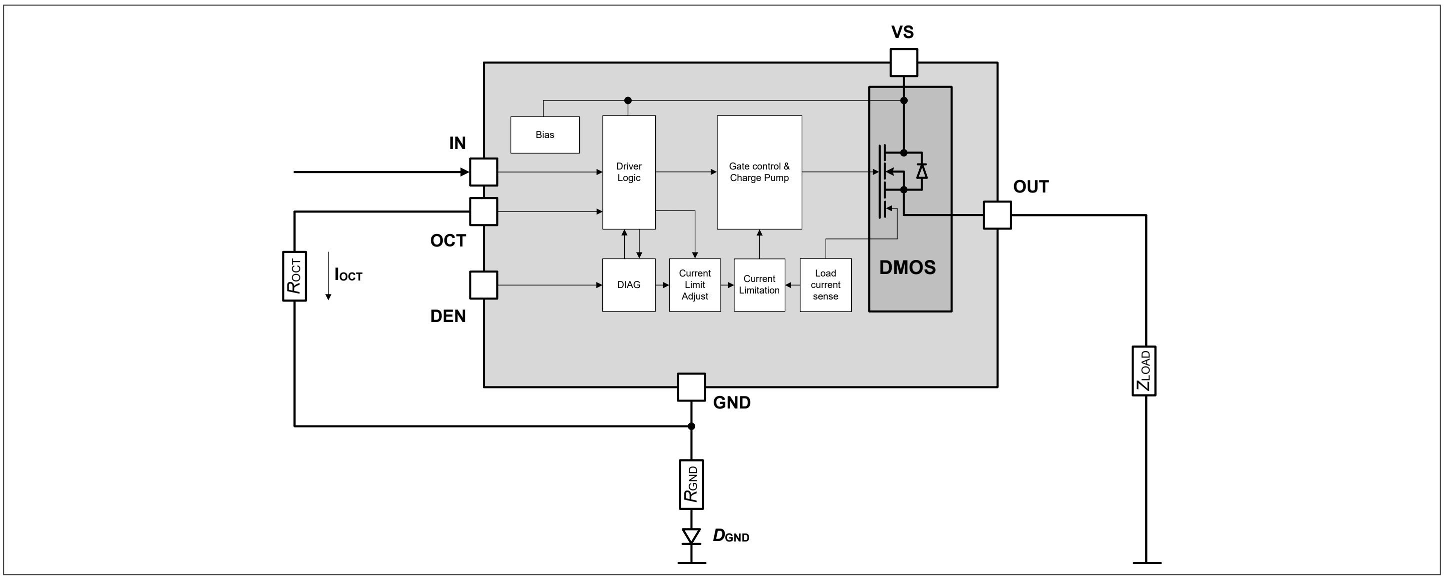


Figure 20 **Adjustment of Current Limit threshold with external resistor R_{OCT}**

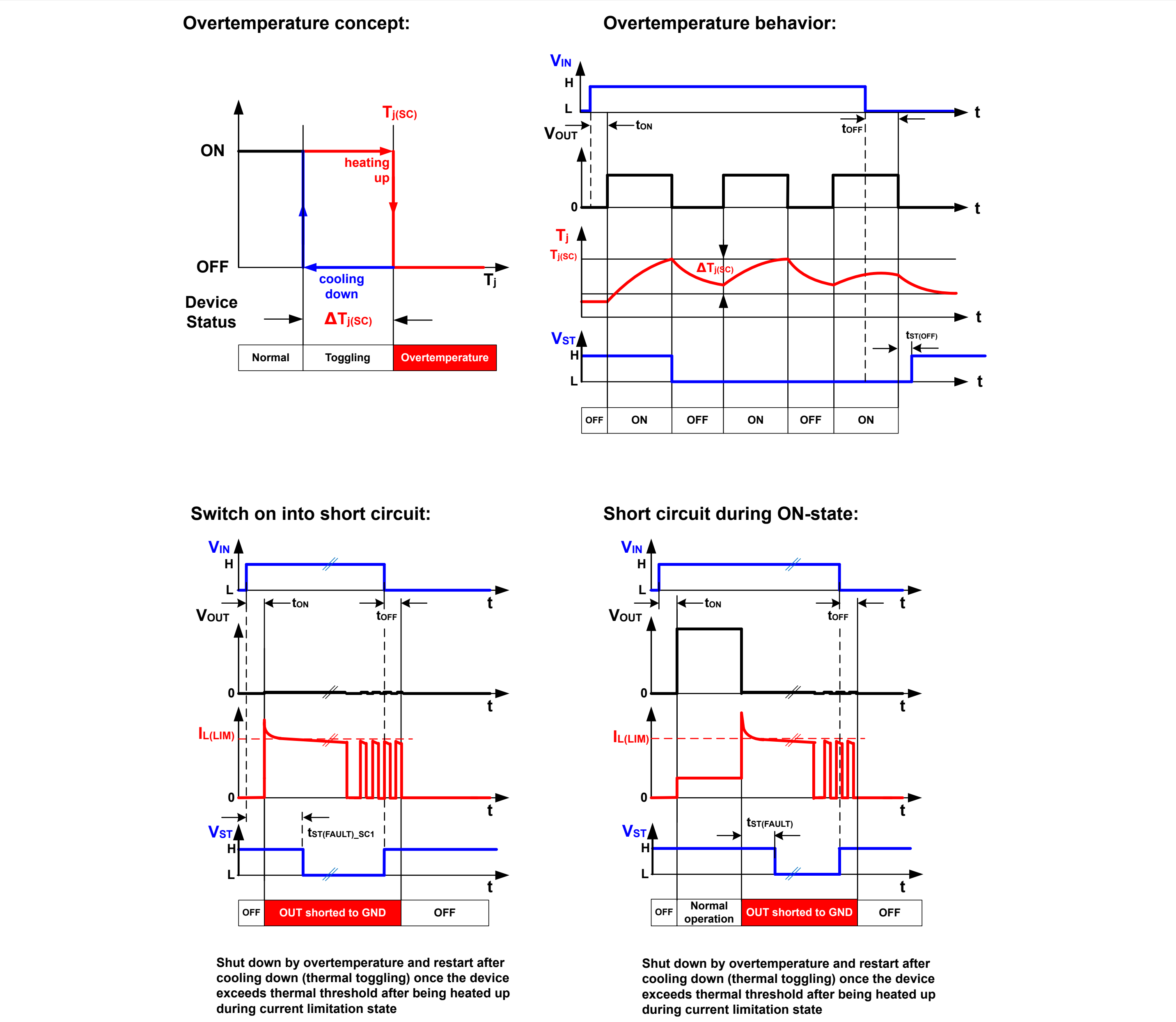


Figure 21 Protection behavior of the ITS6080S-EP-D

7.5.2 Temperature limitation in the power DMOS

The DMOS channel incorporates a temperature sensor concept that allows to detect the absolute junction temperature T_j as well as a temperature gradient resulting of a power stage that heats up too fast. Activation of any of the temperature sensors will cause an overheated channel to switch off to prevent destruction. Any protective overtemperature shutdown event triggered by an overheated channel switches off the output until the temperature reaches an acceptable value again. A restart functionality is implemented that switches the channel on again after the DMOS temperature has sufficiently cooled down.

7.6 Electrical characteristics: Protection functions

Table 6 Electrical Characteristics: Protection Functions

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	1) V_S = 24 V	P_7.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	–	650	700	mV	I_L = -2 A; T_j = 150°C;	P_7.6.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	65	70	75	V	2) I_{SOV} = 5 mA	P_7.6.3
Current limitation							
Allowed I_{OCT} range for adjusting current limit threshold $I_{LIM(th,adj)}$	I_{OCT_range}	6.67	–	97.85	µA	1)	P_7.6.4
OCT-pin voltage	V_{OCT}	0.46	0.5	0.55	V	V_{IN} = high; 6.67 µA ≤ I_{OCT} ≤ 97.85 µA	P_7.6.16
Current limitation value in case of OCT-pin short to device ground	$I_{LIMOCT(short2GND)}$	–	7.78	–	V	1) $I_{OCT} \geq I_{OCT(short2GND)}$	P_7.6.47
Current limitation with setting I_{OCT} < 6.67 µA (corresponds to R_{OCT} > 75 kΩ)							
Current limit when OCT-pin is detected open	$I_{LIM\_int(MIN)}$	–	0.75	–	A	1) 4)	P_7.6.46
Current limitation with setting I_{OCT} = 6.67 µA (corresponds to R_{OCT} = 75 kΩ)							
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 6.67 µA)	I_{LIM}	0.36	0.85	1.30	A	3) I_{OCT} = 6.67 µA (R_{OCT} = 75 kΩ); 25°C ≤T_j ≤ 150°C	P_7.6.19
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 6.67 µA)	I_{LIM}	0.24	0.79	1.39	A	I_{OCT} = 6.67 µA (R_{OCT} = 75 kΩ); T_j = -40°C	P_7.6.35

(table continues...)

Table 6 (continued) Electrical Characteristics: Protection Functions

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current limitation with setting I_{OCT} = 27.47 µA (corresponds to R_{OCT} = 18.2 kΩ)							
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 27.47 µA)	I_{LIM}	0.83	1.41	1.98	A	3) I_{OCT} = 27.47 µA (R_{OCT} = 18.2 kΩ); 25°C ≤ T_j ≤ 150°C	P_7.6.37
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 27.47 µA)	I_{LIM}	0.78	1.46	2.22	A	I_{OCT} = 27.47 µA (R_{OCT} = 18.2 kΩ); T_j = -40°C	P_7.6.38
Current limitation with setting I_{OCT} = 50 µA (corresponds to R_{OCT} = 10 kΩ)							
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 50 µA)	I_{LIM}	1.47	2.17	2.88	A	3) I_{OCT} = 50 µA (R_{OCT} = 10 kΩ); 25°C ≤T_j ≤ 150°C	P_7.6.22
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 50 µA)	I_{LIM}	1.48	2.31	3.24	A	I_{OCT} = 50 µA (R_{OCT} = 10 kΩ); T_j = -40°C	P_7.6.41
Current limitation with setting I_{OCT} = 97.85 µA (corresponds to R_{OCT} = 5.11 kΩ)							
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 97.85 µA)	$I_{LIM\_int(MAX)}$	3.22	5.16	7.46	A	3) 4) 5) I_{OCT} = 97.85 µA (R_{OCT} = 5.11 kΩ); 25°C ≤T_j ≤ 150°C	P_7.6.6
Current limitation $I_{LIM} = I_{LIM}$ (I_{OCT} = 97.85 µA)	$I_{LIM\_int(MAX)}$	2.92	5.50	8.34	A	4) 5) I_{OCT} = 97.85 µA (R_{OCT} = 5.11 kΩ); T_j = -40°C	P_7.6.45
Thermal Protection							
Dynamic thermal shutdown protection threshold (temperature gradient within IC)	$T_{j(SW)}$	–	80	–	K	1)	P_7.6.8
Thermal shutdown temperature (absolute T_J)	$T_{j(SC)}$	150	175	200	°C	1)	P_7.6.10
Thermal shutdown hysteresis	$\Delta T_{j(SC)}$	–	30	–	K	1)	P_7.6.11

1) Not subject to production test; specified by design
2) During transient overvoltage events the current through the GND path needs to be limited. It is recommended to place a resistor in the range of ≥ 27 Ω into the GND path if transient overvoltage events have to be considered in the application
3) Test at T_j = 150°C

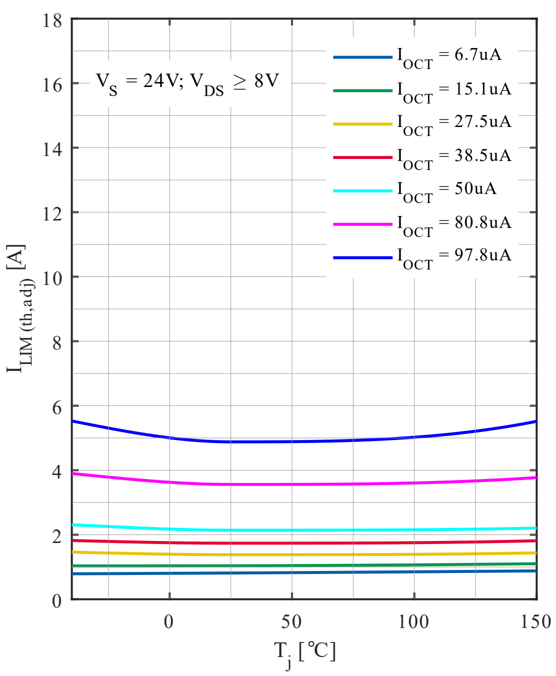
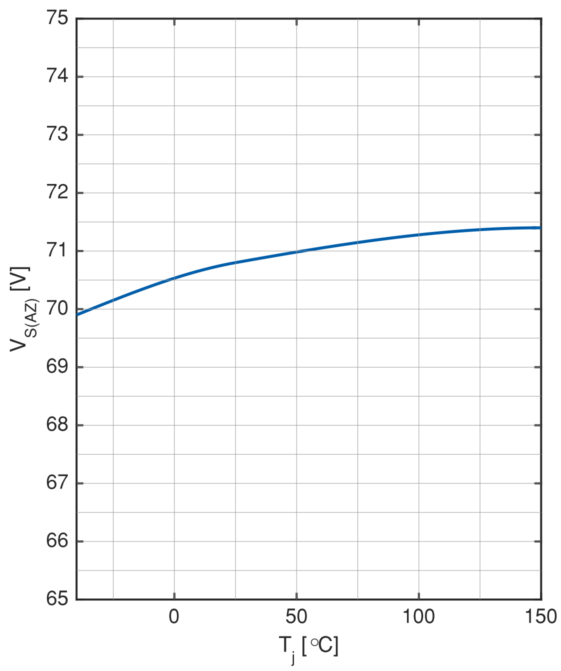
4) Please note that operation above allowed I_{OCT} range is considered as fault condition and will be flagged on the ST-pin. For further details please refer to Chapter 9.1 and Chapter 9.2

5) Without a properly dimensioned R_{OCT} the device can be damaged under reverse polarity condition

7.7 Typical performance characteristics protection functions

Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

Current limit $I_{LIM(th,adj)}$ versus junction temperature T_j	Clamping voltage $V_{S(AZ)}$ versus junction temperature T_j
	

8 Discharge functionality

8.1 Discharge functionality

The discharge feature of ITS6080S-EP-D offers a transient discharge path to device ground. It is realized with a dedicated pin (DC-pin) and a pull-down circuit to device GND, as shown in Figure 22. If the usage of the DC feature is desired, the output pins (OUT) need to be connected externally to the DC-pin (see more detailed explanation below). If the functionality is not needed, the DC-pin can be left open or tied with a series resistor to device GND.

As long as the device is in ON-state, the DC function is inactive and the impedance of DC-pin is HiZ. The DC-pin can be used for a faster discharge of the output or as a trigger signal for external discharge circuits. The discharge functionality is triggered automatically when the channel is switched off and is active for a duration of t_{DC}.

After channel deactivation, there are two ways the discharge is triggered internally

- Drain-source voltage, V_{DS} of the DMOS falls below the threshold $V_{DS\_DC\_on}$
- After the time-out delay, $t_{SW(OFF)\_TO}$, in case the $V_{DS\_DC\_on}$ threshold had not been reached previously

Both options are shown in Figure 23.

The DC function is only activated if no other discharge event occurs within the activation window. If within the activation window, $V_{DS\_DC\_on}$ threshold is reached multiple times, the t_{DC} duration is reset each time. This means that ongoing discharge event is prolonged by t_{DC}. This reduces potential oscillations on the output more effectively. After $t_{SW(OFF)\_TO}$ is expired, no further activations of the discharge function are triggered until the channel gets reactivated. The typical averaged discharge current capability of the DC-pin is specified as I_{DC_sink}. After t_{DC} has expired the DC-pin becomes HiZ, until it is triggered again.

Any change of the input level of the IN-pin from low to high that switches the channel into ON-state will immediately interrupt an ongoing discharge event and the DC-pin will become HiZ again. A timing overview of the DC-pin functionality is summarized in Figure 23 and Table 7.

During ON-state the DC-pin remains always HiZ. If the device shuts off due to an overvoltage event and enters the OVLO active mode, the DC-pin will not become active. Ongoing discharge events are immediately terminated if a voltage above the OVLO threshold is detected by the device.

When the DC-pin is used to discharge the output, it is mandatory to place an external diode, D_{DC}, between OUT and DC-pin to avoid interferences between the DC-pin and the active clamping mechanism of the IC. D_{DC} blocks the current through the body diode of the discharge FET during switching off inductive loads. Without the diode the intended operation could be disturbed, the switch off timings could be influenced and the discharge path could be overstressed and damaged. In addition, this diode ensures proper loss of GND protection when using the DC-pin to discharge the output. For any use case where the DC-pin could be pulled below device GND during operation, the diode D_{DC} has to be used.

***Note**: Please take note that the presence of the D_{GND} does not mean that the blocking diode D_{DC} can be excluded.*

In addition, depending on the output voltage, a resistor, R_{DC}, must be placed in series to the diode in order to limit the power dissipation inside the discharge circuit of the IC. The value of the resistor must be chosen in a way that the voltage drop over the DC-pin is limited to V_{DC_act}. The formula for calculating the discharge resistor R_{DC} is shown in (4).

$$R_{DC} = \frac{V_{OUT} - V_{DC\_act}}{I_{DC\_sink}} \qquad (4)$$

***Note**: For 24 V applications the recommended value for R_{DC} is ≥ 50 Ohm.*

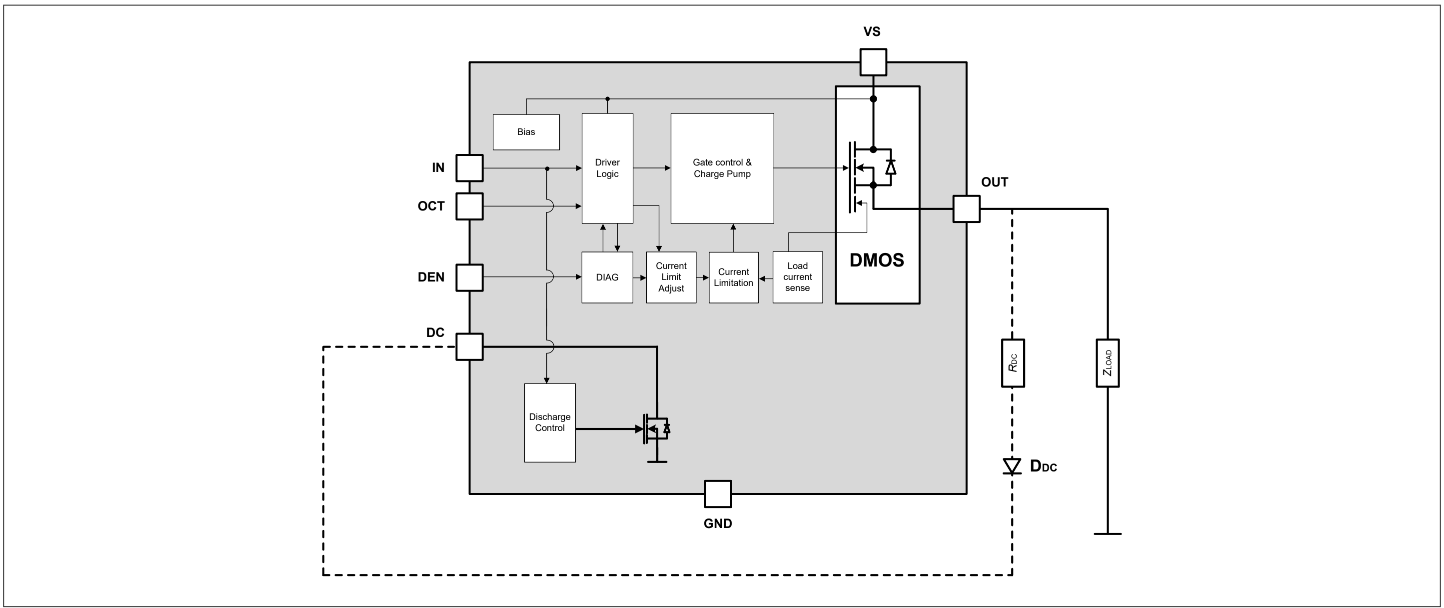


Figure 22 **Discharge pin functionality**

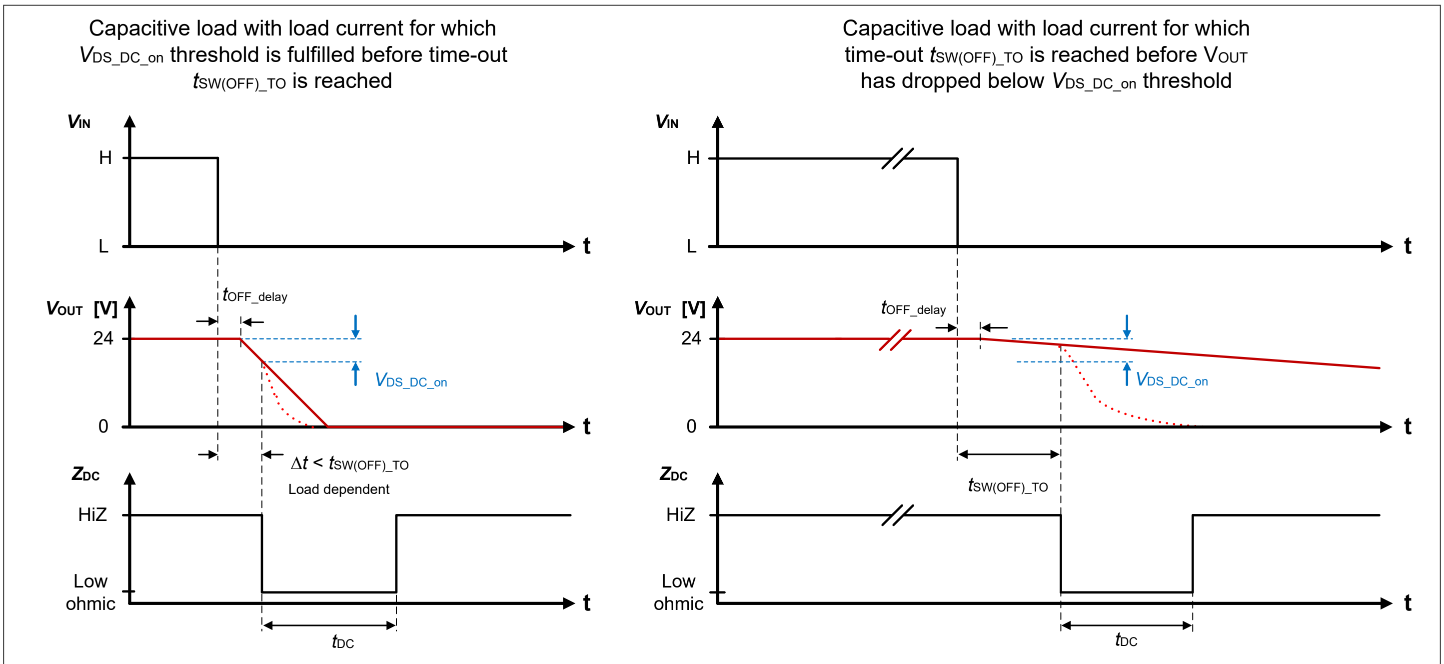


Figure 23 **Dynamic timing behavior discharge pin (dashed lines indicate possible examples of the output voltage when DC-pin used to discharge output)**

Table 7 **Dynamic DC-pin activation/deactivation after switching of the channel during normal operation**

IN	Criteria when DC - path *becomes* active/inactive after trigger event	I_{DC_sink} (T_j = 25°C; V_{DC_act} ~ 20 V)	Duration	Comment
H	–	– (HiZ)	static	In ON-state (active mode) DC-pin remains always HiZ

(table continues...)

Table 7 **(continued) Dynamic DC-pin activation/deactivation after switching of the channel during normal operation**

IN	Criteria when DC - path *becomes* active/inactive after trigger event	I_{DC_sink} (T_j = 25°C; V_{DC_act} ~ 20 V)	Duration	Comment
H → L	When V_{DS} reaches $V_{DS\_DC\_on}$ but latest after $t_{SW(OFF)\_TO}$ following a negative IN edge	~ 145 mA	t_{DC}	Channel being switched off triggers a discharge event of duration t_{DC}
L → H	t_{DC_off}	– (HiZ)	static	Switching channel on will stop any potentially ongoing discharge event

8.2 Electrical characteristics: Discharge functionality

Table 8 Electrical characteristics: Discharge functionality

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

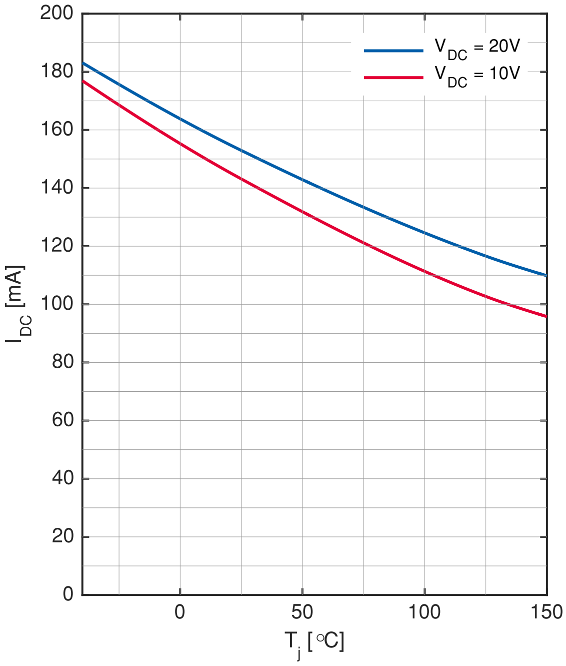
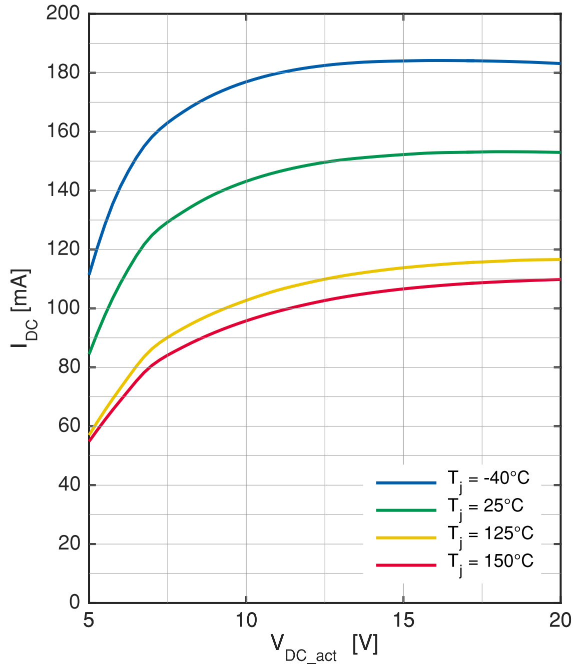
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
DC-pin currents							
Current sink capability of active DC-pin	I_{DC_sink}	80	145	160	mA	[1] 25°C ≤ T_j ≤ 150°C; $V_{DC\_act} < V_S$ From DC-pin to device GND For duration t_{DC} after trigger event	P_8.2.1
Current sink capability of active DC-pin	I_{DC_sink}	–	170	–	mA	[1] 10 V ≤ V_{DC_inact} ≤ 20 V; T_j = - 40°C; $V_{DC\_act} \leq V_S$ From DC-pin to device GND For duration t_{DC} after trigger event	P_8.2.8
DC-pin leakage current when inactive	$I_{DC\_leakage}$	–	–	5	uA	$V_S = V_{DC\_inact} \leq 30$ V; DC-pin inactive for at least 500 µs From DC-pin to device GND	P_8.2.9
DC-pin timings and threshold							
V_{DS} drain-source voltage threshold for activation of discharge pin	$V_{DS\_DC\_on}$	–	3	–	V	[1] V_S = 24 V After transition from high to low of IN-pin	P_8.2.6
Discharge duration (DC - pin conductive) after activation	t_{DC}	150	250	410	µs	V_S = 24 V	P_8.2.3
Deactivation delay of an ongoing discharge event	t_{DC_off}	–	3	–	µs	[1] Interrupt by transition from low to high of IN-pin	P_8.2.4

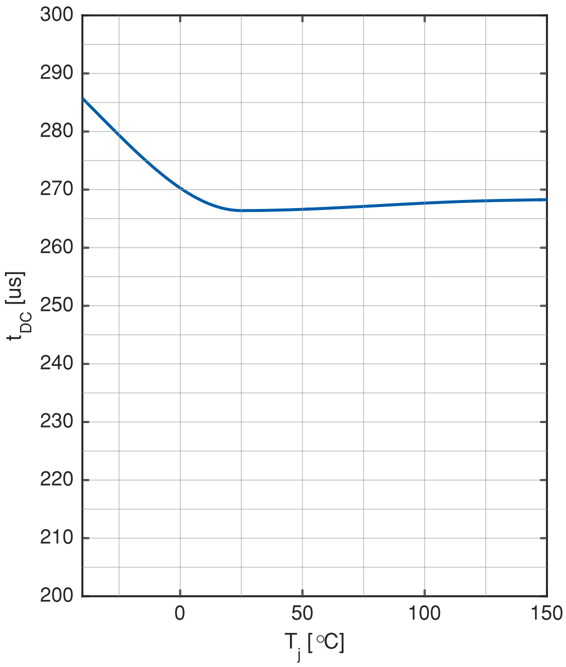
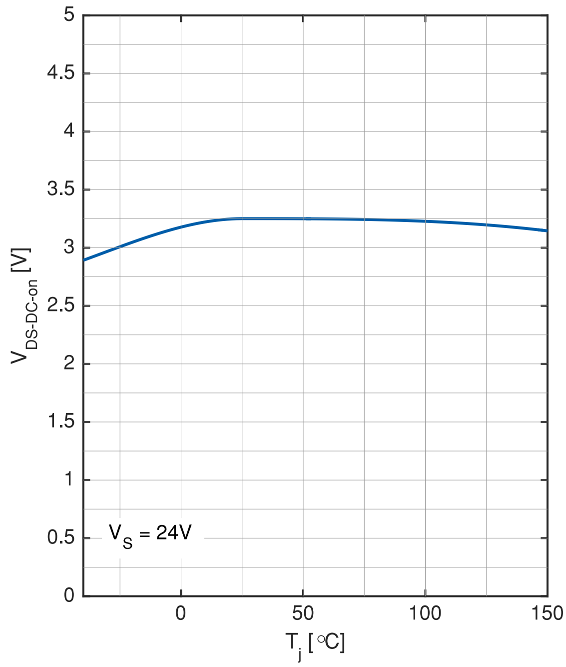
1) Not subject to production test; specified by design

8.3 Typical performance characteristics: Discharge functionality

Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

DC-pin sink current I_{DC_sink} (during t_{DC}) versus junction temperature T_j	DC-pin sink current I_{DC_sink} versus DC-pin voltage V_{DC_act}
	

Discharge duration t_{DC} versus junction temperature T_j	Discharge activation threshold $V_{DS\_DC\_on}$ versus junction temperature T_J
	

9 Diagnostic functions

The ITS6080S-EP-D is able to provide detailed diagnosis information during operation. The diagnosis information can be split into basic diagnosis and extended diagnosis. The basic diagnosis is continuously monitored during the ON-state of the device and given as digital signal to the user via the ST-pin. The only basic diagnosis that is monitored in both, ON-state and OFF-state is the overvoltage lockout detection.

The basic diagnosis comprises:

- Overload/short circuit to GND
- Overtemperature (during ON-state)
- Persisting overvoltage leading to an OVLO event (during ON-state and OFF-state)
- Violation of minimum allowed R_{OCT} (e.g. OCT-pin shorted to GND)

In addition to the basic diagnosis there is also an extended diagnosis that needs to be requested by the DEN-pin.

The extended diagnosis comprises:

- Digital open load detection during ON-state
- Digital open load detection during OFF-state (in combination with external pull-up resistor)
- Digital feedback on Short to V_S during OFF-state (in combination with external pull-down resistor)
- Overtemperature during OFF-state
- I_{OCT} is monitored continuously in ON-state. If $I_{OCT} > I_{OCT(short2GND)}$, a fault state is flagged on ST during ON-state as long as DEN is set to low. In order to be able to distinguish this specific fault condition from overtemperature and overload or overvoltage faults, this flag is blanked if DEN is set to high but re-flagged if DEN is set to low again in case the fault condition persists, as shown in Table 9

Figure 24 and Figure 25 illustrate the timings of basic and extended diagnosis functionality while Figure 26 shows a simplified application example.

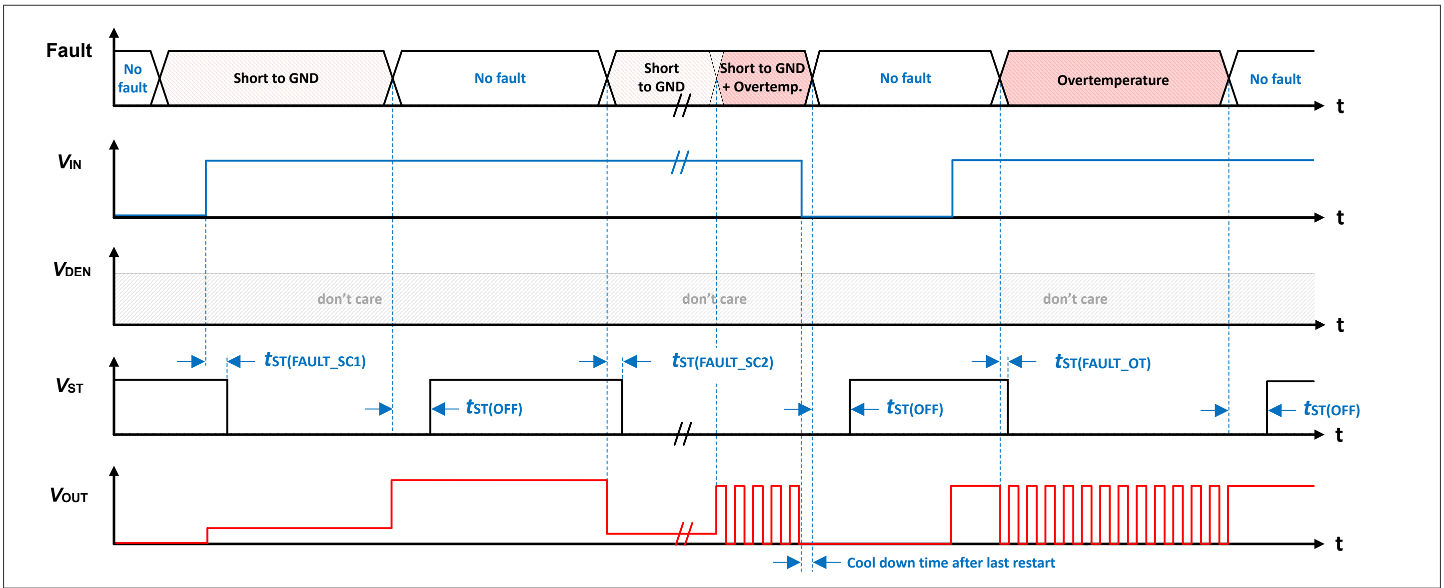


Figure 24 **Behavior and timings of basic diagnosis**

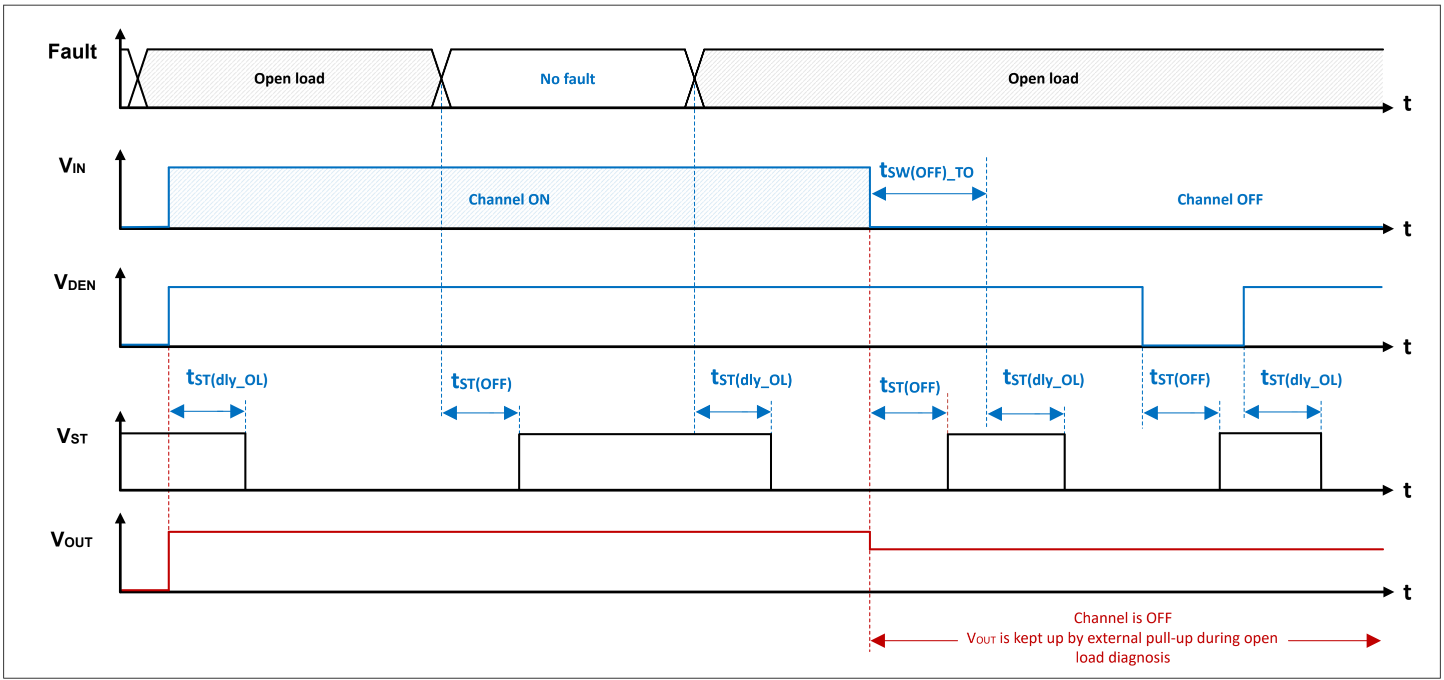


Figure 25 **Behavior and timings of the extended diagnostic "open load detection" (the usage of a DEN - controlled switchable pull-up resistor from OUT to V_S in OFF-state is assumed)**

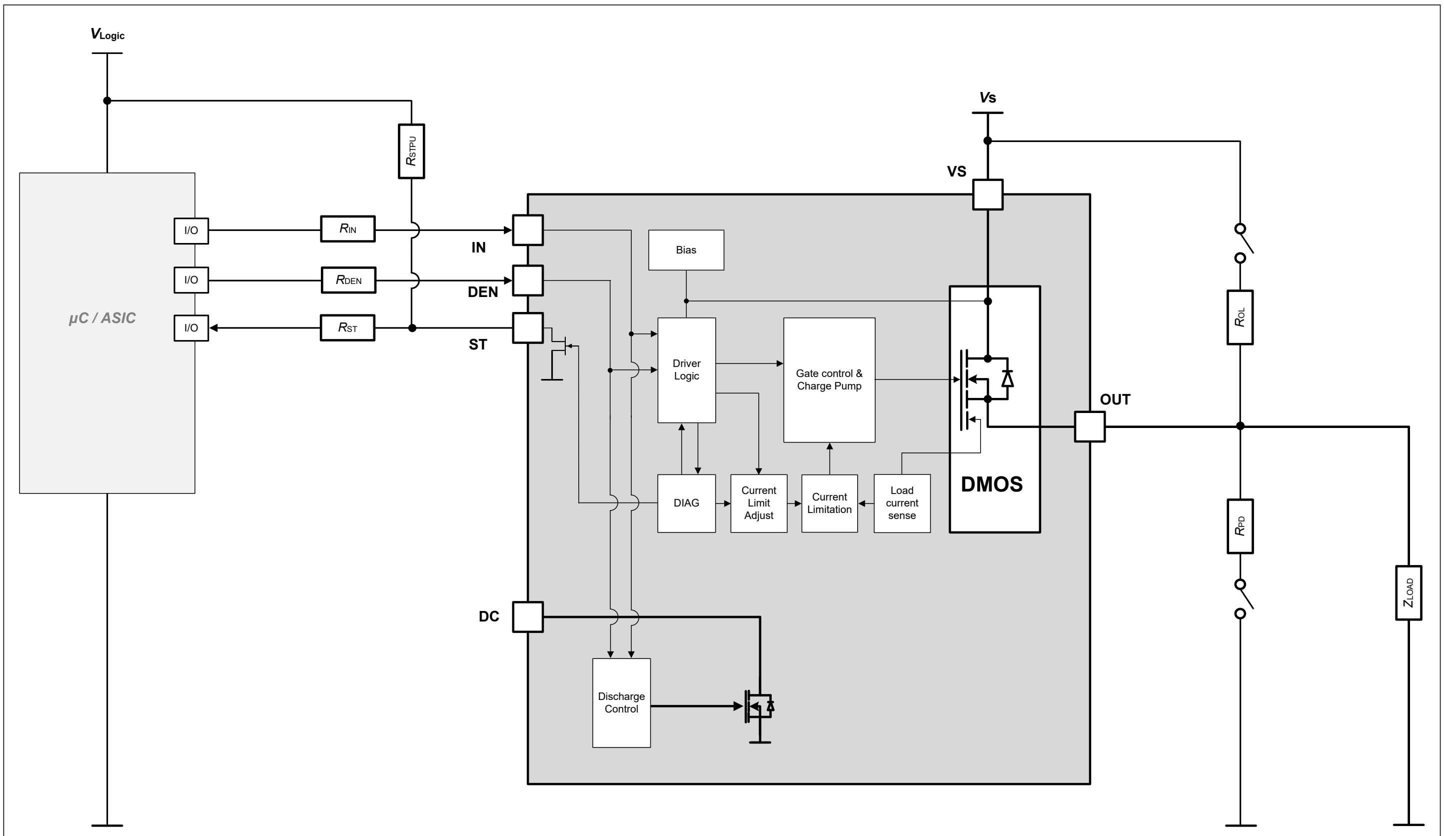


Figure 26 **Overview: usage of diagnosis**

9.1 Digital status flag ST (STATUS)

The ITS6080S-EP-D provides a digital signal for diagnostic information on the ST-pin. This signal is called STATUS. The ST-pin is realized as open drain output and must be connected to an external pull-up resistor to either logic supply or to V_S. During normal operation the STATUS signal is logic high (H). When the device is in ON-state the presence of the fault conditions short circuit to ground, overtemperature, overvoltage lockout or a violation of the allowed minimum resistance of R_{OCT} is flagged by a logic low (L) level on the ST-pin. Table 9 shows the truth table of the ST-pin output. During the OFF-state of the device the ST-pin is flagging only the presence of an overvoltage lockout by default (i.e. independent of the state of DEN). In addition, the extended diagnosis information for detection of open load is also flagged on the ST-pin during OFF-state indicating the presence of an open load condition (OL) in OFF. Open load in OFF-state as well as in ON-state will be flagged on the ST only after the blanking time $t_{ST(dly\_OL)}$ has elapsed which means after the device has been monitored in this fault condition continuously throughout the blanking time. The blanking time counter for $t_{ST(dly\_OL)}$ is always started with the rising DEN edge except directly after switching off the channel. After switching off the channel the open load blanking time counter is started earliest after the switch off time-out delay $t_{SW\_OFF\_TO}$. This means that an open load fault in OFF-state can be detected earliest after $t_{SW\_OFF\_TO}$ + $t_{ST(dly\_OL)}$ referenced to the falling IN edge (for details see also Figure 25). The open load detection in OFF-state is realized by a voltage comparator at the output. If the output voltage is staying or getting closer to V_S than a threshold (V_S - $V_{OUT(OL)}$) for a duration of t > $t_{ST(dly\_OL)}$ the flag is set. This means that for open load detection in OFF-state an external pull-up resistor to V_S must be applied. Adjusting the resistance of the pull-up resistor allows to adjust the desired open load criteria. In the same manner also short circuit to V_S can be realized with a pull-down resistor. In both cases it is recommended to use pull-up or pull-down circuits that can be switched off while not being used to minimize power dissipation. Diagnosis of open load in OFF-state and diagnosis of OUT shorted to V_S cannot be evaluated simultaneously. If both diagnosis features are applied in the same application, the corresponding required external pull-up or pull-down circuits must be controlled with external switches. Open load diagnosis in OFF-state as is open load in ON-state must be requested via the DEN signal. Without setting the DEN-pin to high no open load diagnosis is flagged on ST.

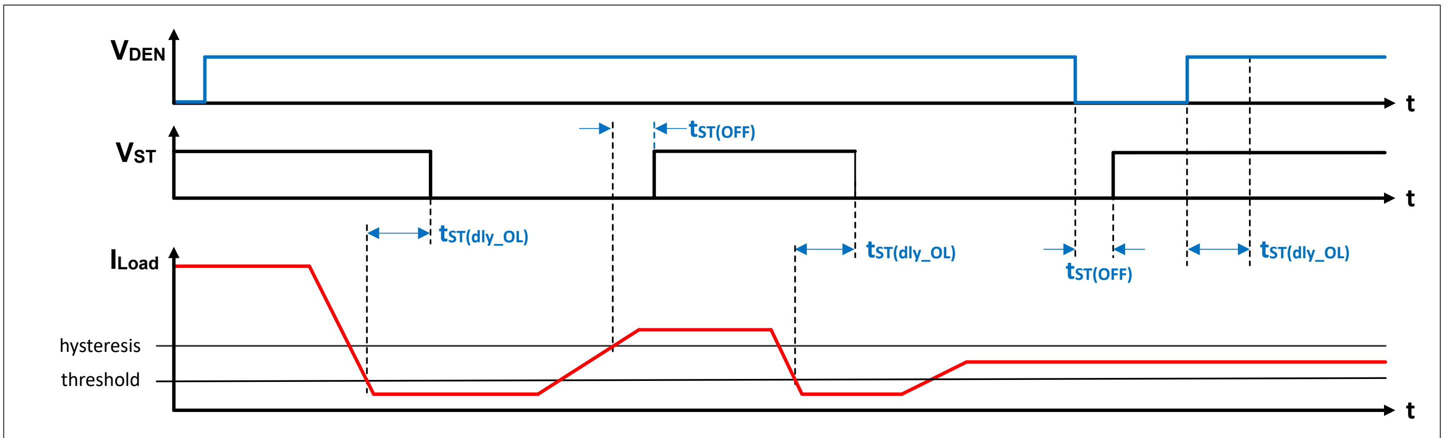


Figure 27 **Criteria for entering and exiting open load detection during ON-state**

Table 9 **Diagnostic truth table ST-pin**

Condition	**IN**	**DEN** [1)]	**OUT**	**ST** [2)]	**Comment**
ON-state					
Normal Operation	H	X	ON	H	–
Short circuit to GND	H	X	ON	L	Resetting of ST flag takes place $t_{ST(OFF)}$ after overload condition has cleared

(table continues...)

Table 9 (continued) Diagnostic truth table ST-pin

Condition	IN	DEN [1]	OUT	ST [2]	Comment
Overtemperature[3]	H	X	OFF [4]	L	Resetting of ST flag takes place a time $t_{ST(OFF)}$ after cooling down has been achieved
Overvoltage lockout event (V_S overvoltage > $V_{S(OV)\_LO}$ persisting for t > t_{OV_BLK})	H	X	OFF [5]	L	Overvoltage lockout becomes active after blanking time t_{OV_BLK} has elapsed
Open load condition	H	H	ON	L	[6] Fault recognized if $I_L < I_{OL}$ persists for longer than blanking time $t_{ST(dly\_OL)}$
Open load condition	H	L	ON	H	Open load in ON-state not diagnosed as long as DEN is not activating extended diagnosis
I_{OCT} exceeding the specified range (e.g. if OCT-pin is shorted to GND)	H	L	ON	L	[7] I_{OCT} is monitored continuously in ON-state. If I_{OCT} is found outside the limit, $I_{OCT(short2GND)}$ is flagged as fault state on ST during ON-state, as long as DEN is set to low. To distinguish this specific fault condition from overtemperature and overload or overvoltage faults, this flag is blanked if DEN is set to high. If the fault condition persists, it gets re-flagged if DEN is set to low.
	H	H	ON	H	
OFF-state					
Open load condition	L	L	OFF	H	Open load in OFF not diagnosed unless extended diagnosis requested by DEN = high
Open load condition	L	H	OFF	L	[8] [9] Requires external pull-up attached from OUT to V_S
OUT shorted to V_S	L	H	OFF	L	Requires external pull-down attached from OUT to GND
Overtemperature	L	H	OFF	L	–
Overvoltage lockout event (V_S > $V_{S(OV)\_LO}$ persisting for t > t_{OV_BLK})	L	X	OFF	L	OVLO is continuously monitored also in OFF-state independent of DEN
Any fault condition except OVLO with DEN set to low	L	L	OFF	H	–

1) "X" denotes that logic level of DEN is irrelevant ("don't care")

2) External pull-up resistor needs to be placed at ST-pin
3) This fault condition can be caused by both - a violation of the maximum allowed T_j but as well by exceeding the maximum allowed temperature gradient $T_{j(SW)}$ within the IC
4) Automatic restart after T_j has sufficiently cooled down
5) Automatic restart after overvoltage event has cleared
6) The status flags get released if the load current is rising up to a value which is higher than the I_{OL} threshold plus the built-in hysteresis I_{OL_hys} or if the extended diagnosis is switched off by setting the DEN-pin back to low. In both cases additionally $t_{ST(OFF)}$ applies
7) Please note that $t_{ST(OFF)}$ will apply when DEN is set from low to high until ST-flag for indicating I_{OCT} outside the limits is cleared
8) Flag will be set after blanking time $t_{ST(dly\_OL)}$ has elapsed
9) Please note that for this fault condition the ST flag is reset directly after the fault situation has cleared. $t_{ST(OFF)}$ does not apply

9.2 Electrical characteristics: Diagnostic functions

Table 10 Electrical characteristics: Diagnostic functions

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Basic diagnostics (ST-pin)							
Status settling time for channel start-up into existing overload (from IN slope to ST low)	$t_{ST(FAULT\_SC1)}$	–	50	–	µs	$V_{DS} \geq$ 5 V	P_9.4.1
Status settling time for channel entering short circuit condition during ON-state (from point where SC is reached to ST low)	$t_{ST(FAULT\_SC2)}$	–	25	–	µs	1) $V_{DS} \geq$ 5 V	P_9.4.2
Status settling time for over-temperature indication on ST-pin	$t_{ST(FAULT\_OT)}$	–	5	–	µs	1)	P_9.4.3
Status blanking time for open load detection (device in stable OFF-state or stable ON- state)	$t_{ST(dly\_OL)}$	–	215	–	µs	–	P_9.4.4
Time-out before status blanking delay timer for open load diagnostics can be started after entering OFF-state	$t_{SW(OFF)\_TO}$	–	195	–	µs	1)	P_9.4.34
Status reset blanking time	$t_{ST(OFF)}$	–	120	–	µs	1)	P_9.4.26
Low level status voltage	$V_{ST(L)}$	–	–	0.5	V	2) I_{ST} = 1.6 mA	P_9.4.5
Open load detection current threshold in ON-state	I_{OL}	4	15	35	mA	$V_{IN} = V_{DEN}$ = high load current dropping from higher values	P_9.4.8
Open load detection reset hysteresis in ON-state	I_{OL_hys}	–	5	–	mA	$V_{IN} = V_{DEN}$ = high (statistical data should be derived from test)	P_9.4.35
Open load detection voltage threshold in OFF-state	$V_S - V_{OUT(OL)}$	4	4.45	6	V	3) V_{IN} = low; V_{DEN} = high	P_9.4.10

(table continues...)

Table 10 (continued) Electrical characteristics: Diagnostic functions

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
OCT-pin short to ground detection threshold in ON-state	$I_{OCT(short2GND)}$	150	–	240	µA	V_{IN} = high; V_{DEN} = low; I_{OCT} exceeding allowed range to higher values (ST will go from high to low	P_9.4.30
OCT-pin short to ground reset hysteresis	$I_{OCT(S2G\_reset)}$	–	25	–	µA	V_{IN} = high; V_{DEN} = low; I_{OCT} going from fault range to pass range (ST will go from low to high	P_9.4.37

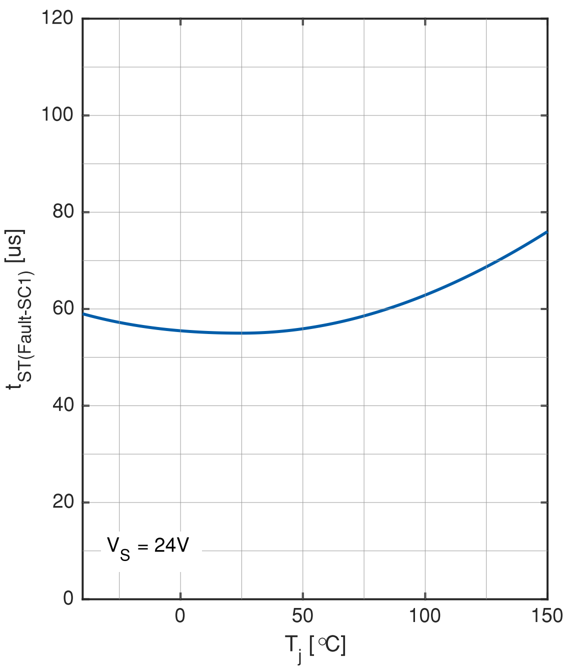
1) Not subject to production test, specified by design
2) Levels referenced to device ground
3) Level for open load detection in OFF referenced to V_S

9.3 Typical performance characteristics: Diagnostic functions

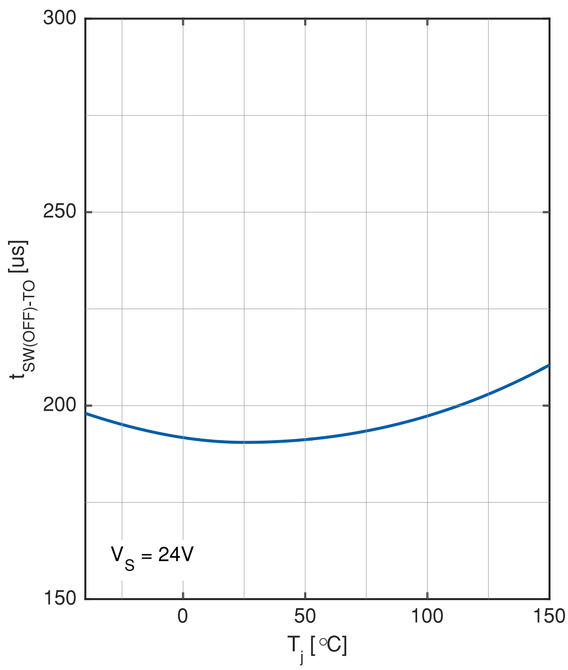
Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

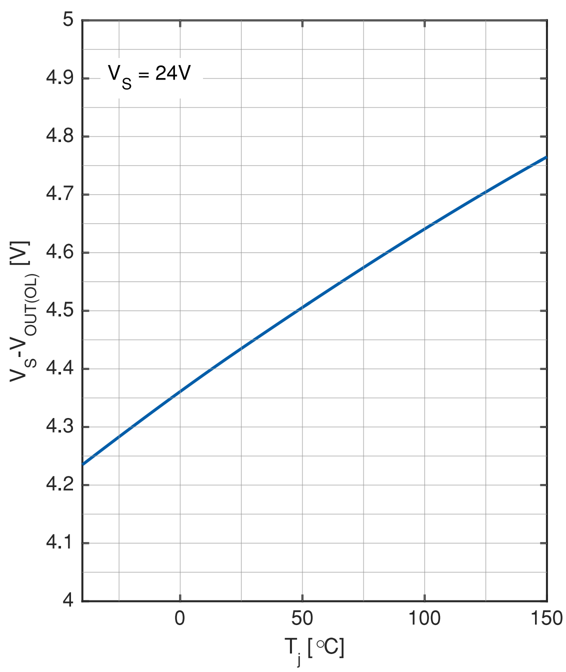
Status settling Time $t_{ST(FAULT\_SC1)}$ versus Junction temperature T_j (switch on into overload)



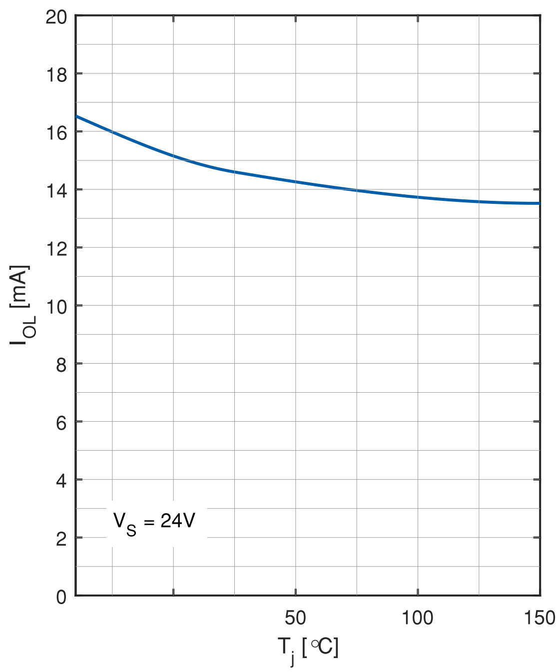
Time-out delay $t_{SW(OFF)\_TO}$ versus Junction temperature T_j



Open load threshold V_S - $V_{OUT(OL)}$ versus Junction temperature T_j



Open load detection threshold I_{OL} in ON versus Junction temperature T_j



10 Control input pins

10.1 Input pin circuitry of control pins (IN and DEN)

The IN-pin and DEN-pin circuitry are compatible with 3.3 V and 5 V microcontrollers as well as input levels up to V_S. V_{IN} must not exceed V_S. The relation $V_{IN} \leq V_S$ must be always fulfilled. The concept of the input pin is to react to voltage thresholds which are referenced to device ground. An implemented Schmitt trigger avoids an undefined state if the voltage on the control pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry of the control pins is compatible with PWM applications. Figure 28 shows the electrical equivalent input pin circuitry.

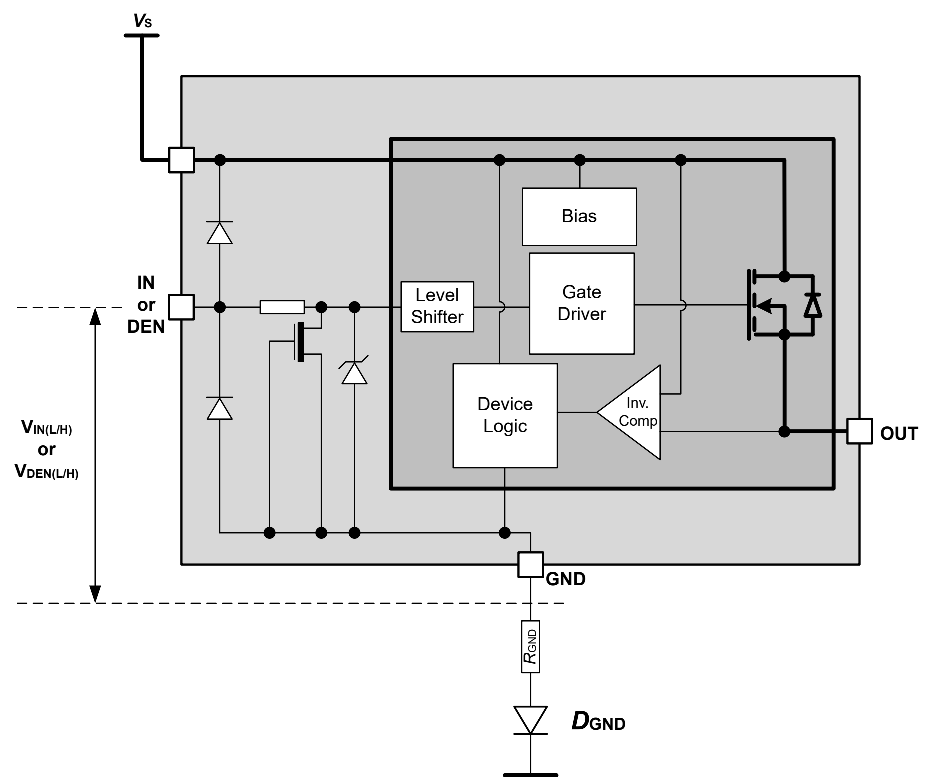


Figure 28 Input pin circuitry

10.2 Input pin voltage (IN and DEN)

The control pins IN and DEN use a comparator with hysteresis which is implemented in order to improve immunity to noise. Switching on/off of the channel takes place in a defined region, set by the thresholds $V_{IN(L),MAX}$ and $V_{IN(H),MIN}$.

10.3 Electrical characteristics: Control input pins

Table 11 Electrical characteristics: Input pins

VS = 8 V to 36 V, Tj = -40°C to 150°C (unless otherwise specified)

Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input pins characteristics							
Low level input voltage range	$V_{IN(L)}$ $V_{DEN(L)}$	-0.3	–	0.8	V	1)	P_10.3.1
High level input voltage range	$V_{IN(H)}$ $V_{DEN(H)}$	2	–	V_S	V	1) $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_10.3.2
Input voltage hysteresis	$V_{IN(HYS)}$ $V_{DEN(HYS)}$	–	250	–	mV	2)	P_10.3.3
Low level input current	$I_{IN(L)}$ $I_{DEN(L)}$	–	35	70	µA	V_{IN} = 0.8 V; V_{DEN} = 0.8 V	P_10.3.4
High level input current	$I_{IN(H)}$ $I_{DEN(H)}$	–	35	70	µA	V_{IN} = 24 V; V_{DEN} = 24 V; $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_10.3.5

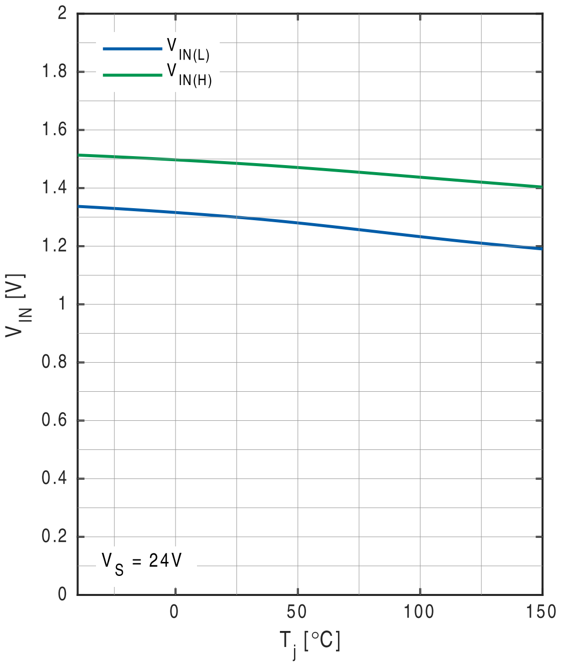
1) Levels referenced to device ground
2) Not subject to production test; specified by design

10.4 Typical performance characteristics: Input pins

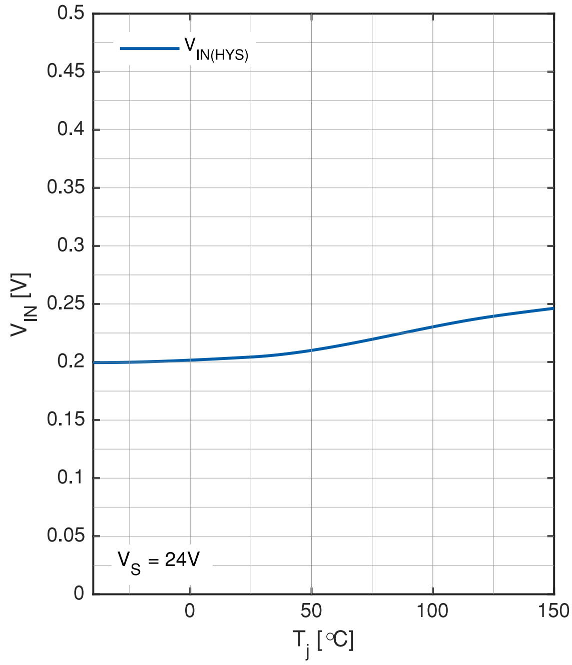
Please note that the data provided in this chapter are typical, based on Infineon's evaluation of a limited number of product samples. Parameters may vary within the minimum and maximum limits as specified.

Typical performance characteristics

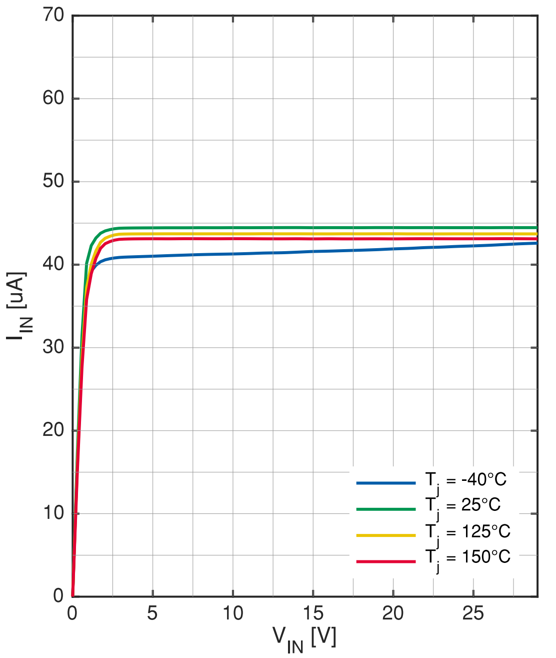
Input voltage thresholds $V_{IN(L)}V_{IN(H)}$ versus
Junction temperature T_j



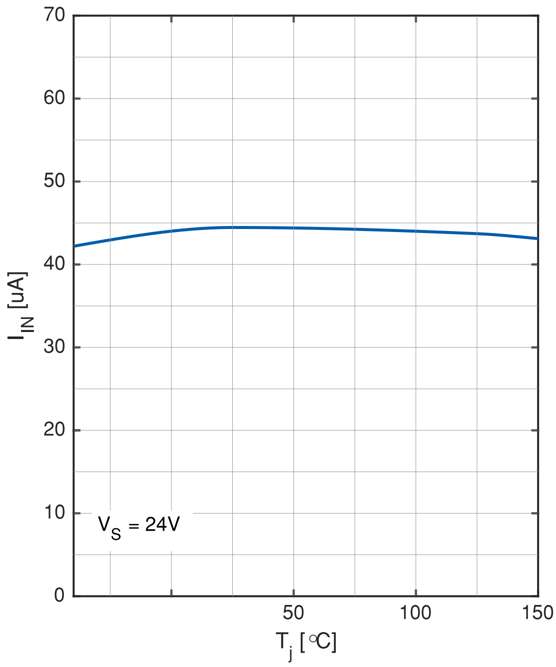
Input voltage hysteresis $V_{IN(HYS)}$ versus
Junction temperature T_j



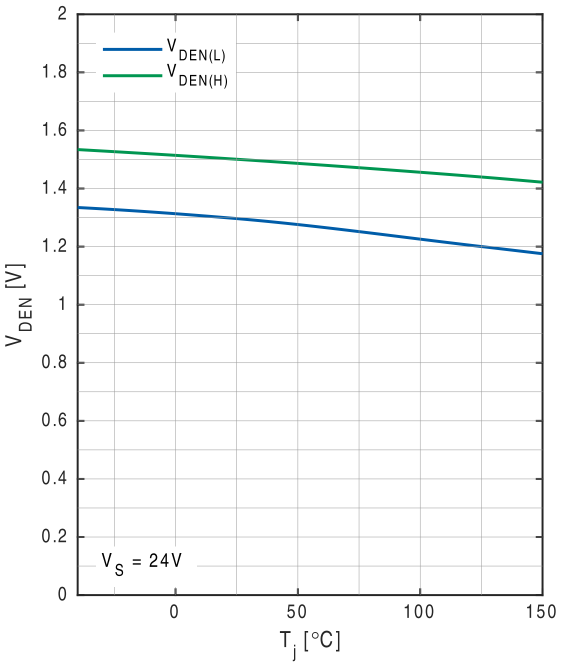
Input pin current $I_{IN(H)}$ versus
Supply voltage V_S



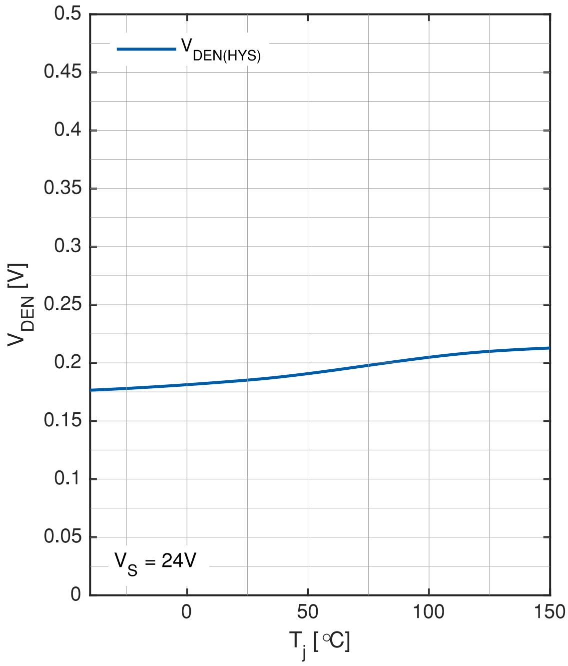
Input pin current $I_{IN(H)}$ versus
Junction temperature T_j



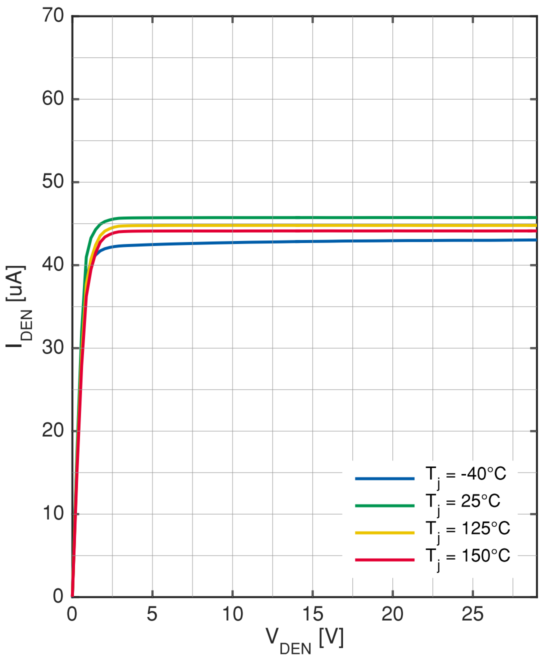
Input voltage thresholds $V_{DEN(L)}V_{DEN(H)}$ versus Junction temperature T_j



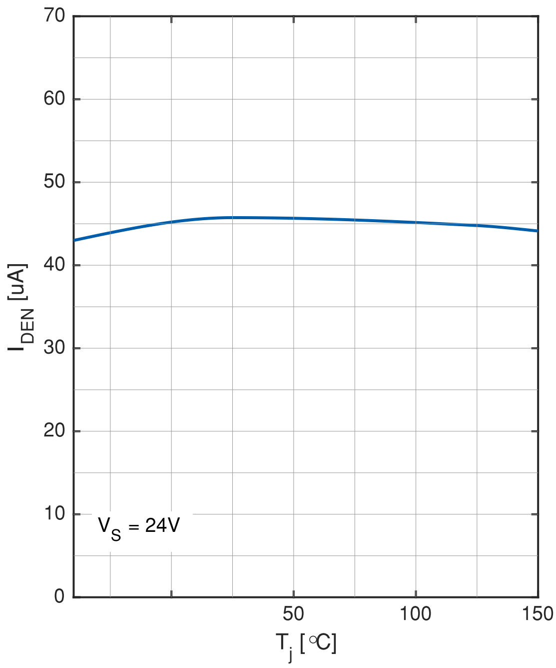
Input voltage hysteresis $V_{DEN(HYS)}$ versus Junction temperature T_j



Input pin current $I_{DEN(H)}$ versus Supply voltage V_S



Input pin current $I_{DEN(H)}$ versus Junction temperature T_j



11 Application information

11.1 Application diagram

***Note**: This is a very simplified example of an application circuit. The function must be verified in the real application.*

Figure 29 and Figure 30 show two simplified application examples where the ITS6080S-EP-D is directly controlled by logic levels of a microcontroller. In Figure 30 the current limitation can be controlled by a microcontroller pin and the DC-pin is used to rapidly discharge the output after being switched off. The usage of a diode in the connection from DC-pin to OUT is mandatory. If the DC-pin is not used, it must be either let open or tied with a series resistor to device ground. The recommended value is 2.2 kΩ. It is recommended to place series input resistors at the interface pins to the microcontroller (IN/DEN) in order to protect the external control circuitry and the input structures of the ITS6080S-EP-D under fault conditions (e.g. reverse polarity, loss of ground or overvoltage).

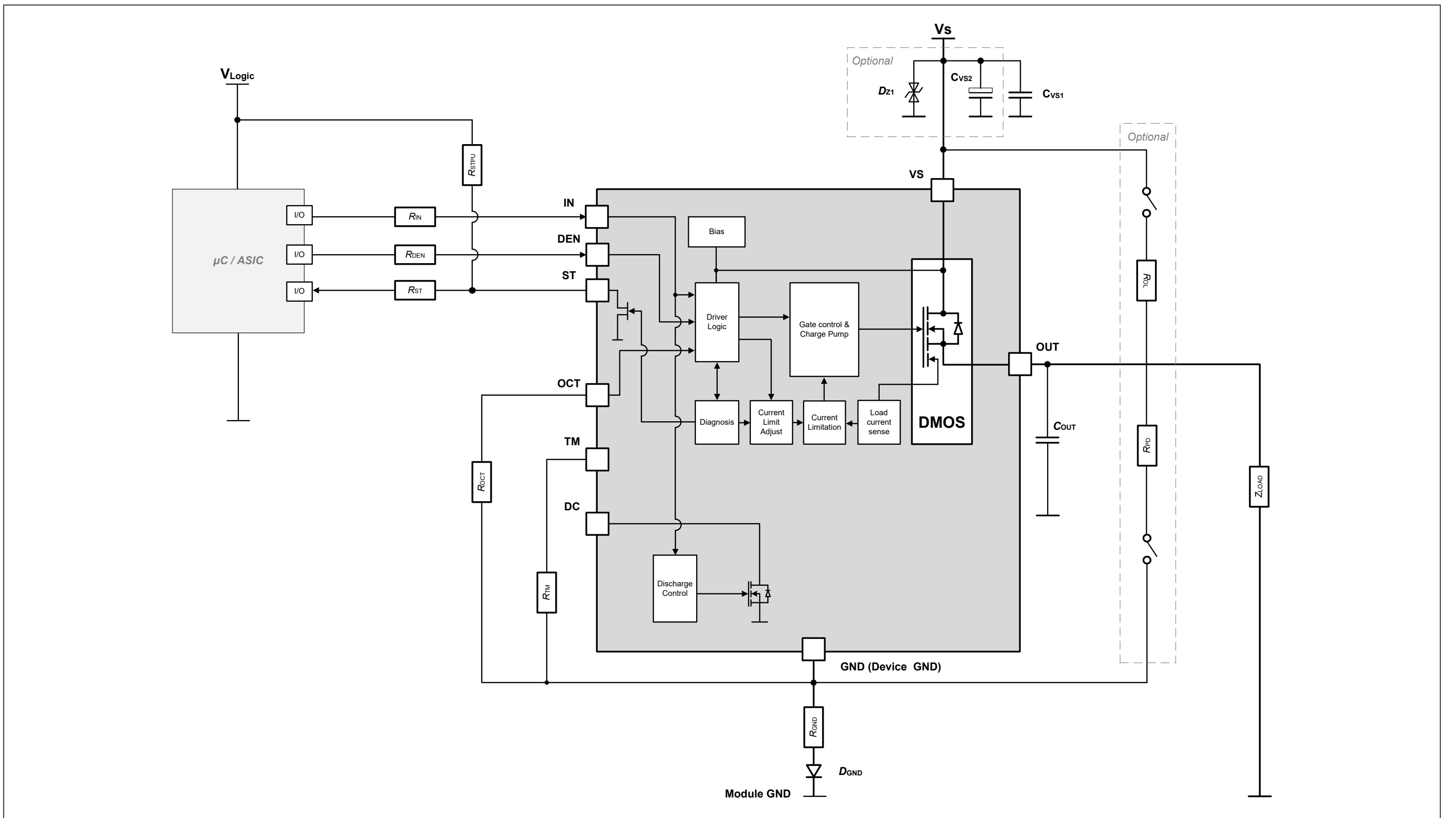


Figure 29 **Application diagram with ITS6080S-EP-D**

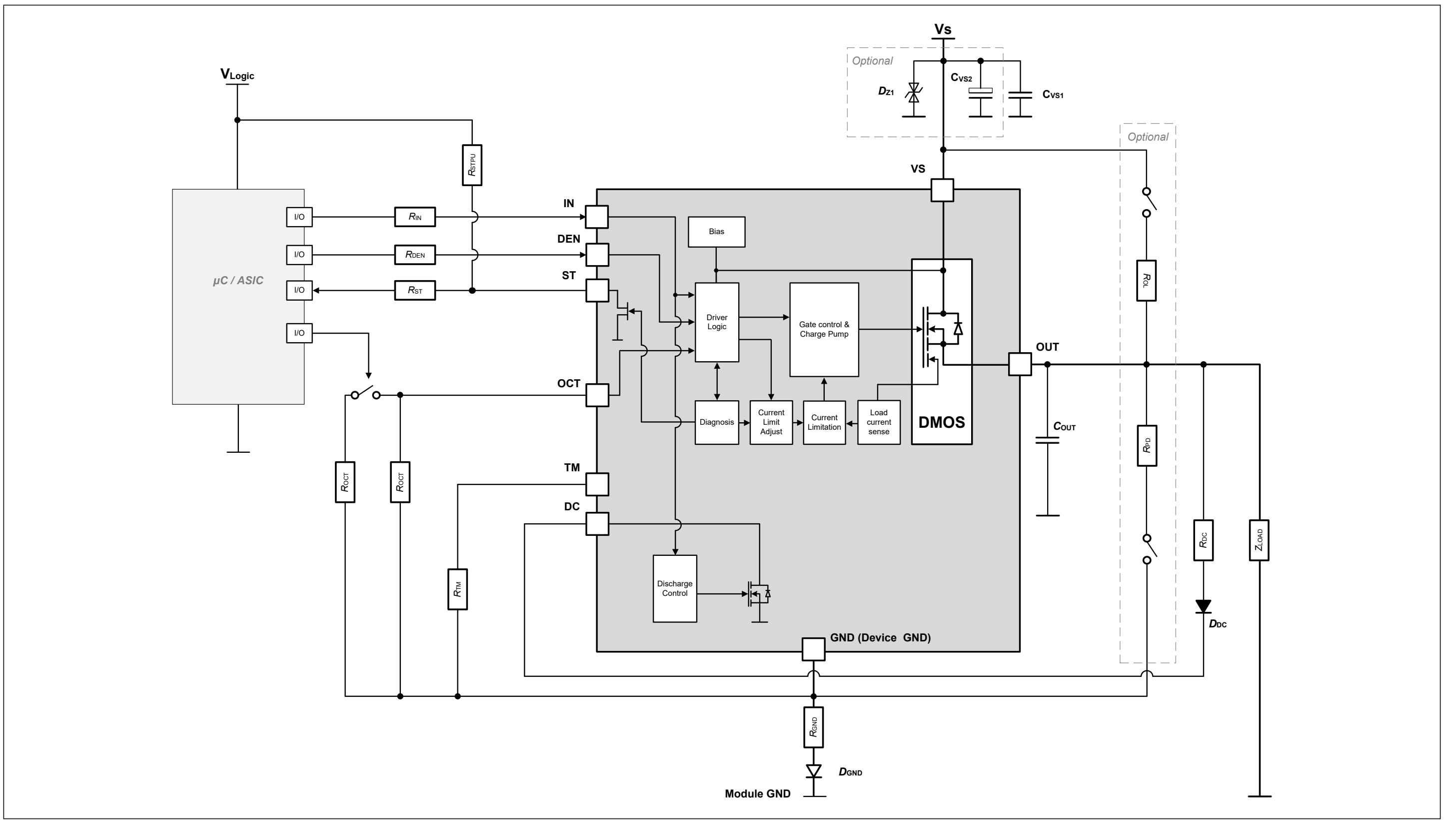


Figure 30 **Application diagram with ITS6080S-EP-D controlled by logic levels [µC] with dynamic inrush current control**

11.2 External components for protection

Some of the features of the ITS6080S-EP-D require external components in order to work properly inside the application.

Table 12 Suggested component values

Reference	Value	Purpose
R_{IN}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{DEN}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{ST}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{TM}	2.2 kΩ	Must be connected with a series resistor to device GND for proper functionality
R_{STPU}	10 kΩ	Pull up resistor for open drain status output
R_{OCT}	–	Adjustable overcurrent limitation resistor connected to device ground. Protection of the device during overvoltage and reverse polarity. Please refer to Table 13
R_{GND}	27 Ω	To limit the GND current at a safe value during ISO pulse
D_{GND}	BAS21	Protection of the ITS6080S-EP-D during reverse polarity

(table continues...)

Table 12 (continued) Suggested component values

Reference	Value	Purpose
D_{Z1}	54 V TVS Diode	Transient voltage suppressor diode. Protection during overvoltage and in case of loss of supply while driving an inductive load
C_{VS1}	100 nF	Filtering of voltage spikes on the supply line
C_{VS2}	10 µF	Supply voltage buffer capacitor at supply
R_{OL}	1.5 kΩ	Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis
R_{PD}	47 kΩ	Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis
C_{OUT}	10 nF	Protection of the output during ESD and BCI
R_{DC}	51 Ω	Lower the power dissipation inside the device during discharge events
D_{DC}	BAS21	Protection against reverse current flow from device GND

11.2.1 Protection of GND path during fault conditions

During specific fault conditions the GND path of the device needs to be protected in order to avoid excessive stress to the device or potential destruction. The most important fault conditions are reverse polarity, transient overvoltage spikes or pulses that are exceeding the absolute maximum ratings of the device. The recommended GND protection in case of reverse polarity is to place a diode into the GND path. This solution is also depicted in the application diagrams. Reverse polarity cannot only be an issue in case of unintended wrong wiring of V_S and GND but may occur as well transiently in combination with pulses at VS or OUT.

If surge pulses (e.g. according IEC61000-4-5) have to be considered the usage of a TVS-protection diode at VS or a comparable protection device is mandatory because the energy content of such pulses is by far higher than what the ITS6080S-EP-D can absorb within the duration of the pulse. The chosen TVS diode for this purpose must provide a clamp voltage that is safely lower than the internal overvoltage clamp $V_{S(AZ)}$ of the ITS6080S-EP-D and should be fast enough to clamp fast transient overvoltage spikes. If by the choice of the TVS-diode or by the nature of the application transient overvoltage spikes > $V_{S(AZ)}$ can be safely excluded the above mentioned blocking diode is sufficient for protecting the GND path. However, in cases where overvoltage spikes > $V_{S(AZ)}$ at VS still need to be considered a resistor in series to the diode needs to be placed in the GND path that limits the current through the GND path during such transient overvoltage events (see also Chapter 7.3.2). In such cases where a resistor in series to the external diode needs to be placed in the GND path, the resulting GND-shifts need to be considered. Especially when using the DC-pin to discharge the output after switch off events the resulting GND-shifts may become big for the duration t_{DC} of the discharge period. If the ITS6080S-EP-D is controlled with logic levels the resulting high ground shifts can mean that depending on load conditions the channel can only be switched on again after the discharge time t_{DC} has elapsed and the related GND shift has reached smaller values again. Therefore, when utilizing the DC-pin, it is recommended to cover transient overvoltage spikes by means of an external TVS-diode.

11.2.2 Input resistors for I/O pins

During fault conditions (e.g. reverse polarity, loss of GND, transient pulses at V_S or OUT, etc.) where the potential of I/O pins may become lower than the potential of device GND or where it may rise above the voltage being present at the VS-pin the ESD protection diodes of the corresponding I/O pins have to be protected by limiting the current through the pin by an external resistor. For the control pins IN and DEN a value of 10 kΩ for an input resistor will be fitting for a broad range of applications.

To use the status functionality, an external pull-up resistor needs to be placed at the ST-pin. This pull-up resistor must be dimensioned in a way that the ST-pin current during fault conditions is not exceeding the maximum ratings given in Table 1. Therefore, the dimensioning of the pull-up resistor will depend on whether it is connected to V_S or to the logic supply rail of the microcontroller. In addition, an input resistor R_{ST} to the microcontroller interface needs to be placed in the same manner and for the same reasons as mentioned above for the control pins IN and DEN.

The OCT-pin will be protected by R_{OCT} in case of reverse polarity. This is also one reason that the OCT-pin must not be directly tied to device GND even if the highest possible current limitation threshold should be used.

A corresponding fault flag will be set, if I_{OCT} exceeds the current threshold $I_{OCT(short2GND)}$ [1].

11.3 Current limitation adjustment

Table 13 below indicates which resistor value R_{OCT} needs to be soldered between OCT-pin and device GND to obtain a desired current limitation threshold $I_{LIM(th,adj)}$. The adjusted current limitation threshold is defined for ambient temperature (T_j = 25°C) and hence, these values coincide with the typical values of the current limit at 25°C. Table 13 provides an overview of the related minimum and maximum values of the current limit. The column "Typical of maximum allowable I_{OUT} [A]" provides information about the required distance of the output current to the adjusted current limit setting in order to avoid unwanted activation of the current limitation circuit during normal operation. This clearance needs to be respected for the nominal load current of a given application and represents an upper limit for the allowable nominal load current [2]. As the typical values of a selected current limit do not vary significantly from T_j = 25°C up to T_j = 150°C for most of the I_{OCT} - settings the given maximum and minimum values of the current limit listed in Table 13 hold true for the temperature range 25°C ≤ T_j ≤ 150°C. Deviations that have to be expected for the typical values of the current limit at 150°C can be seen in Figure 31.

Figure 31 moreover illustrates how the current limitation values will shift for low temperatures. Table 13 provides typical values for the current limitation for the extreme case of T_j = -40°C and an overview of corresponding minimum and maximum values for the current limitations.

Nevertheless R_{OCT} < 5.11 kΩ must not be used. The R_{OCT} resistor must always be placed as close as possible to the OCT-pin and avoid long traces with high inductances. Please note that for excessive I_{OCT} currents a diagnosis flag will be set when reaching the corresponding threshold $I_{OCT(short2GND)}$ [3].

Using R_{OCT} values above 75 kΩ will bring the current limitation outside the allowed lower boundary of the current limit adjust range. It is not recommended to operate the device outside the allowed current limitation adjust range because the accuracy will decrease and stability of the regulation may suffer.

Table 13 **R_{OCT} resistor value selection guide for adjusting current limitation threshold $I_{LIM(th,adj)}$ and overview of resulting current limitation data (typical values & expected range) for temperature range 25°C ≤ T_j ≤150°C**

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM(th,adj)}$ [A] ($I_{LIM,TYP}$ T_j = 25°C) [1]	$I_{LIM,MIN}$ [A] (25°C ≤ T_j ≤150°C)	$I_{LIM,MAX}$ [A] (25°C ≤ T_j ≤150°C)	Typical of max allowable I_{OUT} [A] [2]	Comment
5.11	97.85	5.16	3.22	7.46	3.08	[3]
5.36	93.28	4.76	3.04	6.76	2.82	[4]
5.62	88.97	4.38	2.86	6.09	2.57	[4]
5.90	84.75	4.00	2.69	5.43	2.32	[4]
6.19	80.78	3.65	2.53	4.81	2.09	[5]

(table continues...)

1 The corresponding flag is set in ON-state conditionally if DEN is set to low. See Table 9 for further details
2 Independent of this electrical restriction possibly additional restrictions due to thermal constraints may apply depending on the load current and thermal properties of the PCB
3 This fault flag will be set only in ON-state and will depend on the logic state of the DEN-pin so that it can be distinguished from other fault situations by changing the logic state of DEN to high. For further information please refer to Chapter 9.1

Table 13 (continued) R_{OCT} resistor value selection guide for adjusting current limitation threshold $I_{LIM(th,adj)}$ and overview of resulting current limitation data (typical values & expected range) for temperature range 25°C ≤ T_j ≤150°C

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM(th,adj)}$ [A] ($I_{LIM,TYP}$ T_j = 25°C) [1]	$I_{LIM,MIN}$ [A] (25°C ≤ T_j ≤150°C)	$I_{LIM,MAX}$ [A] (25°C ≤ T_j ≤150°C)	Typical of max allowable I_{OUT} [A] [2]	Comment
6.65	75.19	3.36	2.33	4.42	1.93	[4]
7.15	69.93	3.08	2.14	4.04	1.78	[4]
7.68	65.10	2.83	1.96	3.70	1.63	[4]
8.25	60.61	2.59	1.80	3.37	1.50	[5]
9.09	55.01	2.38	1.63	3.12	1.37	[4]
10.0	50.00	2.17	1.47	2.88	1.26	[6]
11.0	45.45	2.02	1.36	2.69	1.13	[4]
12.1	41.23	1.87	1.23	2.50	1.02	[4]
13.0	38.46	1.77	1.16	2.39	0.94	[5]
15.0	33.33	1.60	1.01	2.20	0.82	[4]
18.2	27.47	1.41	0.83	1.98	0.68	[7]
21.5	23.26	1.31	0.76	1.86	0.62	[4]
26.7	18.73	1.18	0.65	1.71	0.53	[4]
33.2	15.06	1.07	0.56	1.57	0.46	[5]
39.2	12.76	1.01	0.50	1.50	0.40	[4]
56.2	8.90	0.90	0.41	1.37	0.32	[4]
75.0	6.67	0.85	0.36	1.31	0.28	[8]
> 75.0	< 6.67	–	–	–	–	outside specified range [9]

1) $I_{LIM(th, adj)}$ values coincide with typical values of the current limit I_{LIM} @ 25°C. Typical values for I_{LIM} @ 150°C may show deviation from $I_{LINM(th, adj)}$; see Figure 31 for further details
2) The listed values for I_{OUT} indicate the required clearance of the output current from the adjusted current limit without being at risk to interact. These values can be used as a maximum nominal current if there is no constraint from a thermal point of view
3) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 97.85 µA (corresponds to ROCT = 5.11 kΩ)
4) Values given in this line are based on interpolation of corresponding neighboring specified values
5) Not subject to production test, values specified by design.
6) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 50 µA (corresponds to ROCT = 10 kΩ)
7) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 27.47 µA (corresponds to ROCT = 18.2 kΩ)
8) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 6.67 µA (corresponds to ROCT = 75 kΩ)
9) R_{OCT} values > 75 kΩ are not recommended for usage as the accuracy of the current limit will degrade

Table 14 R_{OCT} resistor value selection guide for adjusting current limitation threshold $I_{LIM(th,adj)}$ and an overview of resulting current limitation data (typical values & expected range) for low temperatures T_j = -40°C

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM,TYP}$ [A] (T_j = -40°C)	$I_{LIM,MIN}$ [A] (T_j = -40°)	$I_{LIM,MAX}$ [A] (T_j= -40°C)	Typical of max allowable I_{OUT} [A] [1)]	Comment
5.11	97.85	5.50	2.92	8.34	3.08	[2)]
5.36	93.28	5.06	2.82	7.55	2.82	[3)]
5.62	88.97	4.66	2.72	6.81	2.57	[3)]
5.90	84.75	4.26	2.63	6.08	2.32	[3)]
6.19	80.78	3.89	2.54	5.39	2.09	[4)]
6.65	75.19	3.57	2.34	4.94	1.93	[3)]
7.15	69.93	3.27	2.14	4.52	1.78	[3)]
7.68	65.10	3.00	1.97	4.14	1.63	[3)]
8.25	60.61	2.74	1.80	3.79	1.50	[4)]
9.09	55.01	2.51	1.63	3.50	1.37	[3)]
10.0	50.00	2.31	1.48	3.24	1.26	[5)]
11.0	45.45	2.11	1.33	2.99	1.13	[3)]
12.1	41.23	1.94	1.20	2.77	1.02	[3)]
13.0	38.46	1.82	1.12	2.62	0.94	[4)]
15.0	33.33	1.65	0.96	2.43	0.82	[3)]
18.2	27.47	1.46	0.78	2.22	0.68	[6)]
21.5	23.26	1.32	0.68	2.03	0.62	[3)]
26.7	18.73	1.17	0.56	1.85	0.53	[3)]
33.2	15.06	1.03	0.45	1.68	0.46	[4)]
39.2	12.76	0.98	0.40	1.62	0.40	[3)]
56.2	8.90	0.85	0.29	1.46	0.32	[3)]
75.0	6.67	0.79	0.24	1.39	0.28	[7)]
> 75.0	< 6.67	–	–	–	–	outside specified range [8)]

1) The listed values for I_{OUT} indicate the required clearance of the output current from the adjusted current limit without being at risk to interact. These values can be used as a maximum nominal current if there is no constraint from a thermal point of view
2) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 97.85 µA (corresponds to ROCT = 5.11 kΩ)
3) Values given in this line are based on interpolation of corresponding neighboring specified values
4) Not subject to production test, values specified by design.
5) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 50 µA (corresponds to ROCT = 10 kΩ)
6) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 27.47 µA (corresponds to ROCT = 18.2 kΩ)
7) See Electrical Characteristics: Protection Functions; Current limitation with setting IOCT = 6.67 µA (corresponds to ROCT = 75 kΩ)
8) R_{OCT} values > 75 kΩ are not recommended for usage as the accuracy of the current limit will degrade

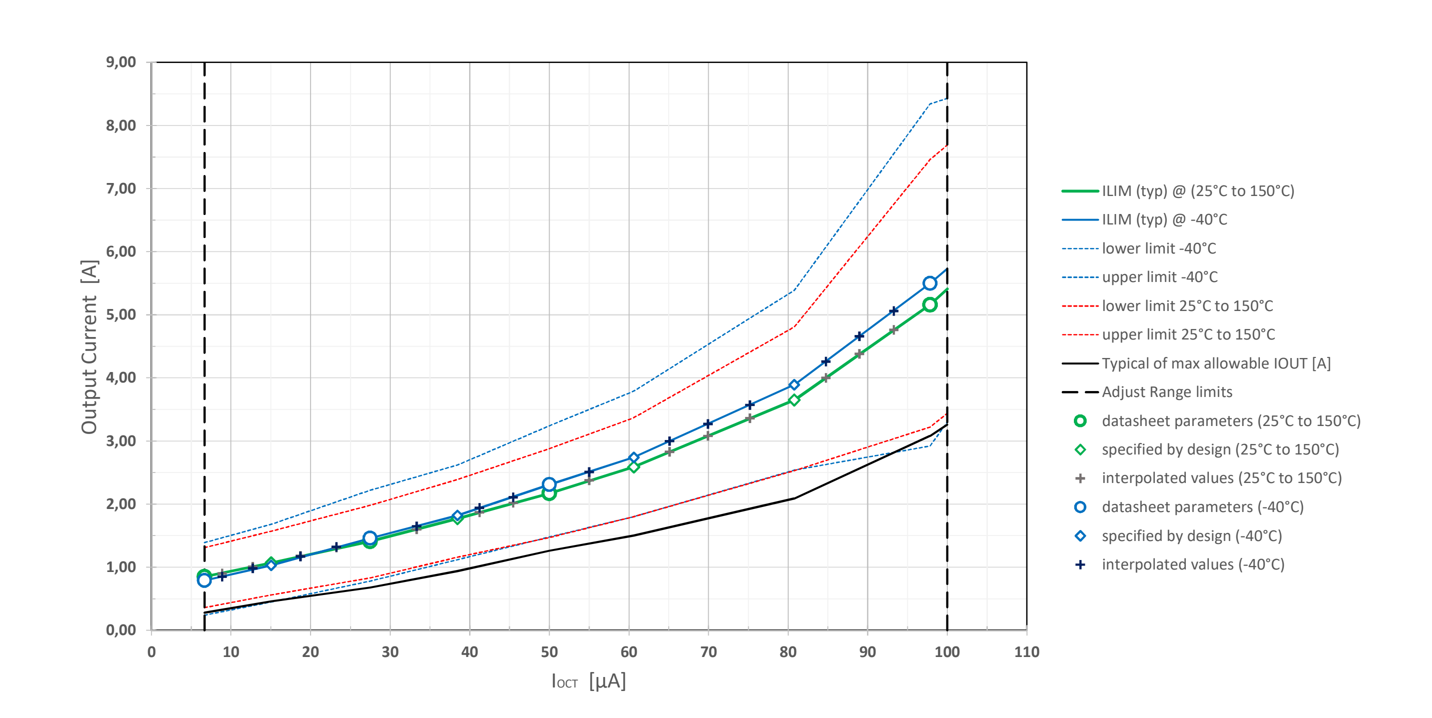
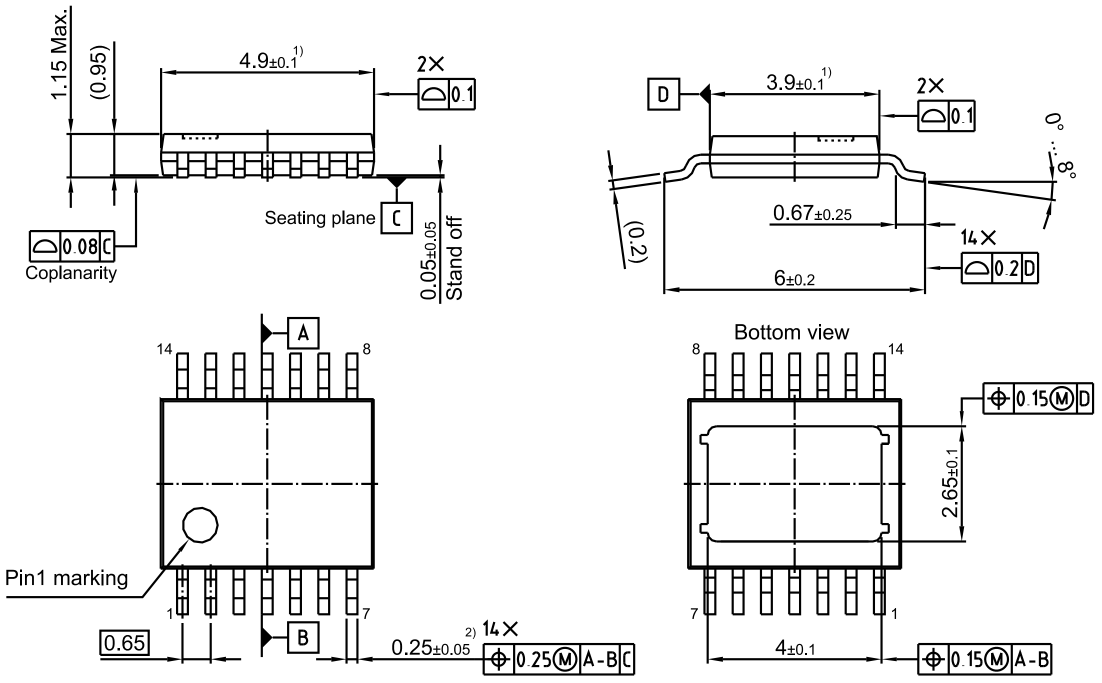


Figure 31 **Current limitation threshold $I_{LIM(th,adj)}$ as function of I_{OCT} and related limitation values for different temperatures**

12 Package outlines



1) Does not include plastic or metal protrusion of 0.15 mm max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ±0.05; ±1°30'

Figure 32 **PG-TSDSO-14(Plastic Dual Small Outline Package) (RoHS-Compliant)**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:

https://infineon.com/packages

13 Revision history

Revision	Date	Changes
1.10	2025-02-21	Editorial changes Figure "Typical values of the current limitation as function of the adjusted I_{OCT} current" removed Figure "Current limitation threshold $I_{LIM(th,adj)}$ as function of I_{OCT} and related limitation values for different temperatures" updated P_7.6.4, P_7.6.16, P_7.6.6, P_7.6.45, P_9.4.37 updated P_7.6.47 added Table 13, Table 14 updated
1.00	2024-03-08	Datasheet release