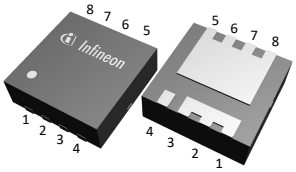
MOSFET

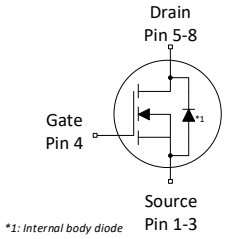
PG-TSDSON-8 FL

OptiMOS™ 6 Power-Transistor, 150 V



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	17.3	mΩ
I_D	48	A
Q_{oss}	45	nC
Q_G	14.8	nC
Q_{rr}(500 A/µs)	101	nC

Type/Ordering Code	Package	Marking	Related Links
ISZ173N15NM6	PG-TSDSON-8	17315N6	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	48 34 32 7.9	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=8 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=60 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	192	A	T_C=25 °C
Avalanche current, single pulse [4]	I_{AS}	-	-	16	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	140	mJ	I_D=7 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	94 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5]	R_{thJA}	-	-	60	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.5	4.0	V	V_{DS}=V_{GS}, I_D=35 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	13.8 15.3 17.2	16.3 17.3 20.2	mΩ	V_{GS}=15 V, I_D=16 A V_{GS}=10 V, I_D=16 A V_{GS}=8 V, I_D=8 A
Gate resistance	R_G	-	0.82	1.23	Ω	-
Transconductance	g_{fs}	14	27	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=16 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	1000	1300	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance [6]	C_{oss}	-	330	430	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance [6]	C_{rss}	-	9	14	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	9	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	11	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge [8)]	Q_{gs}	-	5.5	7.2	nC	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	3.6	-	nC	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Gate to drain charge [8)]	Q_{gd}	-	3.8	5.7	nC	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	5.7	-	nC	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Gate charge total [8)]	Q_g	-	14.8	19.2	nC	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=75 V, I_D=8 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	12	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8)]	Q_{oss}	-	45	59	nC	V_{DS}=75 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

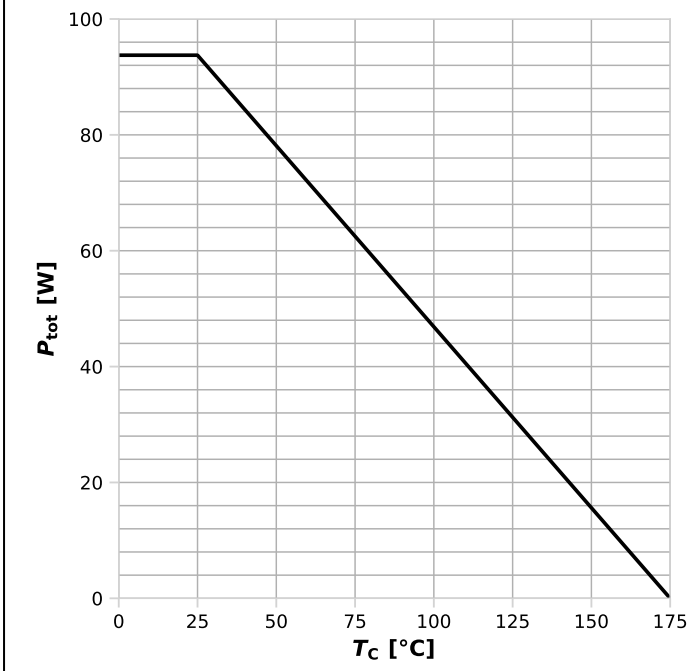
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	48	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	192	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.0	V	V_{GS}=0 V, I_F=16 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	31	62	ns	V_R=75 V, I_F=8 A, di_F/dt=500 A/µs
Reverse recovery charge [9)]	Q_{rr}	-	101	202	nC	V_R=75 V, I_F=8 A, di_F/dt=500 A/µs
Reverse recovery time [9)]	t_{rr}	-	21	42	ns	V_R=75 V, I_F=8 A, di_F/dt=1000 A/µs
Reverse recovery charge [9)]	Q_{rr}	-	128	256	nC	V_R=75 V, I_F=8 A, di_F/dt=1000 A/µs

9) Defined by design. Not subject to production test.

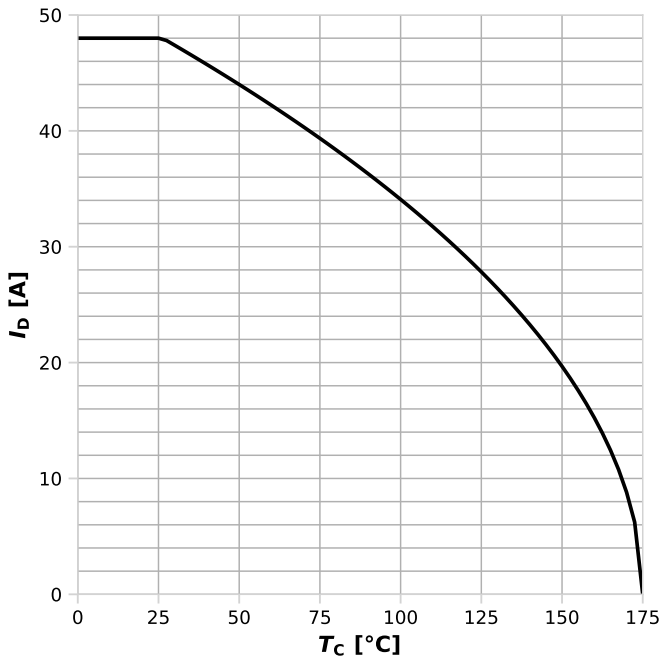
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



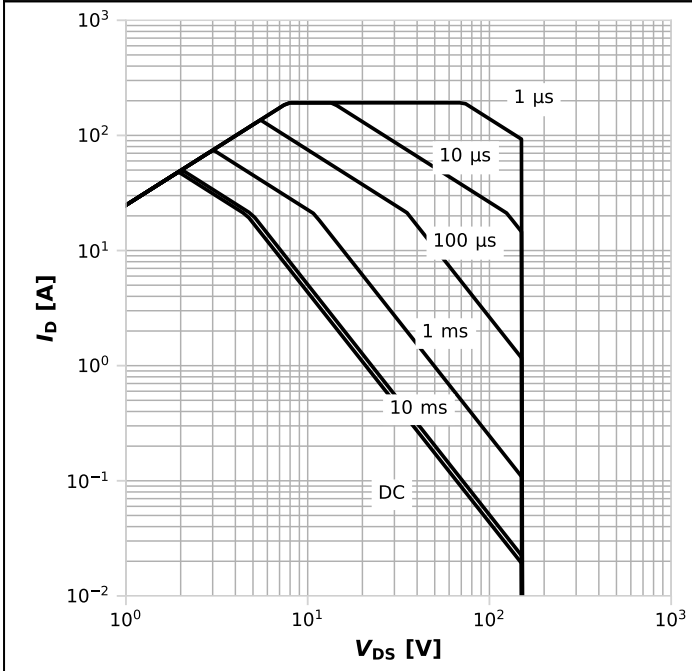
P_{tot}=f(T_C)

Diagram 2: Drain current



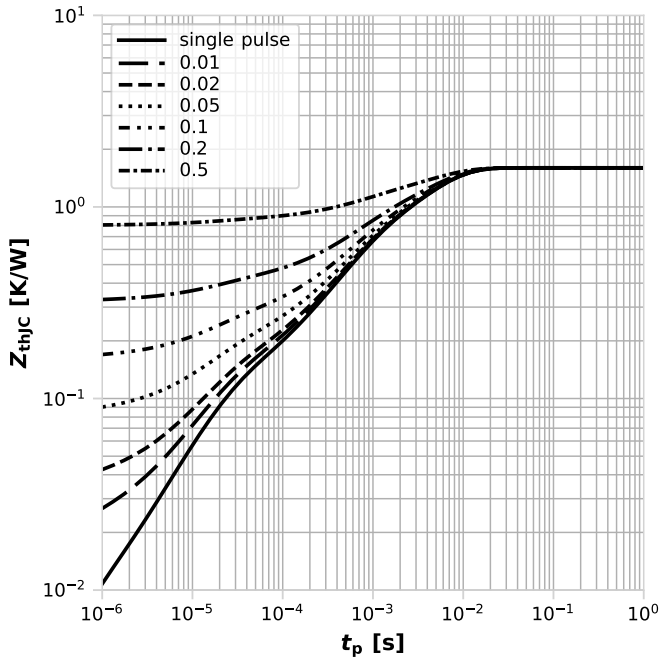
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



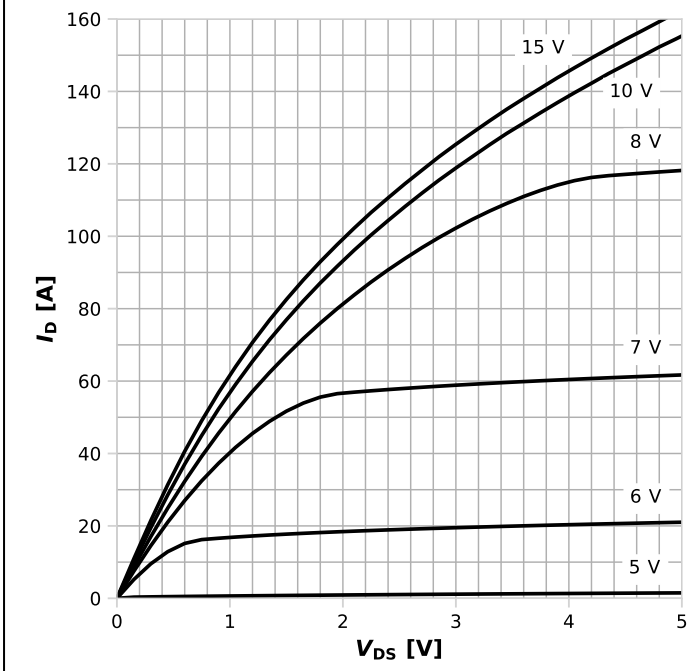
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



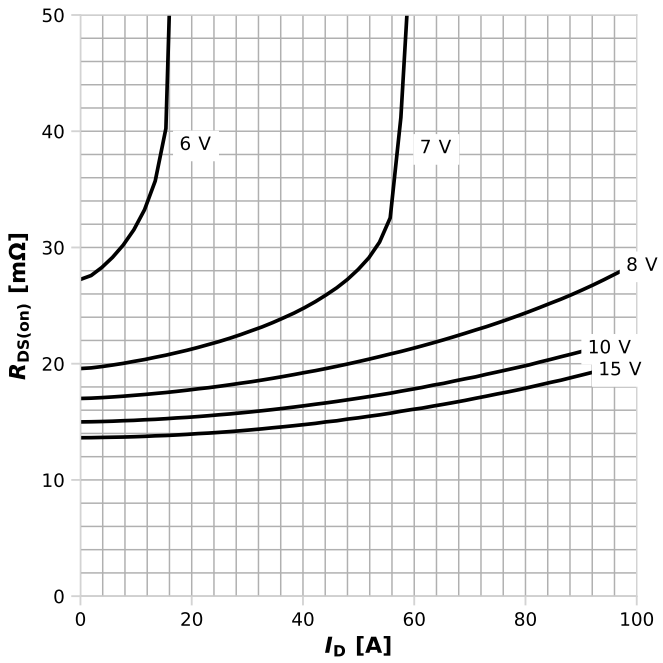
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



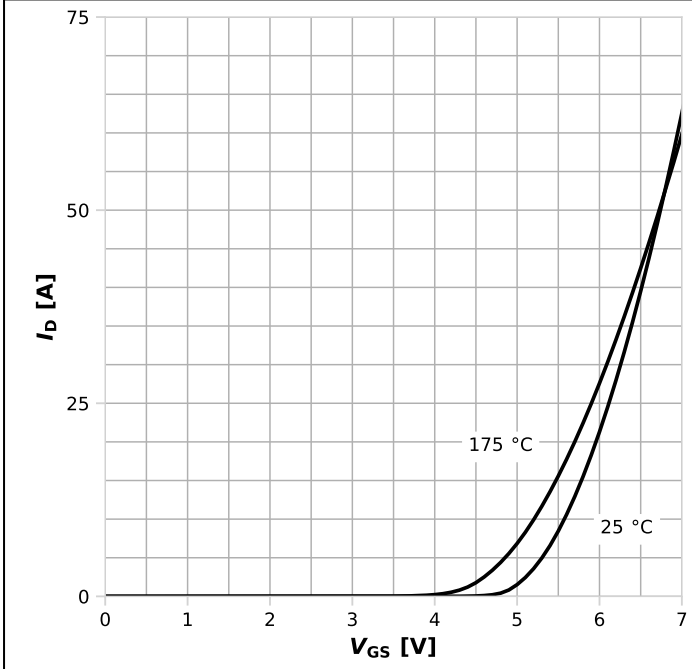
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



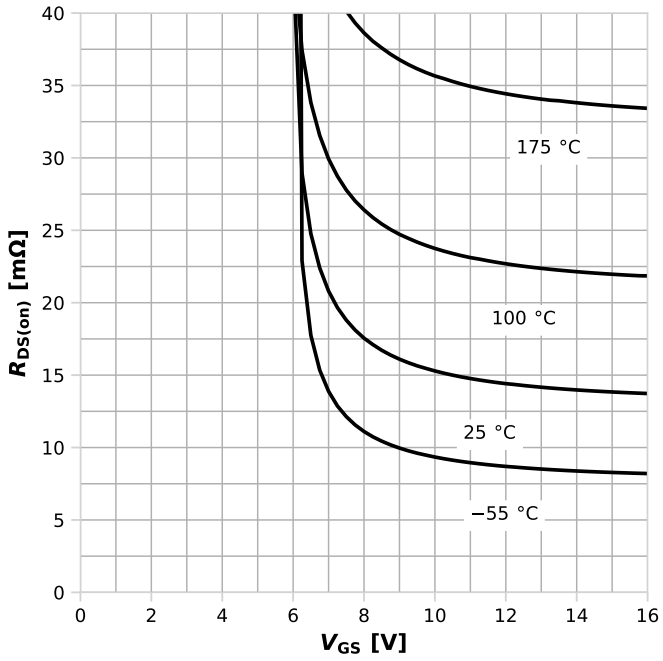
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=16 A; parameter: T_j

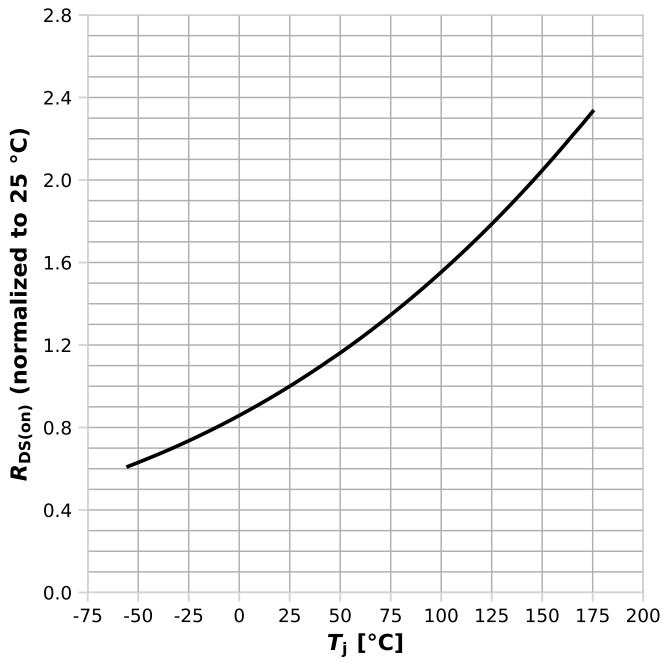
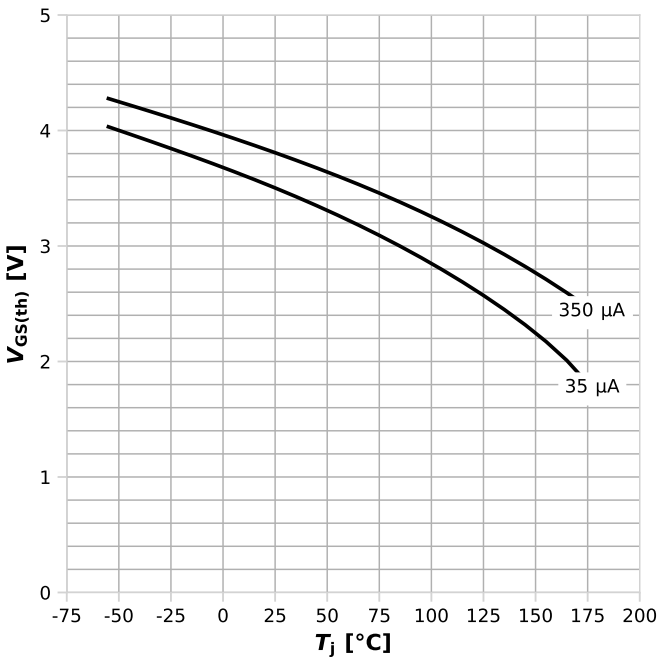
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=16 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

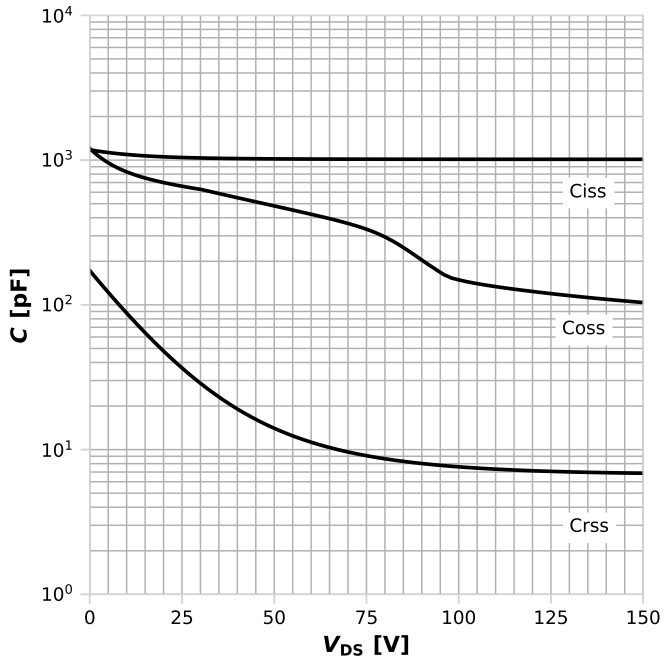
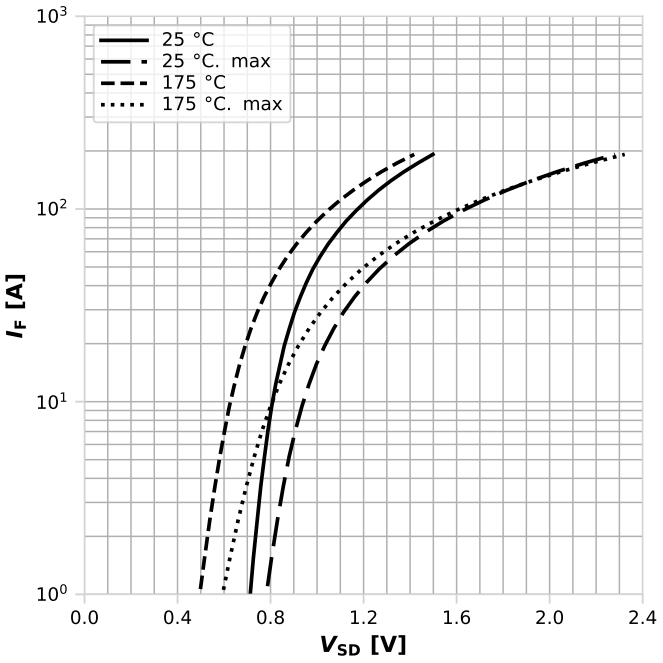
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

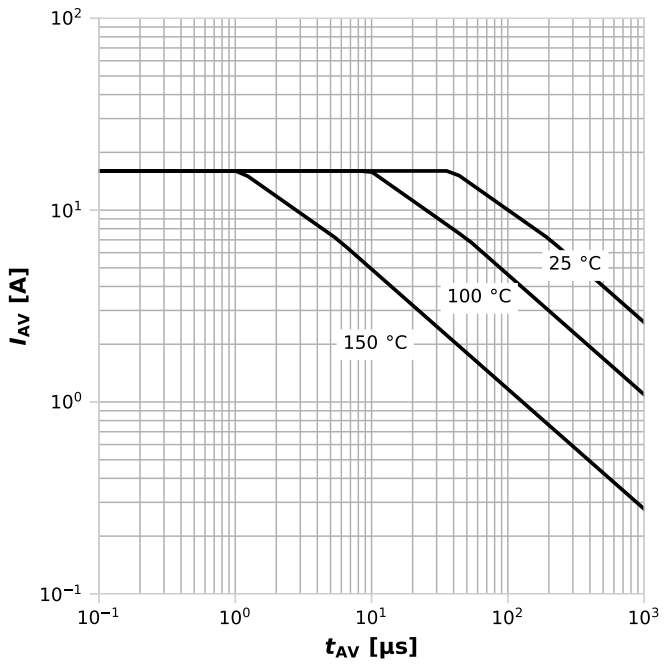
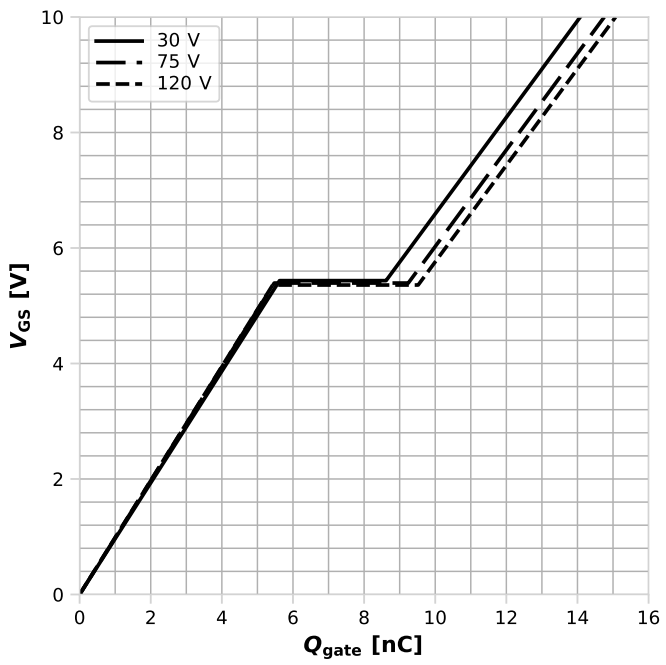
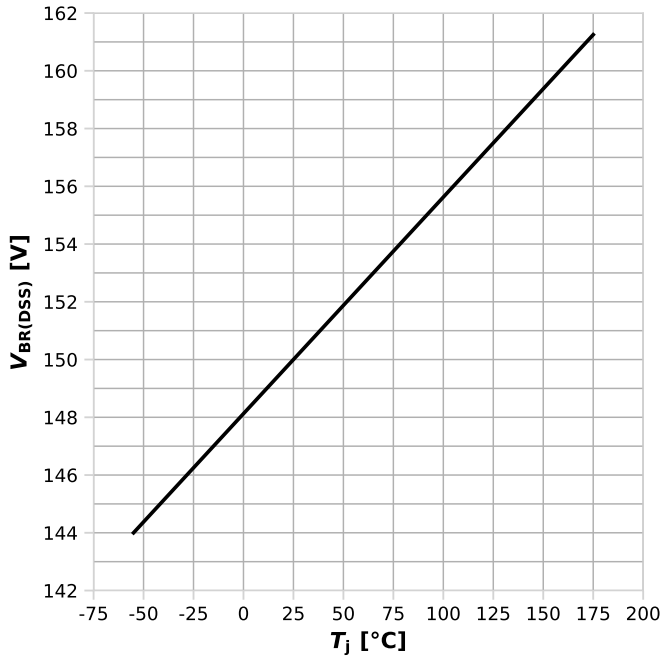
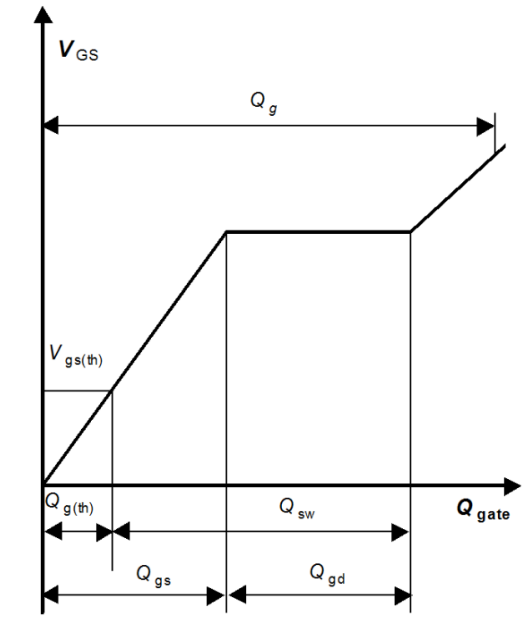
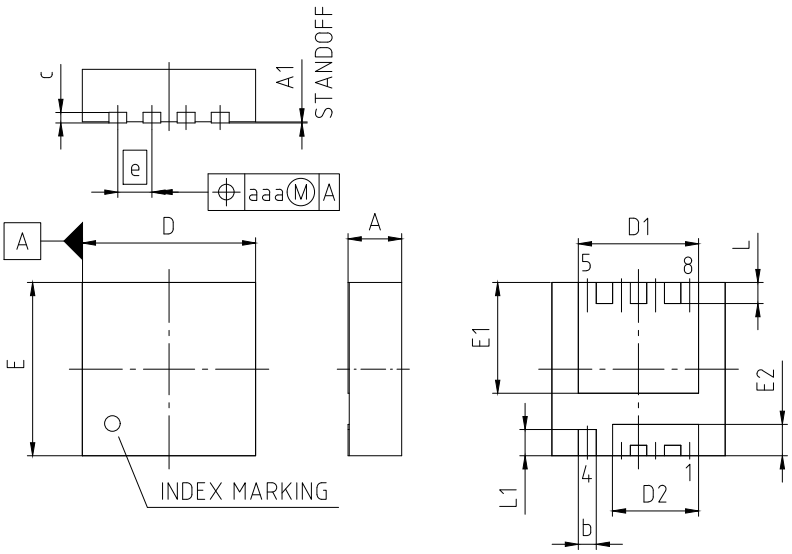
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=8 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	0.10	0.30
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.50	0.70
e	0.65	
L	0.30	0.50
L1	0.40	0.60
aaa	0.06	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSDSON-8, dimensions in mm

Revision History

ISZ173N15NM6

Revision 2024-04-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-03-15	Release of preliminary version
2.0	2024-04-22	Release of final

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