

MOSFET

OptiMOS™ 8 Power-MOSFET, 80 V

Features

- N-channel, normal level
- Optimized for motor drives, synchronous rectification and battery protection
- Soft recovery body diode
- 100% avalanche tested
- Superior thermal resistance
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

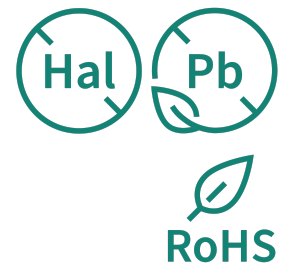
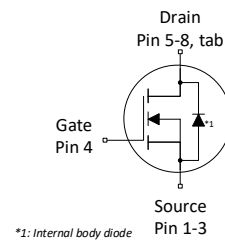
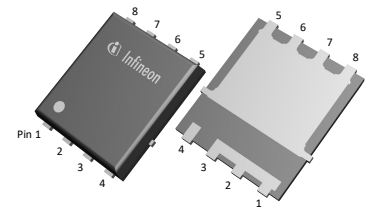
Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.64	mΩ
I_D	268	A
Q_{oss}	147	nC
Q_G (0 V..10 V)	76	nC
Q_{rr} (100 A/μs)	162	nC

PG-TDSON-8



Part number	Package	Marking	Related links
ISC016N08NM8	PG-TDSON-8	16N08N8	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	268	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				190		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				196		$V_{GS}=15\text{ V}$, $T_C=100\text{ °C}$
				29		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1072	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	442	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	263	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 13 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.38	0.57	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		-	20		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	50		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}$, $I_D=111\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
Zero gate voltage drain current ⁶⁾	I_{DSS}	-	10	100	μA	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.33	1.54	m Ω	$V_{GS}=15\text{ V}$, $I_D=50\text{ A}$
			1.46	1.64		$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
			1.63	1.87		$V_{GS}=8\text{ V}$, $I_D=25\text{ A}$
Gate resistance	R_G	-	0.95	-	Ω	-
Transconductance ⁶⁾	g_{fs}	55	110	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	5500	7200	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		2230	2900		
Reverse transfer capacitance ⁷⁾	C_{rss}		24	42		
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		6.1			
Turn-off delay time	$t_{d(off)}$		28			
Fall time	t_f		7.2			

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	29	-	nC	$V_{DD}=40\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		17	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}		15	19	nC	
Switching charge	Q_{sw}		27	-	nC	
Gate charge total ⁹⁾	Q_g		76	99	nC	
Gate plateau voltage	$V_{plateau}$		5.3	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	69	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁹⁾	Q_{oss}	-	147	191	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See figure 16 for gate charge parameter definition.

⁹⁾ Defined by design. Not subject to production test.

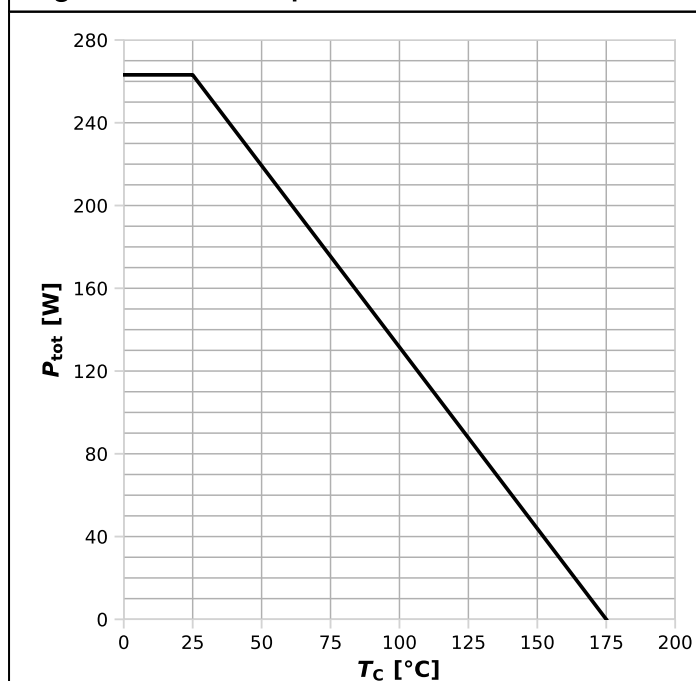
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	232	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1072		
Diode forward voltage	V_{SD}	-	0.84	1.0	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁰⁾	t_{rr}	-	187	374	ns	$V_R=40\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		162	325	nC	
Reverse recovery time ¹⁰⁾	t_{rr}	-	39	78	ns	$V_R=40\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		209	418	nC	

¹⁰⁾ Defined by design. Not subject to production test.

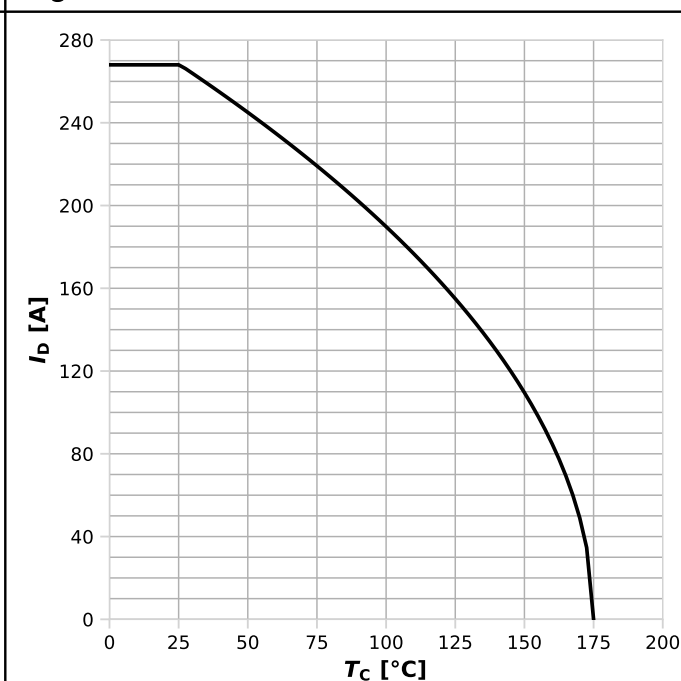
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



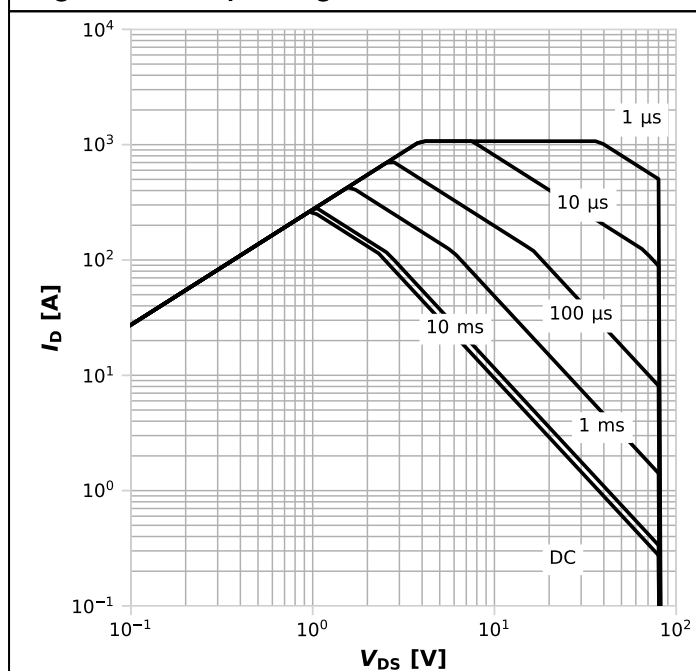
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Drain current



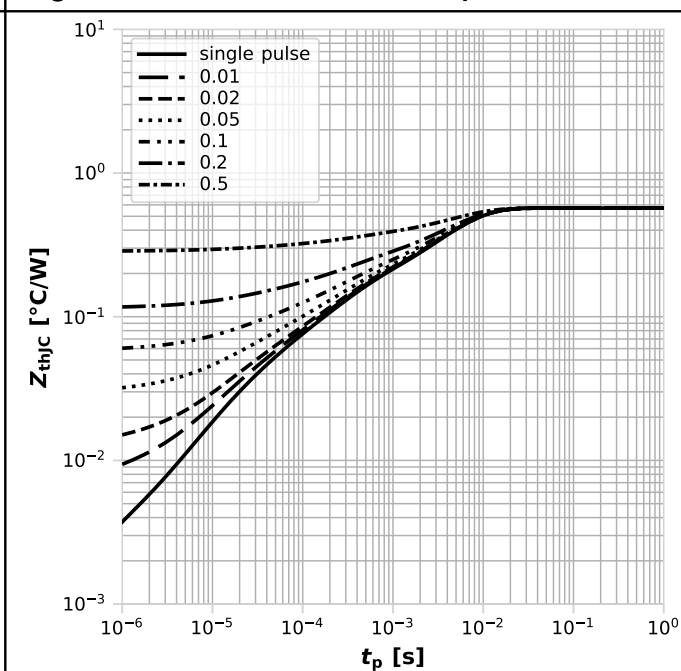
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$

Diagram 3: Safe operating area



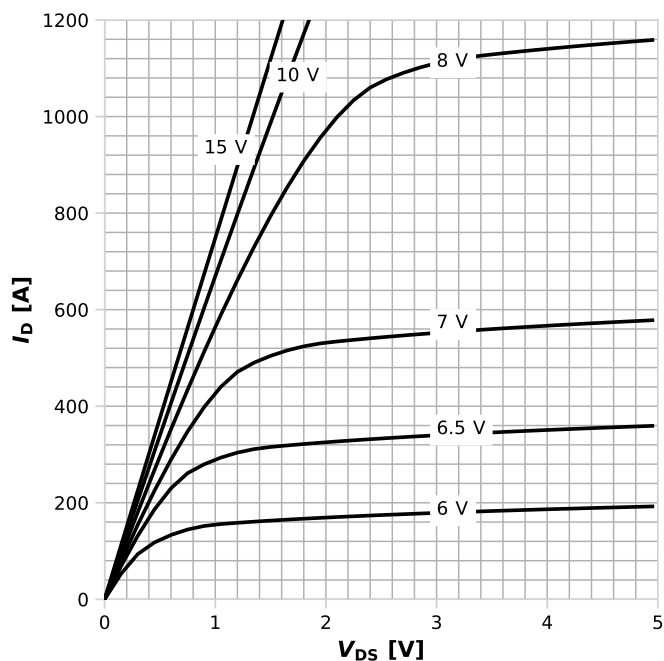
$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



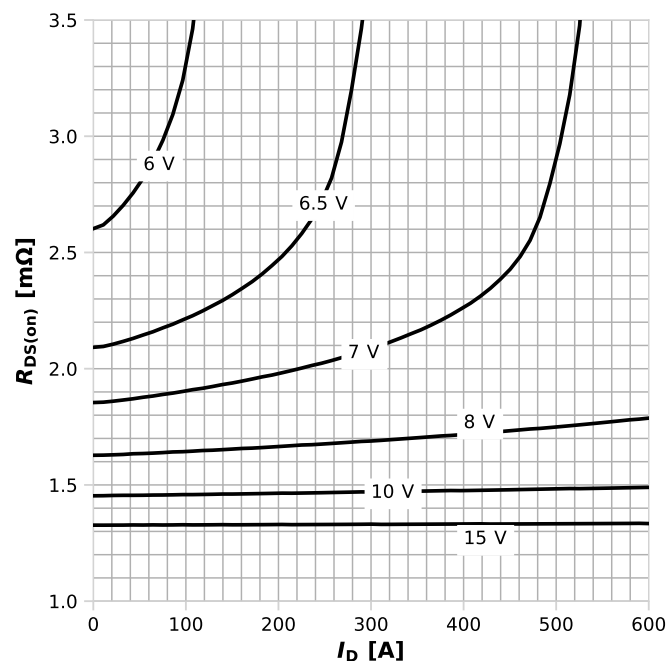
$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics



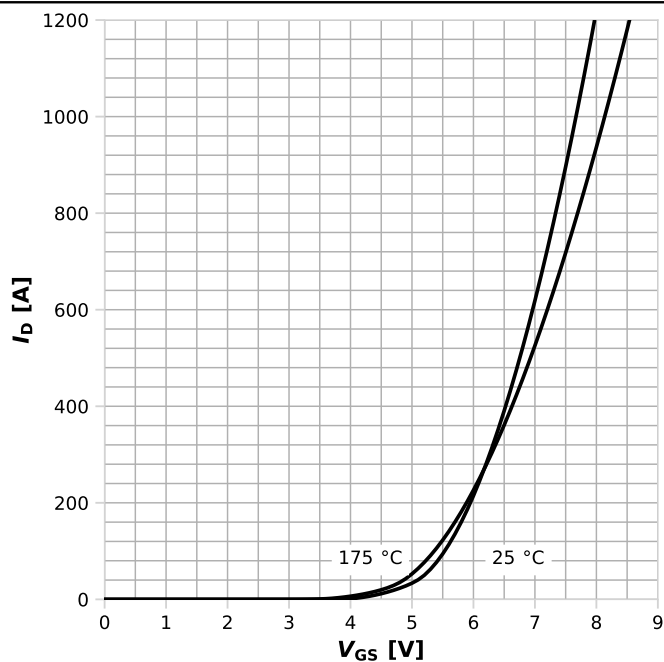
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



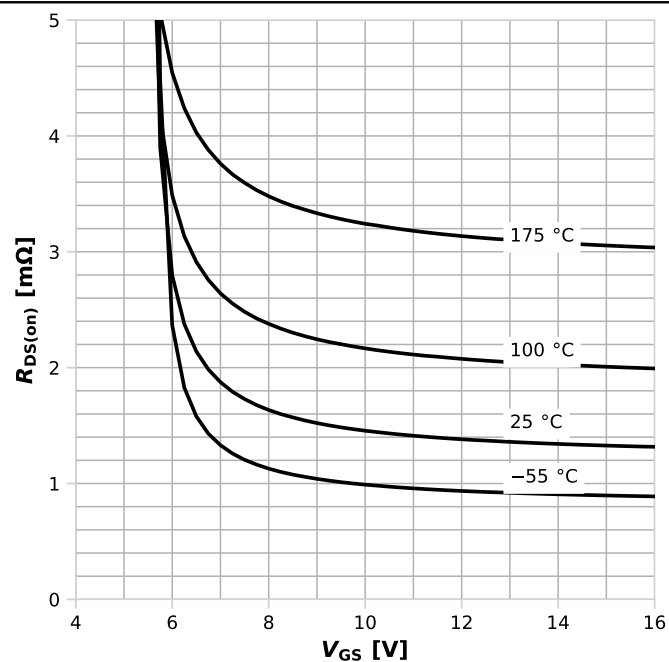
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



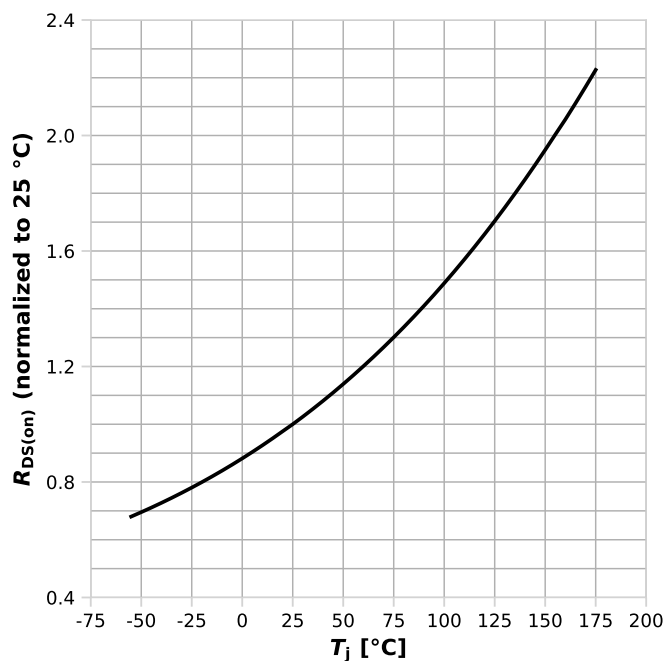
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



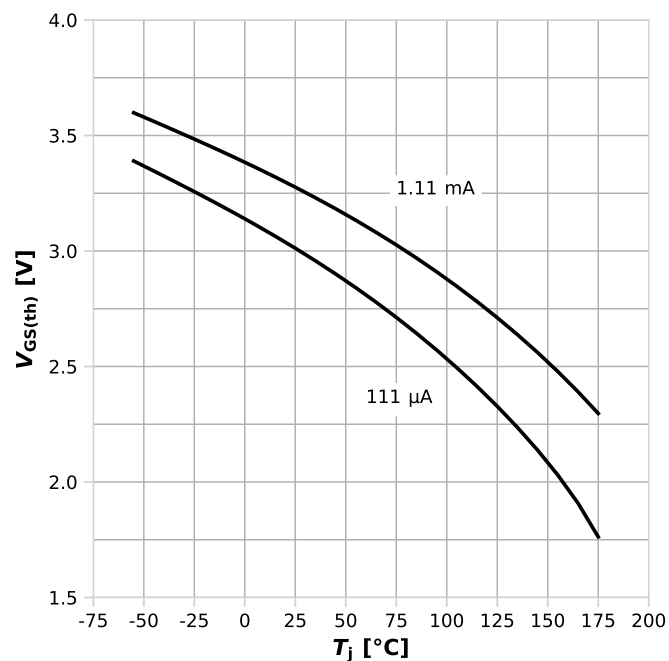
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



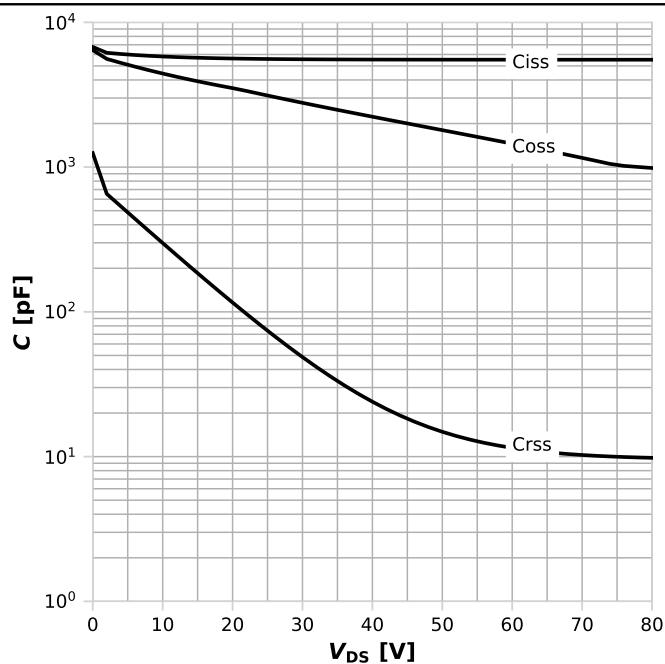
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



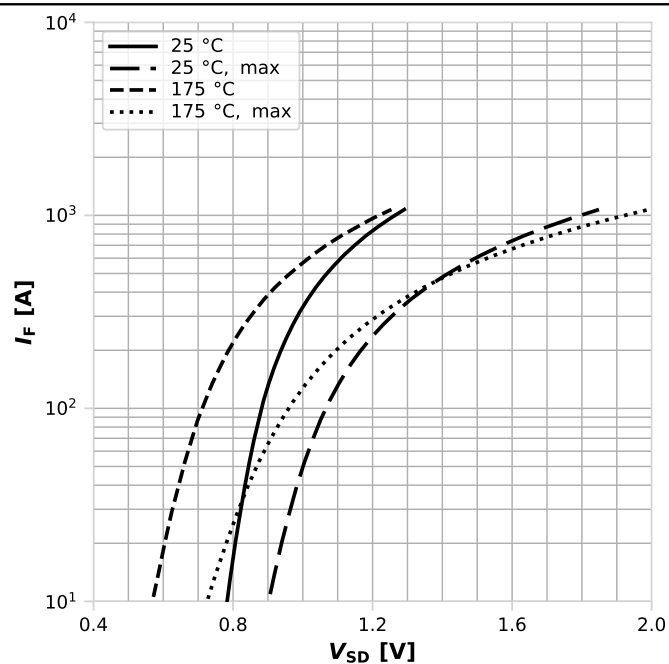
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



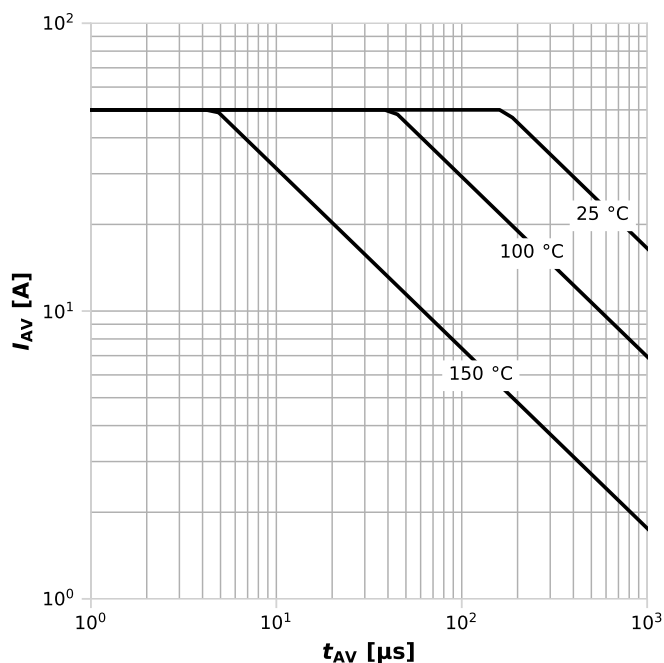
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



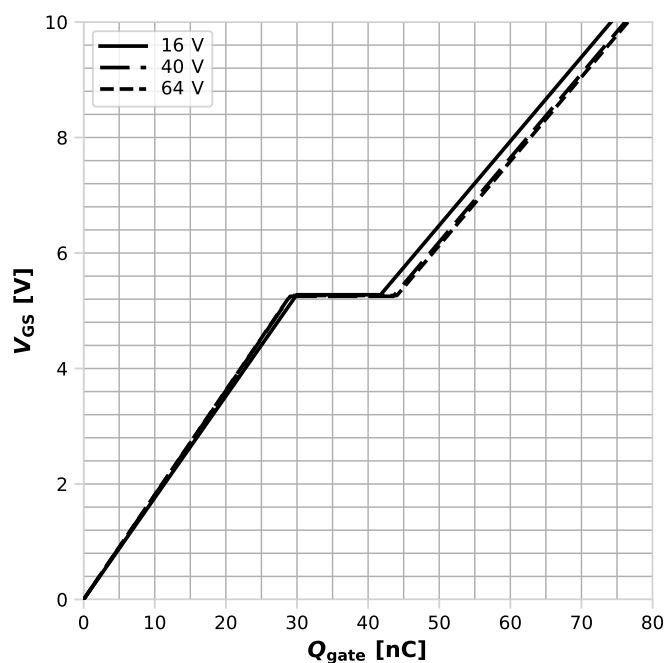
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



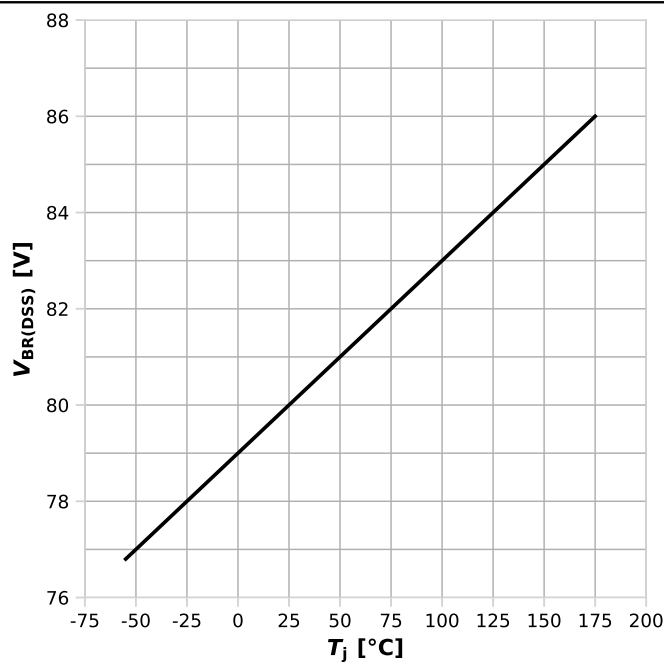
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



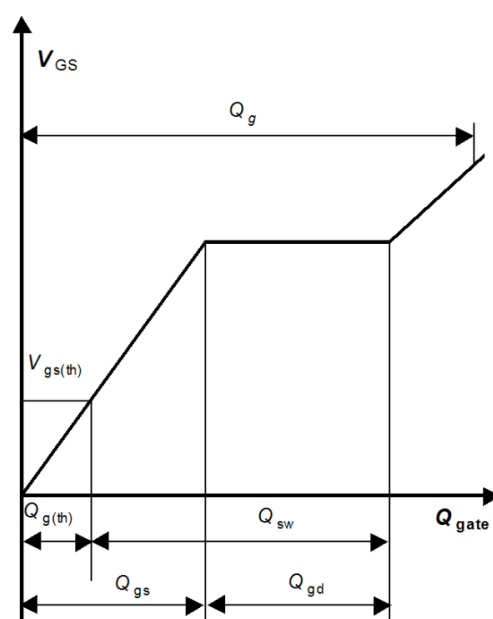
$V_{GS}=f(Q_{gate})$, $I_D=50\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package outlines

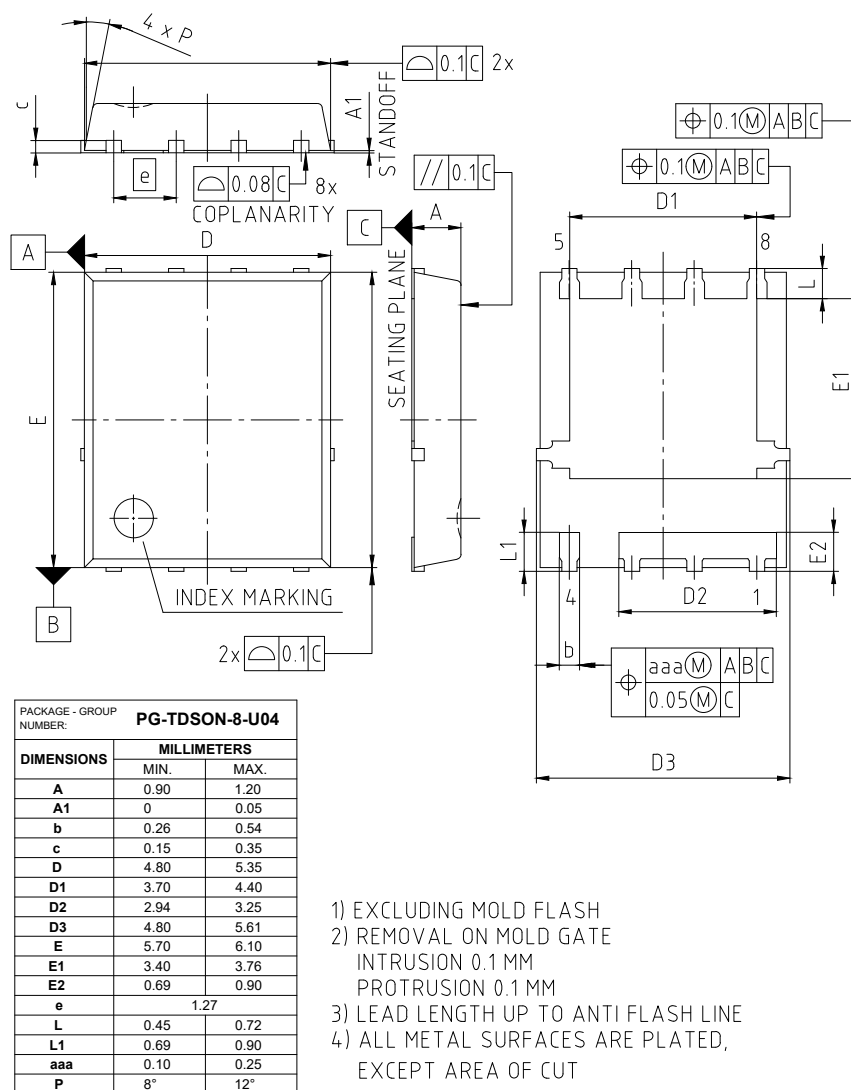


Figure 1 Outline PG-TDSON-8, dimensions in mm

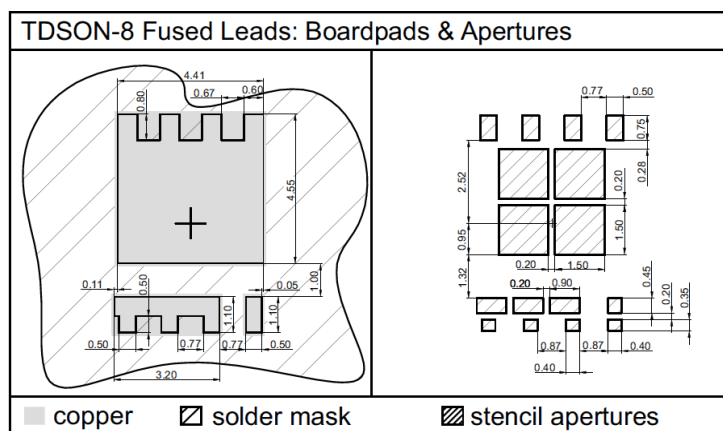


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

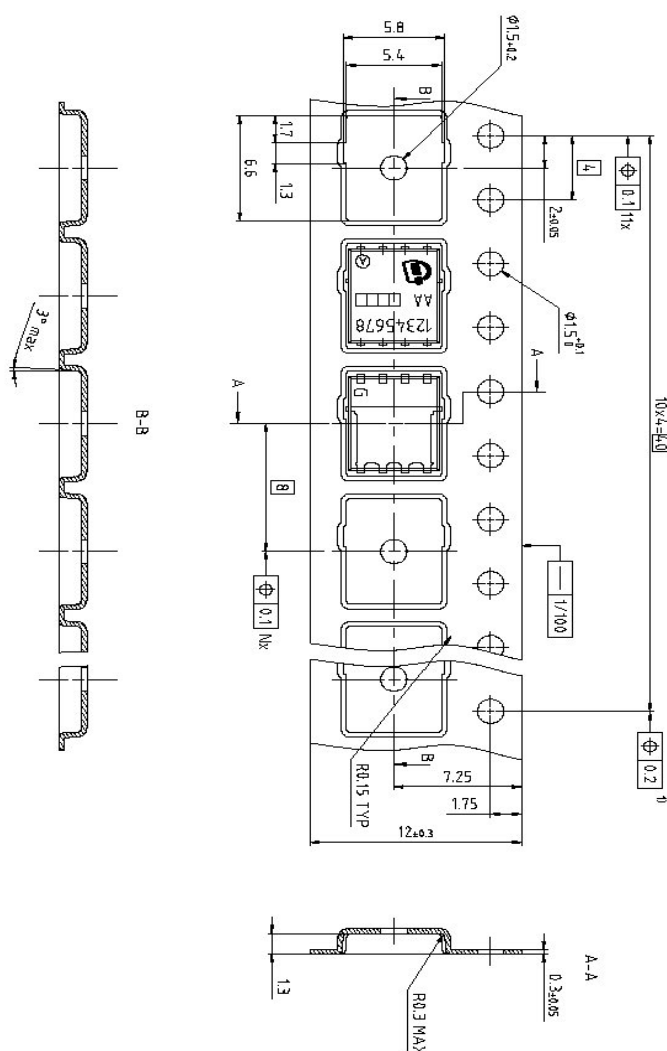


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

ISC016N08NM8

Revision 2025-12-17, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-07-17	Release of final version
1.1	2025-12-17	Updated RthJC

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