

MOSFET

OptiMOS™6 Power-Transistor, 40 V

Features

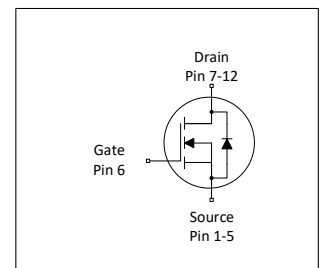
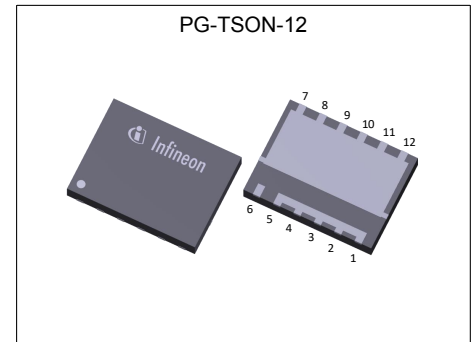
- Optimized for Low Voltage Drives applications
- Optimized for Battery Powered applications
- Optimized for Synchronous Rectification
- Very low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel, normal level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- 175°C rated

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------------|
| V_{DS} | 40 | V |
| $R_{DS(on),max}$ | 0.39 | m Ω |
| I_D | 600 | A |
| Q_{oss} | 199 | nC |
| $Q_G (0V..10V)$ | 182 | nC |



RoHS

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|------------|-----------|---------------|
| IQFH39N04NM6 | PG-TSON-12 | H39N04NM6 | - |

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------------|--------|------|------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 600 422 63 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}^2)$ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 2400 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 1260 | mJ | $I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 273 3.0 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}^2)$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 175 | °C | - |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | R_{thJC} | - | - | 0.55 | °C/W | - |
| Thermal resistance, junction - case, top | R_{thJC} | - | - | 20 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾ | R_{thJA} | - | - | 50 | °C/W | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at specified. For other case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|--------------|--------------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 40 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 1.8 | 2.3 | 2.8 | V | $V_{DS}=V_{GS}$, $I_D=1050\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.27 0.31 | 0.39 0.43 | $\text{m}\Omega$ | $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$ |
| Gate resistance | R_G | - | 0.8 | - | Ω | - |
| Transconductance ¹⁾ | g_{fs} | 310 | - | - | S | $ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|-------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 12600 | 16400 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance ¹⁾ | C_{oss} | - | 4090 | 5320 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance ¹⁾ | C_{rss} | - | 93 | 158 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 23 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 70 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 69 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Fall time | t_f | - | 14 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |

Table 6 Gate charge characteristics²⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 42 | - | nC | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 28 | - | nC | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge ¹⁾ | Q_{gd} | - | 25 | 38 | nC | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 39 | - | nC | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ¹⁾ | Q_g | - | 182 | 273 | nC | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 3.3 | - | V | $V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 172 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge ¹⁾ | Q_{oss} | - | 199 | 259 | nC | $V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$ |

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 275 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 2400 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.78 | 1 | V | $V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$ |
| Reverse recovery time ¹⁾ | t_{rr} | - | 49 | 98 | ns | $V_R=20\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁾ | Q_{rr} | - | 312 | 624 | nC | $V_R=20\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$ |

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

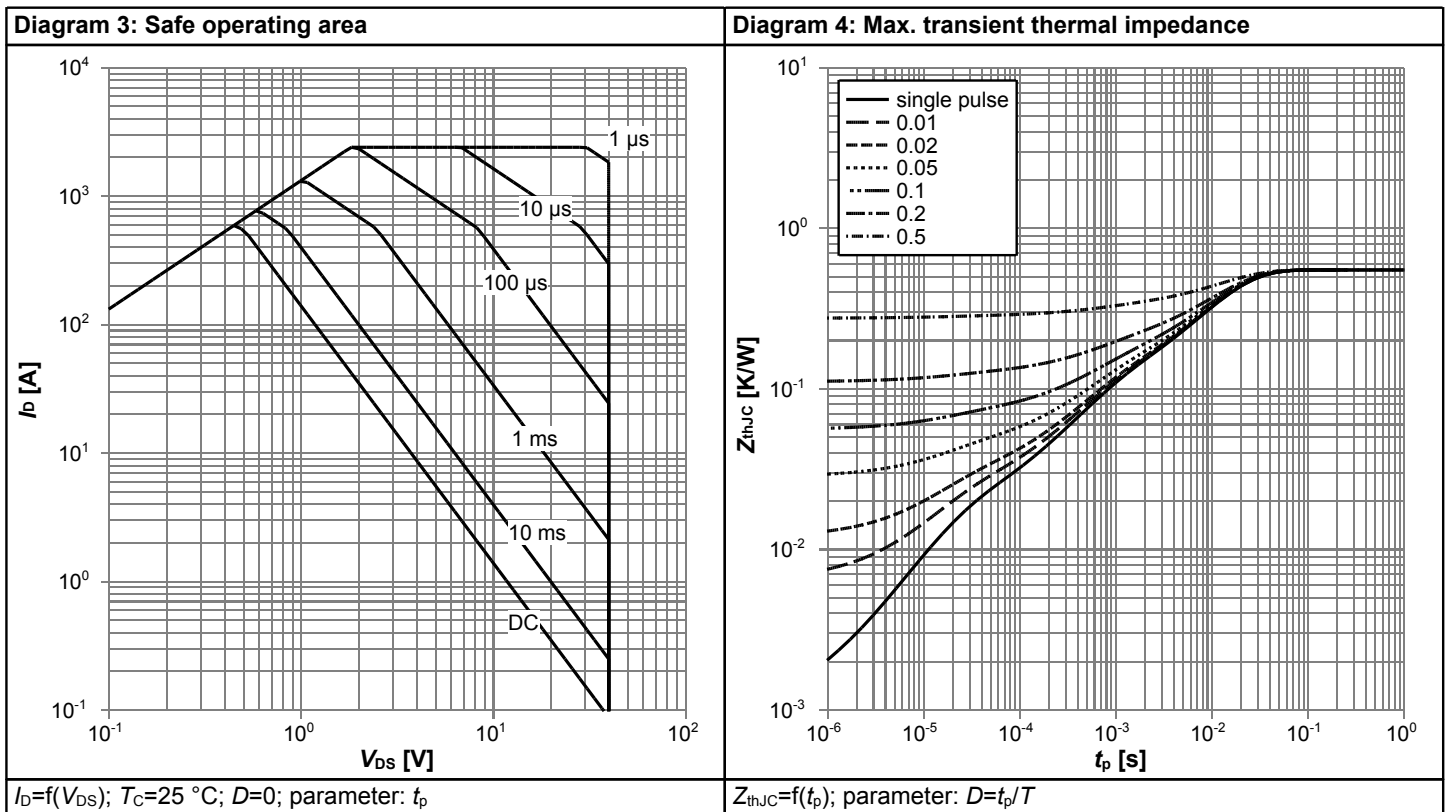
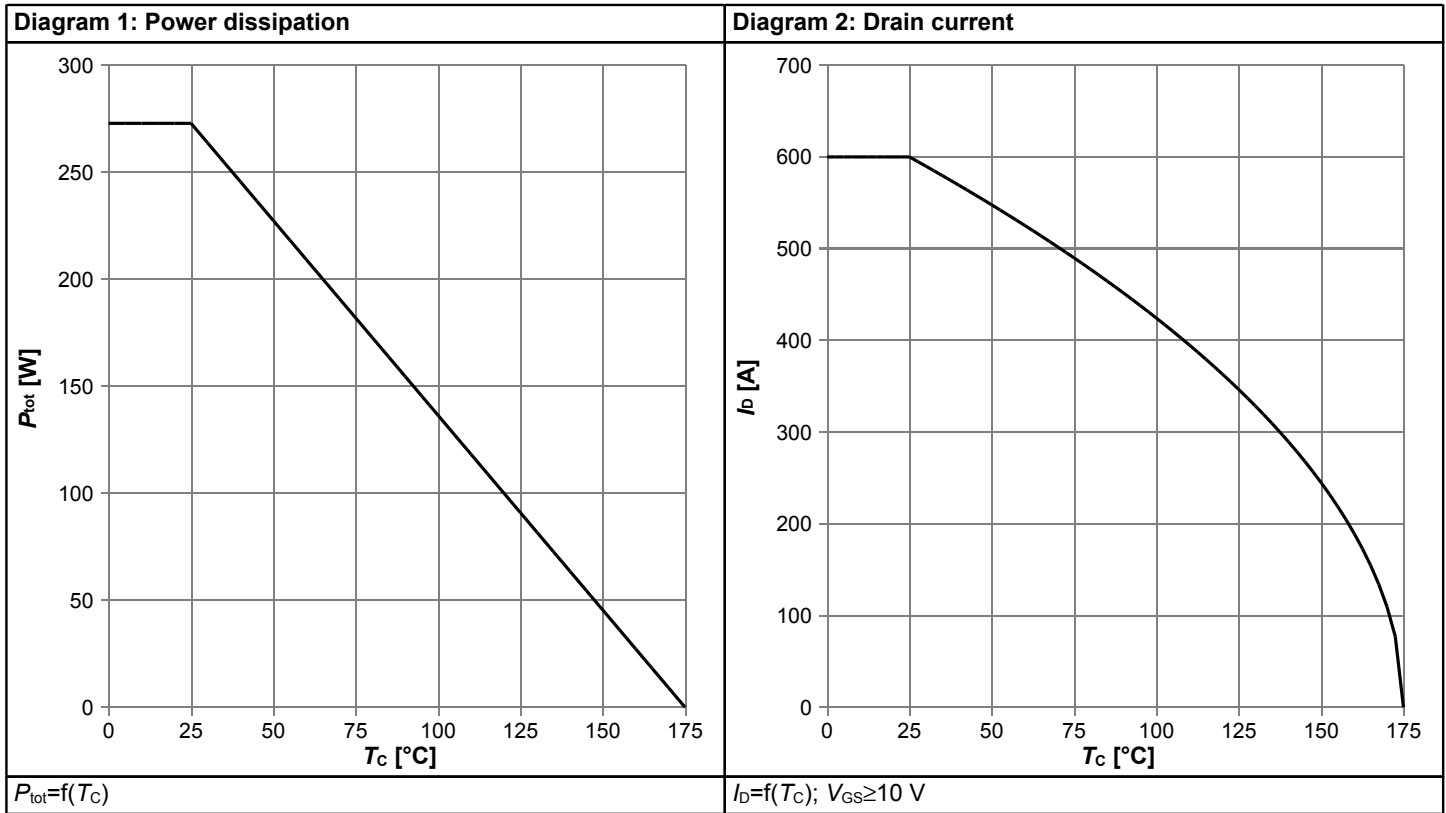
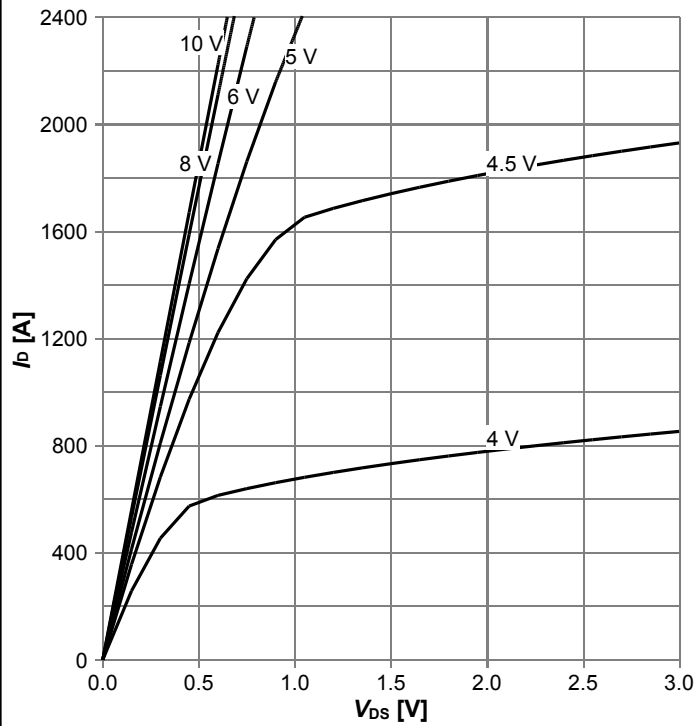
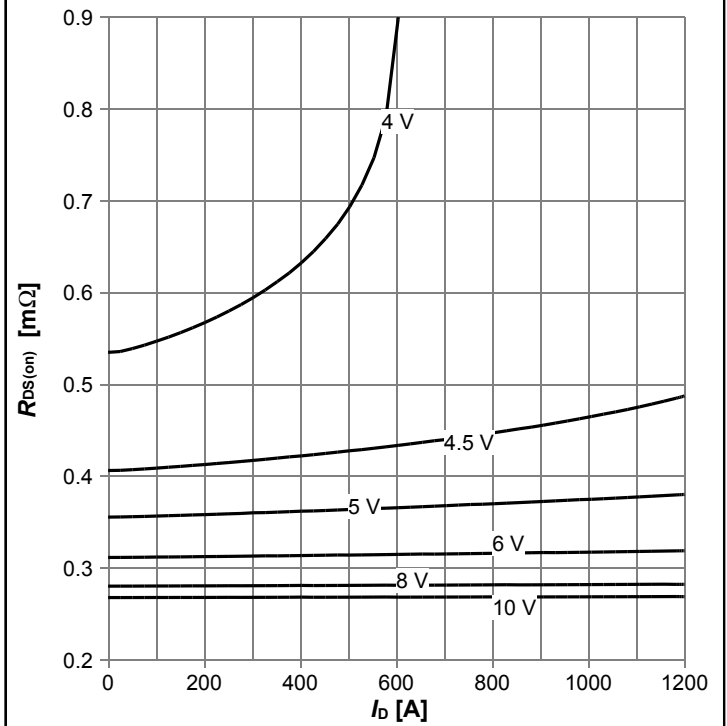


Diagram 5: Typ. output characteristics



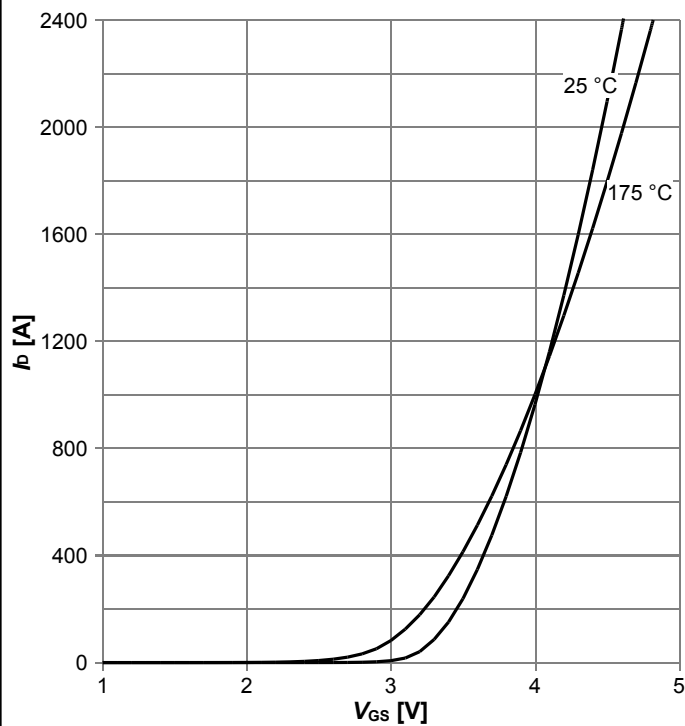
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



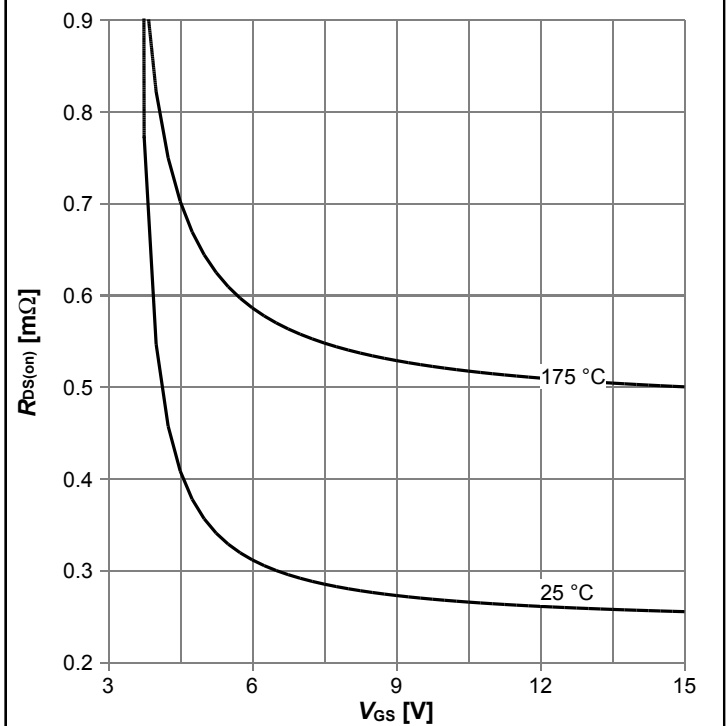
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



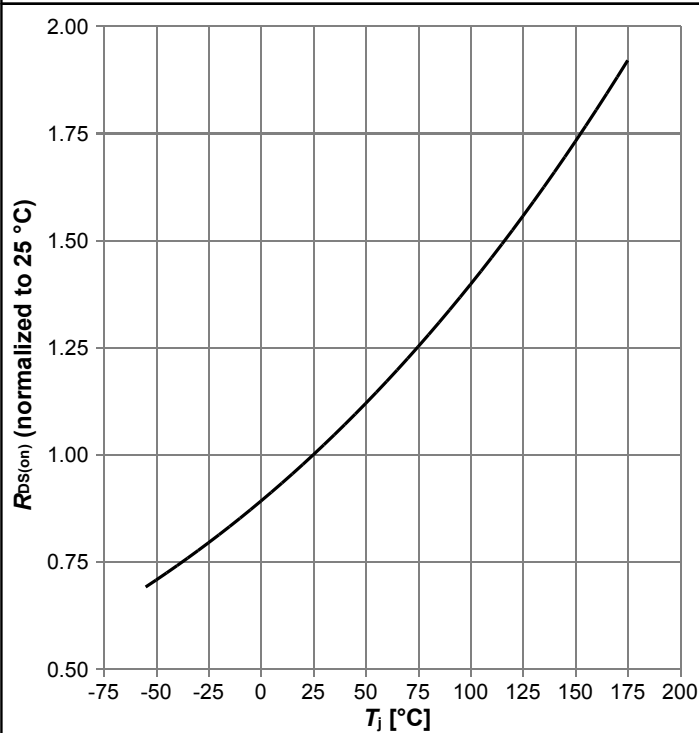
$I_D = f(V_{GS})$, $|V_{DS}| > 2 I_D R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



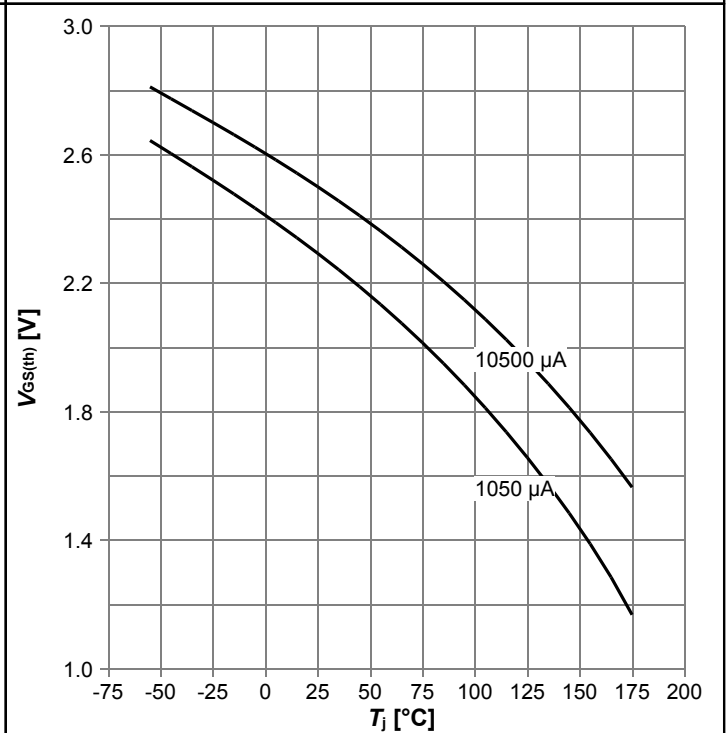
$R_{DS(on)} = f(V_{GS})$, $I_D = 100\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



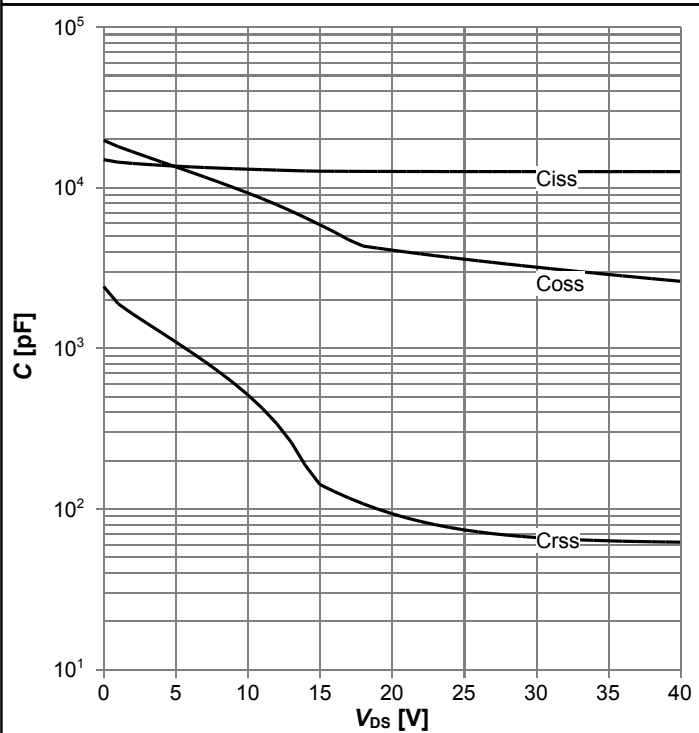
$R_{DS(on)}=f(T_j)$, $I_D=100$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



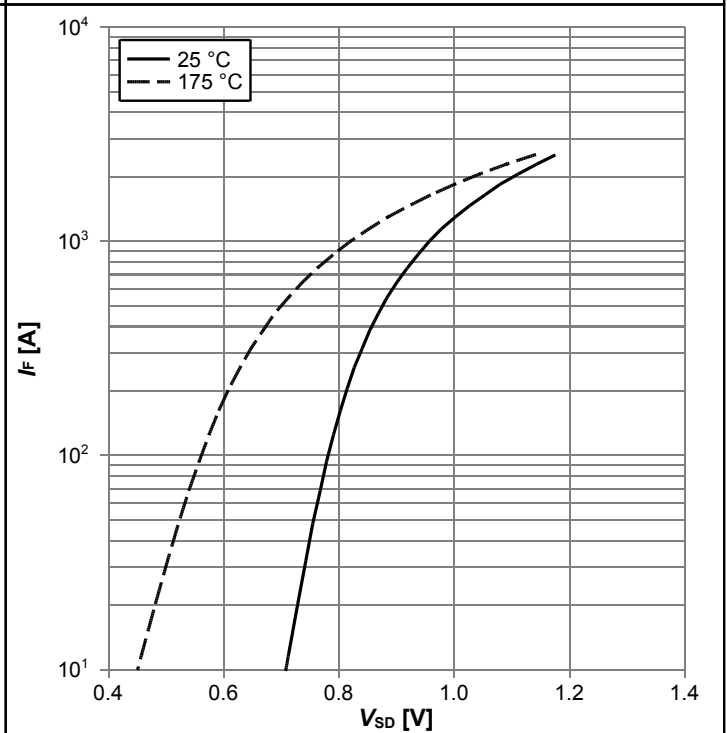
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



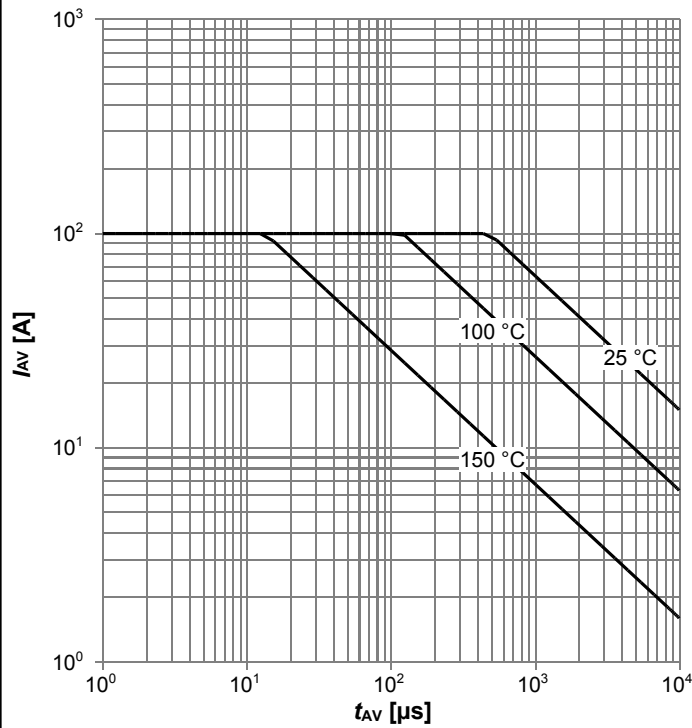
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode



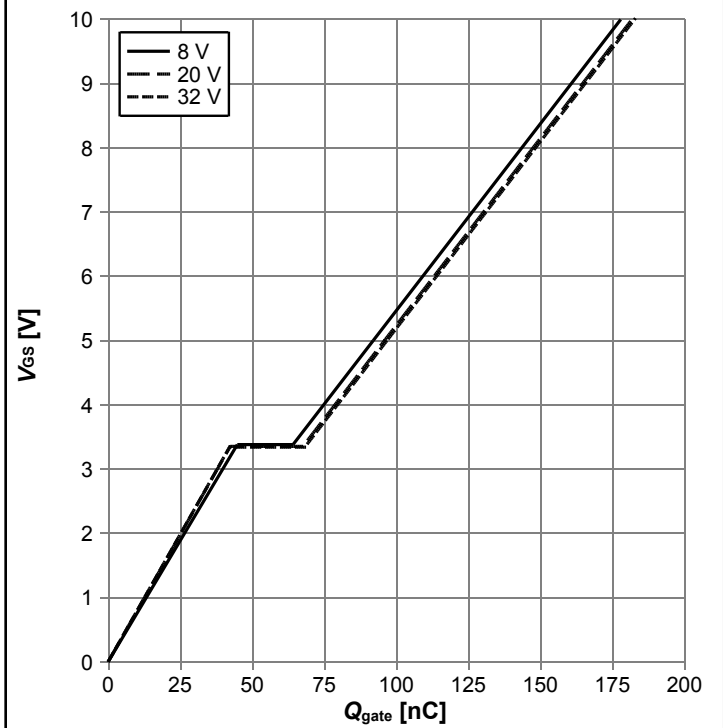
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



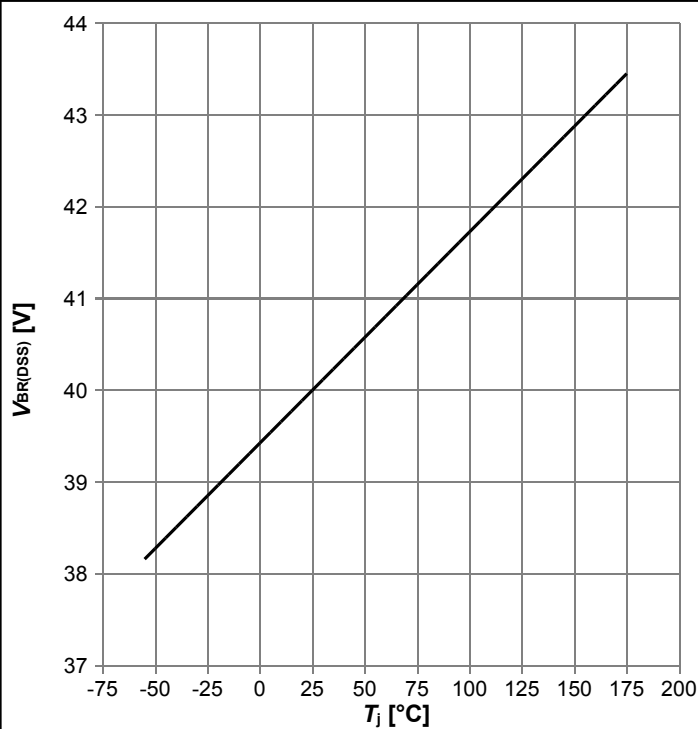
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



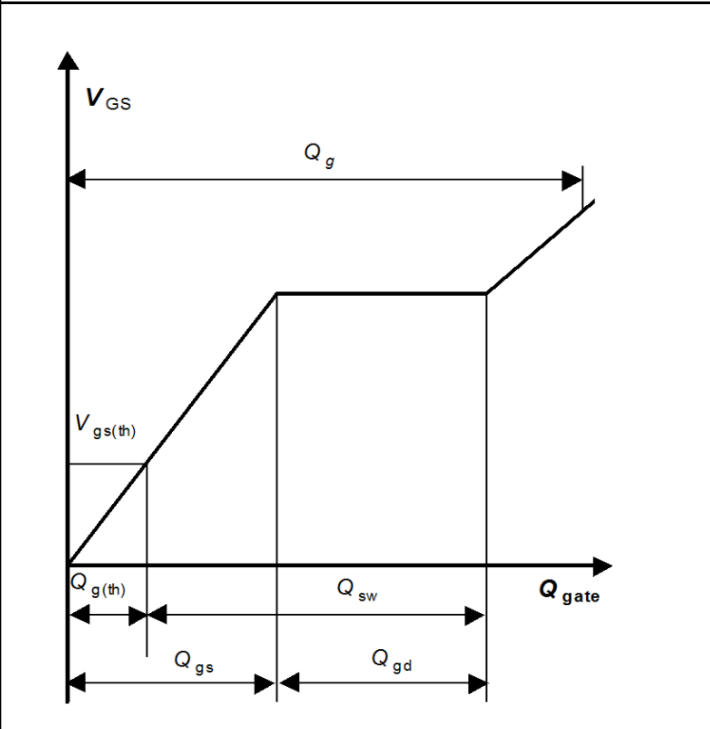
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

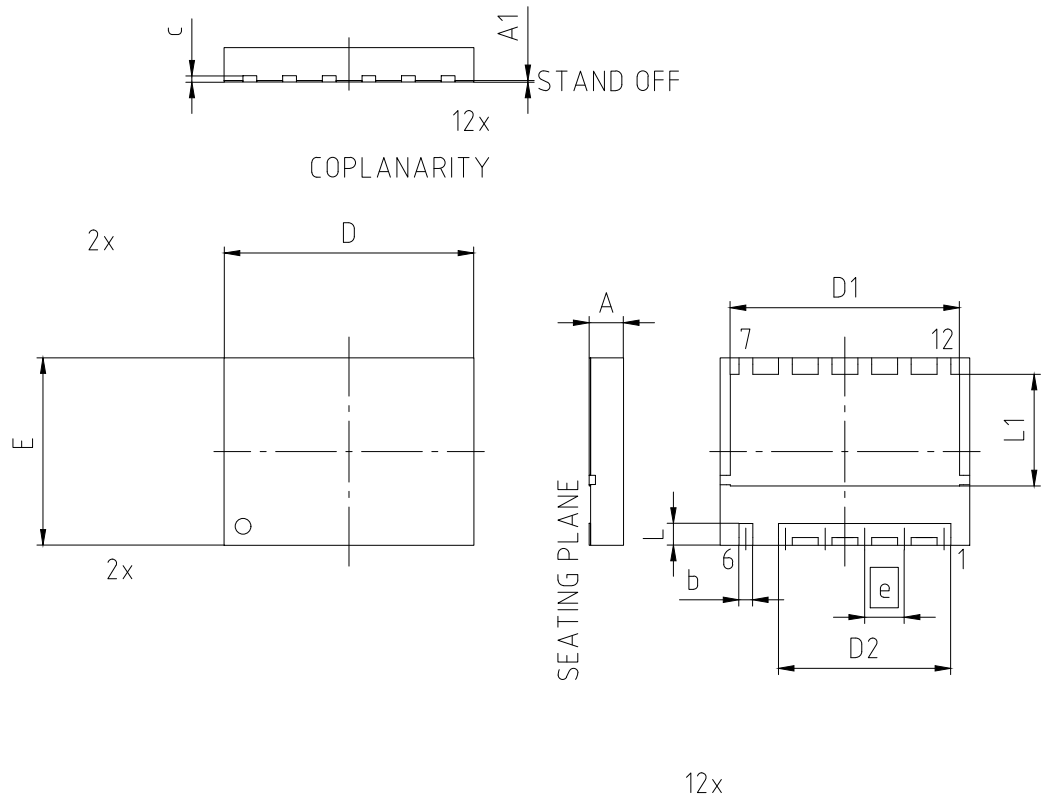


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines

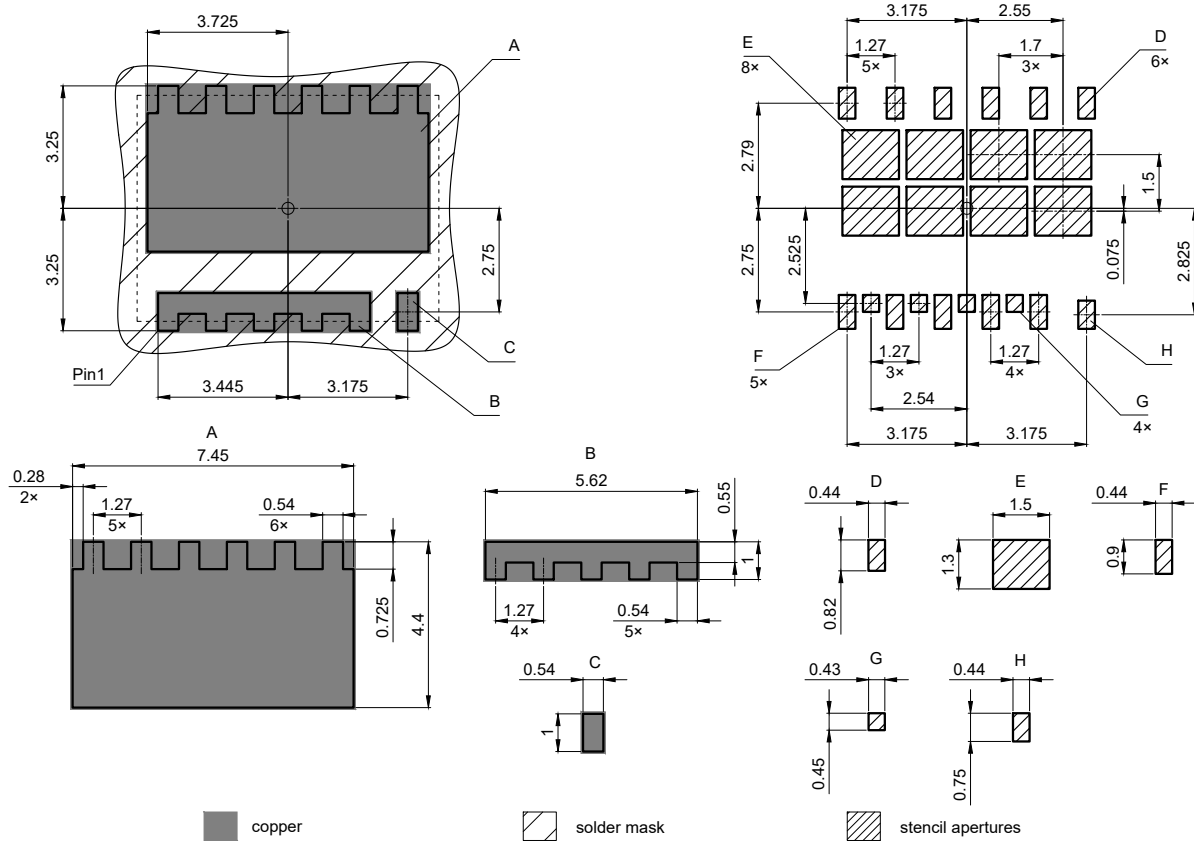


| PACKAGE - GROUP NUMBER: | | PG-TSON-12-U01 | |
|-------------------------|-------------|----------------|--|
| DIMENSIONS | MILLIMETERS | | |
| | MIN. | MAX. | |
| A | - | 1.10 | |
| A1 | - | 0.05 | |
| b | 0.39 | 0.49 | |
| c | 0.20 | | |
| D | 8.00 | | |
| D1 | 7.25 | 7.45 | |
| D2 | 5.42 | 5.62 | |
| E | 6.00 | | |
| e | 1.27 | | |
| L | 0.60 | 0.80 | |
| L1 | 3.48 | 3.68 | |

Figure 1 Outline PG-TSON-12, dimensions in mm

OptiMOS™6 Power-Transistor, 40 V

IQFH39N04NM6



All dimensions are in units mm
All pads are solder mask defined

Figure 2 Outline Boardpad (PG-TSON-12), dimensions in mm

Revision History

IQFH39N04NM6

Revision: 2023-09-06, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2023-09-06 | Release of final version |

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