

MOSFET
OptiMOS™ 7 Power-Transistor, 25 V

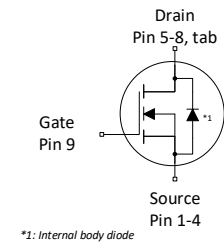
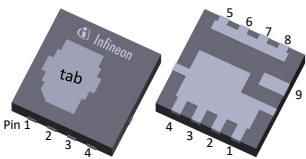
PG-WHTFN-9 (3x3)

Features

- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Optimized for hard-switching topologies
- Optimized for best FOM_{oss}
- Excellent Miller ratio for dv/dt ruggedness
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.



*1: Internal body diode

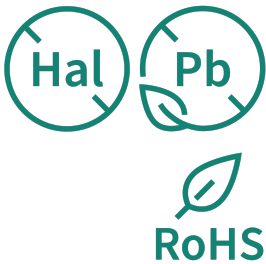


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	0.80	mΩ
I_D	282	A
Q_{oss}	24	nC
Q_G (0V...10V)	37	nC

Part number	Package	Marking	Related links
IQEH80NE2LM7UCGSC	PG-WHTFN-9	F	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	282	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				199		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				159		$V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$
				43		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1128	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	140	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	-	-	107	W	$T_C=25\text{ °C}$
				2.5		$T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.4	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		2.1	-		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	60		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.4	1.7	2.0	V	$V_{DS}=V_{GS}$, $I_D=279\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=22\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=22\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=16\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.71	0.8	m Ω	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
			1.0	1.26		$V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	0.85	-	Ω	-
Transconductance	g_{fs}	50	100	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3000	3900	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		1100	-		
Reverse transfer capacitance	C_{rss}		52	-		
Turn-on delay time	$t_{d(on)}$	-	5.4	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r		1.4			
Turn-off delay time	$t_{d(off)}$		20.1			
Fall time	t_f		2.7			

Table 6 Gate charge characteristics ⁶⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.8	-	nC	$V_{DD}=12\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		5.2		nC	
Gate to drain charge	Q_{gd}		2.7		nC	
Switching charge	Q_{sw}		6.4		nC	
Gate charge total	Q_g		17.2		nC	
Gate plateau voltage	$V_{plateau}$		2.9		V	
Gate charge total	Q_g	-	37	-	nC	$V_{DD}=12\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	24	-	nC	$V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$

⁶⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	98	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1128		
Diode forward voltage	V_{SD}	-	0.77	1.0	V	$V_{GS}=0\text{ V}$, $I_F=20\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	30	-	ns	$V_R=12\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		26		nC	
Reverse recovery time	t_{rr}	-	21	-	ns	$V_R=12\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		75		nC	

4 Electrical characteristics diagrams

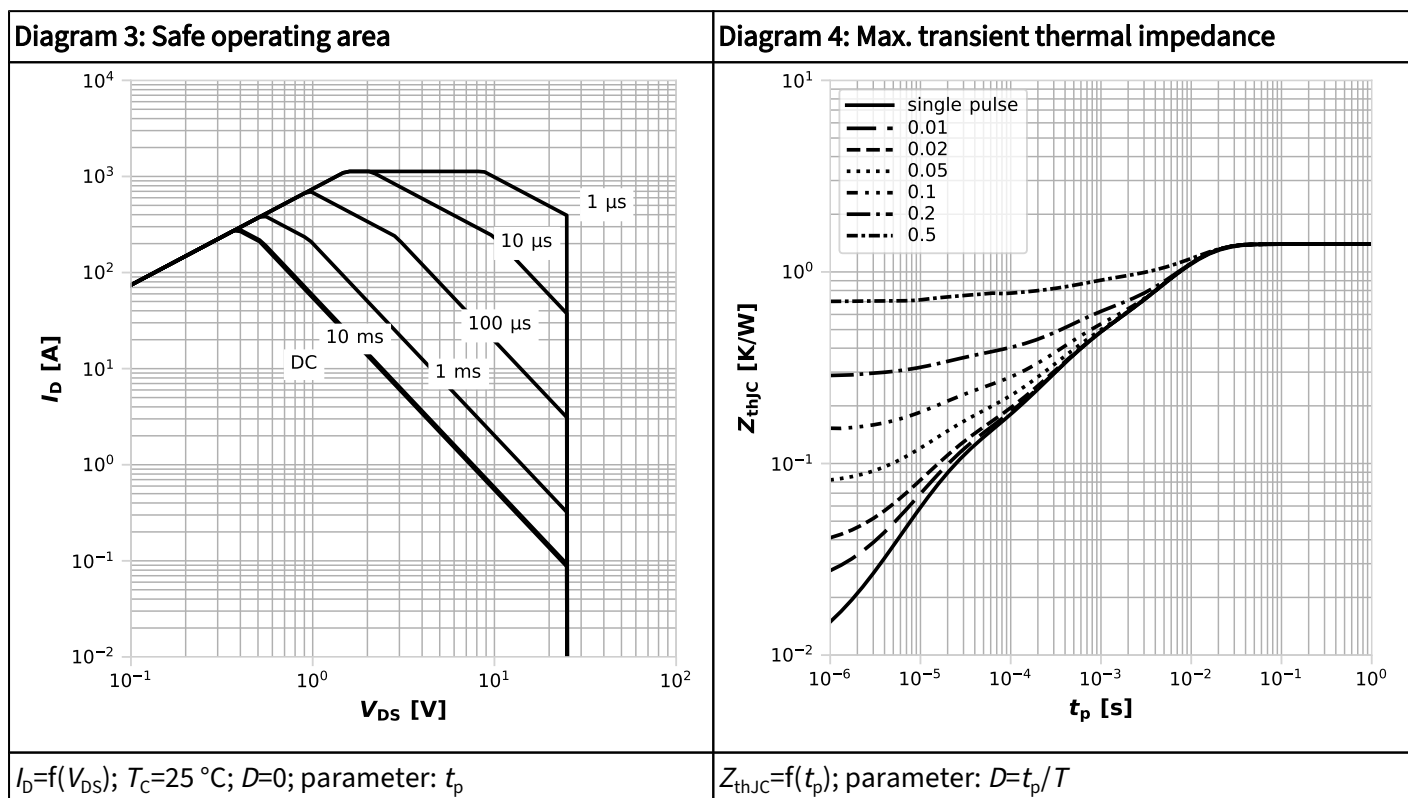
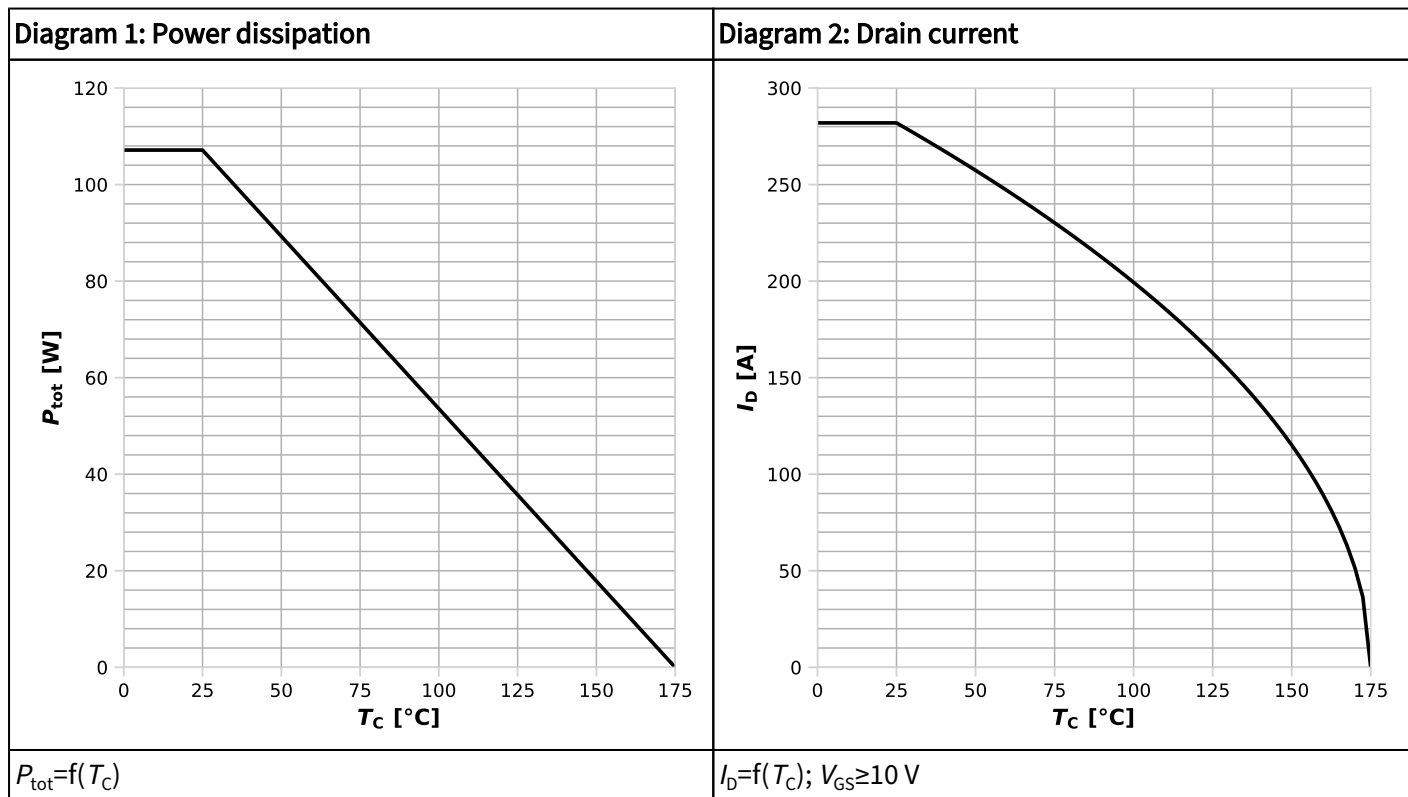
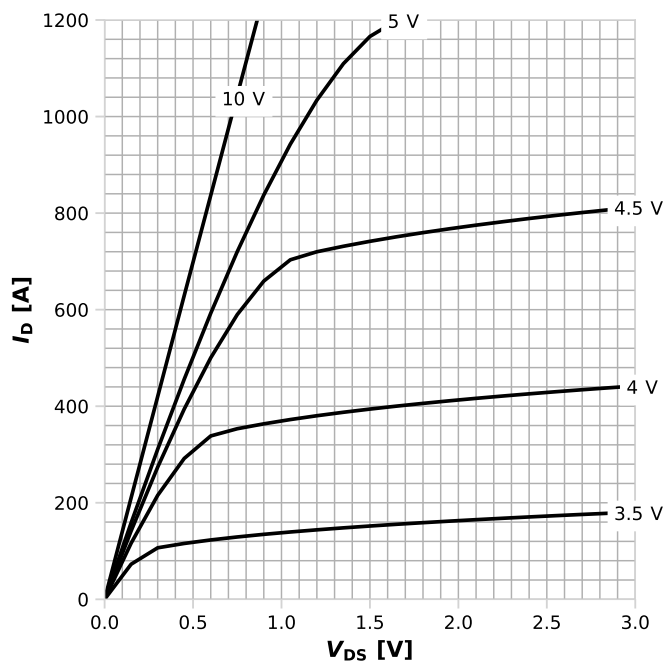
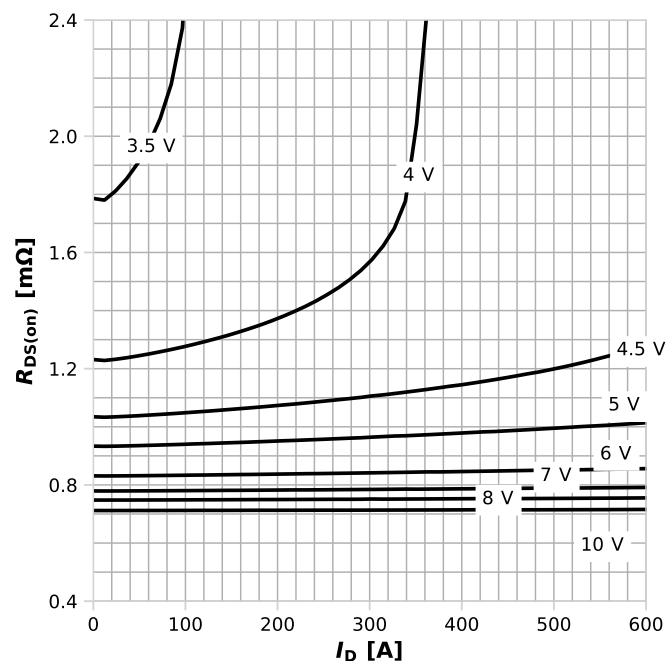


Diagram 5: Typ. output characteristics



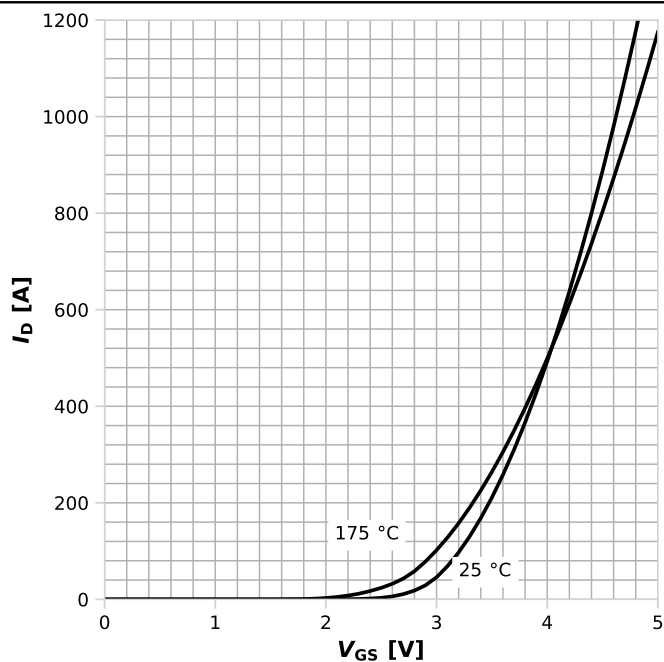
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



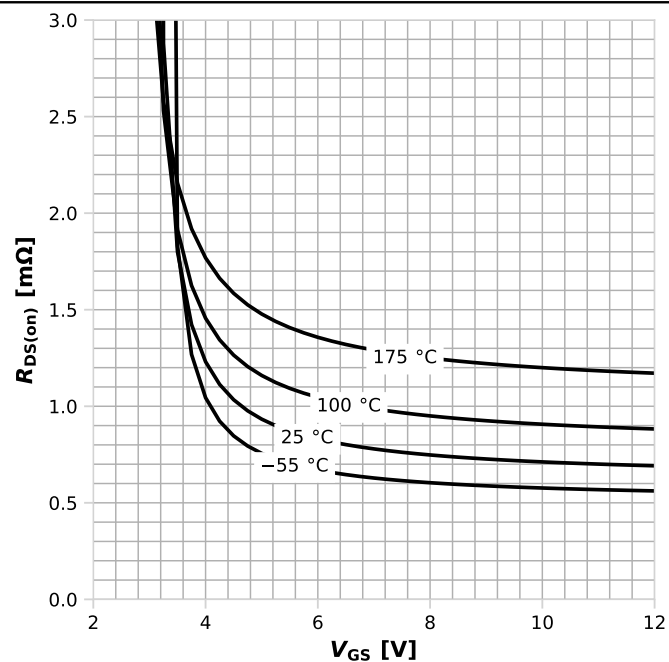
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



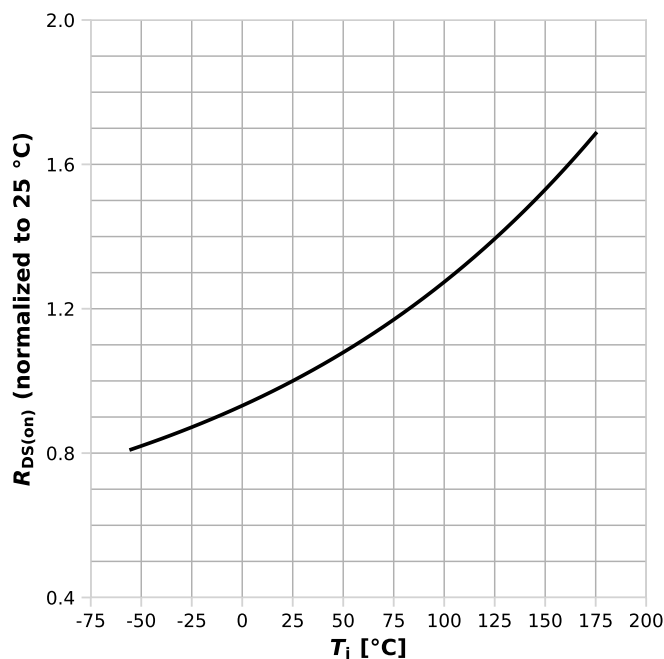
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



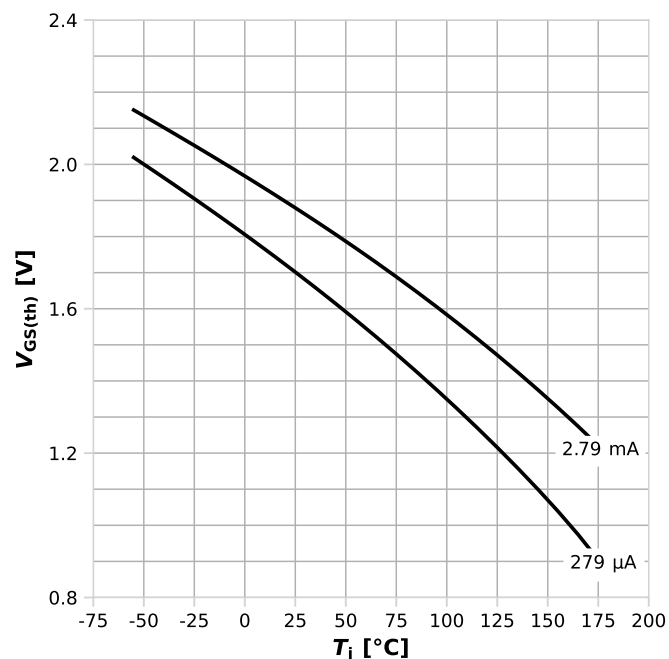
$R_{DS(on)} = f(V_{GS})$, $I_D = 20\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



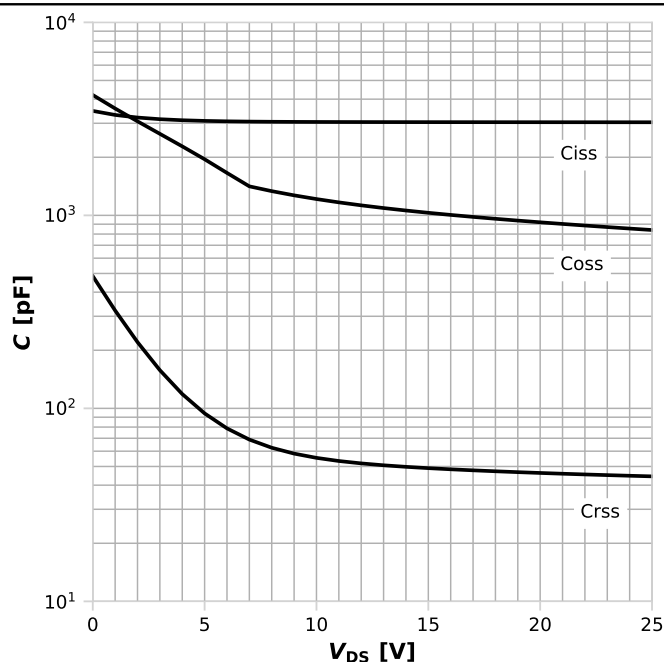
$$R_{DS(on)} = f(T_j), I_D = 20 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



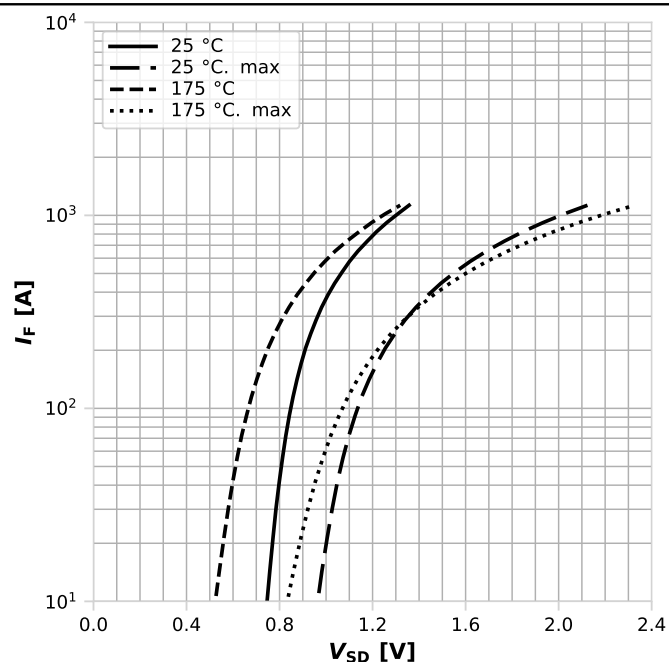
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



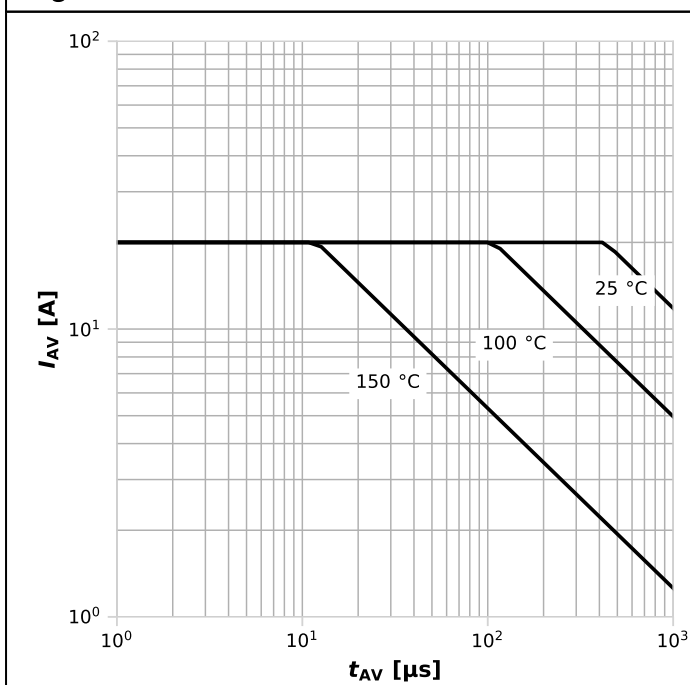
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



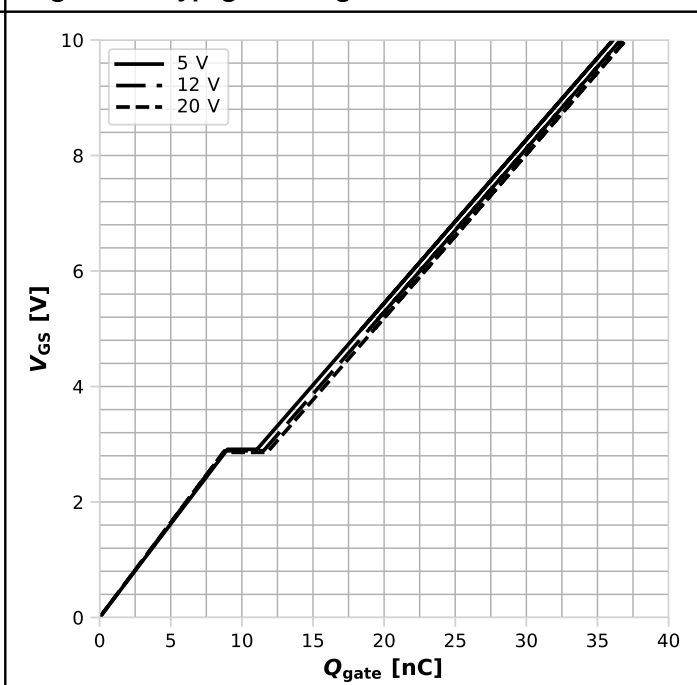
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



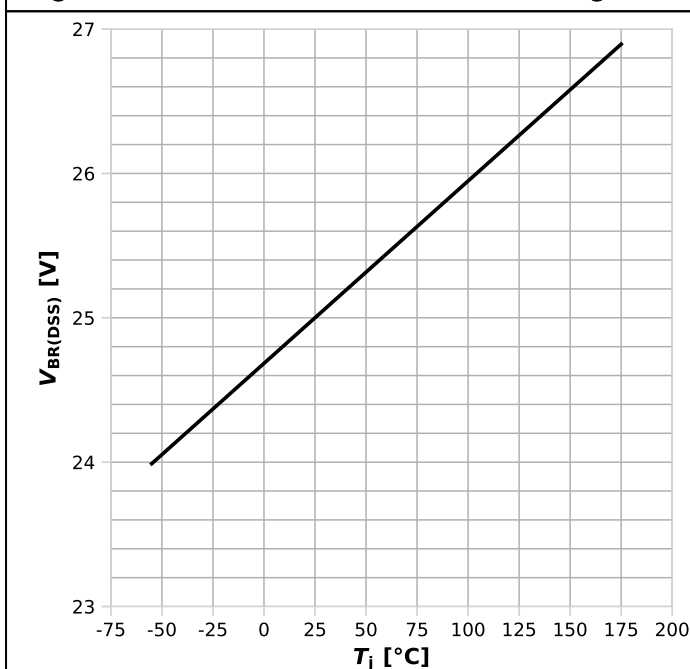
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



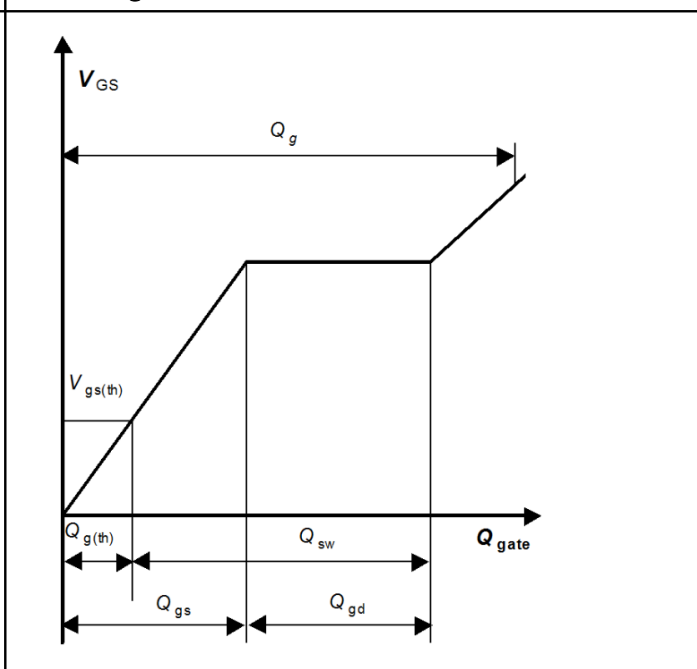
$V_{GS}=f(Q_{gate})$, $I_D=20\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



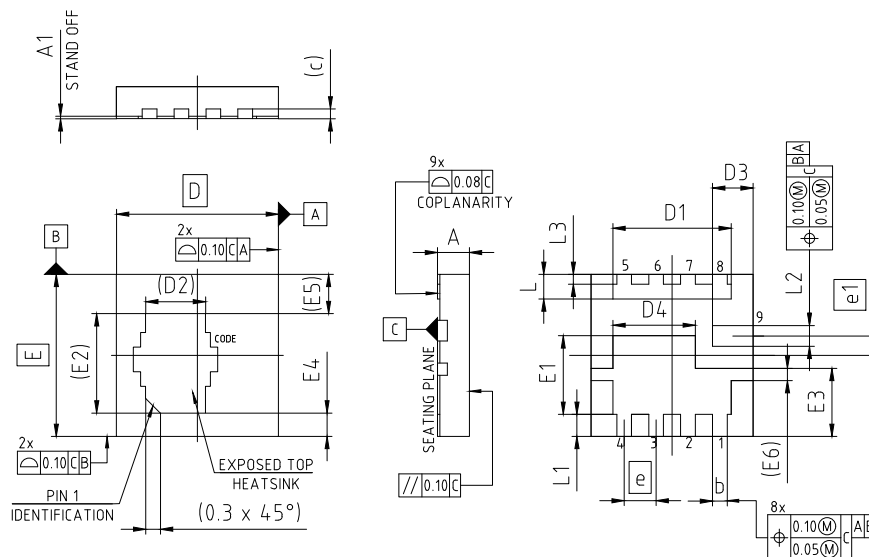
$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package outlines



PACKAGE - GROUP
NUMBER:

PG-WHTFN-9-U03

DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS			
	MIN.	MAX.		MIN.	MAX.		
A	0.55	0.75	E4	0.27	0.67		
A1	---	0.05	E5				
b	0.20	0.40	E6			0.80	
c	0.20		e			0.25	
D	3.30		e1			0.65	
D1	2.31	2.51	e1			0.395	
D2	1.22		L	0.40	0.60		
D3	0.73	0.93	L1	0.35	0.55		
D4	1.58	1.78	L2	0.32	0.52		
E	3.30		L3	0.10	0.30		
E1	1.50	1.70					
E2	2.03						
E3	1.285	1.485					

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WHTFN-9, dimensions in mm

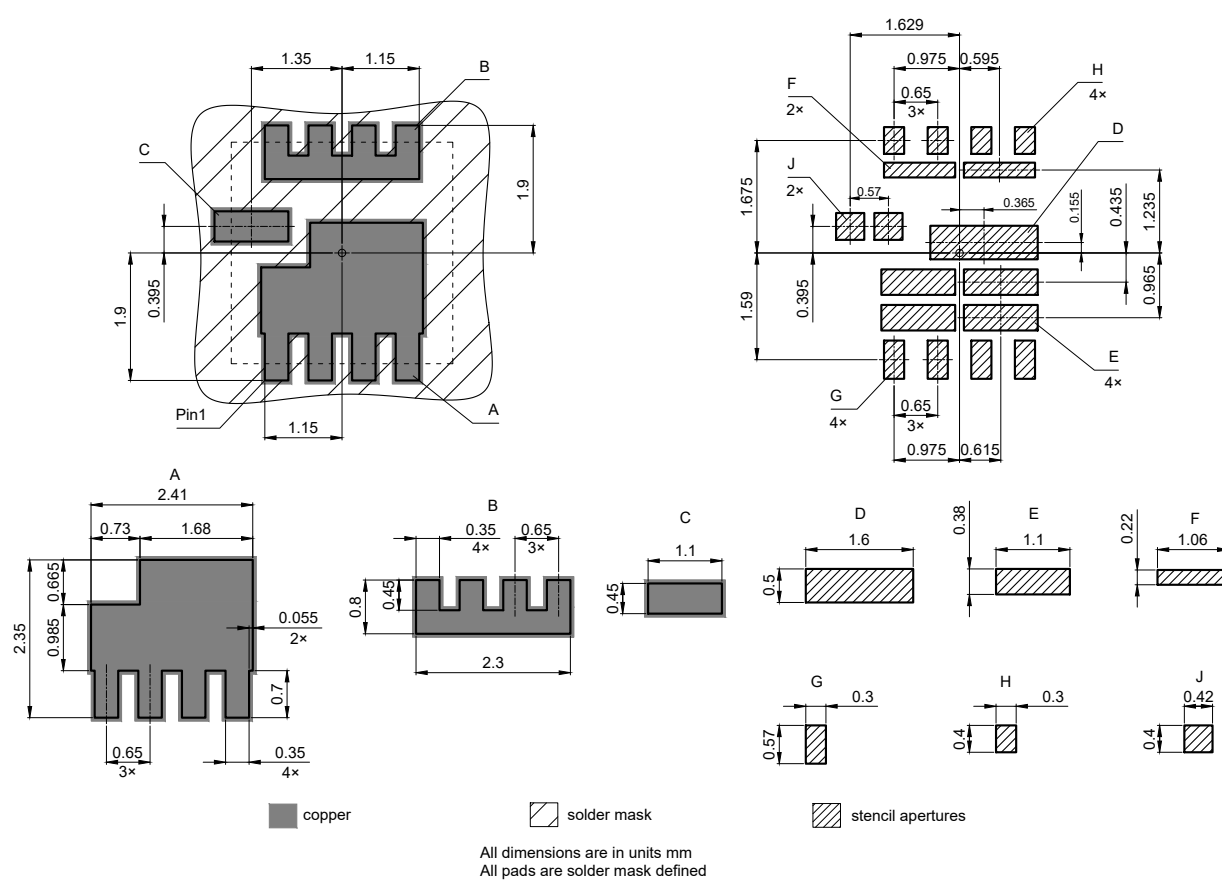


Figure 2 Footprint drawing PG-WHTFN-9, dimensions in mm

Revision history

IQEH80NE2LM7UCGSC

Revision 2025-08-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-08-07	Release of final datasheet

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