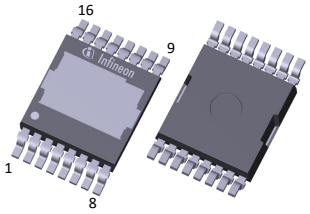
MOSFET

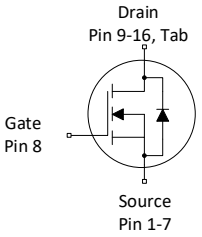
OptiMOS™ 6 Power-Transistor, 200 V

TOLT



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested

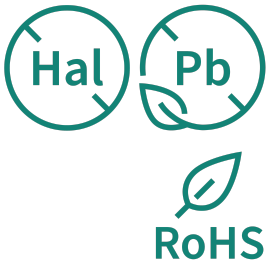


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	6.8	mΩ
I_D	140	A
Q_{oss}	226	nC
Q_G	71	nC
Q_{rr} (1000A/µs)	339	nC



Part number	Package	Marking	Related links
IPTC068N20NM6	PG-HDSOP-16	068N20N6	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	140	A	V_{GS}=10 V, T_C=25 °C
				99		V_{GS}=10 V, T_C=100 °C
				103		V_{GS}=15 V, T_C=100 °C
				15.2		V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	560	A	T_C=25 °C
Avalanche current, single pulse [4]	I_{AS}			75		
Avalanche energy, single pulse	E_{AS}	-	-	503	mJ	I_D=75 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	319	W	T_C=25 °C
				3.8		T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, Top	R_{thJC}	-	0.24	0.47	°C/W	-
Thermal characterization parameter, juntion to lead (Pin 1-7) [5]	Ψ_{JL}		9	-		
Thermal characterization parameter, juntion to lead (Pin 9-16) [5]	Ψ_{JL}		3	-		
Thermal resistance, junction - ambient	R_{thJA}	-	40	-	°C	6 cm^2 cooling area [6]

[5] Ψ_{JL} is a temperature characterization parameter according to JESD51-12 referring to the temperature difference between junction and leads in the case of natural convection. It can be used to estimate the component junction temperature in the application by measuring the temperature at the leads in the stated application environment

[6] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	V_{DS}=V_{GS}, I_D=251 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=160 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=160 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	5.7	6.8	mΩ	V_{GS}=10 V, I_D=126 A
			4.9	6.25		V_{GS}=15 V, I_D=126 A
Gate resistance	R_G	-	2.2	-	Ω	-
Transconductance [7]	g_{fs}	33	65	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

[7] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [8]	C_{iss}	-	5600	7300	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance [8]	C_{oss}		890	1200		
Reverse transfer capacitance [8]	C_{rss}		29	51		
Turn-on delay time	$t_{d(on)}$	-	19	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω
Rise time	t_r		15			
Turn-off delay time	$t_{d(off)}$		28			
Fall time	t_f		9			

[8] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [9)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	37	-	nC	V_{DD}=100 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		21	-	nC	
Gate to drain charge [10)]	Q_{gd}		14	21	nC	
Switching charge	Q_{sw}		30	-	nC	
Gate charge total [10)]	Q_g		71	107	nC	
Gate plateau voltage	$V_{plateau}$		6.6	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	61	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [10)]	Q_{oss}	-	226	294	nC	V_{DS}=100 V, V_{GS}=0 V

[9)] See "Gate charge waveforms" for parameter definition

[10)] Defined by design. Not subject to production test.

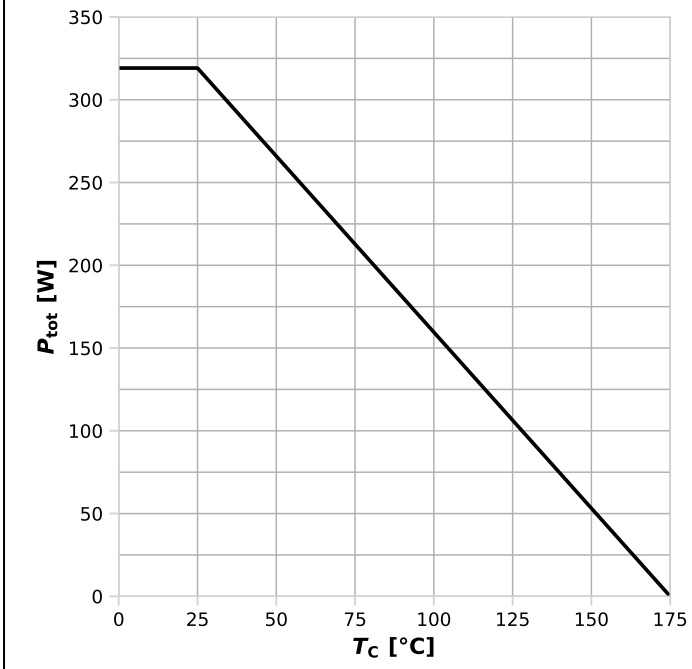
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	140	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			560		
Diode forward voltage	V_{SD}	-	0.91	1.0	V	V_{GS}=0 V, I_F=126 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	56	-	ns	V_R=100 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [11)]	Q_{rr}		63	126	nC	
Reverse recovery time	t_{rr}	-	36	-	ns	V_R=100 V, I_F=50 A, di_F/dt=1000 A/µs
Reverse recovery charge [11)]	Q_{rr}		339	678	nC	

[11)] Defined by design. Not subject to production test.

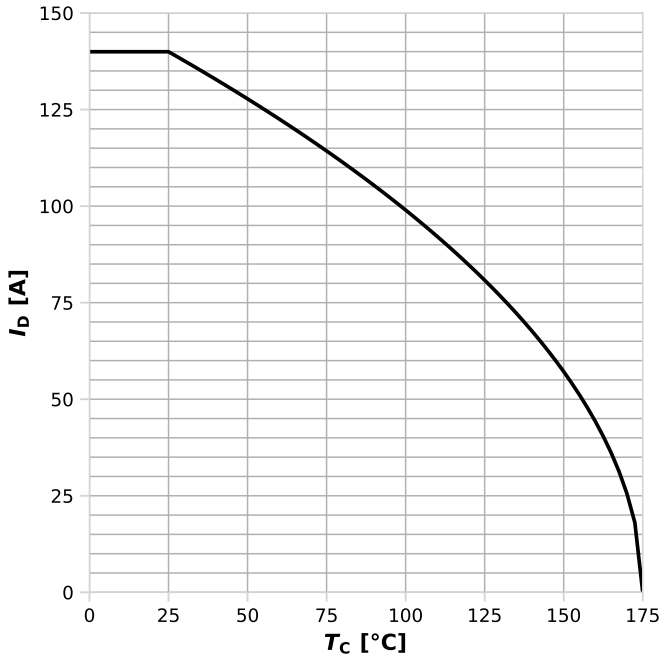
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



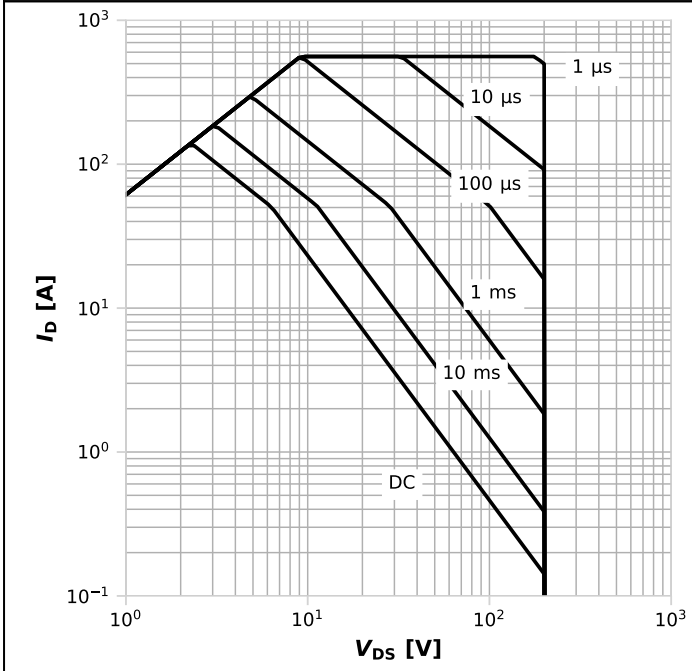
P_{tot}=f(T_C)

Diagram 2: Drain current



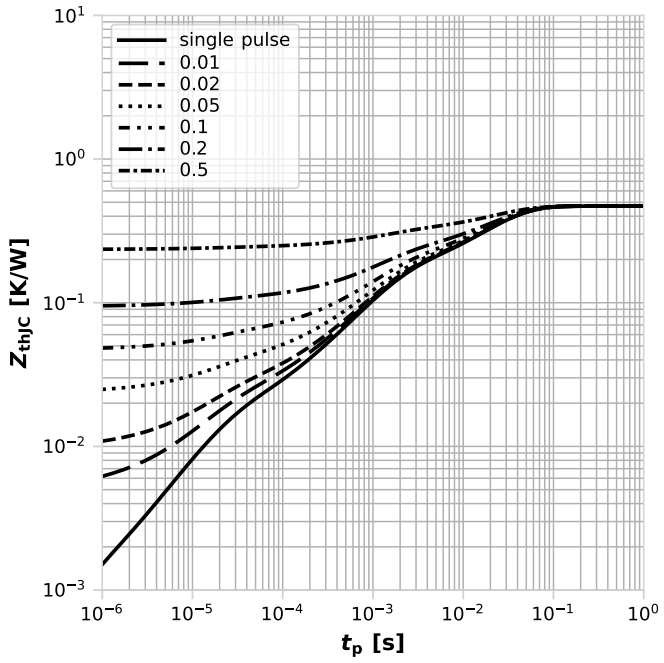
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

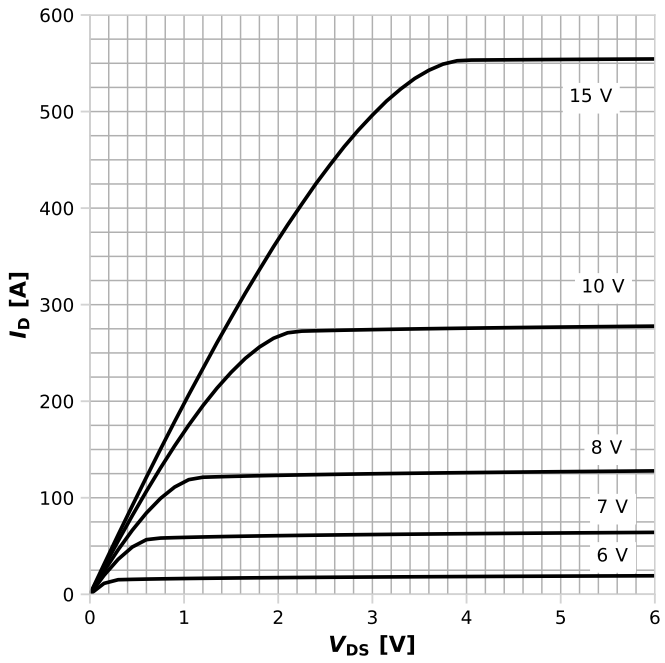
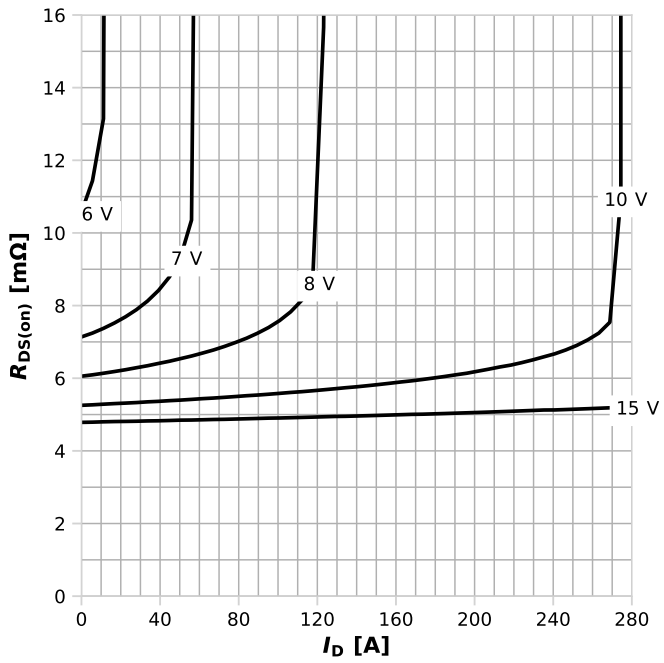
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

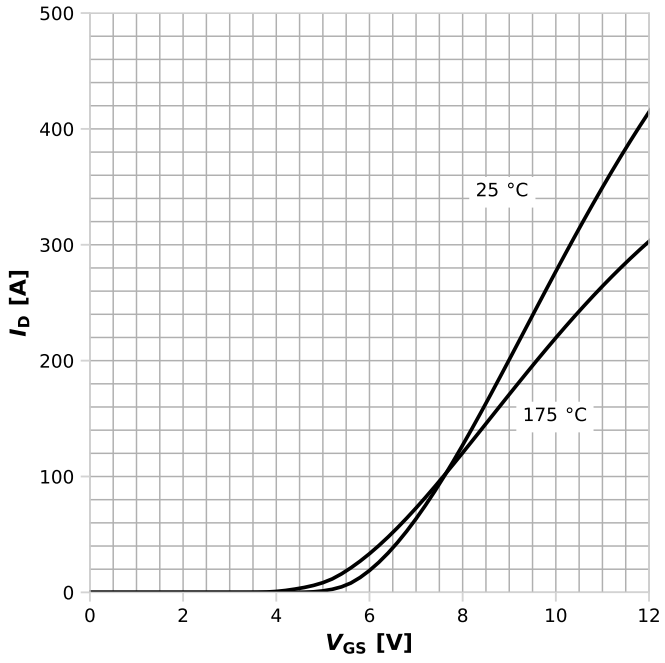
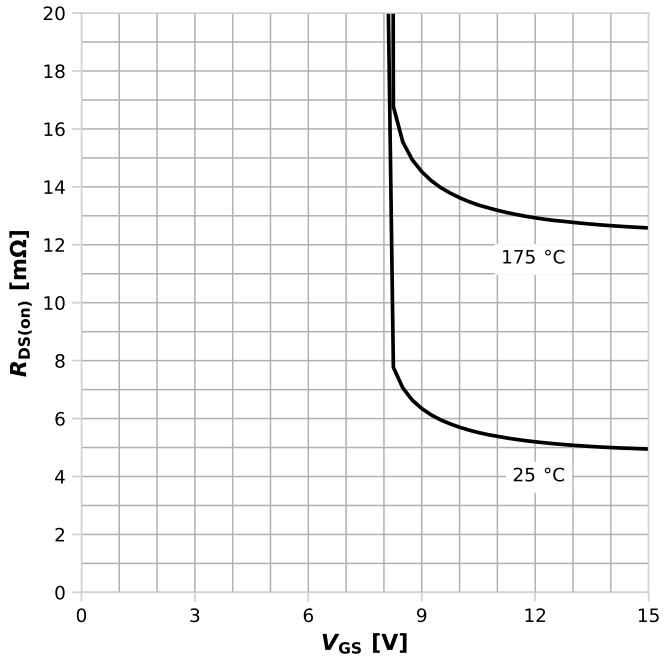
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$; parameter: T_j	$R_{DS(on)}=f(V_{GS})$, I_D=126 A; parameter: T_j

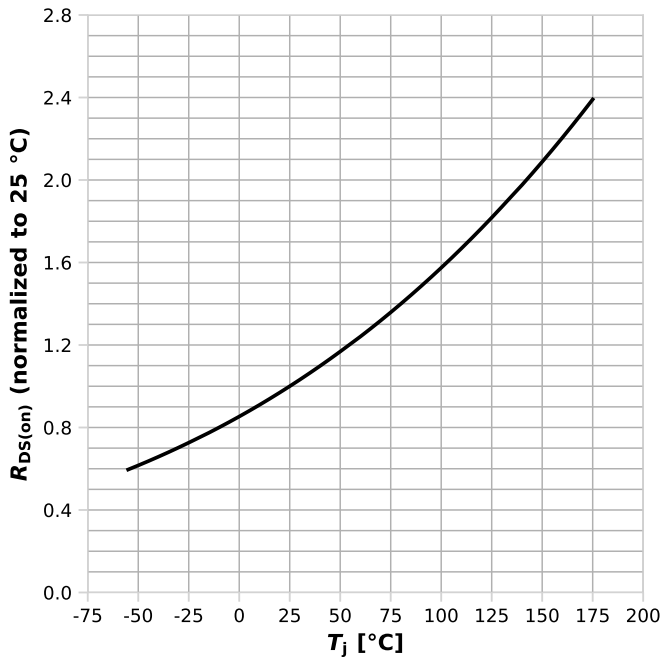
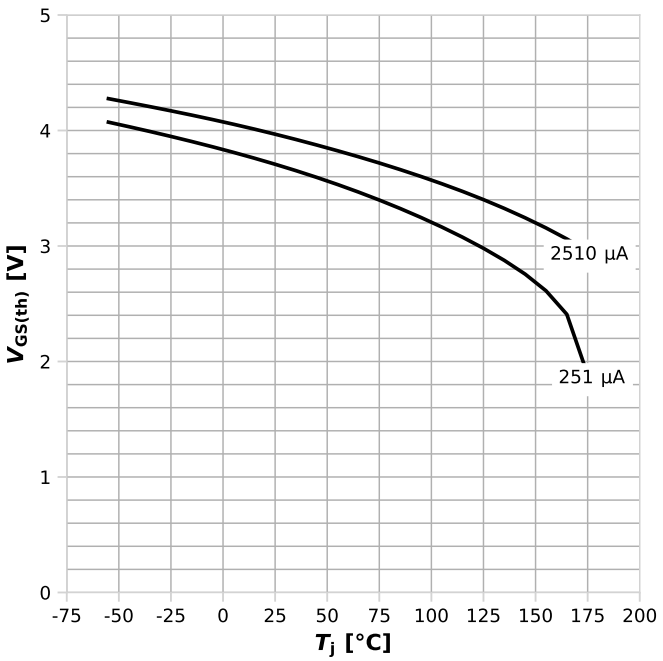
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=126 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

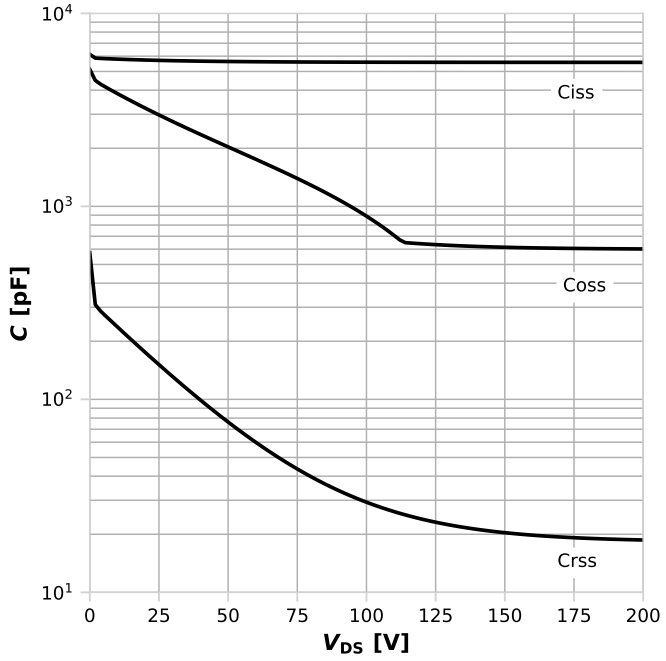
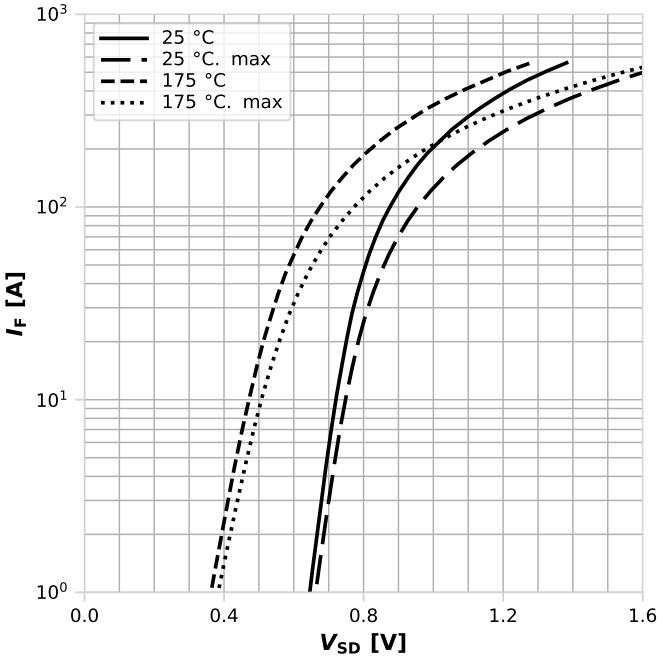
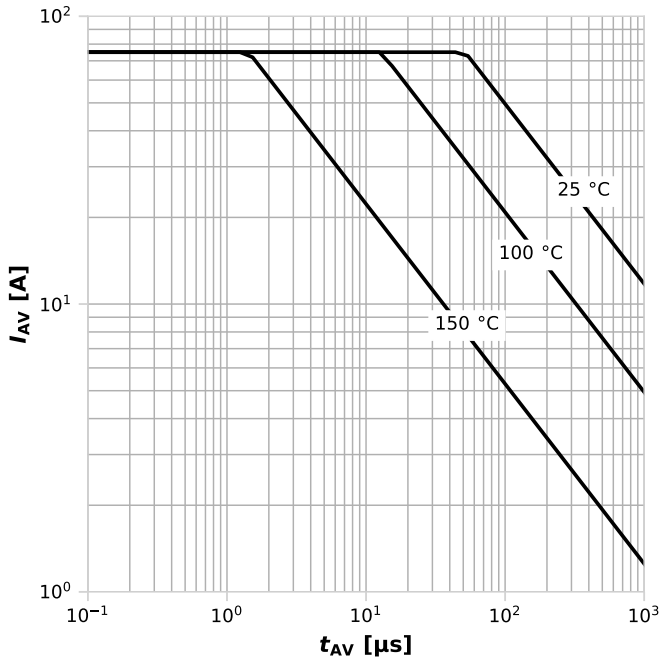
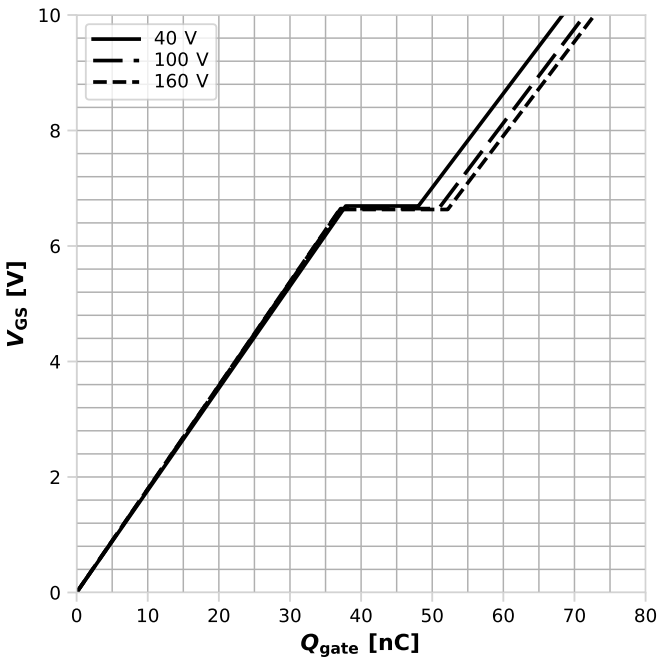
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



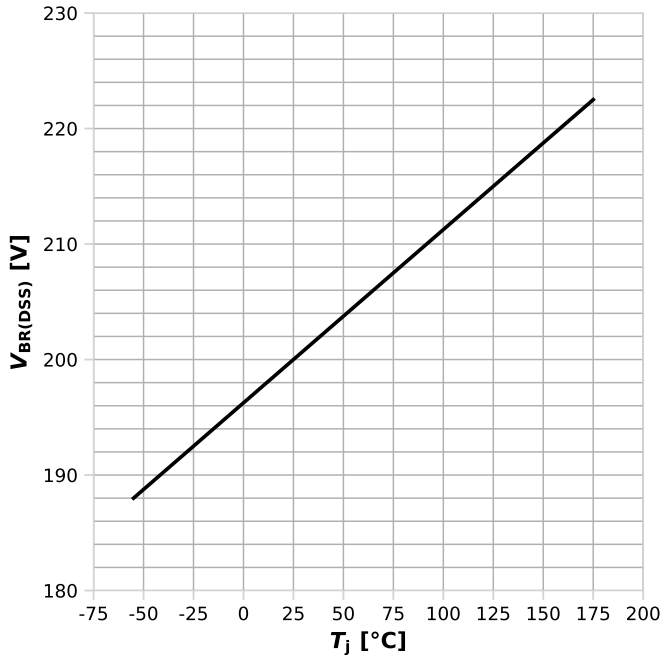
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



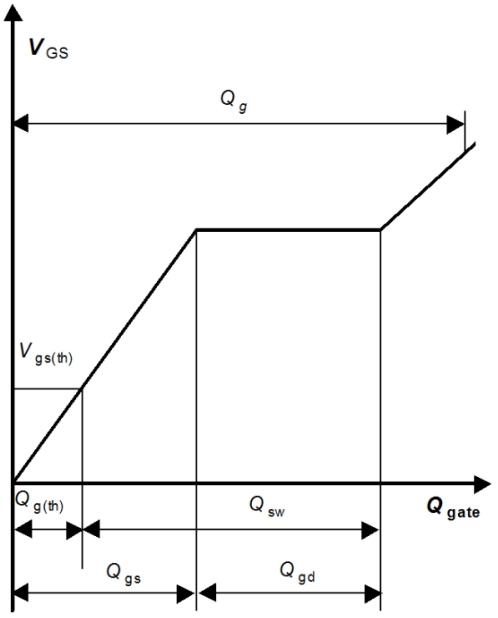
V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



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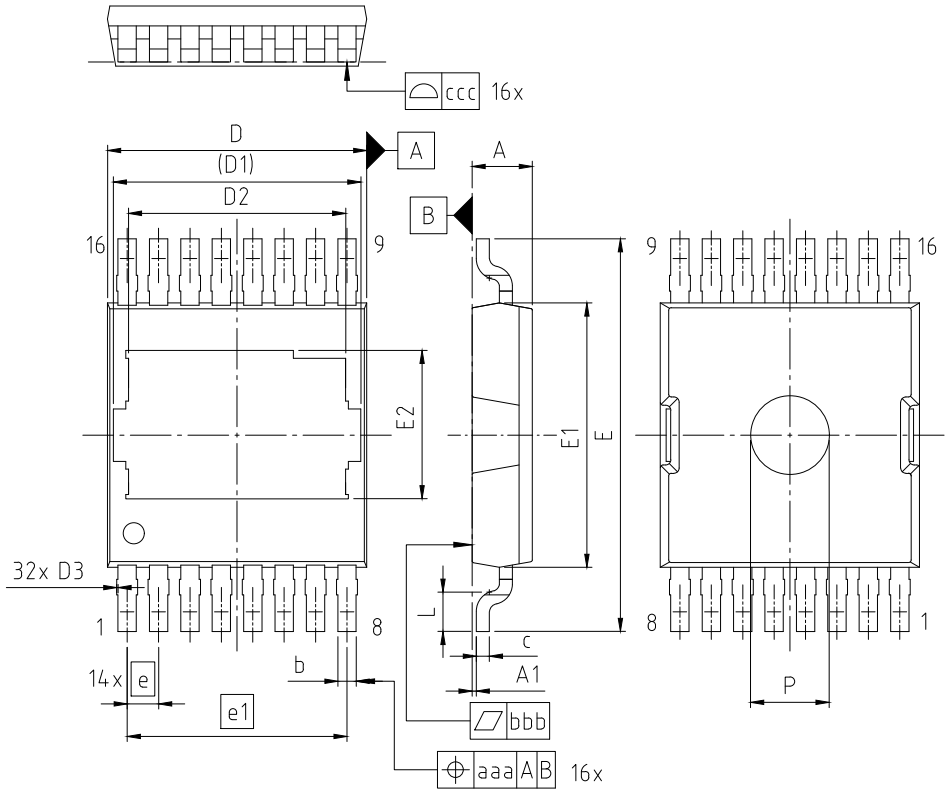
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U04				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	2.25	2.35	e	1.20	
A1	0.01	0.16	e1	8.40	
b	0.60	0.80	L	1.40	1.60
c	0.40	0.60	P	2.90	3.10
D	9.70	10.10	aaa	0.25	
D1	9.46		bbb	0.02	
D2	8.20	8.40	ccc	0.10	
D3	---	0.15			
E	14.80	15.20			
E1	10.00	10.30			
E2	5.57	5.77			

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

Figure 1 Outline PG-HDSOP-16, dimensions in mm

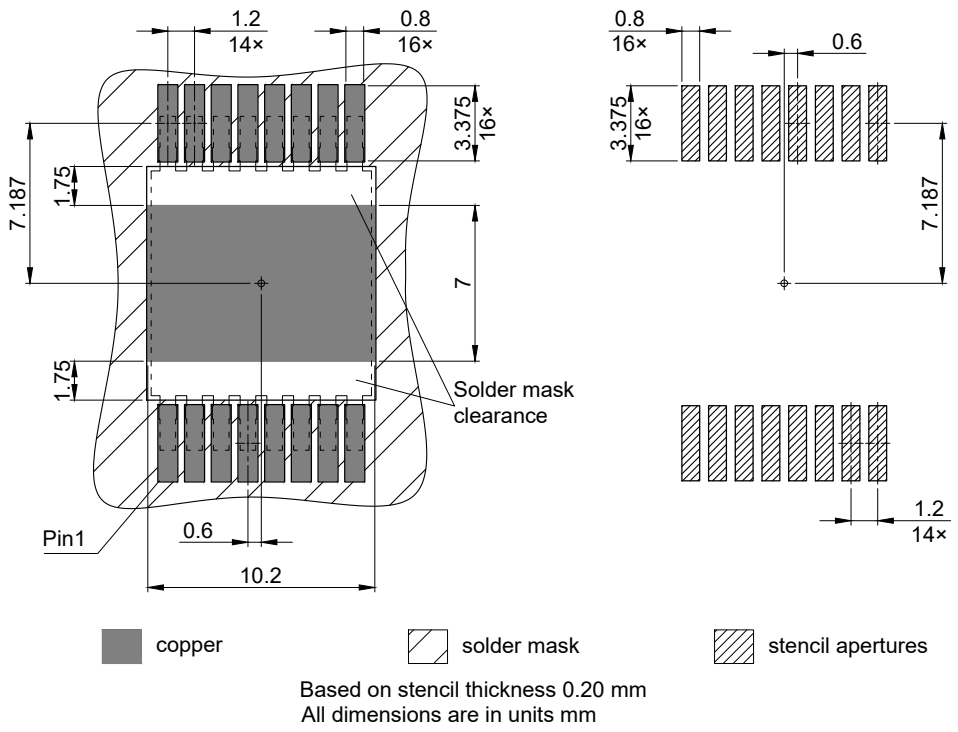


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm

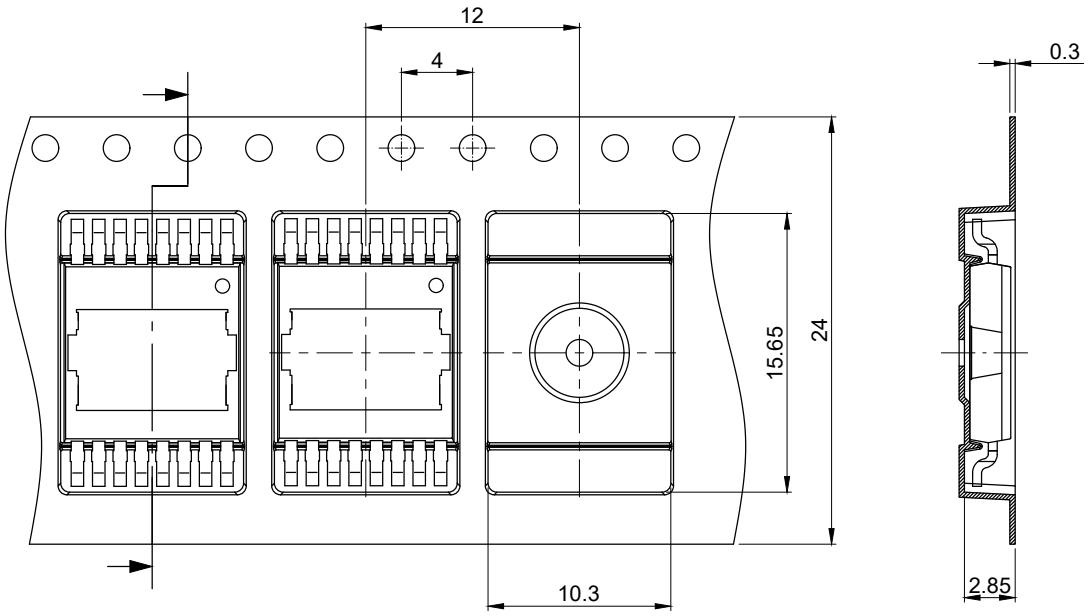


Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

Revision history

IPTC068N20NM6

Revision 2025-03-27, Rev. 2.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2025-03-27	Release of final datasheet

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