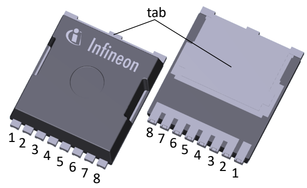
MOSFET

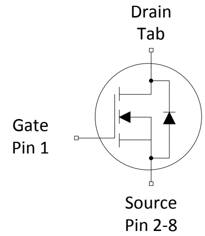
OptiMOS™ 5 Linear FET 2, 100 V

TOLL



Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.7	mΩ
I_D	321	A
I_{pulse} (V_{DS}=56 V, t_p=10 ms)	6.7	A

Type/Ordering Code	Package	Marking	Related Links
IPT017N10NM5LF2	PG-HSOF-8	17N10LF2	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	321 227 234 32	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=15 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1284	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	775	mJ	I_D=150 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	375 3.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3) See Diagrams 3 and 4 for more detailed information

4) See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.9	V	V_{DS}=V_{GS}, I_D=280 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3 1.5	1.6 1.7	mΩ	V_{GS}=15 V, I_D=150 A V_{GS}=10 V, I_D=150 A
Gate resistance	R_G	-	1.4	2.1	Ω	-
Transconductance	g_{fs}	80	160	-	S	$\|V_{DS}\|≥2\|I_D\|R_{DS(on)max}$, I_D=150 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [6)]	C_{iss}	-	13000	17000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [6)]	C_{oss}	-	1800	2300	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance [6)]	C_{rss}	-	35	61	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	29	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	24	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	45	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	20	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω

6) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	84	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	41	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge [8)]	Q_{gd}	-	27	41	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	70	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total [8)]	Q_g	-	165	206	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	150	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8)]	Q_{oss}	-	211	281	nC	V_{DS}=50 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition
8) Defined by design. Not subject to production test.

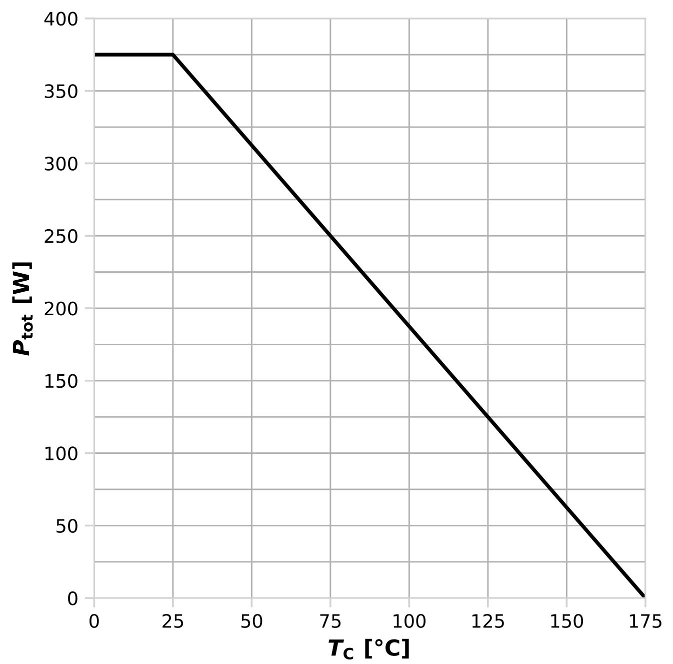
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	252	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1284	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	58	116	ns	V_R=50 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}	-	103	206	nC	V_R=50 V, I_F=100 A, di_F/dt=100 A/µs

9) Defined by design. Not subject to production test.

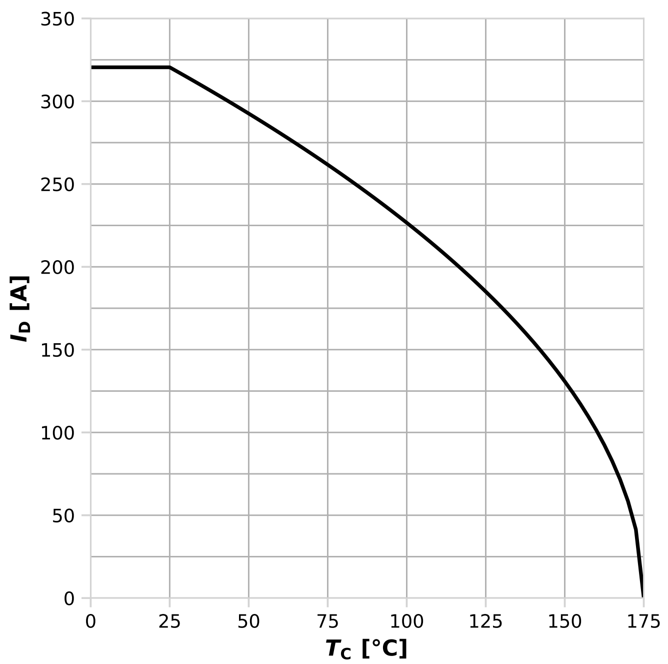
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



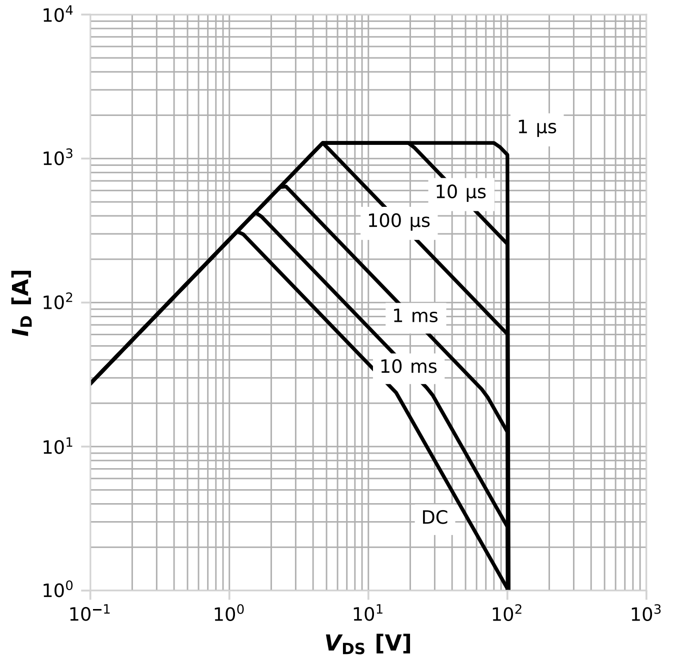
P_{tot}=f(T_C)

Diagram 2: Drain current



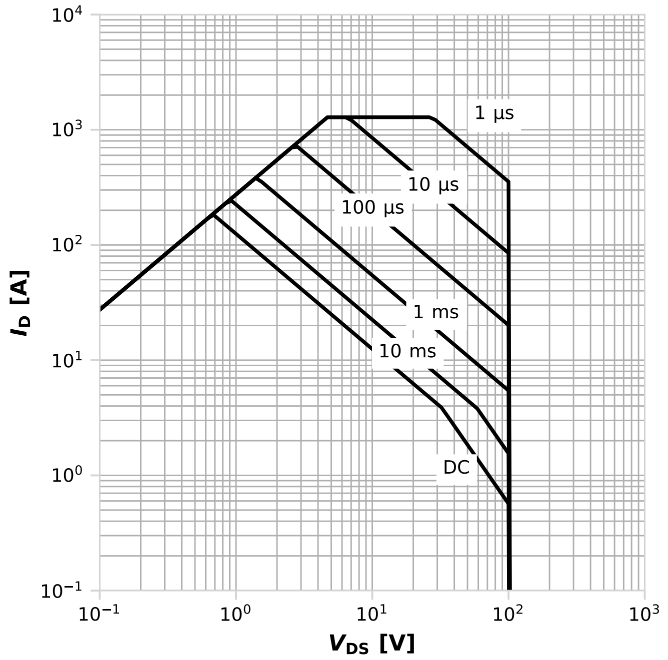
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



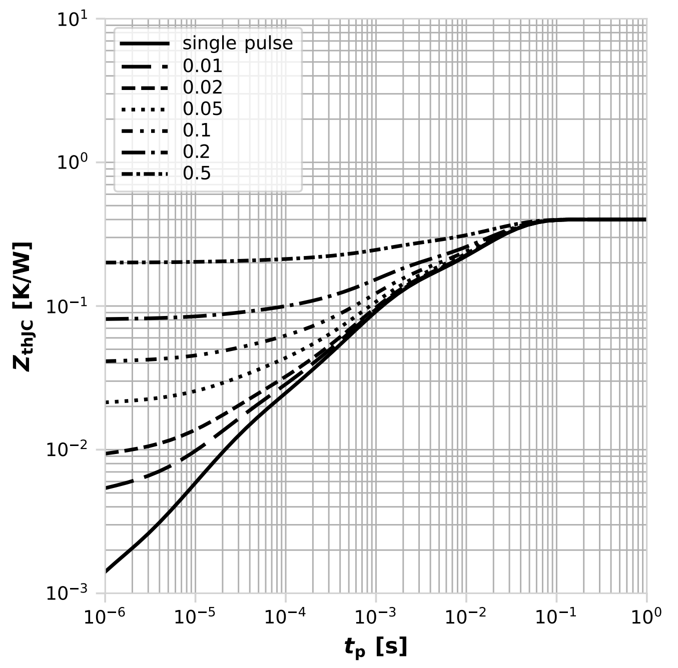
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Safe operating area



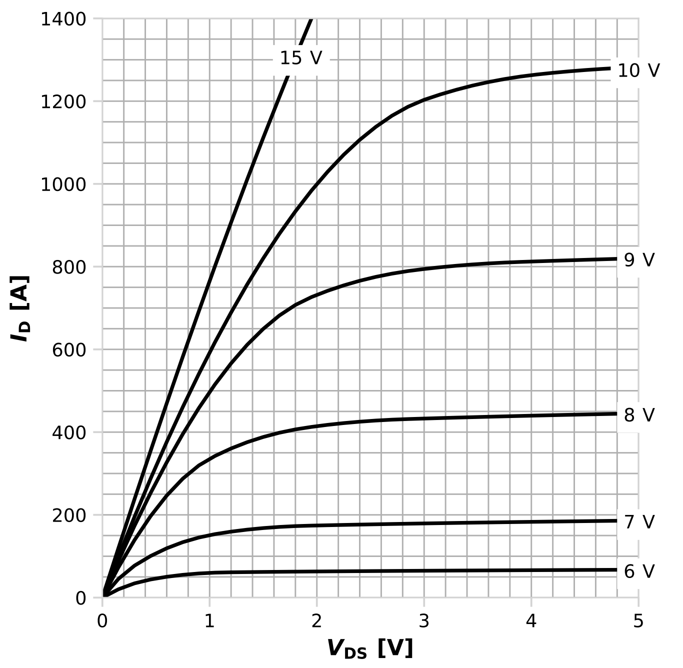
I_D=f(V_{DS}); T_C=125 °C; D=0; parameter: t_p

Diagram 5: Max. transient thermal impedance



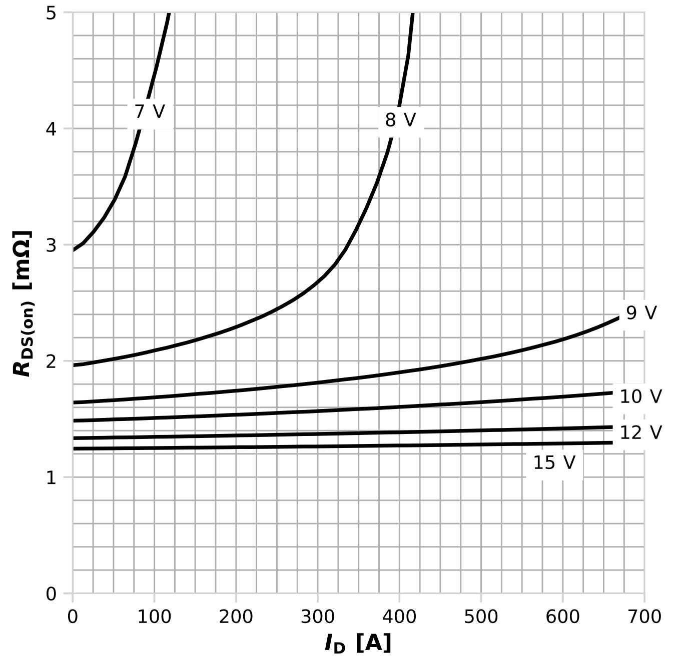
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 6: Typ. output characteristics



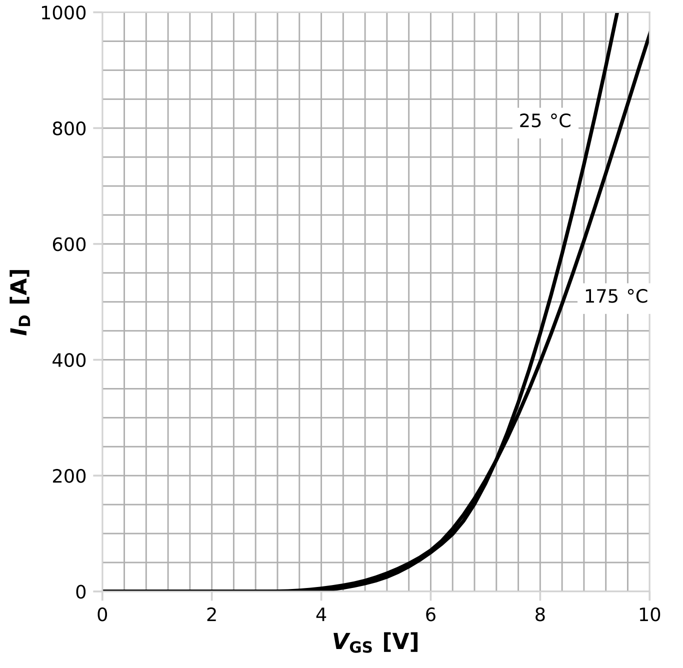
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on resistance



$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 8: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

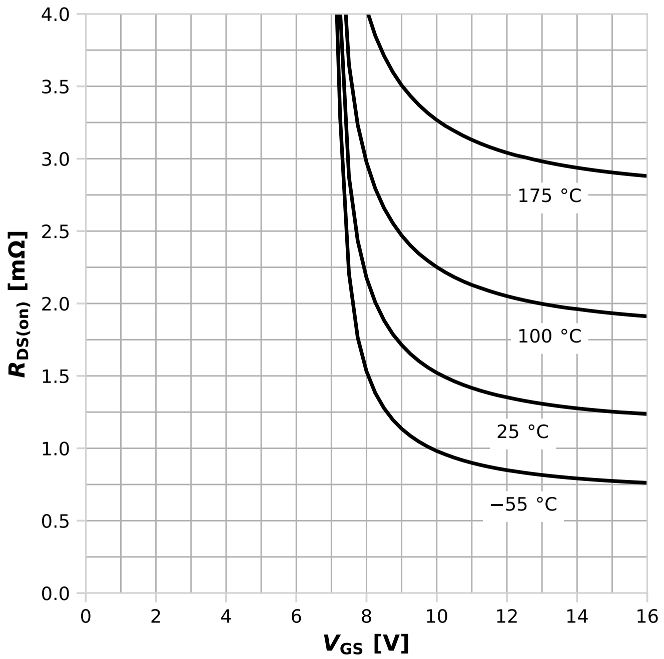
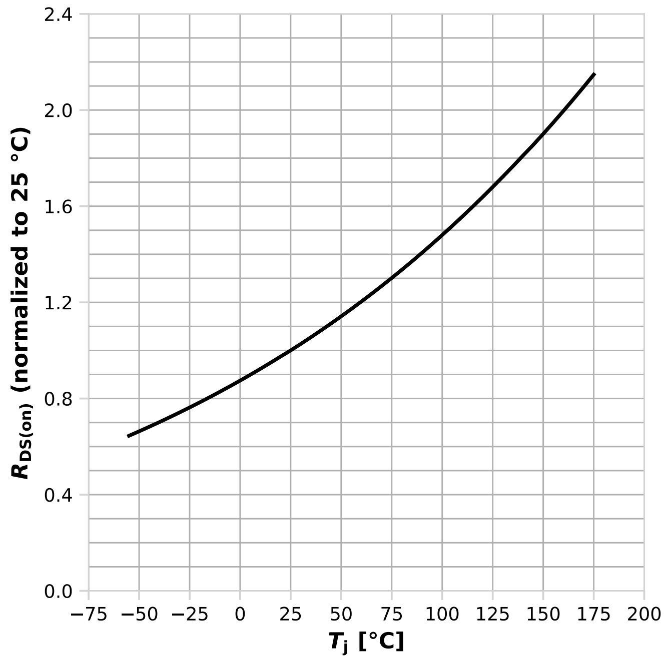
Diagram 9: Typ. drain-source on resistance	Diagram 10: Normalized drain-source on resistance
	
$R_{DS(on)}$=f(V_{GS}), I_D=150 A; parameter: T_j	$R_{DS(on)}$=f(T_j), I_D=150 A, V_{GS}=10 V

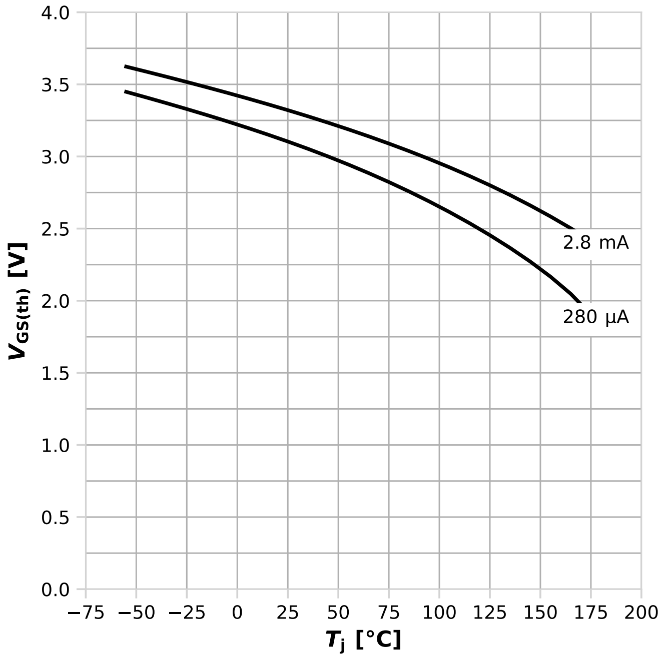
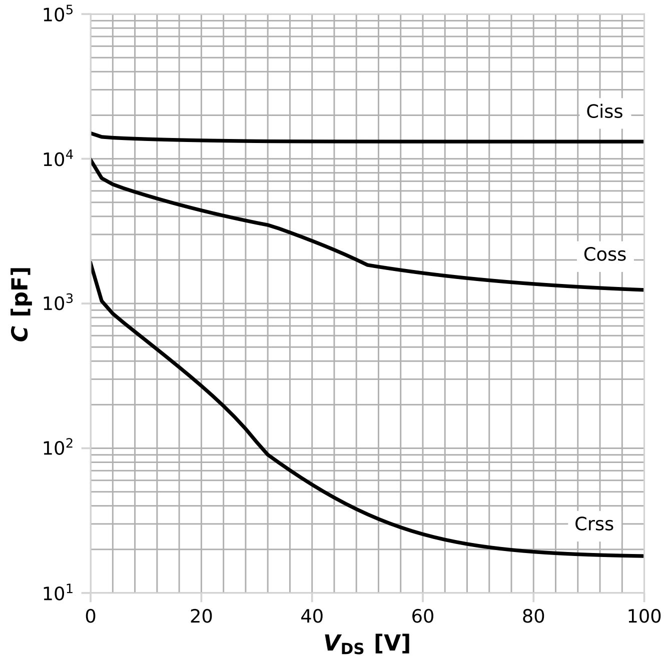
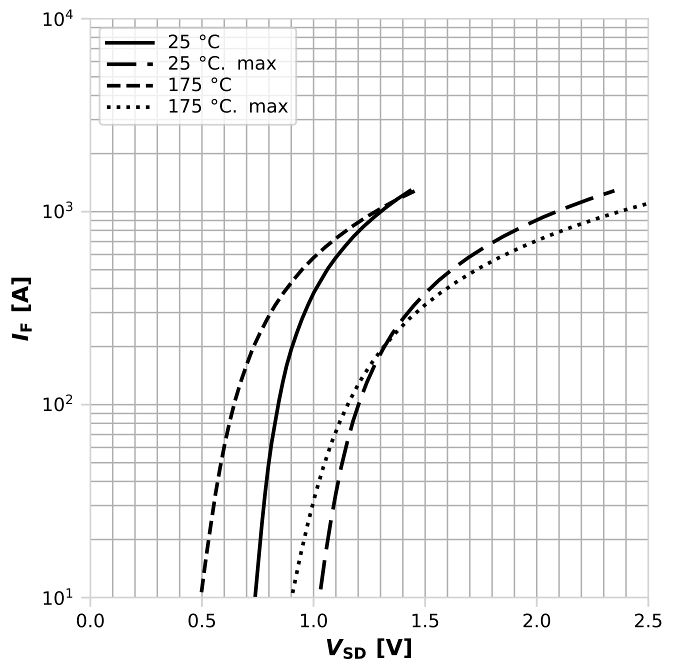
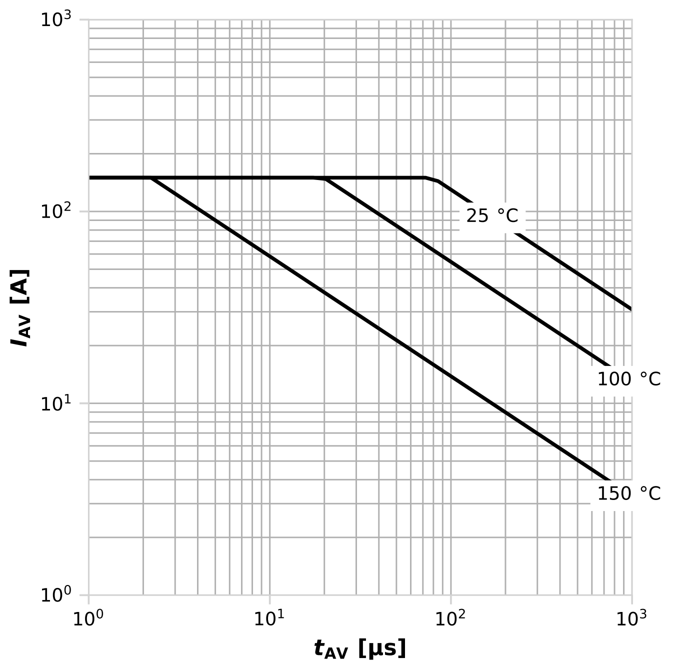
Diagram 11: Typ. gate threshold voltage	Diagram 12: Typ. capacitances
	
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D	C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 13: Forward characteristics of reverse diode



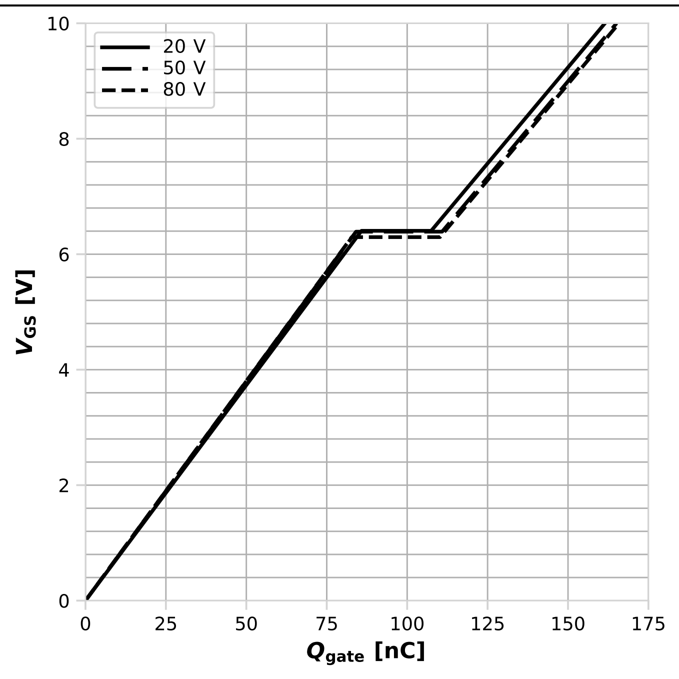
I_F=f(V_{SD}); parameter: T_j

Diagram 14: Avalanche characteristics



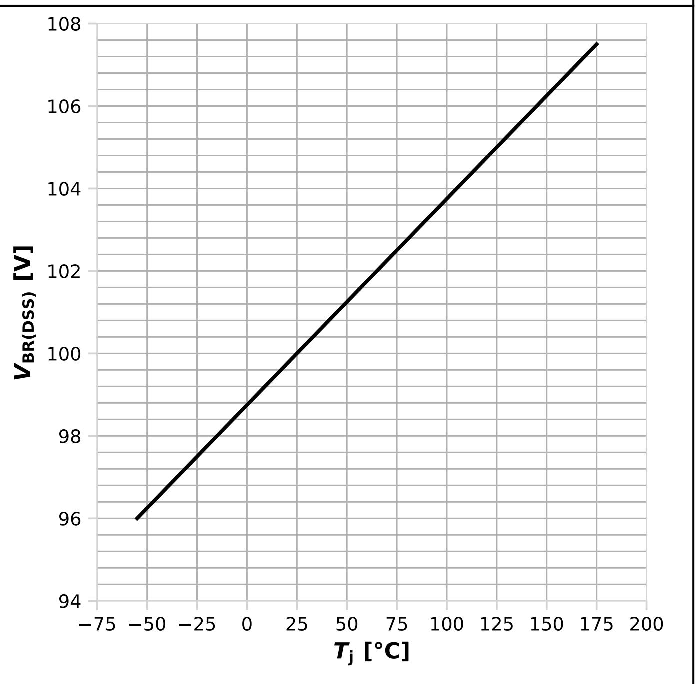
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge

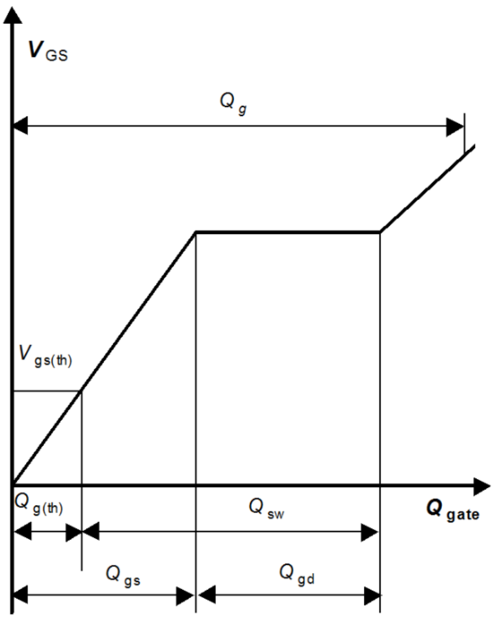


V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 16: Min. drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms

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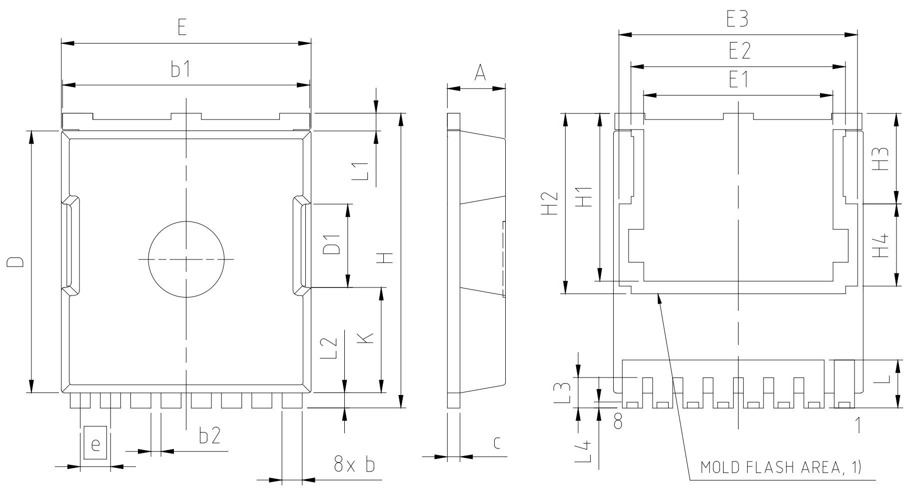
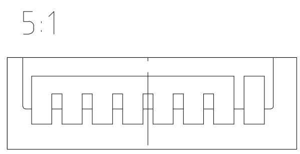
5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K	4.18	
L	1.60	2.10
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	0.13	0.33



OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

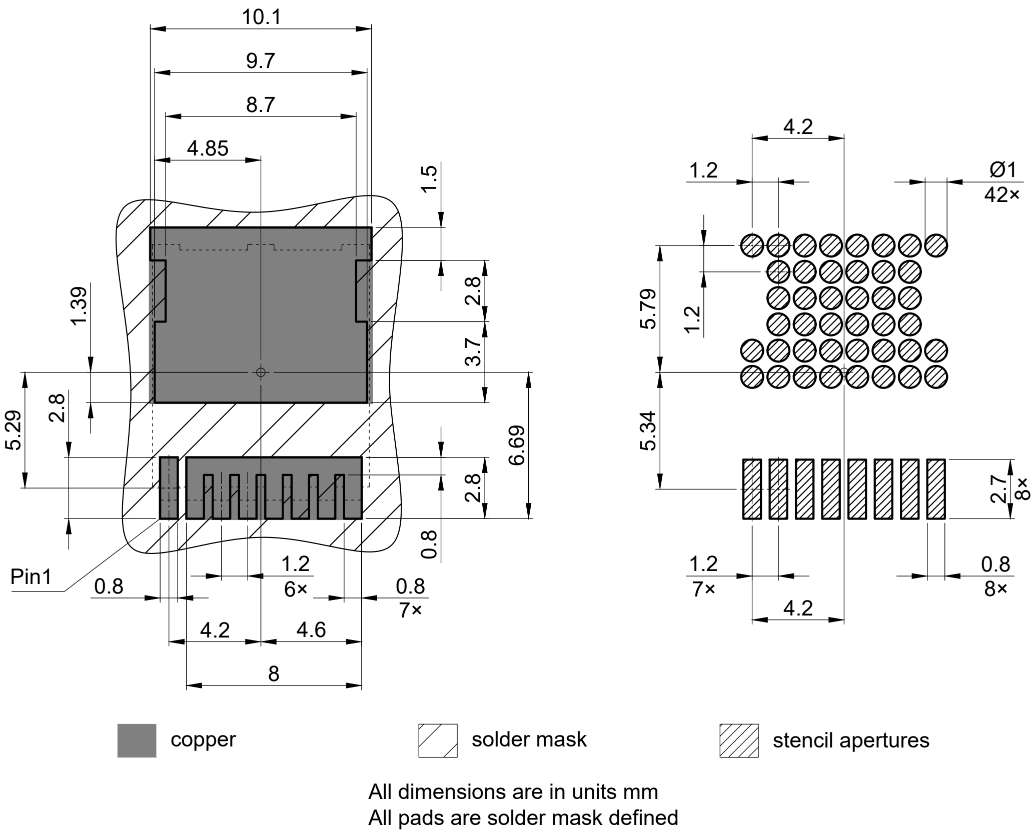


Figure 2 Footprint Drawing PG-HSOF-8, dimensions in mm

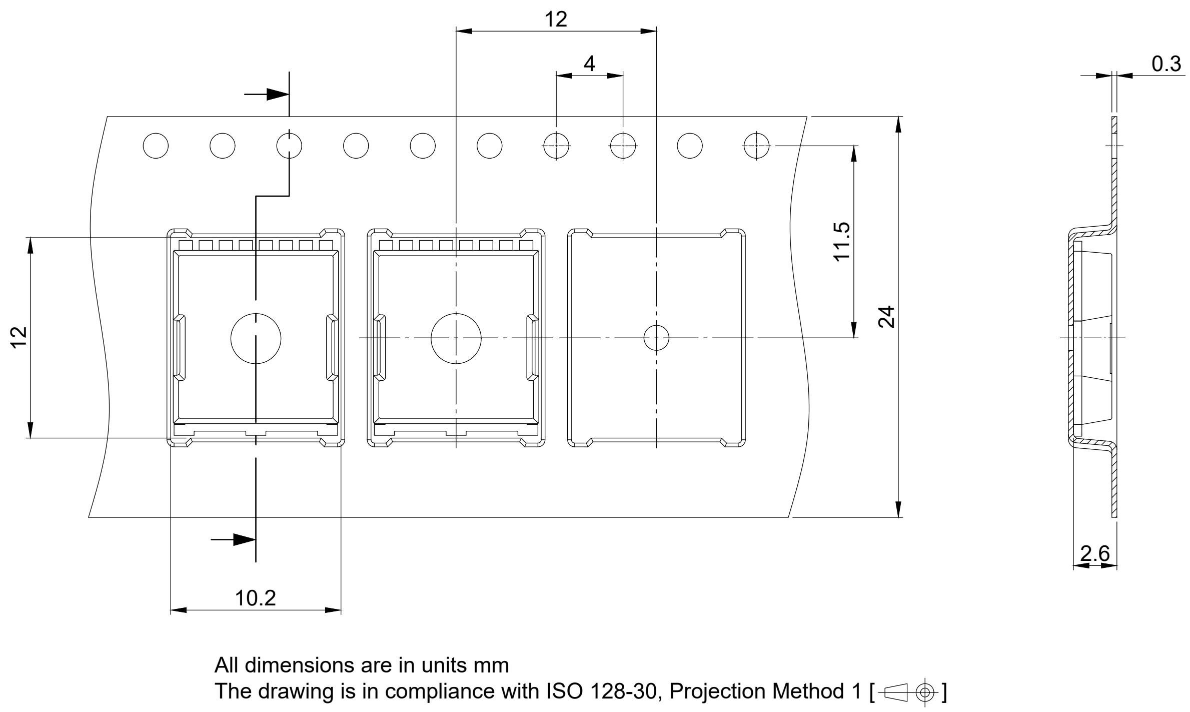


Figure 3 Packaging Variant PG-HSOF-8, dimensions in mm

Revision History

IPT017N10NM5LF2

Revision 2024-08-22, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-08-22	Release of final datasheet

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