

MOSFET

600V CoolMOS™ CM8 Power Transistor

Built on Infineon's world-class super-junction MOSFET platform with an integrated fast body diode, making it suitable for a wide range of applications. It enables highest power density at lowest possible system cost with superior reliability. It is enhancing Infineon's WBG offering and the successor of the 600 V CoolMOS™ 7 MOSFET family.

Features

- Best-In-Class SJ Mosfet Performance
- Address broad hard and soft switching applications with outstanding commutation ruggedness
- Integrated fast body diode and ESD protection
- .XT interconnection technology for best-in-class thermal performance

Benefits

- Provides the best price performance ratio with Best-In-Class SJ Mosfet Performance
- Ease of use and shorter design in cycle
- Enable multiple topologies
- 14-42% lower R_{th} for improved thermal performance

Potential applications

- Datacenter, AI server, Telecom Power Supply
- Micro and Residential Hybrid Inverter
- Portable and Residential Energy Storage, UPS
- EV Charging, Light electric vehicles, Electric Forklift
- High Voltage Solid State Power Distribution
- Home & Professional Tools
- Charger, Adapters, TV and Console SMPS

Product validation

Qualified according to relevant JEDEC tests.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	24	mΩ
$Q_{g,typ}$	122	nC
$I_{D,pulse}$	359	A
$E_{oss} @ 400 V$	16.4	μJ
Body diode di_F/dt	1300	A/μs
ESD class (HBM)	2	

Part number	Package	Marking	Related links
IPLT60R024CM8	PG-HDSOP-16	60R024C8	see Appendix A

TOLT

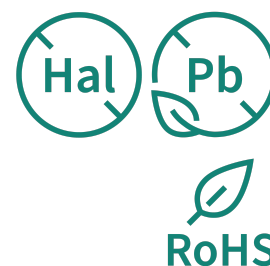
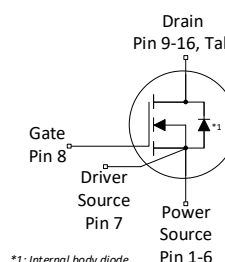
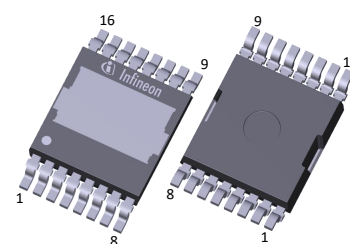




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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	103	A	$T_C = 25^\circ\text{C}$
Continuous drain current	I_D	-	-	64	A	$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	359	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	211	mJ	$I_D = 6.0\text{ A}$; $V_{DD} = 50\text{ V}$; see table 10
Avalanche energy, repetitive	E_{AR}			1.06		
Avalanche current, single pulse	I_{AS}	-	-	6.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS} = 0...400\text{ V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	543	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j					
Extended operating junction temperature	T_j	150	-	175	$^\circ\text{C}$	$\leq 50\text{ h}$ in the application lifetime
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	103	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$			359		
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS} = 0...400\text{ V}$, $I_{SD} \leq 103\text{ A}$, $T_j = 25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di_F/dt			1300	A/ μs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C = 25^\circ\text{C}$, $t = 1\text{ min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.23	K/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	K/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	45	55	K/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm ² (one layer, 70 μm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$
Gate threshold voltage	$V_{(GS)th}$	3.7	4.2	4.7	V	$V_{DS} = V_{GS}$, $I_D = 1.06\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1.5	μA	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$
			151	-		$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	0.1	μA	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.020	0.024	Ω	$V_{GS} = 10\text{ V}$, $I_D = 41.7\text{ A}$, $T_j = 25^\circ\text{C}$
			0.044	-		$V_{GS} = 10\text{ V}$, $I_D = 41.7\text{ A}$, $T_j = 150^\circ\text{C}$
Gate resistance	R_G	-	1.1	-	Ω	$f = 1\text{ MHz}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5382	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$
Output capacitance	C_{oss}		66			
Effective output capacitance, energy related ⁴⁾	$C_{o(er)}$	-	205	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\ldots 400\text{ V}$
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$	-	2128	-	pF	$I_D = \text{constant}$, $V_{GS} = 0\text{ V}$, $V_{DS} = 0\ldots 400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 13\text{ V}$, $I_D = 21.1\text{ A}$, $R_G = 3.3\text{ }\Omega$; see table 9
Rise time	t_r		7			
Turn-off delay time	$t_{d(off)}$		111			
Fall time	t_f		5			

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	32	-	nC	$V_{DD} = 400\text{ V}$, $I_D = 21.1\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}		43		nC	
Gate charge total	Q_g		122		nC	
Gate plateau voltage	$V_{plateau}$		5.9		V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS} = 0\text{ V}$, $I_F = 21.1\text{ A}$, $T_j = 25^\circ\text{C}$
Reverse recovery time	t_{rr}	-	150	187	ns	$V_R = 400\text{ V}$, $I_F = 21.1\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$; see table 8
Reverse recovery charge	Q_{rr}		1.11	1.66	μC	
Peak reverse recovery current	I_{rrm}		16.1	-	A	

4 Electrical characteristics diagrams

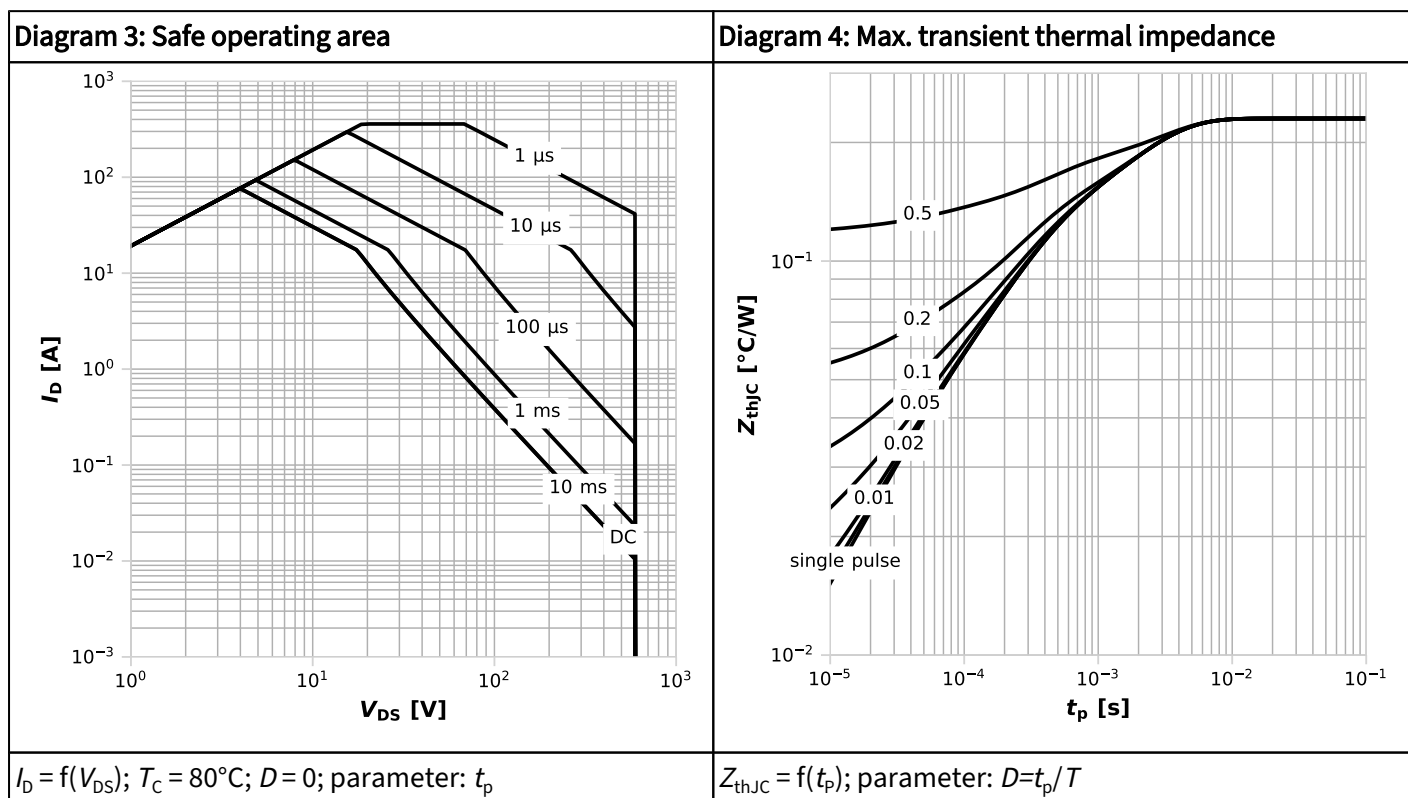
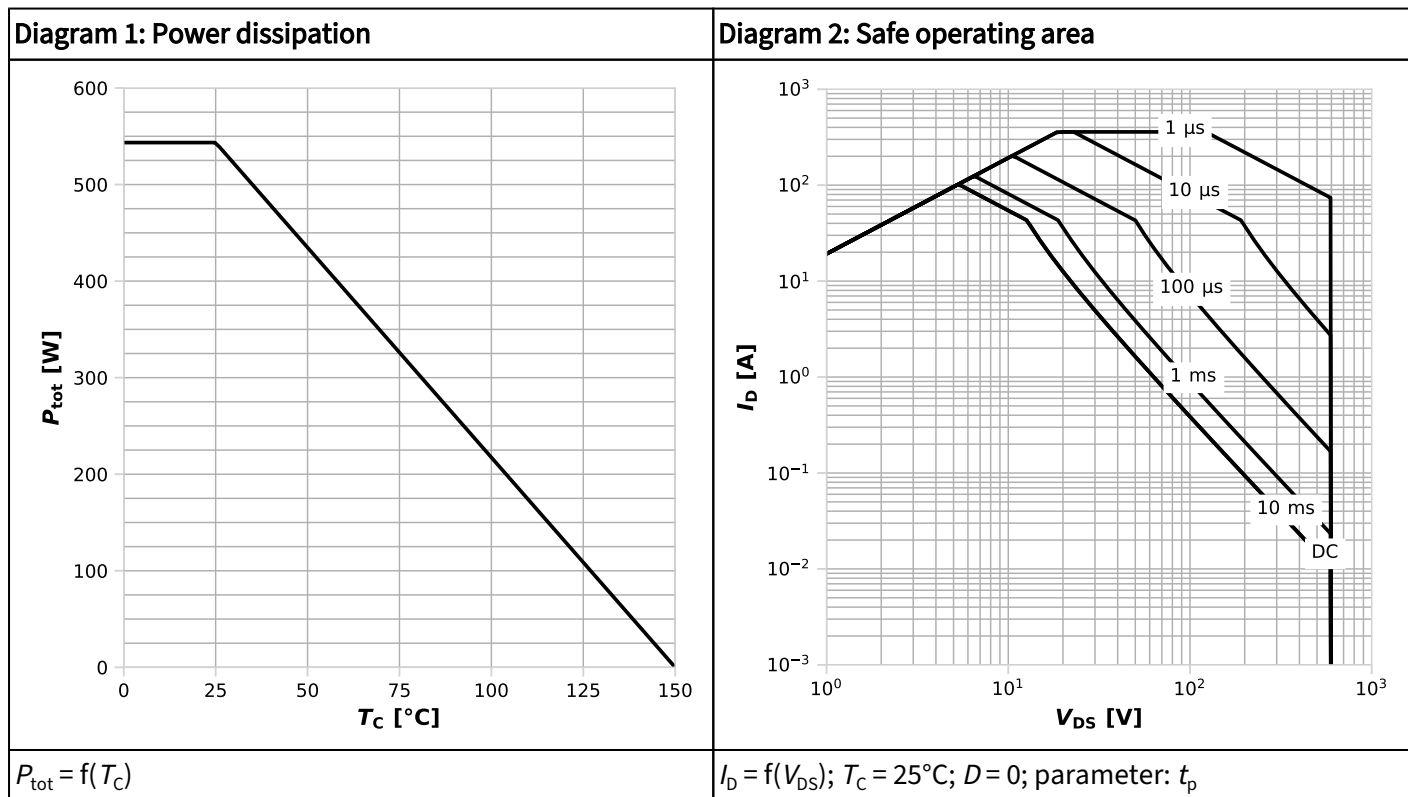
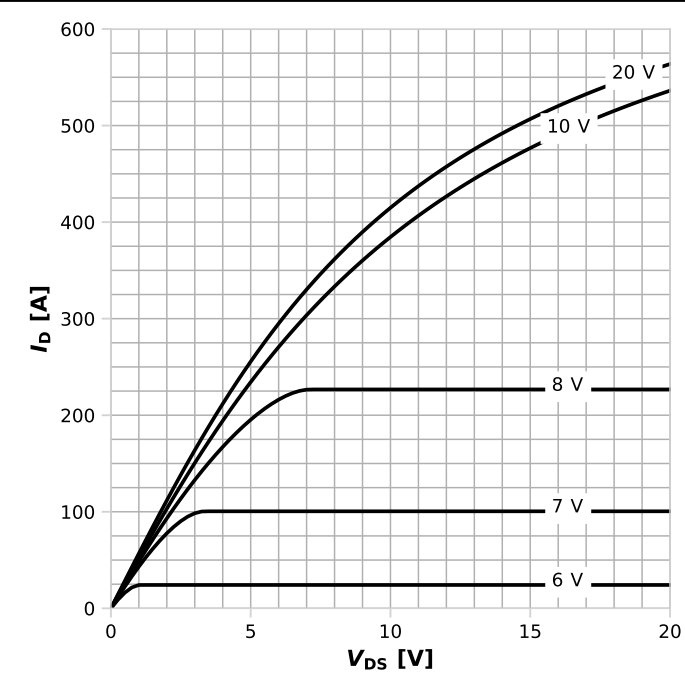
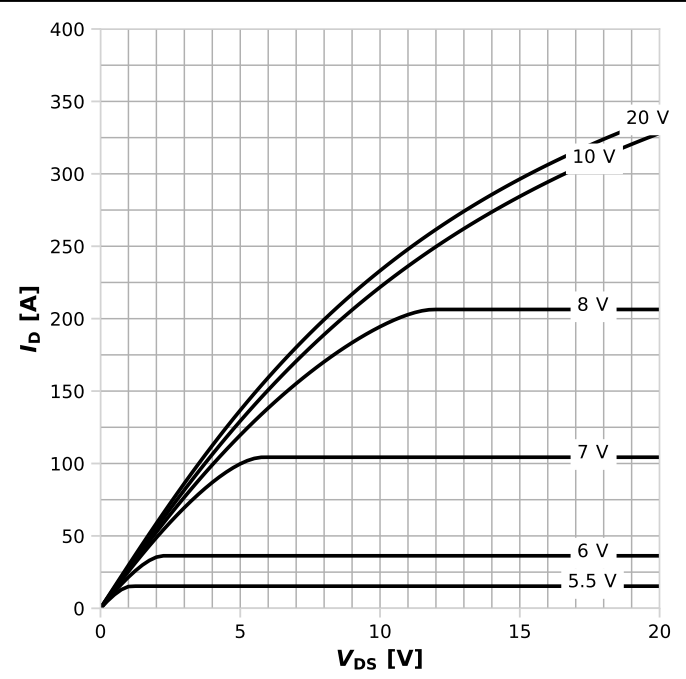


Diagram 5: Typ. output characteristics



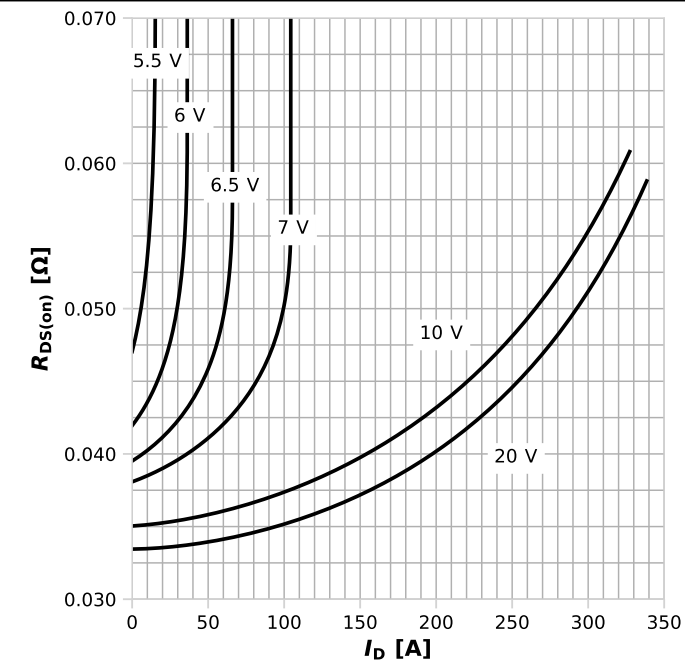
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



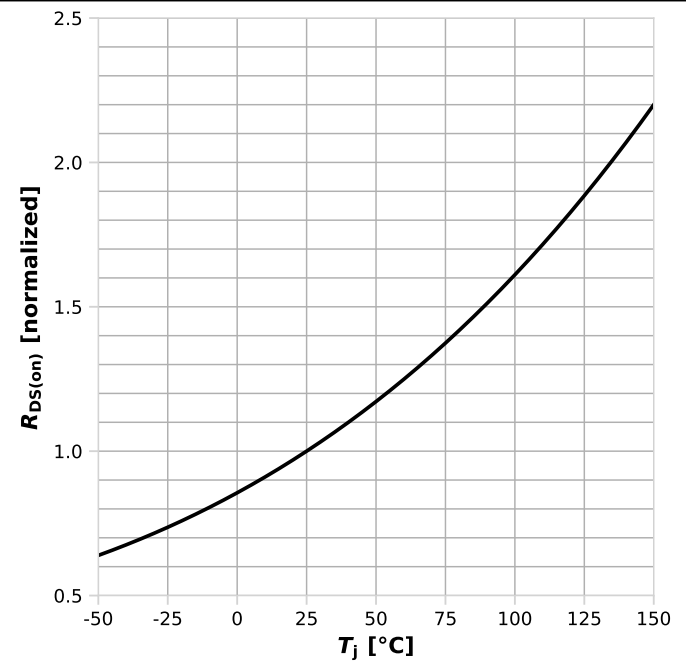
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



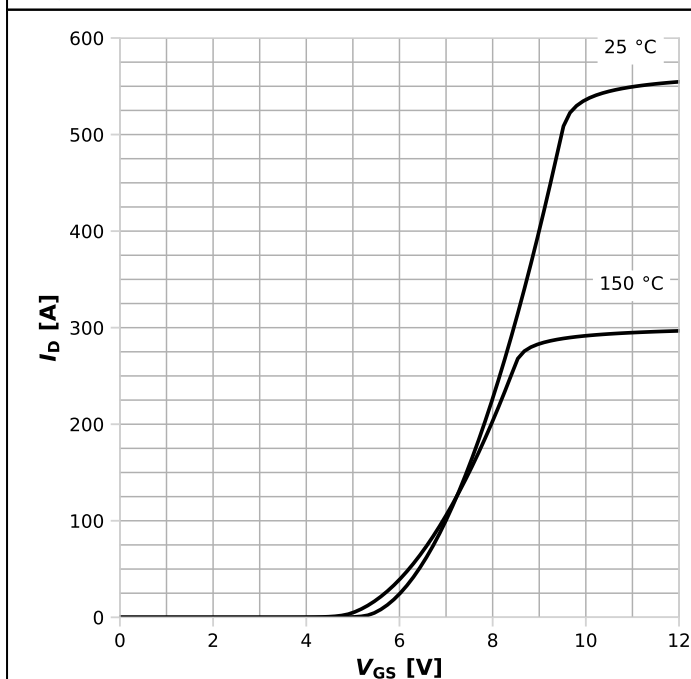
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



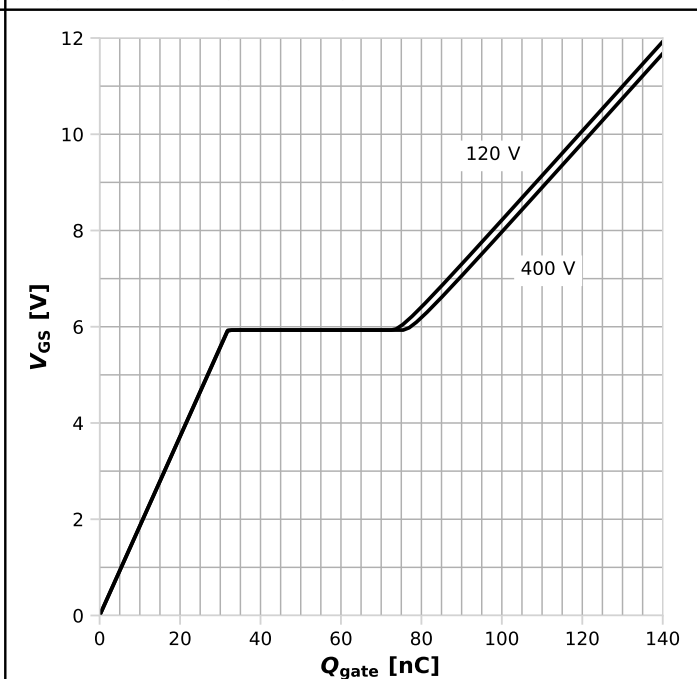
$R_{DS(on)} = f(T_j)$; $I_D = 41.7$ A; $V_{GS} = 10$ V

Diagram 9: Typ. transfer characteristics



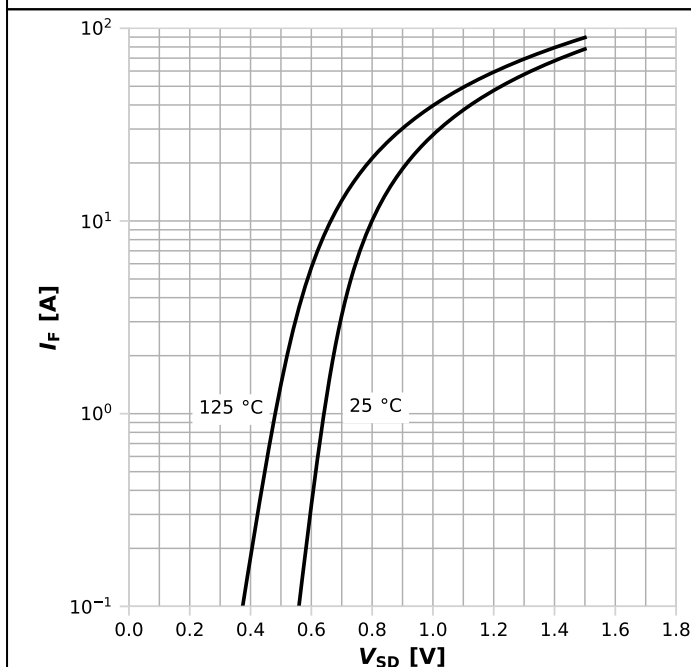
$I_D = f(V_{GS}); V_{DS} = 20 \text{ V}; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



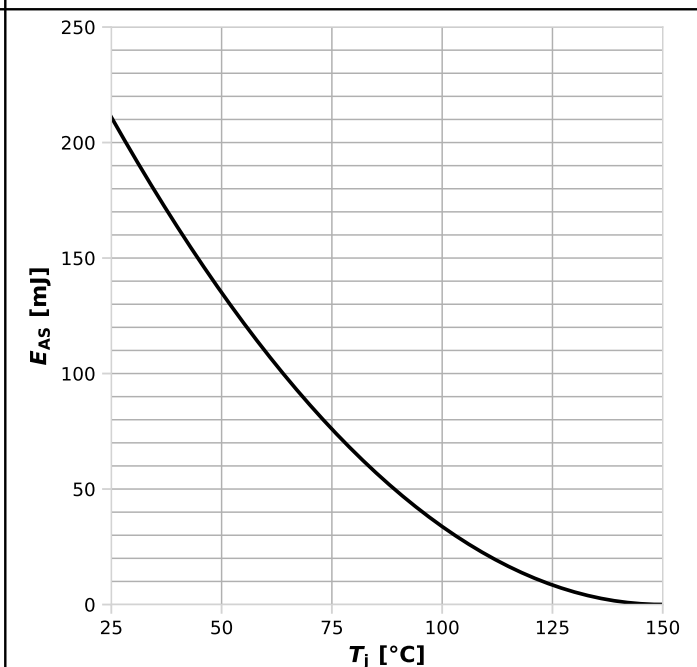
$V_{GS} = f(Q_{gate}); I_D = 21.1 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



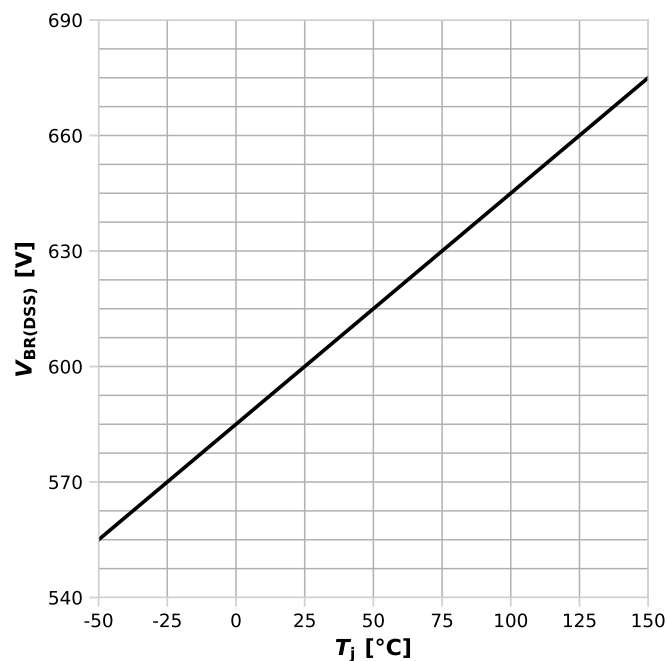
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



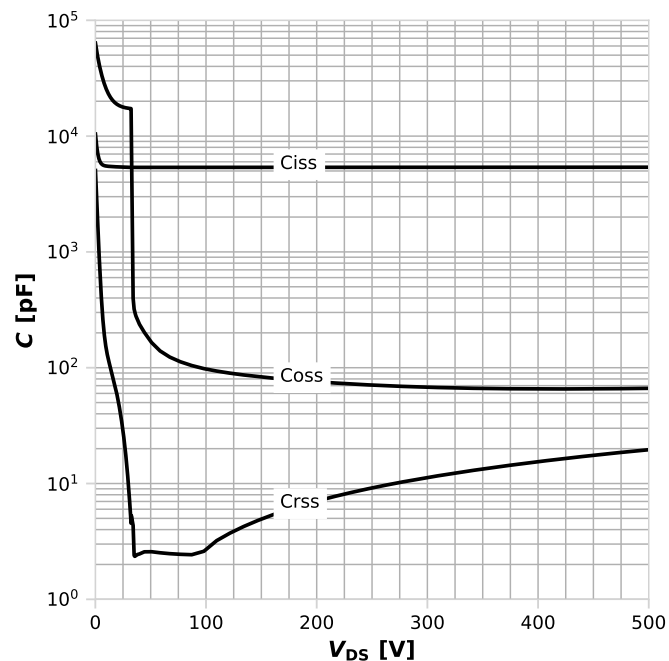
$E_{AS} = f(T_j); I_D = 6.0 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



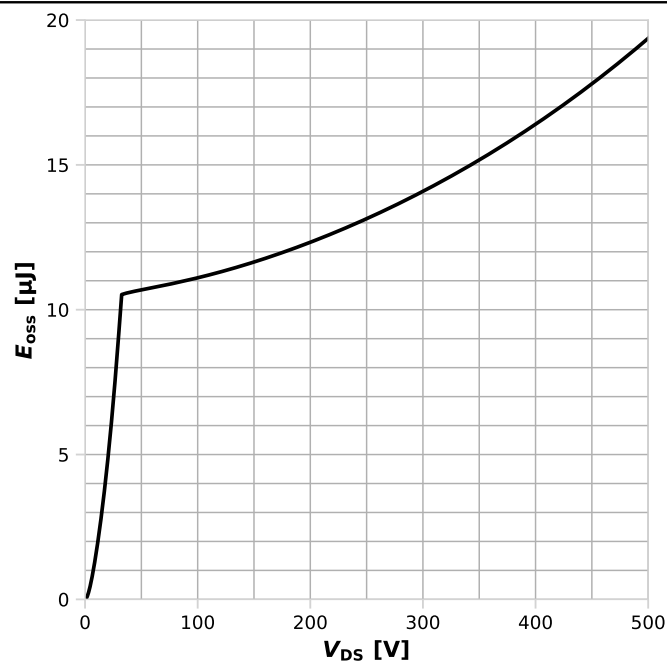
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

5 Test circuits

Table 8 Diode characteristics

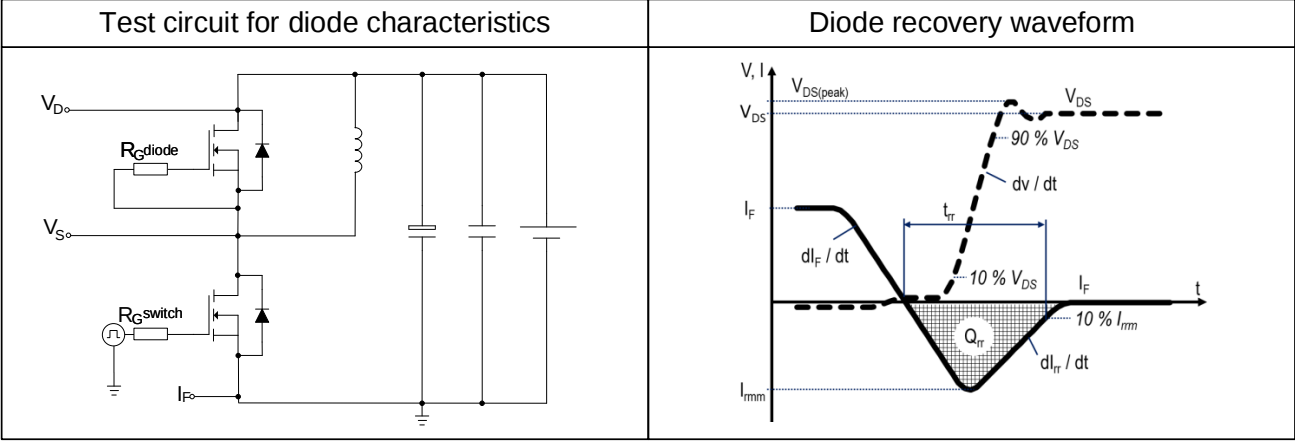


Table 9 Switching times (ss)

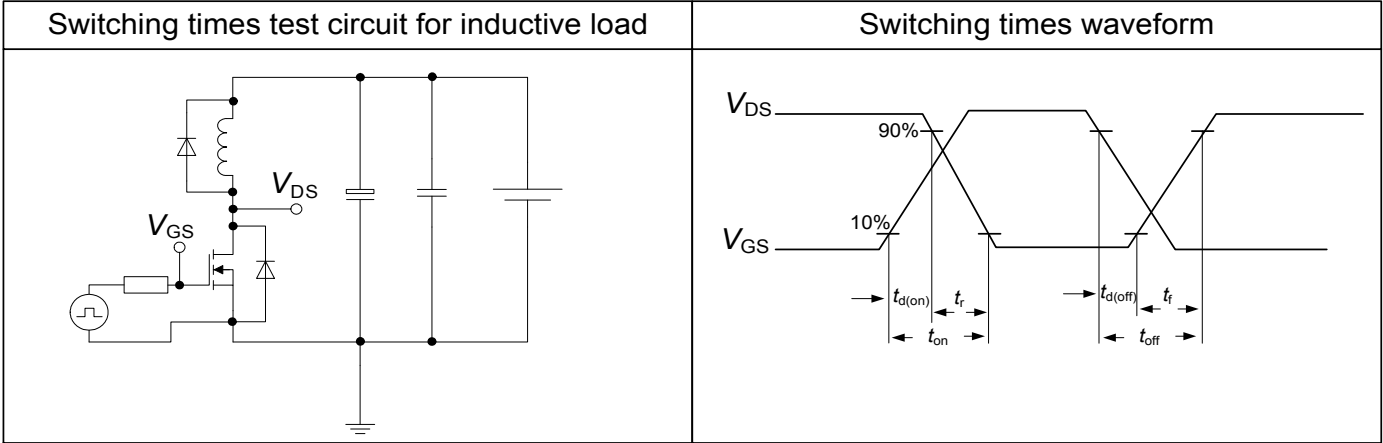
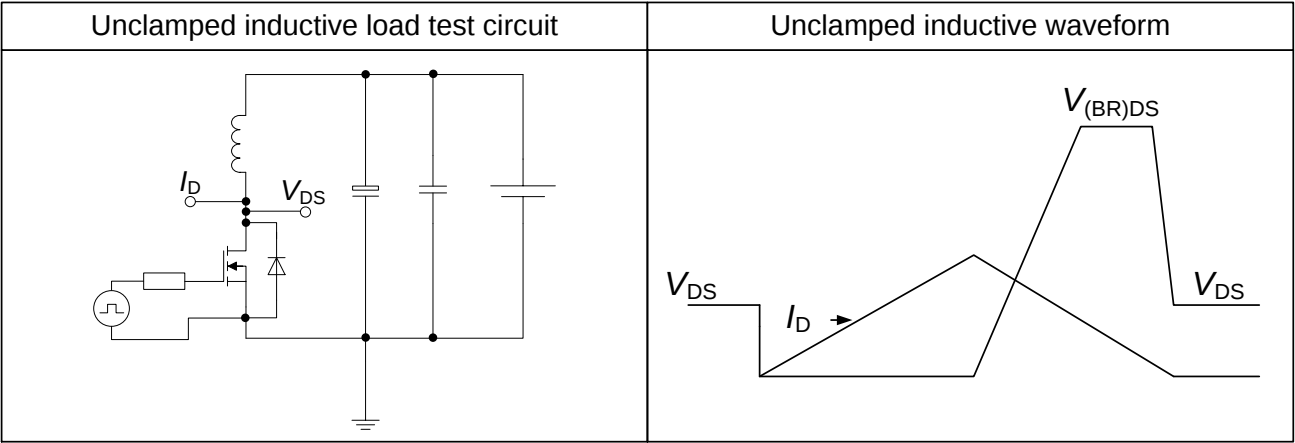


Table 10 Unclamped inductive load (ss)



6 Package outlines

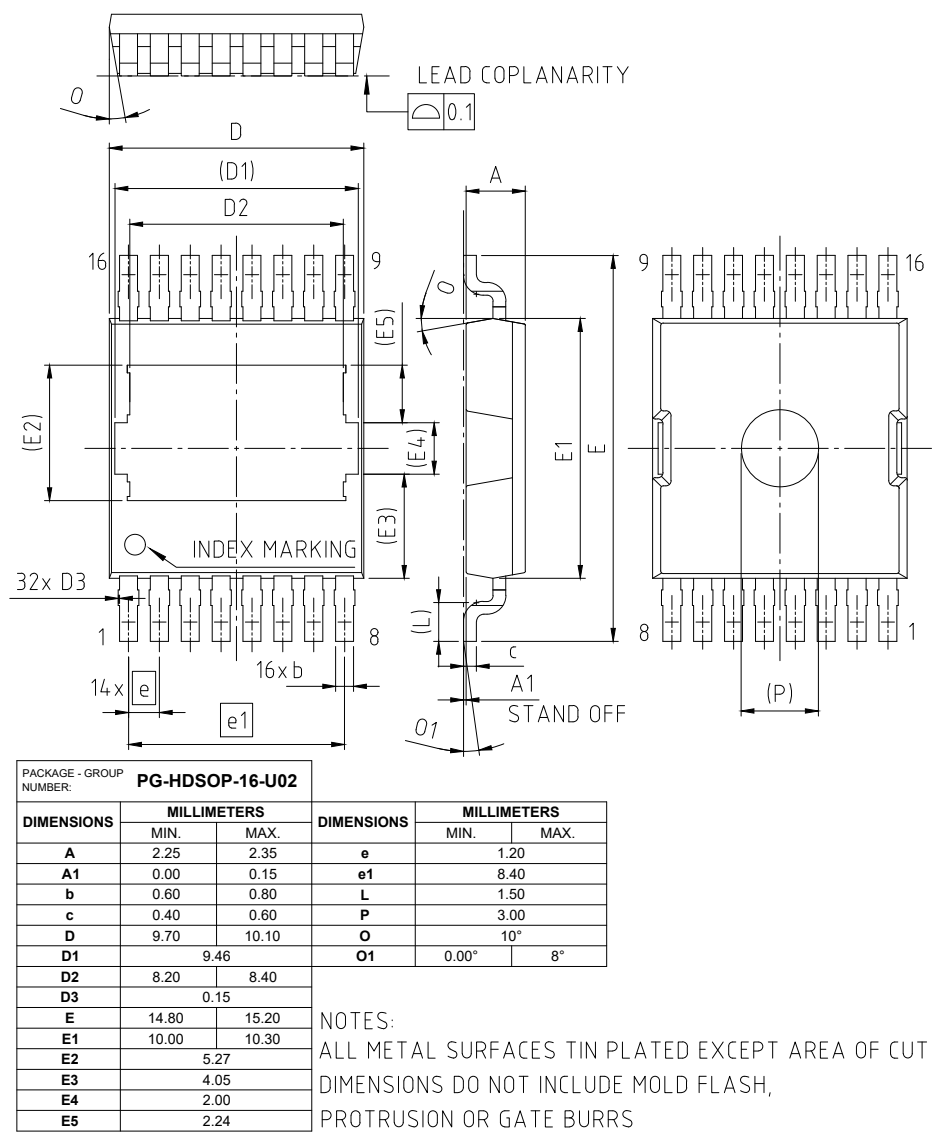


Figure 1 Outline PG-HDSOP-16, dimensions in mm

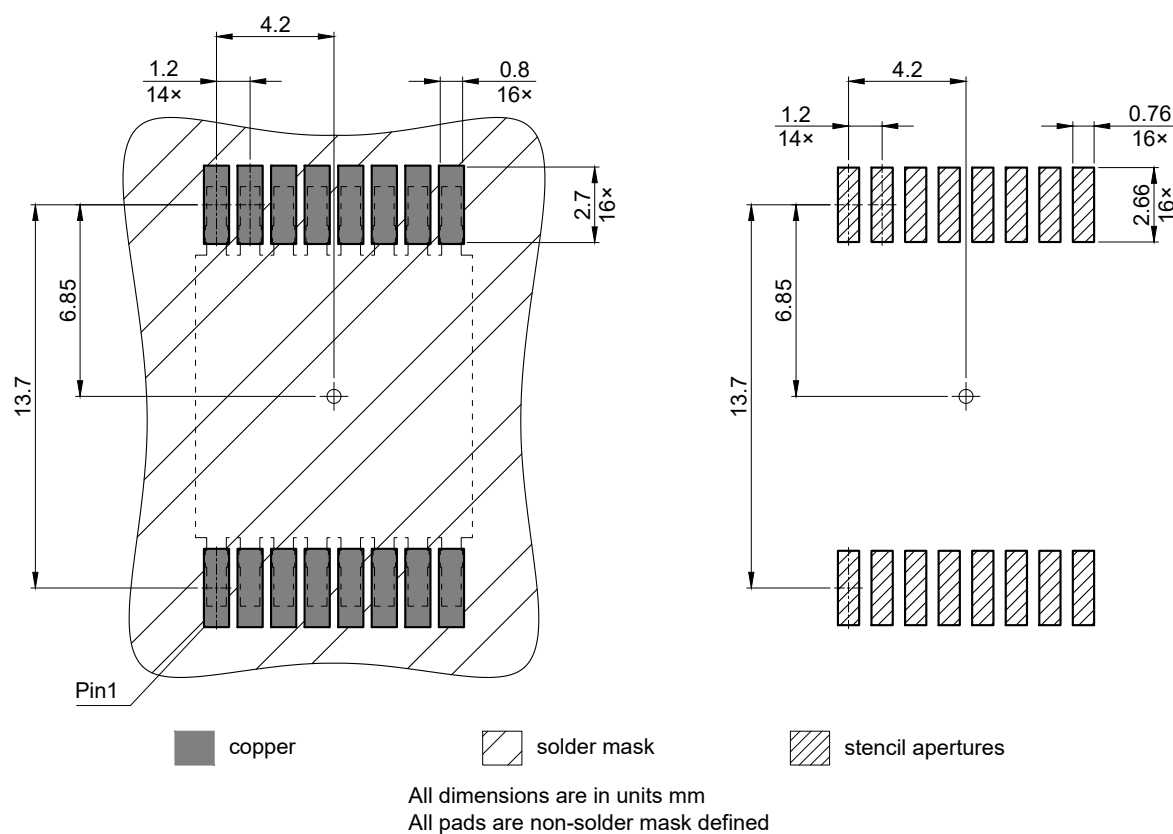
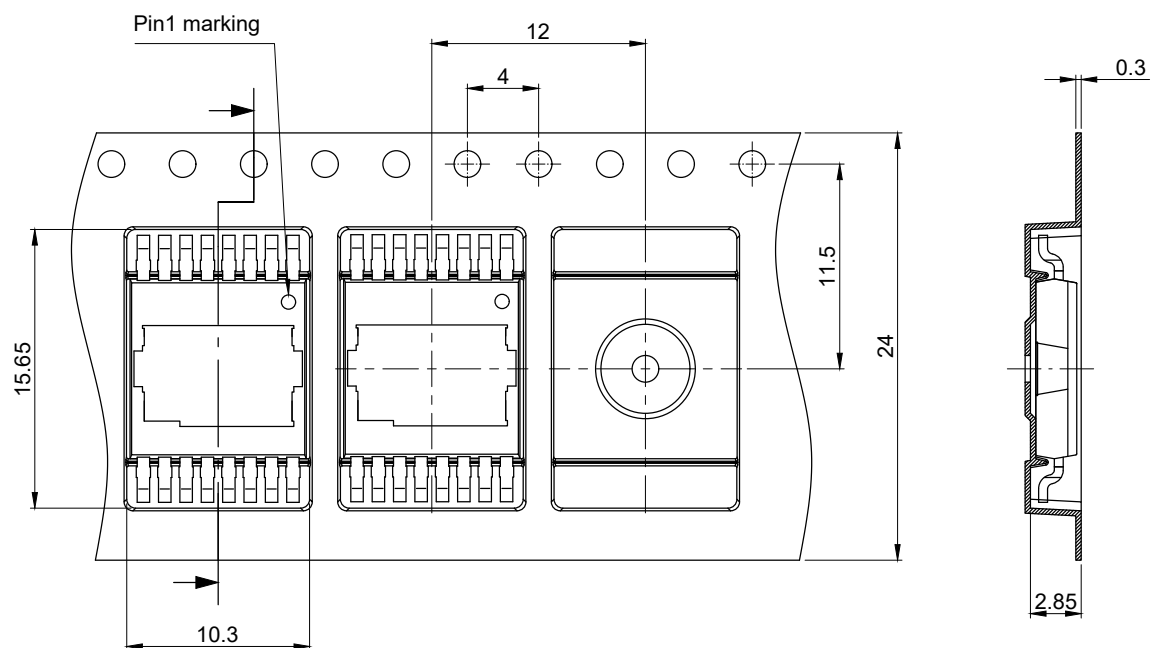


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

7 Appendix A

Table 11 **Related links**

- [IFX CoolMOS CM8 Webpage](#)
- [IFX CoolMOS CM8 application note](#)
- [IFX CoolMOS CM8 simulation model](#)
- [IFX Design tools](#)

Revision history

IPLT60R024CM8

Revision 2025-11-18, Rev. 2.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2025-11-18	Release of final version

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