

SiC MOSFET

CoolSiC™ MOSFET 650 V G2

Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

Features

- Ultra-low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5\text{ V}$
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance

Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|-----------------------------------|-------|------|
| V_{DSS} over full $T_{j,range}$ | 650 | V |
| $R_{DS(on),typ}$ | 20 | mΩ |
| $R_{DS(on),max}$ | 24 | mΩ |
| $Q_{G,typ}$ | 57 | nC |
| $I_{D,pulse}$ | 293 | A |
| Q_{oss} @ 400 V | 108 | nC |
| E_{oss} @ 400 V | 14.7 | μJ |

| Type/Ordering Code | Package | Marking | Related Links |
|--------------------|-------------|----------|----------------|
| IMLT65R020M2H | PG-HDSOP-16 | 65R020M2 | see Appendix A |

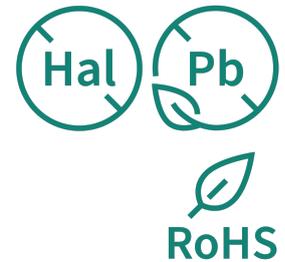
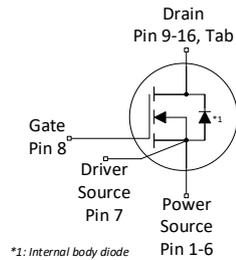
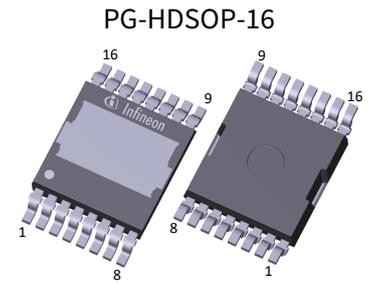




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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------------------------|------------------|--------|------|-----------|------|-------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Continuous DC drain current ¹⁾ | I_{DDC} | - | - | 107 75 | A | $T_c = 25\text{ °C}$ $T_c = 100\text{ °C}$ |
| Peak drain current ²⁾ | I_{DM} | - | - | 293 | A | $T_c = 25\text{ °C}$, $V_{\text{GS}} = 18\text{ V}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 272 | mJ | $I_{\text{D}} = 10.2\text{ A}$, $V_{\text{DD}} = 50\text{ V}$; see table 11 |
| Avalanche energy, repetitive | E_{AR} | - | - | 1.36 | mJ | $I_{\text{D}} = 10.2\text{ A}$, $V_{\text{DD}} = 50\text{ V}$; see table 11 |
| Avalanche current, single pulse | I_{AS} | - | - | 10.2 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 200 | V/ns | $V_{\text{DS}} = 0 \dots 400\text{ V}$ |
| Gate source voltage (static) ³⁾ | V_{GS} | -7 | - | 23 | V | - |
| Gate source voltage (transient) | V_{GS} | -10 | - | 25 | V | $t_p \leq 500\text{ ns}$, duty cycle $\leq 1\%$ |
| Power dissipation | P_{tot} | - | - | 454 | W | $T_c = 25\text{ °C}$ |
| Storage temperature | T_{stg} | -55 | - | 150 | °C | - |
| Operating junction temperature | T_j | -55 | - | 175 | °C | - |
| Mounting torque | - | - | - | - | Ncm | - |
| Continuous reverse drain current ¹⁾ | I_{SDC} | - | - | 107 70 | A | $V_{\text{GS}} = 18\text{ V}$, $T_c = 25\text{ °C}$ $V_{\text{GS}} = 0\text{ V}$, $T_c = 25\text{ °C}$ |
| Peak reverse drain current ²⁾ | I_{SM} | - | - | 293 88 | A | $T_c = 25\text{ °C}$, $t_p \leq 250\text{ ns}$ $T_c = 25\text{ °C}$ |
| Insulation withstand voltage | V_{ISO} | - | - | n.a. | V | V_{rms} , $T_c = 25\text{ °C}$, $t = 1\text{ min}$ |

1) Limited by $T_{j,\text{max}}$.

2) Pulse width t_{pulse} limited by $T_{j,\text{max}}$.

3) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|-------------------------------------------------|---------------|--------|------|------|------|----------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{th(j-c)}$ | - | - | 0.33 | °C/W | Not subject to production test. Parameter verified by design/characterization according to JESD51-14. |
| Soldering temperature, reflow soldering allowed | T_{sold} | - | - | 260 | °C | reflow MSL1 |

3 Operating range

Table 4 Operating range

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------|---------------|--------|------|------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Recommended turn-on voltage | $V_{GS(on)}$ | - | 18 | - | V | - |
| Recommended turn-off voltage | $V_{GS(off)}$ | - | 0 | - | V | - |

4 Electrical characteristics

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--------------------------------------|--------------|--------|----------------------|------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Drain-source voltage | V_{DSS} | 650 | - | - | V | $V_{GS} = 0\text{ V}$, $I_D = 0.95\text{ mA}$ |
| Gate threshold voltage ⁴⁾ | $V_{GS(th)}$ | 3.5 | 4.5 | 5.6 | V | $V_{DS} = V_{GS}$, $I_D = 9.5\text{ mA}$ |
| Zero gate voltage drain current | I_{DSS} | - | 1 3 | 75 - | μA | $V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25\text{ °C}$ $V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 175\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 26 20 18 33 | - - - - | m Ω | $V_{GS} = 15\text{ V}$, $I_D = 46.9\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$, $I_D = 46.9\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 20\text{ V}$, $I_D = 46.9\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$, $I_D = 46.9\text{ A}$, $T_j = 175\text{ °C}$ |
| Internal gate resistance | $R_{G,int}$ | - | 2.5 | - | Ω | $f = 1\text{ MHz}$ |

⁴⁾ Tested after 1 ms pulse at $V_{GS} = +20\text{ V}$. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------------------------------------|-------------|--------|------|------|------|-----------------------------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 2038 | - | pF | $V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$ |
| Reverse transfer capacitance | C_{rss} | - | 11.5 | - | pF | $V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$ |
| Output capacitance ⁵⁾ | C_{oss} | - | 151 | 197 | pF | $V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$ |
| Output charge ⁵⁾ | Q_{oss} | - | 108 | 141 | nC | calculation based on C_{oss} |
| Effective output capacitance, energy related ⁶⁾ | $C_{o(er)}$ | - | 183 | - | pF | $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{...}400\text{ V}$ |
| Effective output capacitance, time related ⁷⁾ | $C_{o(tr)}$ | - | 271 | - | pF | $I_D = \text{constant}$, $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{...}400\text{ V}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 10.3 | - | ns | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\text{ }\Omega$; see table 10 |
| Rise time | t_r | - | 12.0 | - | ns | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\text{ }\Omega$; see table 10 |

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|-----------------------------------------|--------------|--------|------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Turn-off delay time | $t_{d(off)}$ | - | 19 | - | ns | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$; see table 10 |
| Fall time | t_f | - | 5.6 | - | ns | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$; see table 10 |
| Turn-ON switching losses ⁸⁾ | E_{on} | - | 59 | - | μJ | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$ |
| Turn-OFF switching losses ⁸⁾ | E_{off} | - | 64 | - | μJ | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$ |
| Total switching losses ⁸⁾ | E_{tot} | - | 123 | - | μJ | $V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 46.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$ |

⁵⁾ Maximum specification is defined by calculated six sigma upper confidence bound

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

⁷⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

⁸⁾ Values for 4-pin configuration based on TO-263-7 measurements; MOSFET used in half-bridge configuration without external diode

Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|-------------------------------|--------------|--------|------|------|------|-----------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Plateau gate to source charge | $Q_{GS(pl)}$ | - | 15 | - | nC | $V_{DD} = 400\text{ V}$, $I_D = 46.9\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$ |
| Gate to drain charge | Q_{GD} | - | 10.7 | - | nC | $V_{DD} = 400\text{ V}$, $I_D = 46.9\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$ |
| Total gate charge | Q_G | - | 57 | - | nC | $V_{DD} = 400\text{ V}$, $I_D = 46.9\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$ |

Table 8 Reverse diode characteristics

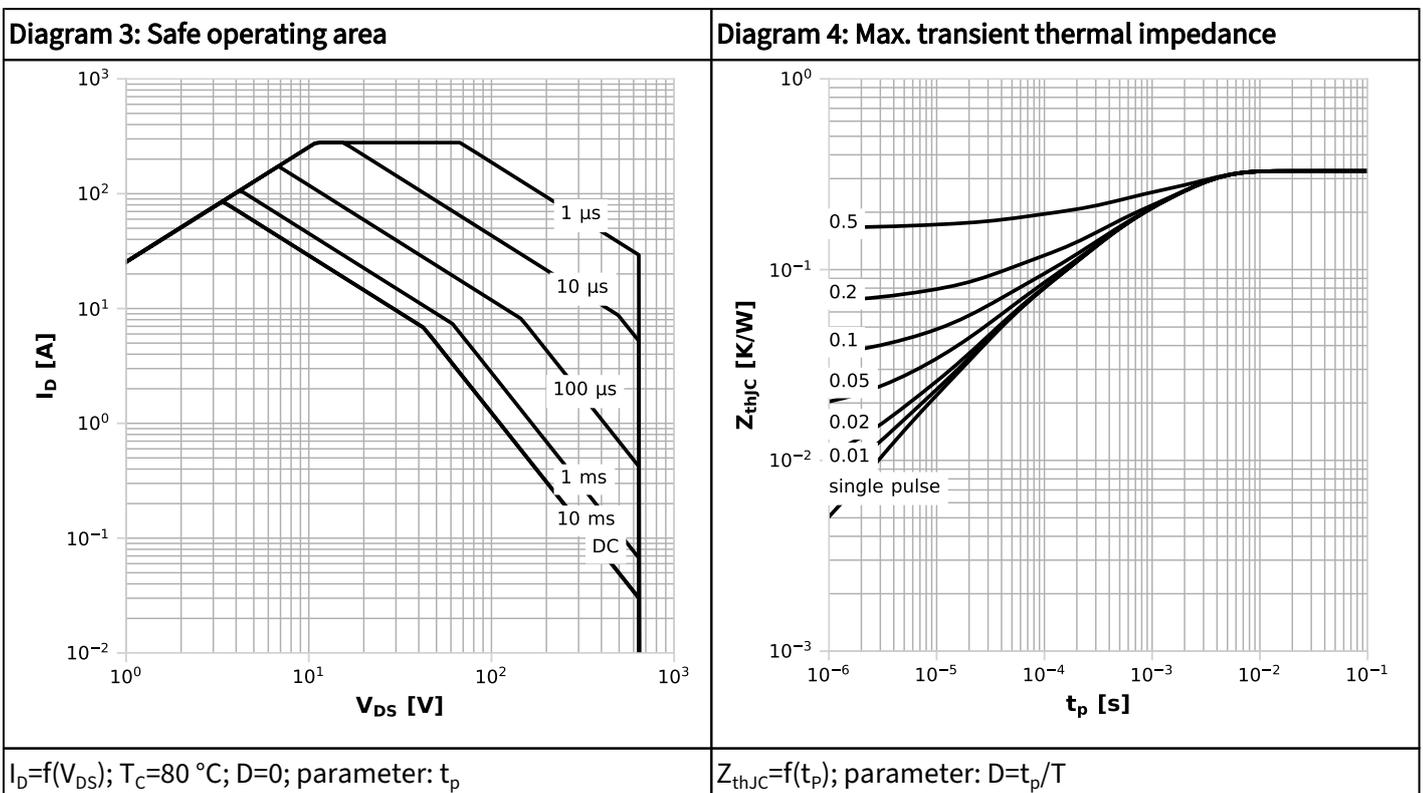
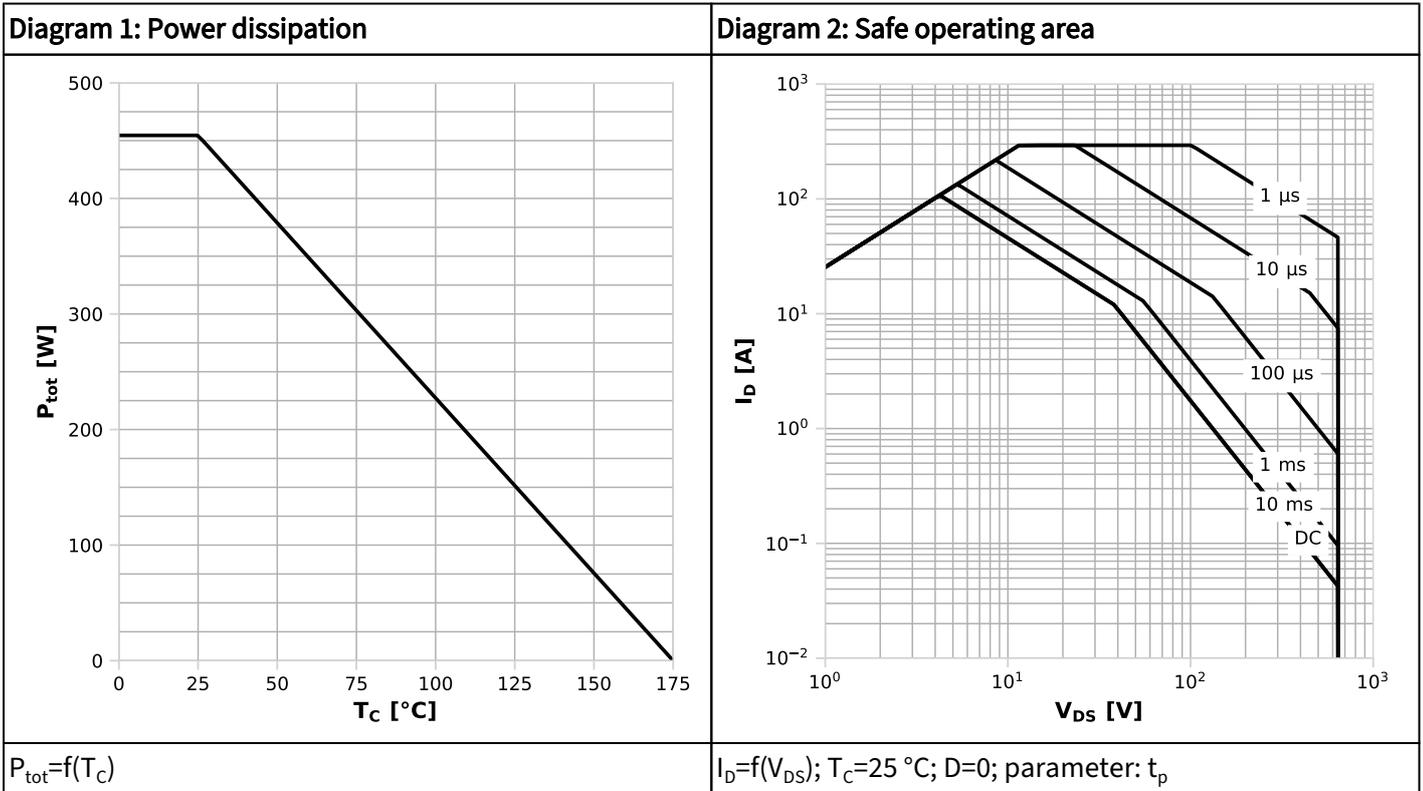
| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------|----------|--------|------------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Drain-source reverse voltage | V_{SD} | - | 4.3 | - | V | $V_{GS} = 0\text{ V}$, $I_S = 46.9\text{ A}$, $T_j = 25\text{ }^\circ\text{C}$ |
| MOSFET forward recovery time | t_{fr} | - | 18 13.2 | - | ns | $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9 |

Table 8 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|----------------------------------------------|-----------|--------|--------------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | Min. | Typ. | Max. | | |
| MOSFET forward recovery charge ⁹⁾ | Q_{fr} | - | 110 184 | - | nC | $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9 |
| MOSFET peak forward recovery current | I_{frm} | - | 12.2 27.8 | - | A | $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 400\text{ V}$, $I_S = 46.9\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9 |

⁹⁾ Q_{fr} includes Q_{oss}

5 Electrical characteristics diagrams



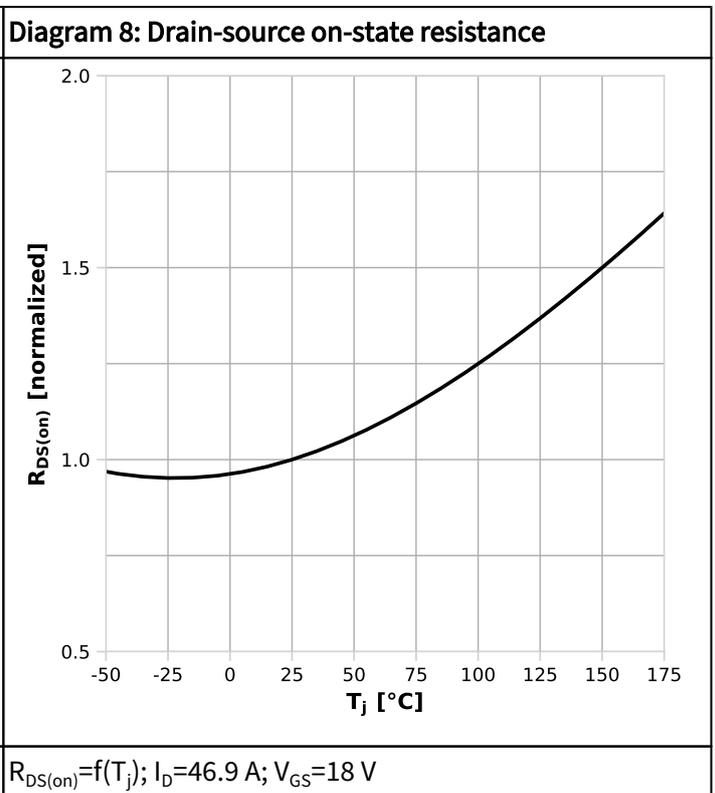
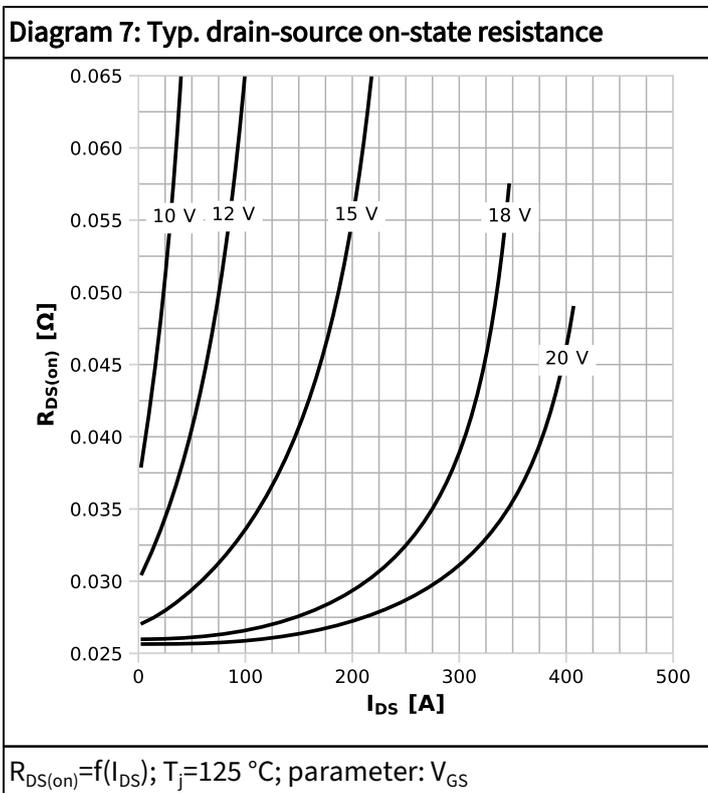
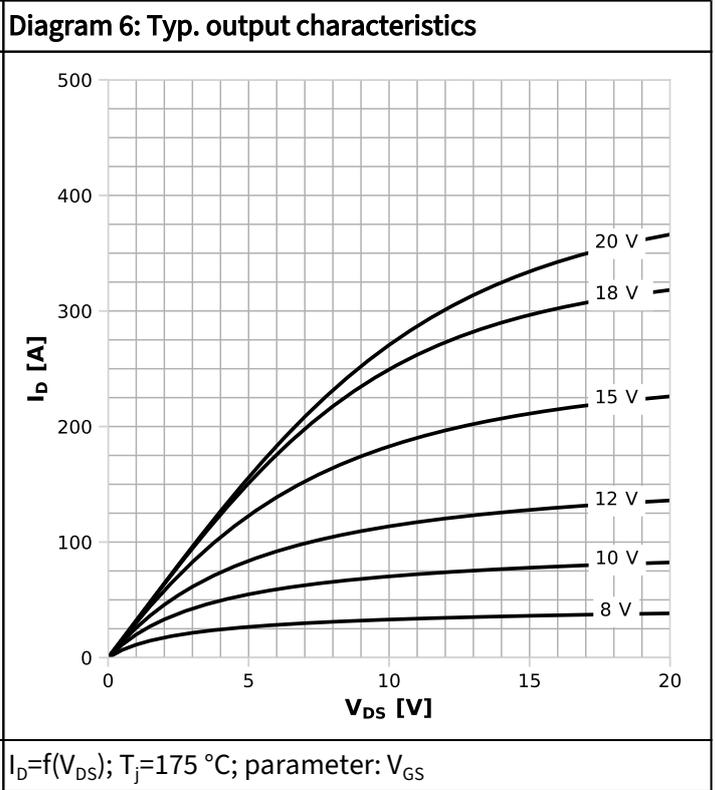
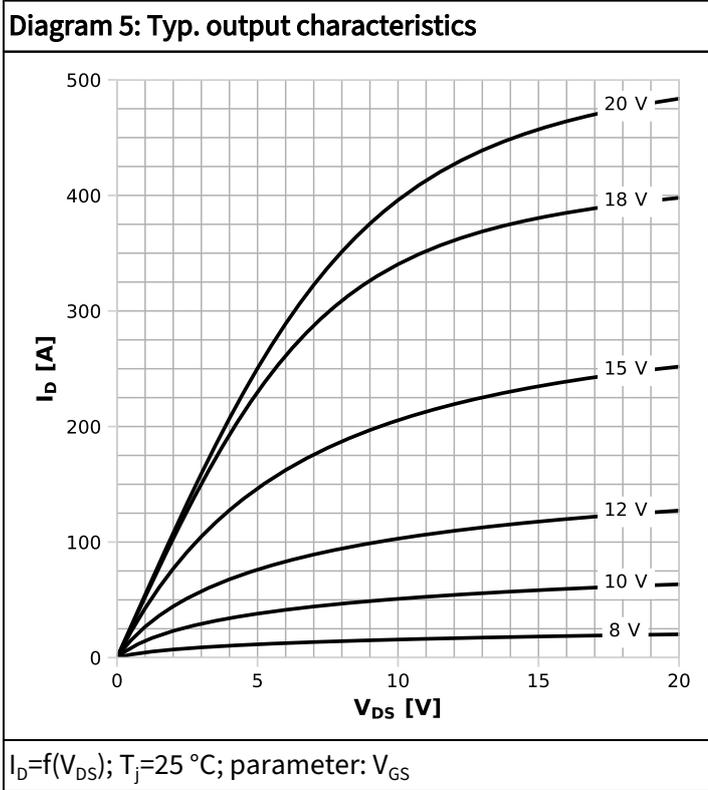
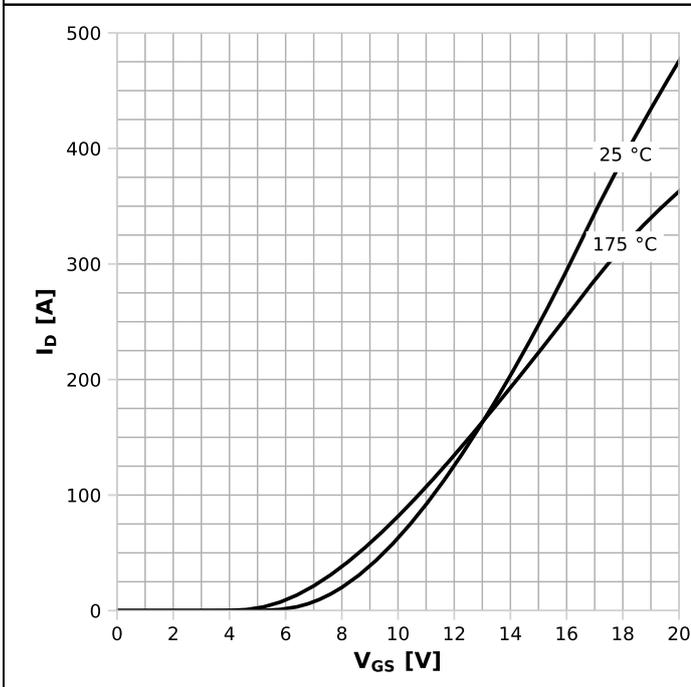
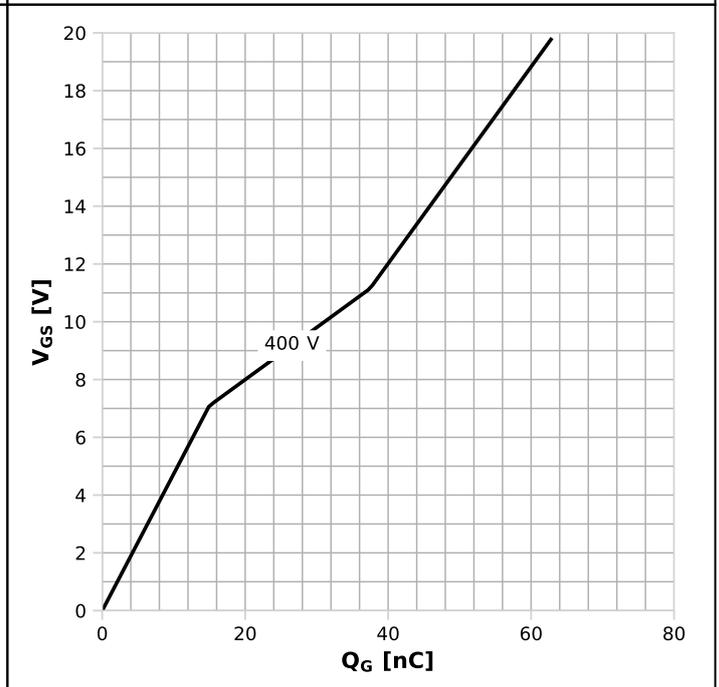


Diagram 9: Typ. transfer characteristics



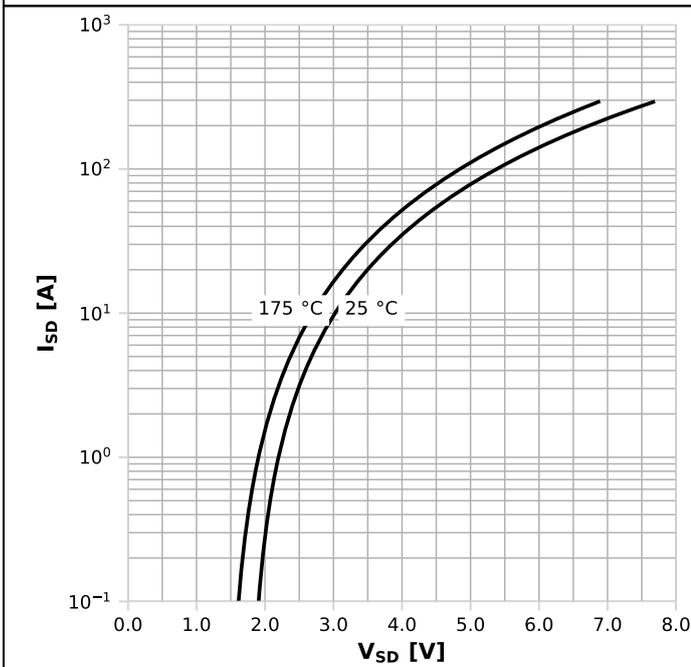
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



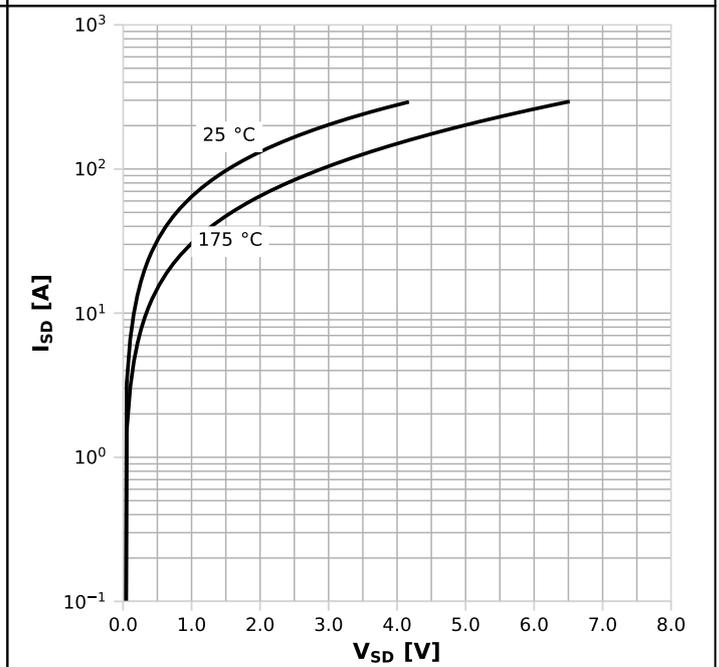
$V_{GS} = f(Q_{gate}); I_D = 46.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Typ. reverse characteristics



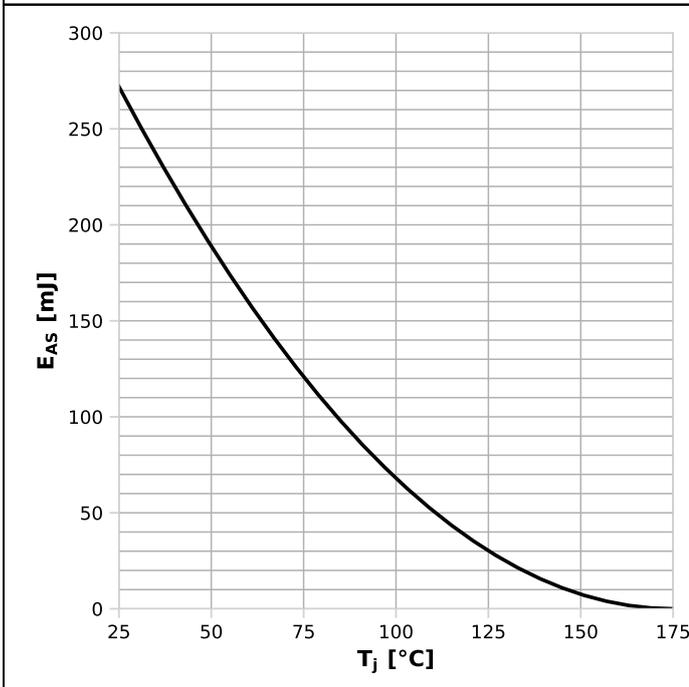
$I_{SD} = f(V_{SD}); V_{GS} = 0 \text{ V}; \text{parameter: } T_j$

Diagram 12: Typ. reverse characteristics



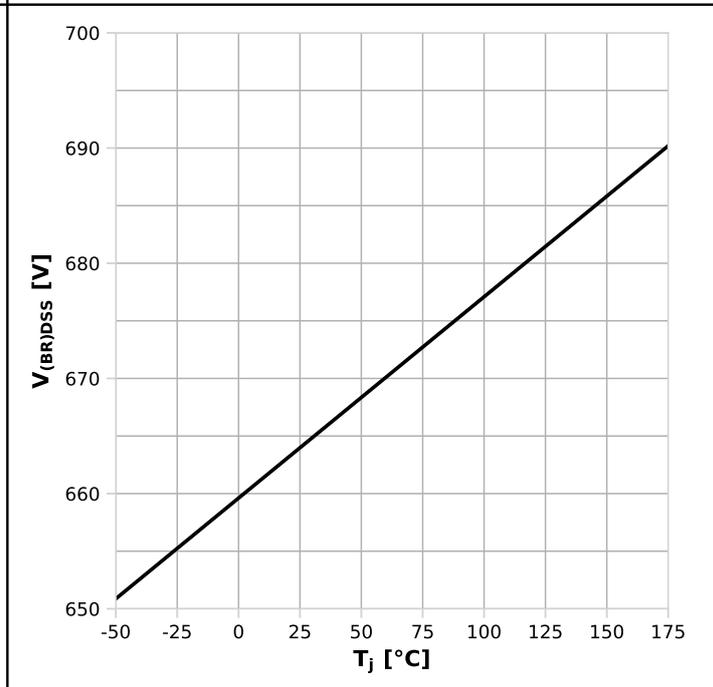
$I_{SD} = f(V_{SD}); V_{GS} = 18 \text{ V}; \text{parameter: } T_j$

Diagram 13: Avalanche energy



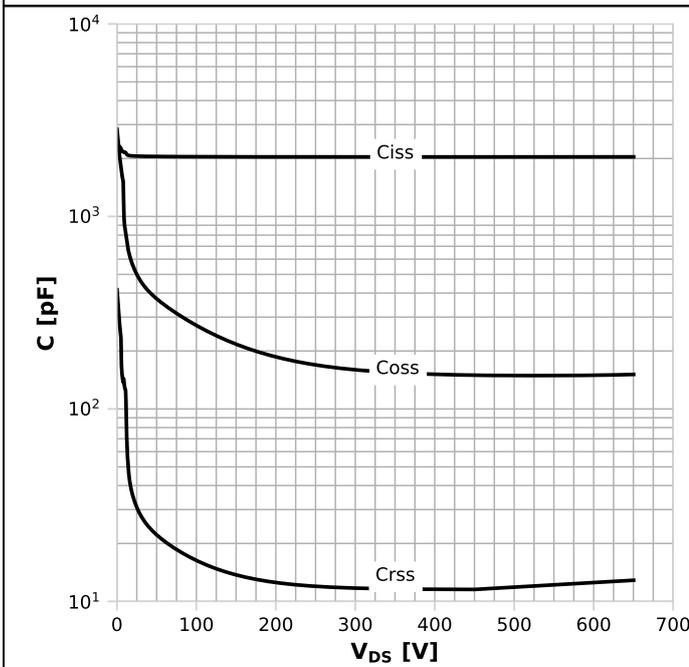
$E_{AS}=f(T_j); I_D=10.2 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 14: Drain-source breakdown voltage



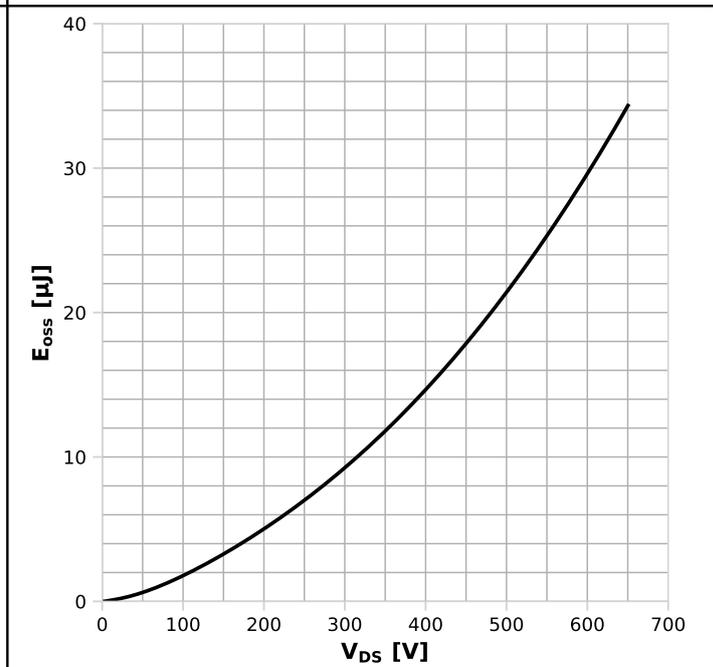
$V_{(BR)DSS}=f(T_j); I_D=0.95 \text{ mA}$

Diagram 15: Typ. capacitances



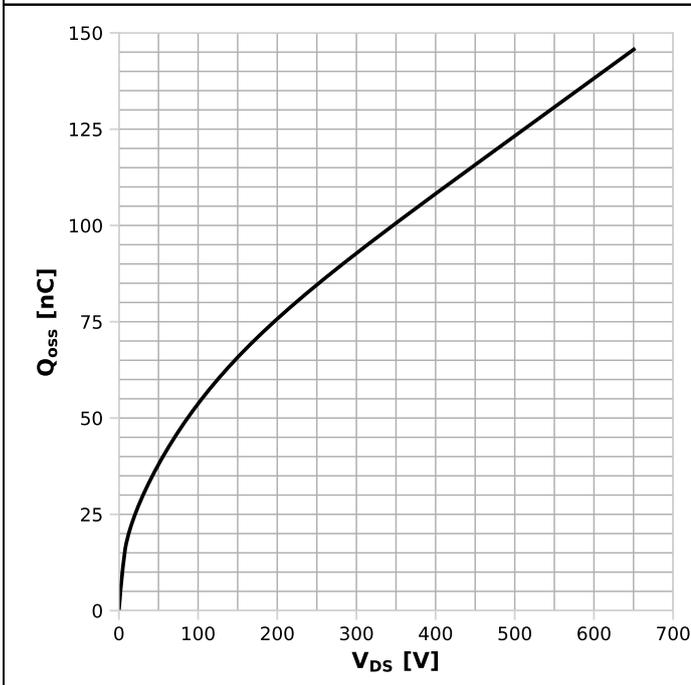
$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 16: Typ. Coss stored energy



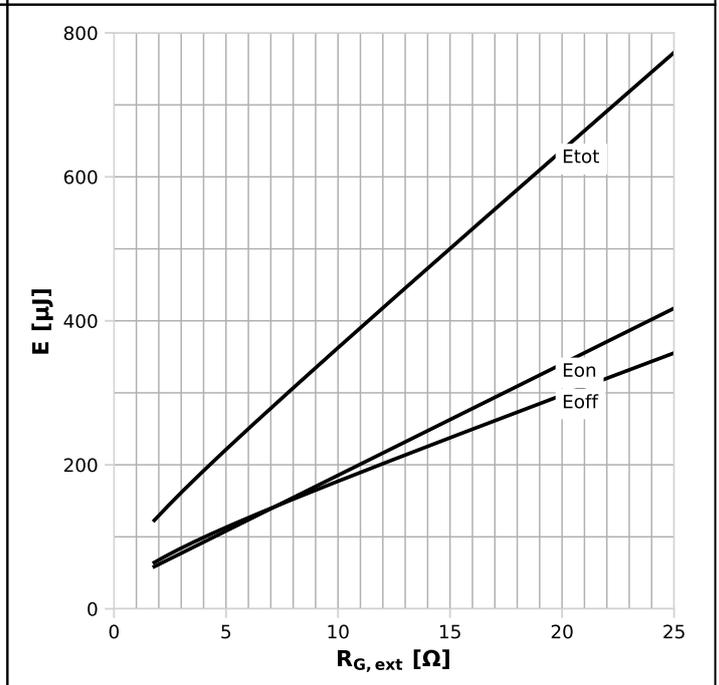
$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



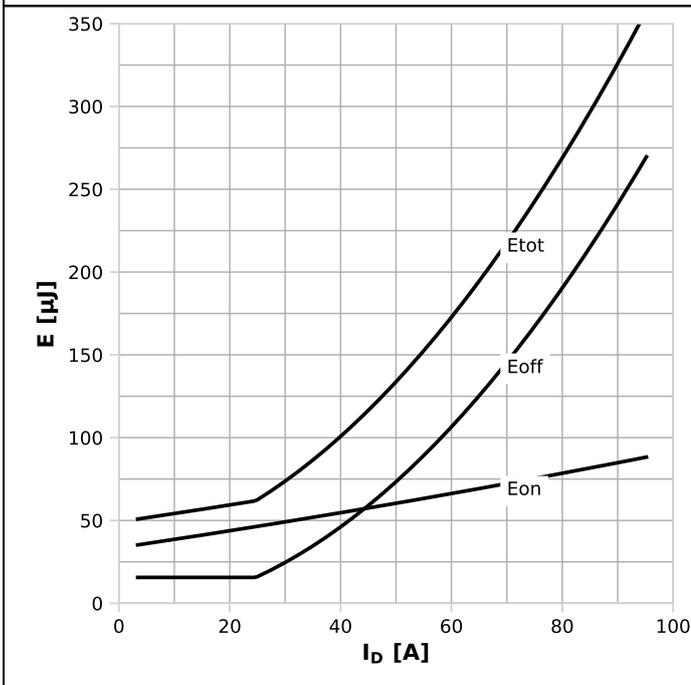
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. Switching Losses vs R_{G,ext}



$E=f(R_{G,ext}); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; I_D=46.9\text{ A}$

Diagram 19: Typ. Switching Losses vs switching current



$E=f(I_D); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; R_{G,ext}=1.8\ \Omega$

6 Test Circuits

Table 9 Body diode characteristics (CoolSiC)

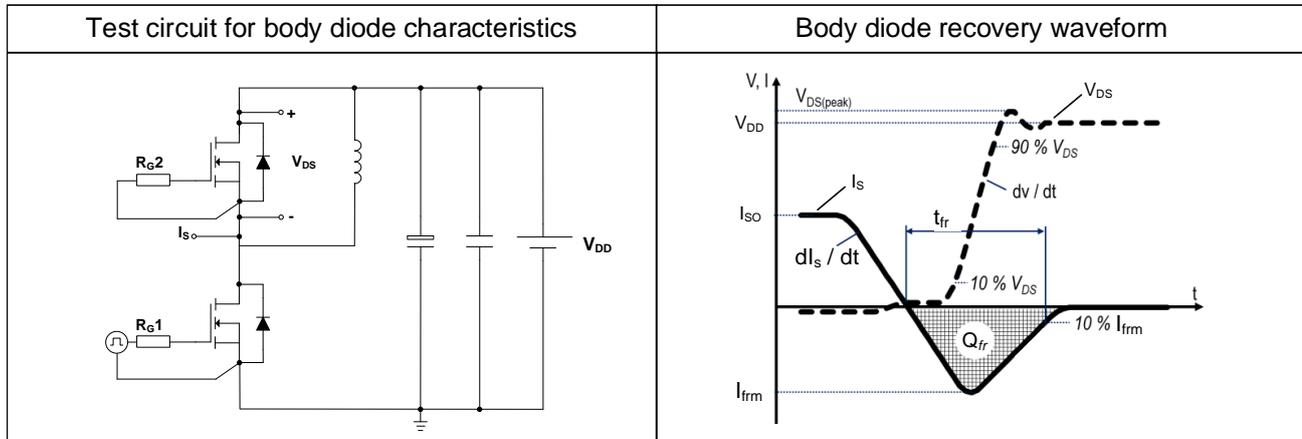


Table 10 Switching times (CoolSiC)

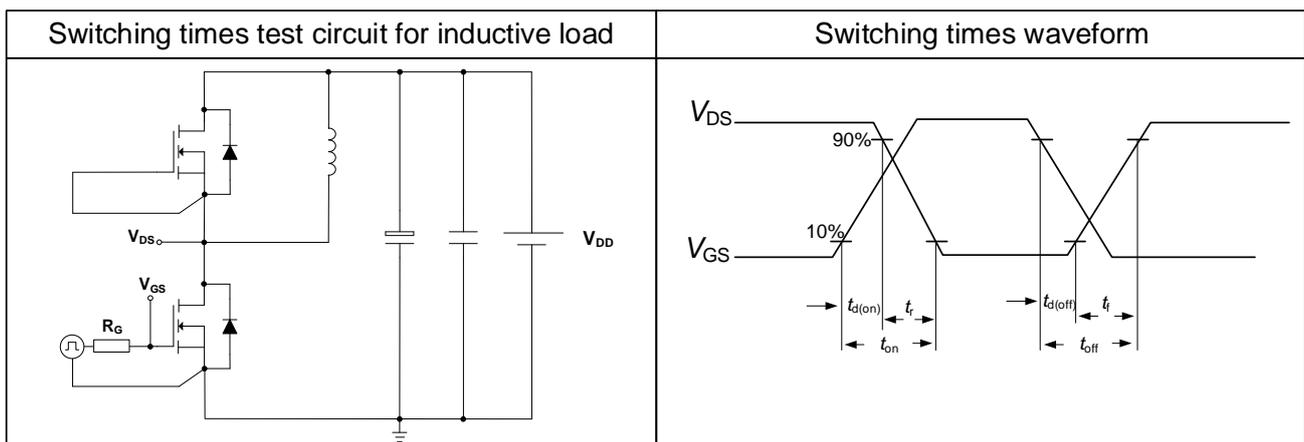
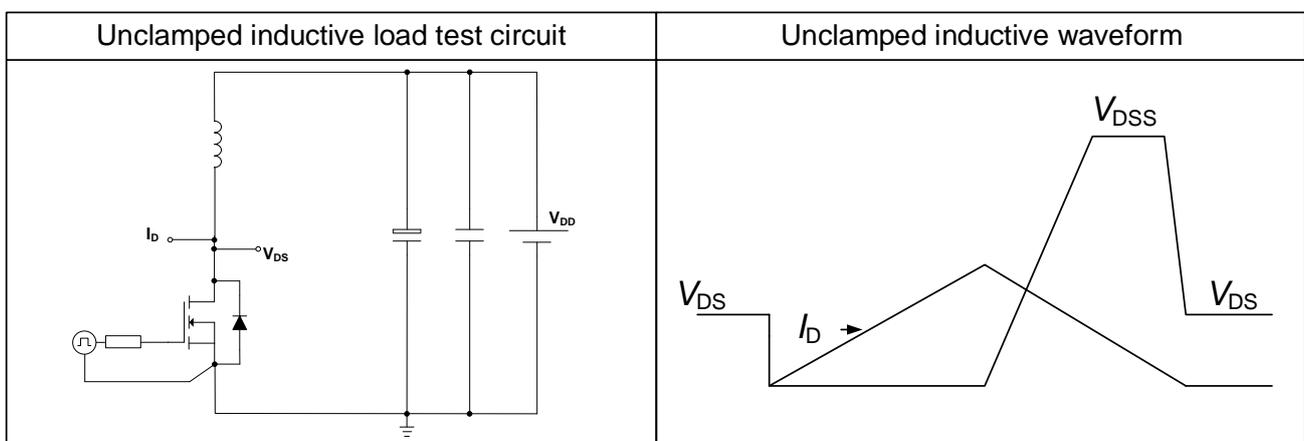


Table 11 Unclamped inductive load



7 Package Outlines

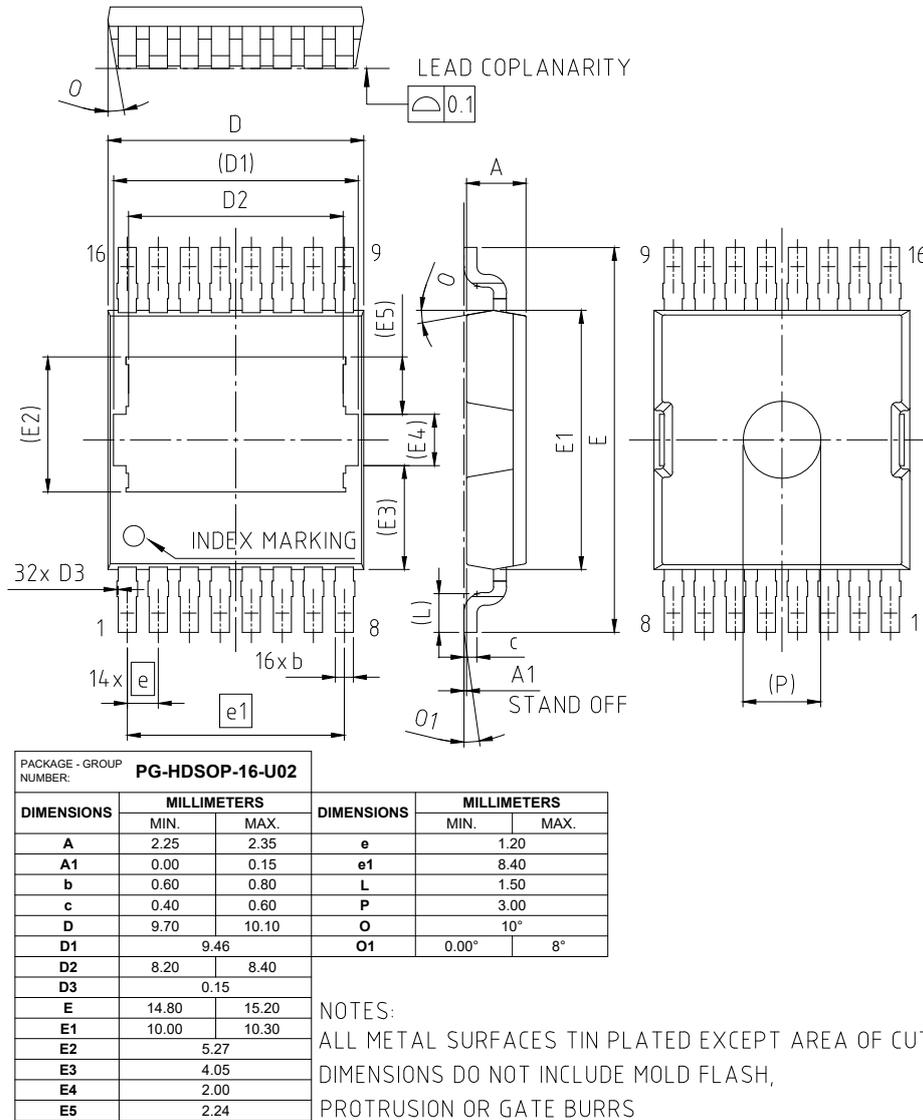


Figure 1 Outline PG-HDSOP-16, dimensions in mm

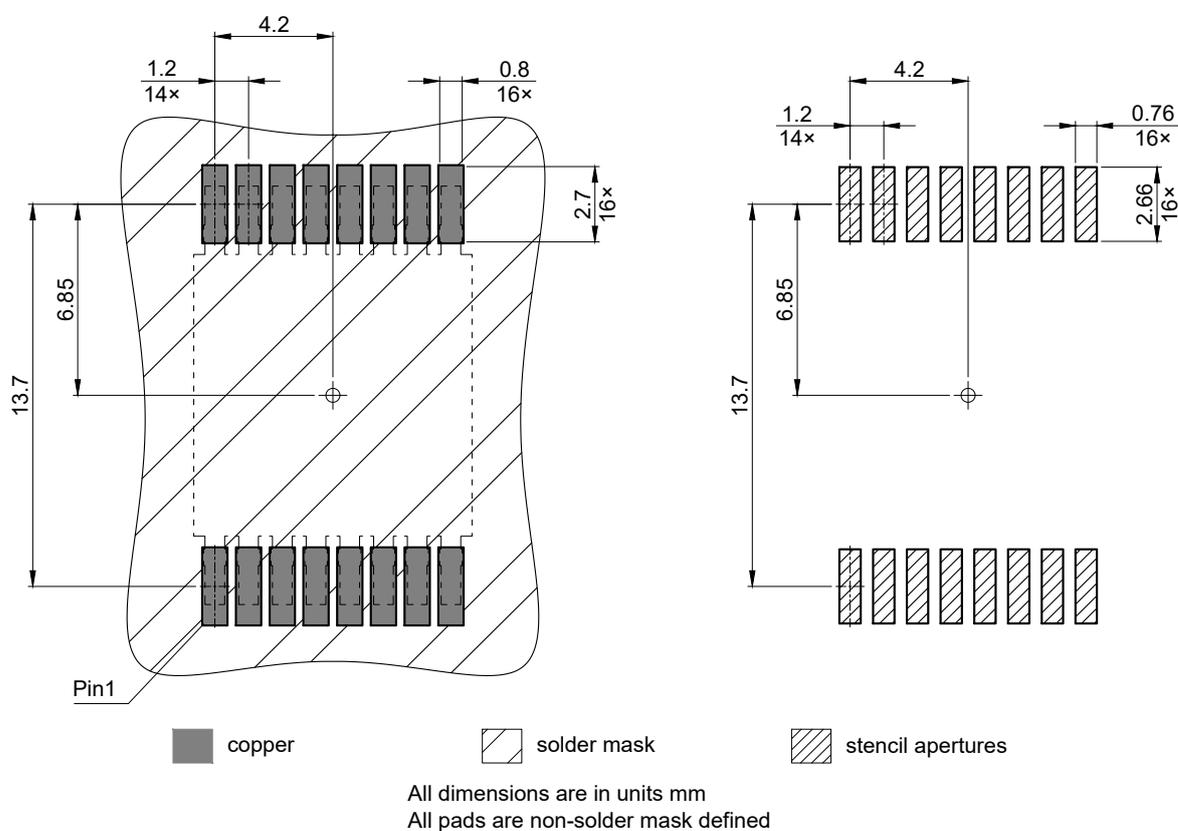
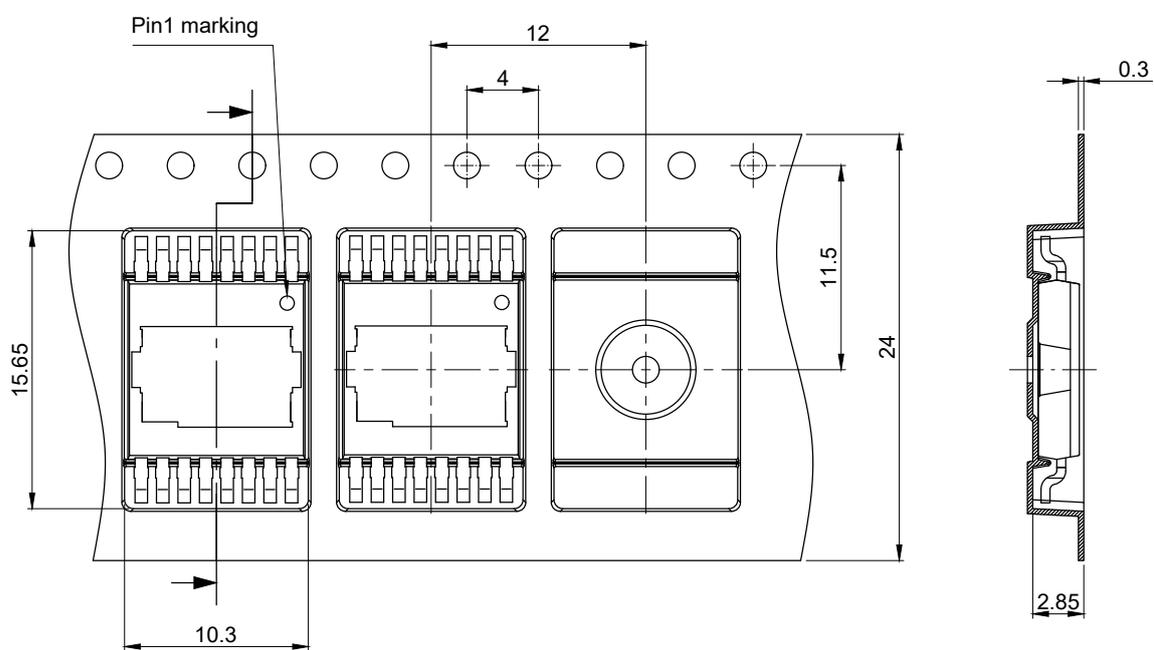


Figure 2 Outline PG-HDSOP-16, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Outline PG-HDSOP-16, dimensions in mm

8 Appendix A

Table 12 Related Links

- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model](#)
- [IFX Design tools](#)

Revision History

IMLT65R020M2H

Revision 2024-05-03, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|----------------------------------------------|
| 2.0 | 2024-05-03 | Release of final |

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