ICL8830

High frequency, single-stage PFC flyback controller for constant voltage output

Features

The ICL8830 controller is tailored for high-frequency switching operation and capable to drive GaN and Si MOSFET switching devices. It detects flyback switch drain voltage high frequency oscillation and provides the gate signal with small delay for accurate and reliable quasi-resonant mode (QRM) operation.

- SSR-CV output flyback topology
- Optimized for high-frequency operation. Suitable for operation with GaN devices
- High power factor and low THD, across wide AC input voltage and output load range
- Supports universal AC input voltage (90 V_{AC} to 300 V_{AC}, 45 Hz to 66 Hz) and DC input voltage operation
- QRM operation with valley switching and continuous conduction mode (CCM)-prevention
- Burst mode for very light loads and low system standby power consumption
- Adjustable on-time mapping at valley changing position, for the desired maximum operating switching frequency
- Adjustable maximum on-time – limits input power and current allowing safe-operation under low line condition
- Comprehensive set of protections:
  - internal overtemperature protection (OTP)
  - flyback output overvoltage protection (OVP)
  - primary side overcurrent protection (OCP)
  - brownin protection
  - brownout protection
  - *VCC* overvoltage protection
  - open loop protection
  - input overvoltage protection
- Soft start to reduce component stress during turn-on
- External start-up circuit control signal
- Reduced gate driver voltage during start-up sequence, to allow smaller *VCC* capacitance for faster start-up
- *VCC* wake-up burst operation, to maintain sufficient V_{VCC} in burst mode
- Reduced gate driver voltage in burst mode, to reduce gate charge loss, for lower standby power

Potential applications

High-frequency PFC flyback SSR-CV

- SMPS
- LED drivers, smart lighting, emergency lighting
- Adapter, charger, home appliances, ceiling fan

Product validation

Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC20/22.

Description

The ICL8830 is a voltage mode controller for flyback topologies operating in QRM with valley switching, to achieve high efficiency while providing high power factor. It is designed for high-frequency switching applications, and is capable to detect drain voltage high-frequency oscillation of the flyback switch. The IC is designed for flyback and PFC flyback topologies, and for AC/DC and DC/DC applications. The IC can operate with GaN and Si MOSFET switches. The integrated burst mode function allows designs with a very low power consumption during standby mode and very light loads. The controller is easy to design in and requires a minimum number of external components.

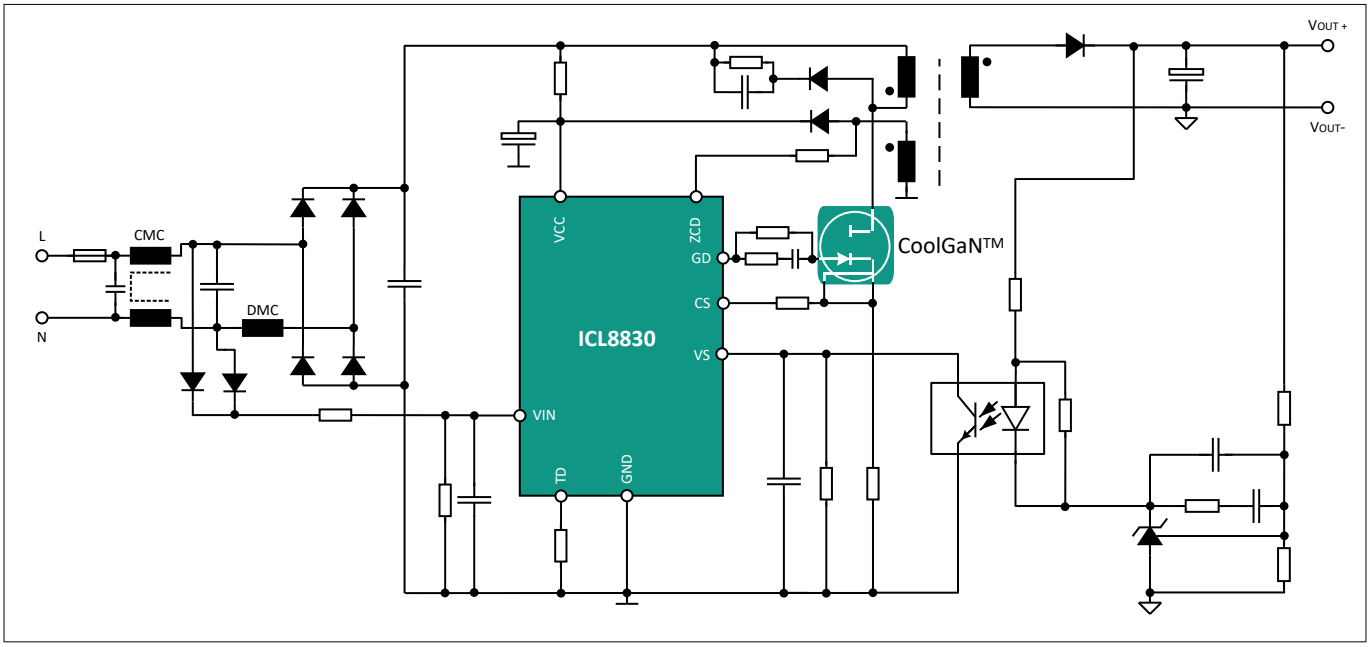

Figure 1 PFC Flyback-SSR-CV with GaN FET

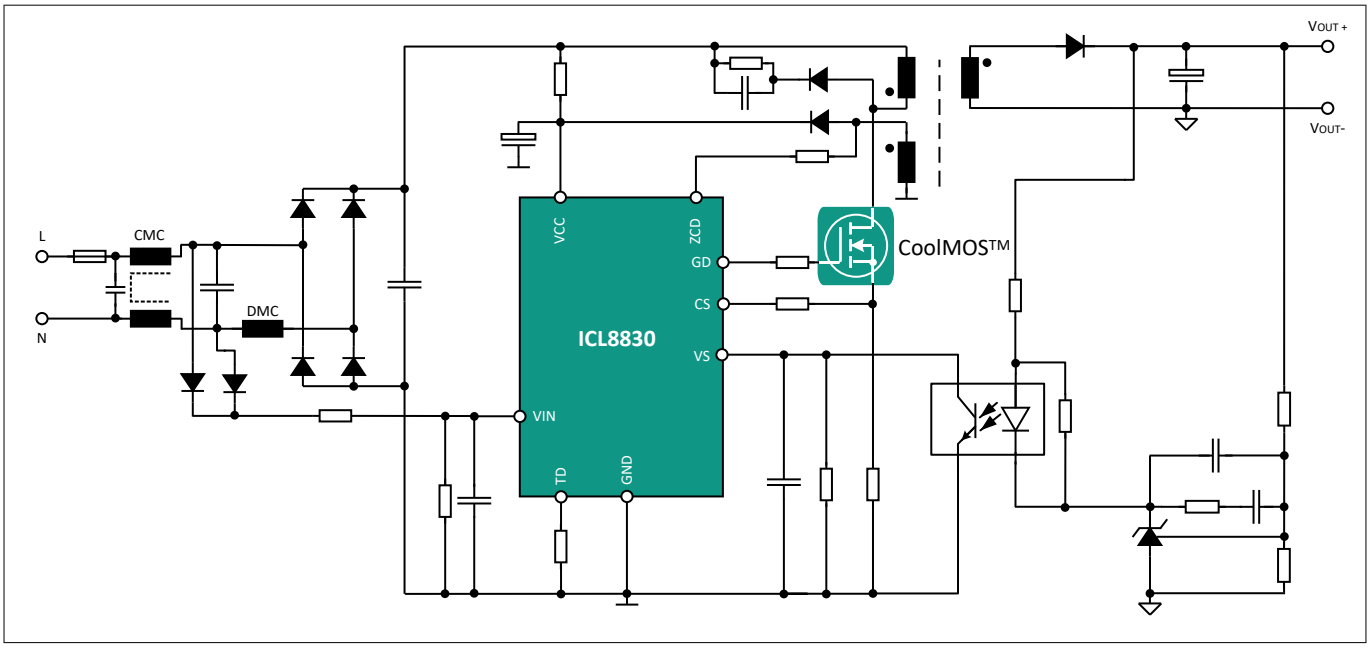

Figure 2 PFC Flyback-SSR-CV with Si MOSFET

Product type	Package	Marking	Ordering code
ICL8830	PG-DSO-8	L8830	SP006071841

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1 Pin configuration

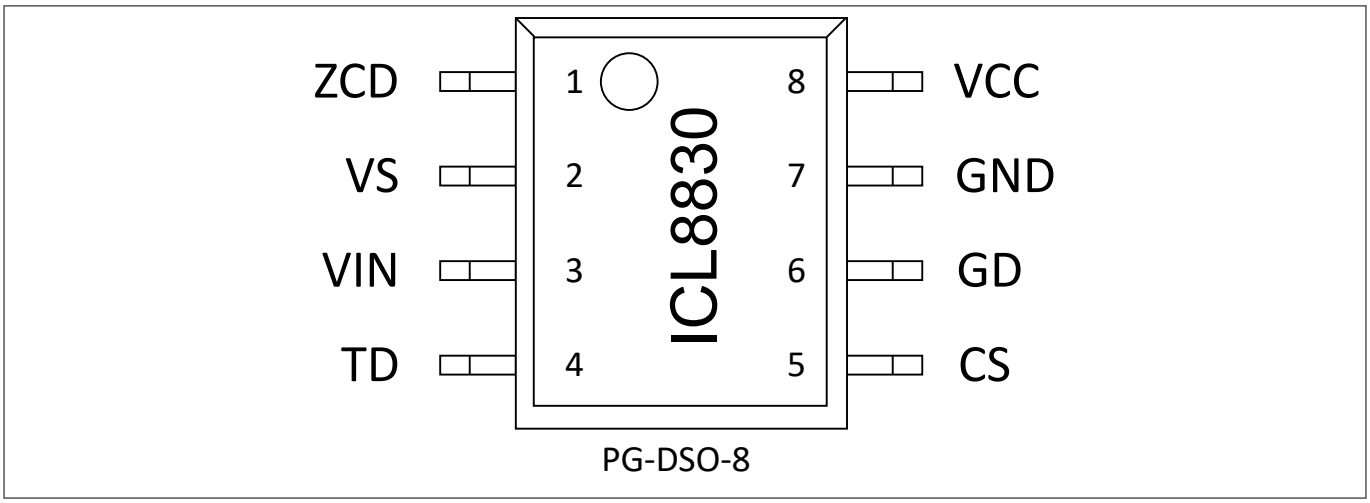


Figure 3 Pin configuration

Table 1 Pin definition and function

Symbol	Pin	Function
ZCD	1	**Zero crossing detection** This pin is connected to an auxiliary winding via a series resistor to detect the zero crossing, for QRM valley switching. This series resistor value can be adjusted to configure the on-time mapping and maximum on-time.
VS	2	**Feedback sensing** This pin measures the feedback signal in the form of load current, for output regulation with voltage mode control.
VIN	3	**Input voltage detection** This pin is used to measure the rectified input voltage via a resistor divider for the power limitation function, brownin, brownout and input overvoltage protection.
TD	4	**Turn-on delay** The resistance to ground R_{TD} of this pin can adjust the turn-on delay upon zero crossing detection for QRM valley switching. The internal pull-up of this pin can also be used to control an external start-up circuit for active V_{VCC} charging.
CS	5	**MOSFET current sense and flyback output overvoltage protection** This pin is used for primary side overcurrent protection. The series resistance (connected between this pin and the primary MOSFET current shunt resistor) can be used to adjust the flyback output overvoltage protection level.
GD	6	**Gate driver** This pin controls the gate of the MOSFET.
GND	7	**Ground** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate driver and sense signals.
VCC	8	**Operating voltage supply** This pin supplies the IC.

2 Block diagram

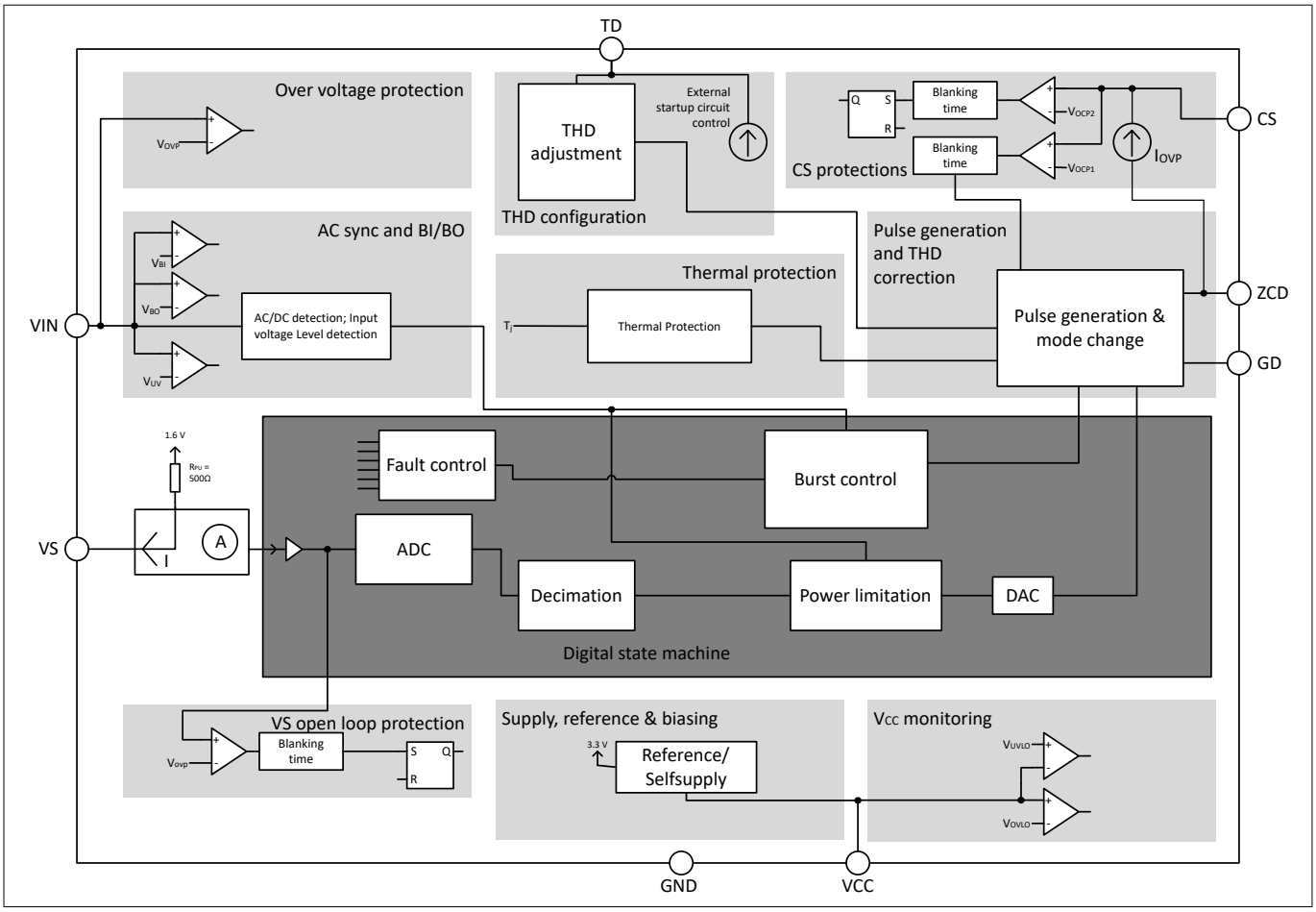


Figure 4 Block diagram

3 Functional description

These sections describe the listed functions in detail.

3.1 Start-up

In the pre-start-up phase, ICL8830 measures the *TD* pin resistance to ground R_{TD}, the average *VIN* pin voltage $V_{VIN,avg}$, and its internal junction temperature T_j. If the conditions for start-up are met, ICL8830 initiates a soft start, to reduce the component stress during start-up.

After the soft start is completed without any protection triggering, ICL8830 enters the RUN state for output regulation based on *VS* pin signal sensing.

***Note**: The reduced gate driver voltage V_{GDred} (7 V typ.) is applied during start-up.*

3.2 TD pin internal pull-up and external start-up circuit control

Apart from charging the V_{VCC} from the HV bus voltage via the current limiting resistor in Figure 1 and Figure 3, ICL8830 *TD* pin also supports the control of an exemplary external start-up circuit in Figure 5 for active V_{VCC} charging, with the following typical start-up sequence:

1. When ICL8830 is in the undervoltage lockout (UVLO) state and $V_{VCC} < V_{VCCon}$ (12.5 V typ.), the *TD* pin internal pull-up is disabled.
2. V_{VCC} is charged to V_{VCCon} by the external start-up circuit, to activate ICL8830.
3. In the pre-start-up phase, ICL8830 enables the *TD* pin internal pull-up resistor of $R_{TD,RUN}$ (10 kΩ typ.) and $R_{TD,flyback}$ (40 kΩ typ.) sequentially, to measure the *TD* pin resistance to ground of R_{TD}.
4. If the start-up conditions are met and the start-up is successful, $R_{TD,RUN}$ is enabled in the soft start phase and in RUN state, to disable the external start-up circuit from charging the V_{VCC}. If any protection is triggered, ICL8830 enters UVLO state (returns sequence number 1) after a restart timer is expired.

***Note**: The internal voltage reference for the TD pin internal pull-up, V_{REF} is typically 3.3 V.*

***Note**: $R_{TD,RUN}$ is disabled in burst mode when VCC drops to $V_{VCCwake}$ (7.6 V typ.), to allow the external start-up circuit to charge V_{VCC} to $V_{VCCburst}$ (8.1 V typ).*

Figure 5 shows the equation for R_{TD} calculation when the exemplary start-up circuit is connected to the *TD* pin. The R_{TD} detected in the pre-start-up phase must be designed to be at least 18 kΩ when *TD* pin is internally pulled up by $R_{TD,RUN}$, and not more than 68 kΩ when *TD* pin is internally pulled up by $R_{TD,flyback}$. The is to activate the *VS* pin load current sensing for output regulation and stay within the TD configuration limit.

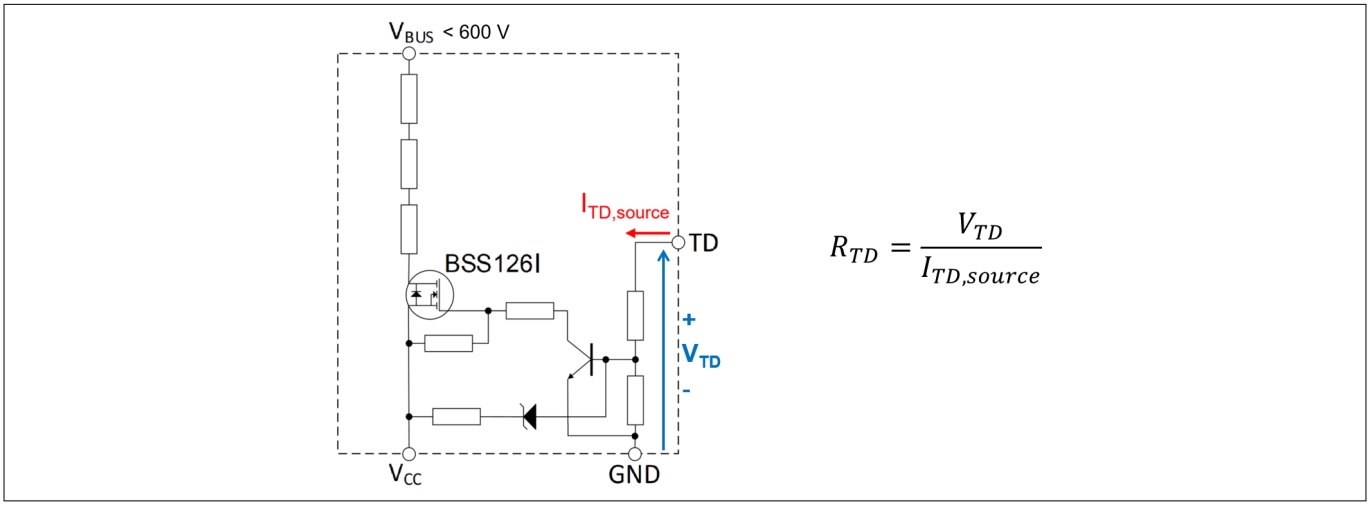


Figure 5 Exemplary external start-up circuit for active V_{VCC} charging, and R_{TD} generic equation

3.3 Input voltage detection and protection

ICL8830 detects the AC or DC amplitude based on the ADC sampling of the *VIN* pin voltage. For the power limiting function, brownin and brownout protections, the controller measures the average *VIN* pin voltage $V_{VIN,avg}$ based on the middle value of the highest *VIN* pin voltage sample and the lowest *VIN* pin voltage sample within an observation time. The observation time in RUN state is around 10.6 ms and 12.7 ms, based on the last synced AC line frequency of 50 Hz and 60 Hz, respectively.

***Note**: In case of non-line-syncing, the observation time is around 10.6 ms. For example, non-line-syncing can happen when the system is started up with a DC input.*

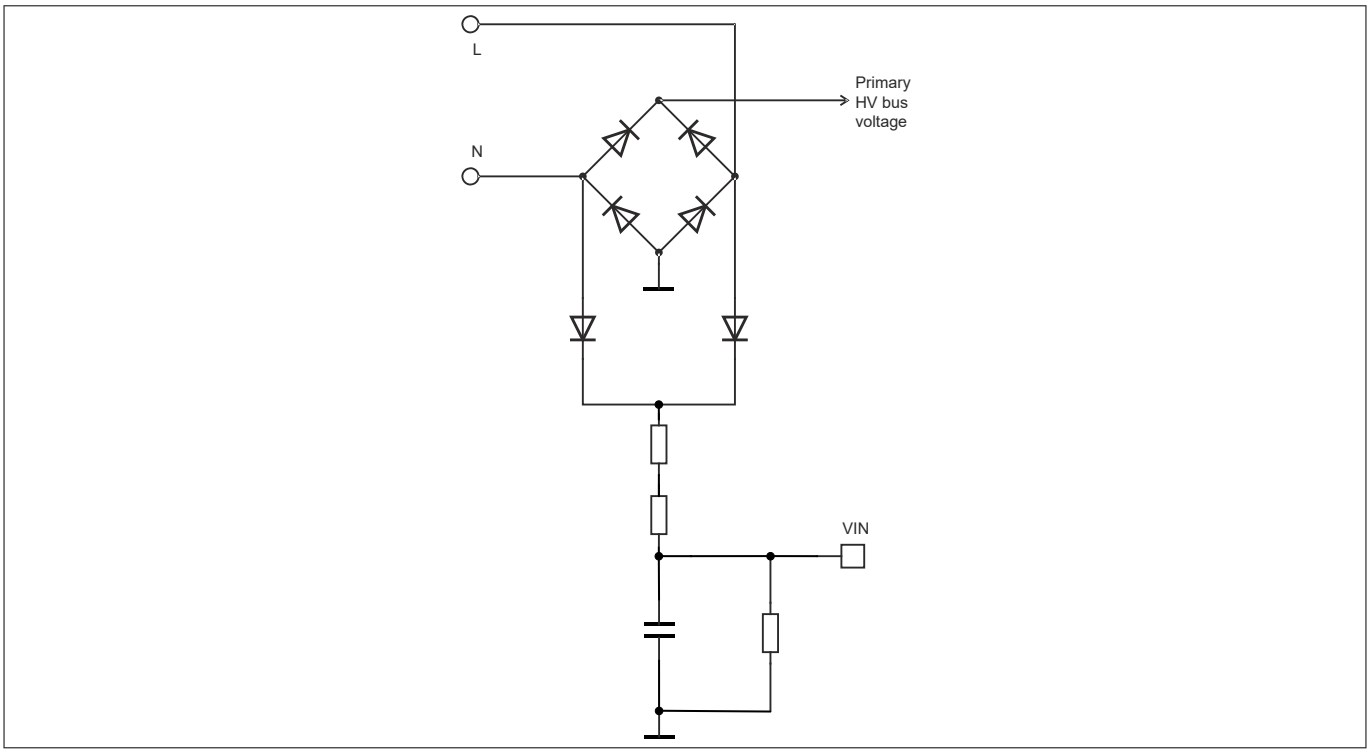


Figure 6 V_{IN} pin circuit

In addition, the ICL8830 *VIN* pin has an input overvoltage threshold of V_{VINOV} (2.0 V typ.) and a short protection with a threshold of $V_{VINshort}$ (200 mV typ.).

During operation, if a sampled *VIN* pin voltage $V_{VIN} < V_{VINshort}$ is detected for more than a blanking time, the *VIN* pin short protection is triggered. If the $V_{VIN} < V_{VINshort}$ condition remains after the *VIN* pin short protection restart time of $t_{restart}$ (200 ms typ.), the brownin protection is triggered based on $V_{VIN,avg} < V_{BI}$ detection instead. This leads to a fast restart cycle of $t_{restart,fast}$ (25 ms typ.) afterwards.

By pulling down the *VIN* pin signal to a level that triggers the *VIN* pin short protection or brownout protection, ICL8830 gate pulse generation can be disabled and the controller current consumption can be lowered.

3.4 ZCD pin signal sensing

ICL8830 *ZCD* pin detects the auxiliary winding voltage zero-crossing via a *ZCD* series resistor of R_{ZCD} connected to the winding. A zero-crossing is detected with the hysteresis of V_{ZCDUp} (55 mV typ.) and $V_{ZCDDown}$ (45 mV typ.) thresholds.

In QRM, ICL8830 counts the number of zero crossings until the target valley number is reached, and switches on at the valley to minimize the switching loss. If the target valley number is not reached and further zero crossing signals are not detectable via *ZCD* pin, zero crossing events can be generated internally by extrapolation. Figure 7 shows an example of the 1st zero-crossing detection and the 1st valley switching in QRM operation.

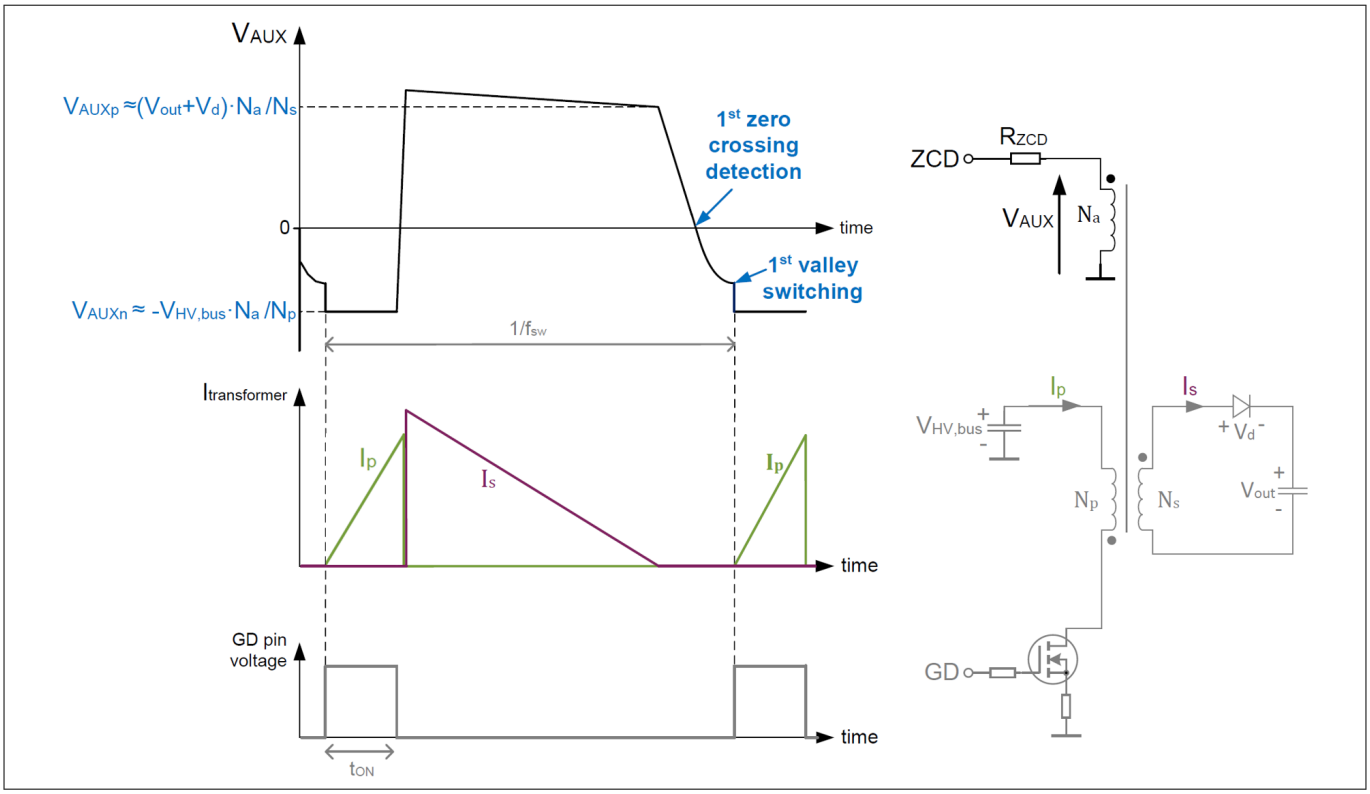


Figure 7 **Exemplary waveform of QRM operation with 1st zero crossing detection and 1st valley switching**

R_{ZCD} limits the *ZCD* pin sink and source currents when the auxiliary winding voltage exceeds the *ZCD* pin internal clamping levels $V_{ZCDpclp}$ (0.55 V typ.) and $V_{ZCDnclp}$ (-0.5 V typ.), respectively. When the sensed voltage level of the auxiliary winding is not sufficient (for example, during start-up), an internal start-up timer initiates a new cycle every t_{Rep} (52 µs typ.) after turn-off of the gate driver. From the *ZCD* pin sink and source currents, ICL8830 detects the *ZCD* pin positive peak settled clamping current $I_{ZCDpclp}$ and negative peak settled clamping current $I_{ZCDnclp}$, for its internal operations, such as THD correction and flyback output overvoltage protection.

$$I_{ZCDpclp} = \frac{V_{AUXp} - V_{ZCDpclp}}{R_{ZCD}} \quad (1)$$

$$I_{ZCDnclp} = \frac{|V_{AUXn}| - |V_{ZCDnclp}|}{R_{ZCD}} \quad (2)$$

Where V_{AUXp} and V_{AUXn} are the positive peak and negative peak values, respectively, of the settled auxiliary winding voltages, as shown in Figure 7.

In addition, ICL8830 derives the *ZCD* pin peak to peak settled clamping current I_{ZCDclp} based on the sum of $I_{ZCDpclp}$ and $I_{ZCDnclp}$, for its internal operations, such as pulse generation and power limitation.

$$I_{ZCDclp} = I_{ZCDpclp} + I_{ZCDnclp} \quad (3)$$

3.5 Power factor correction and THD correction

In RUN state, ICL8830 achieves power factor correction, when the *VS* pin feedback signal maps to a stable operating point in QRM. Additionally, ICL8830 THD correction function extends the on-time, especially when it is near AC input voltage zero crossing, to optimize the AC input current waveform.

As shown in Figure 8 area A, ICL8830 increases the on-time extension near AC input voltage zero crossing, where $I_{ZCDnclp}$ is less than 80% of $I_{ZCDpclp}$.

The gain of the THD correction on-time extension is configurable based on the detected *TD* pin resistance to ground R_{TD} in the pre-start-up phase. Since the THD correction on-time extension also affects the turn-on delay upon zero crossing detection, the R_{TD} value has to be fine-tuned manually for a given system, to achieve a balance between the QRM valley switching point optimization and THD correction.

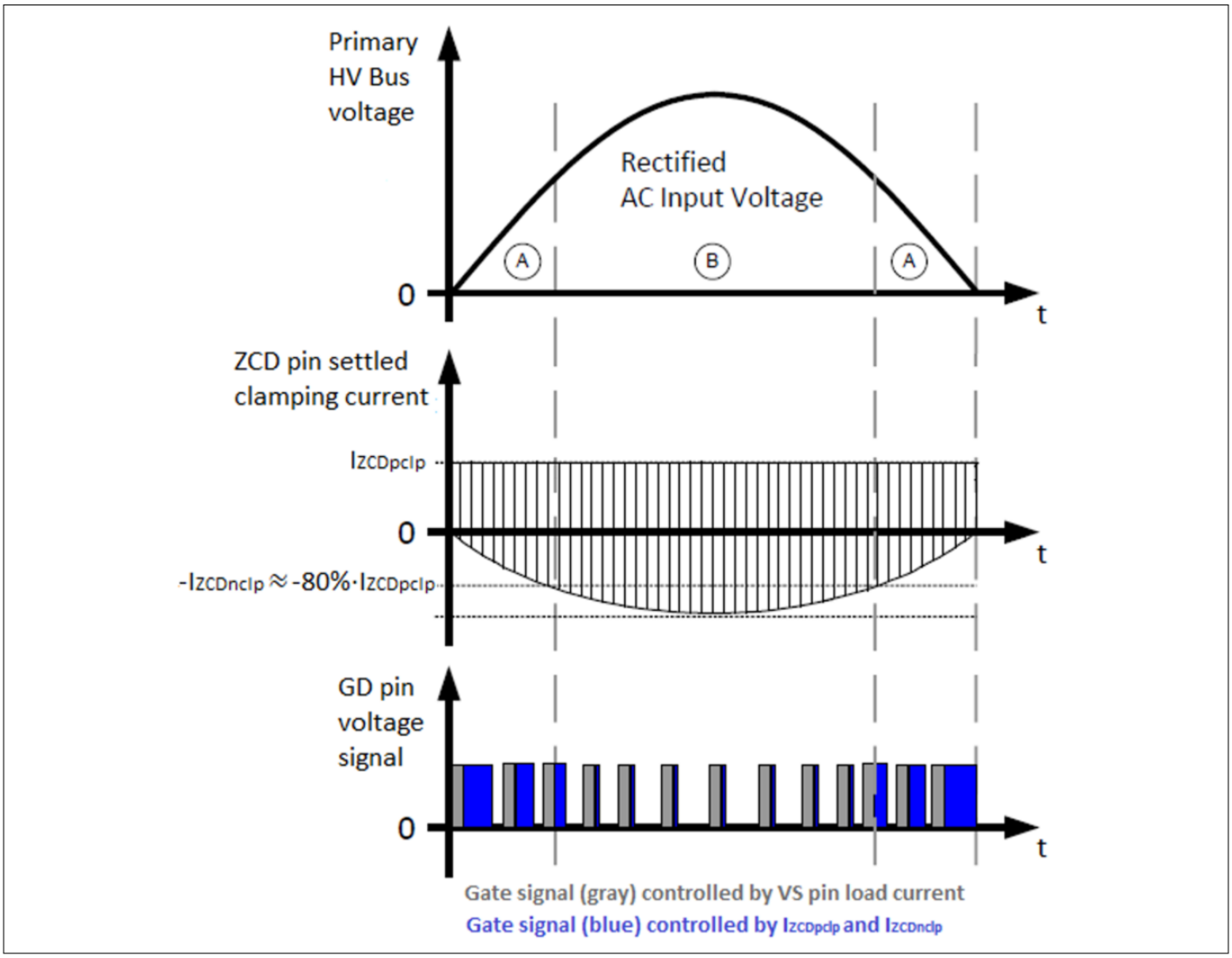


Figure 8 ICL8830 THD correction with on-time extension near AC input voltage zero crossing

If the *TD* pin is only used for THD correction gain configuration, but not for other purpose like controlling an external start-up circuit, a resistor can be connected from *TD* pin to ground, and simply fine-tuned between 18 kΩ and 68 kΩ.

If there is any circuit more than just a resistor connected between *TD* pin and ground, the following generic equation for R_{TD} calculation is applied:

$$R_{TD} = \frac{V_{TD}}{I_{source,\,TD}} \tag{4}$$

Where V_{TD} is the *TD* pin voltage with reference to ground and $I_{source,TD}$ is the current flowing out of *TD* pin, when the internal pull-up resistor of $R_{TD,RUN}$ or $R_{TD,flyback}$ is enabled in the pre-start-up phase.

The minimum R_{TD} value for TD configuration and to activate the *VS* pin load current sensing for output regulation in RUN state is 18 kΩ, when *TD* pin is internally pulled up by $R_{TD,RUN}$ in the pre-start-up phase.

The maximum R_{TD} value for TD configuration is 68 kΩ, when *TD* pin is internally pulled up by $R_{TD,flyback}$ in the pre-start-up phase.

3.6 VS pin signal sensing

In RUN state, ICL8830 measures the feedback signal for output regulation based on the ADC sampling of the *VS* pin load current. When operating in QRM with AC input, ICL8830 also synchronizes some of its operation to the line frequency or AC half cycle, when the *VS* pin load current ripple is large enough.

To activate the *VS* pin load current sensing for output regulation in RUN state, a 12 kΩ resistor must be connected from the *VS* pin to ground, and R_{TD} must be at least 18 kΩ when *TD* pin is internally pulled up by $R_{TD,RUN}$ in the pre-start-up phase.

For secondary side regulation, the *VS* pin load current consists of the current flowing through the opto coupler and the 12 kΩ resistor. When the *VS* pin load current is $-I_{VSADCmin}$ (210 µA typ.) or less, the power transfer is maximum. When the *VS* pin load current is $-I_{VSADCmax}$ (610 µA typ.) or more, the power transfer is minimum.

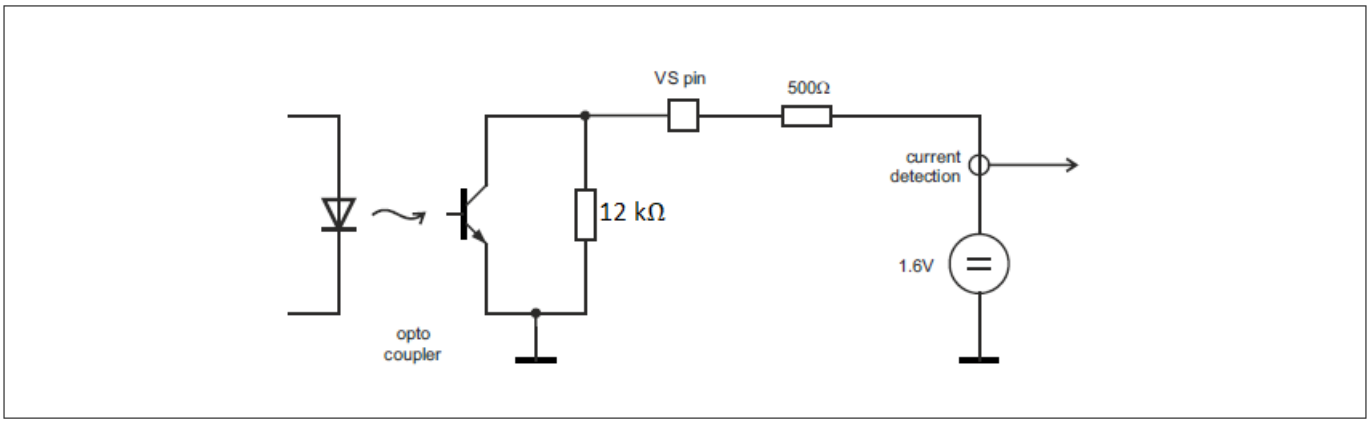


Figure 9 *VS* pin load current sensing based on secondary side regulation

3.7 Operating modes

In RUN state, ICL8830 operates in either QRM with valley switching or burst mode.

Quasi-resonant mode (QRM)

QRM maximizes the efficiency and minimizes the EMI by turning on the power switch at the drain voltage valley.

ICL8830 controls the on-time and valley number in QRM. When the valley number changes, the controller compensates the QRM on-time to achieve a relatively constant power transfer for a smooth transition.

Figure 10 areas highlighted in blue show the on-time compensation effect (in zig-zag pattern) when, for example, the QRM valley number is increased from 1 to 2, from 2 to 3, and from 3 to 4. When the relative power is further decreased, the on-time compensation continues at higher valley changing position (in smaller zig-zag), until it reaches the maximum valley number of 32. To ensure the QRM switching frequency reduction stays above the audible range, the QRM off-time is limited to a maximum value of t_{Off} (47 µs typ.).

Increasing the ICL8830 valley number ensures that the system-dependent QRM remains below a certain limit, to achieve a high efficiency and low EMI spectrum over a wide operating range.

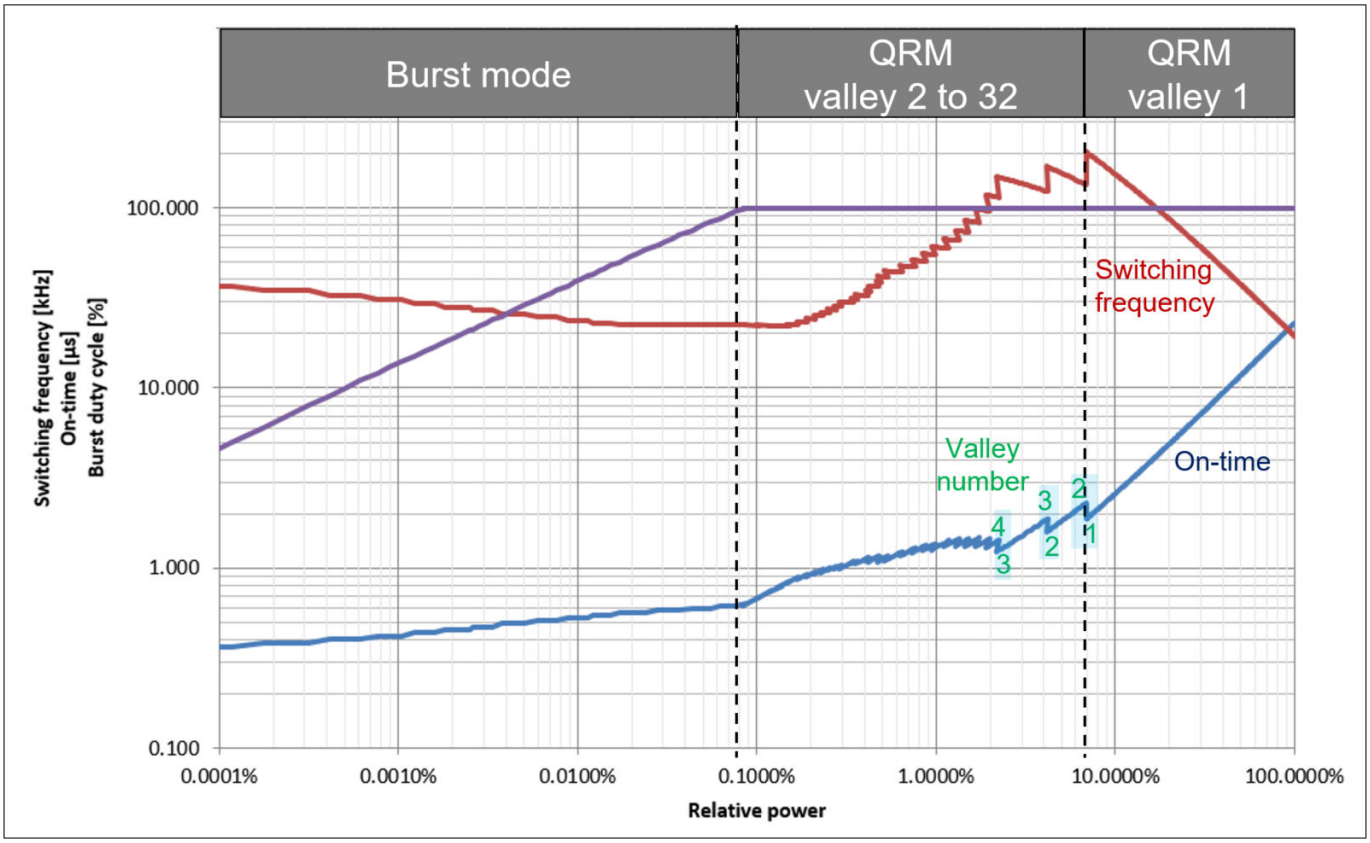


Figure 10 Exemplary switching characteristics versus relative power, with on-time compensation for valley changing

Burst mode

Burst mode transfers lesser power than QRM, to support light loads and no load/standby operation.

To achieve a low standby power, the controller sleeps during burst pause, to reduce its current consumption. In addition, the controller operates in burst mode with a reduced gate driver voltage level of V_{GDred} (7 V typ.), to minimize the gate charge loss.

The controller wakes up at a regular repetition frequency $f_{wake,reg}$, to do the burst pulsing based on the measured *VS* pin load current signal, and goes to sleep during burst pause, as shown in Figure 11.

$f_{wake,reg}$ is approximately four times the last synced input line frequency. For example, $f_{wake,reg}$ is around 240 Hz, if the last synced input line frequency is 60 Hz.

***Note**: In case of non-line-syncing happened before entering the burst mode, $f_{wake,reg}$ = 200 Hz typ. is applied. For example, non-line-syncing can happen when the system is supplied with a DC input or when the VS pin load current ripple is very small at low load.*

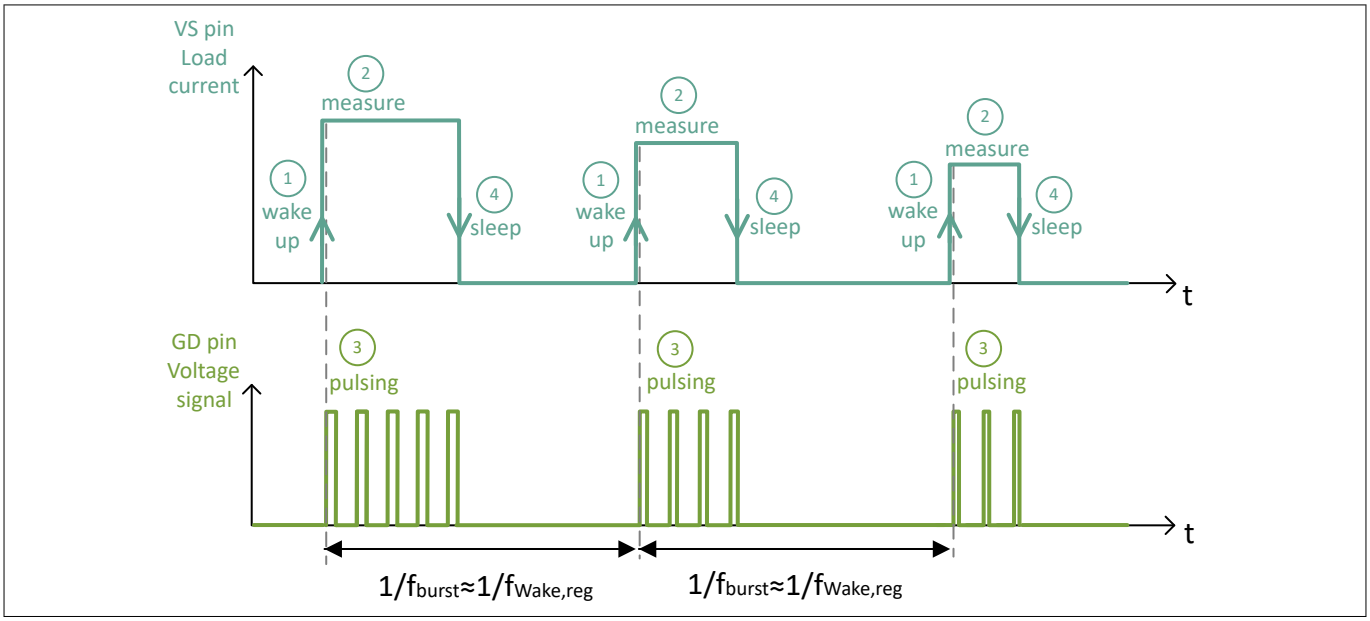


Figure 11 Illustration of burst mode with regular wake-up interval

To maintain sufficient V_{VCC} in burst mode, the controller operates with the following two mechanisms:

- Instead of waking up based on the regular $f_{wake,reg}$, a higher priority *VCC* wake-up threshold can trigger a burst start if V_{VCC} drops to $V_{VCCwake}$ (7.6 V typ.). The controller continues the burst pulsing until V_{VCC} = $V_{VCCburst}$ (8.1 V typ.).
- The *TD* pin internal pull-up resistor is disabled when V_{VCC} drops to $V_{VCCwake}$, to allow an external start-up circuit to charge V_{VCC} to $V_{VCCburst}$.

As a result, the burst cycle $1/f_{burst}$ does not necessarily follow $1/f_{wake,reg}$, as shown in Figure 11. The burst cycle can be extended by an integer times of $1/f_{wake,,reg}$ in case of a burst pulse skipping, or can be reduced by a portion of $1/f_{wake,reg}$ in case of a *VCC* wake-up burst triggering, or from a combination of both effects.

Attention**: **The VCC wake-up burst control mechanism is intended to work with the VCC voltage supply via the ZCD winding. In case of the VCC voltage is supplied via a winding voltage, which follows a certain ratio of the primary bus voltage, it is a must to ensure that the VCC voltage during burst mode is always higher than $V_{VCCburst}$ maximum value (9.1 V maximum) by a sufficient margin, especially when the input voltage is low and close to brownout level, so that the VCC wake-up burst mechanism can be avoided, to achieve a good output regulation.

3.8 Pulse generation

In RUN state, the ICL8830 maps the measured *VS* pin load current to the virtual pulse length, valley number and burst duty cycle, as shown in Figure 12.

These internal parameters are processed together with the power limitation, and fed to the pulse generation and correction function block, as shown in the Chapter 2.

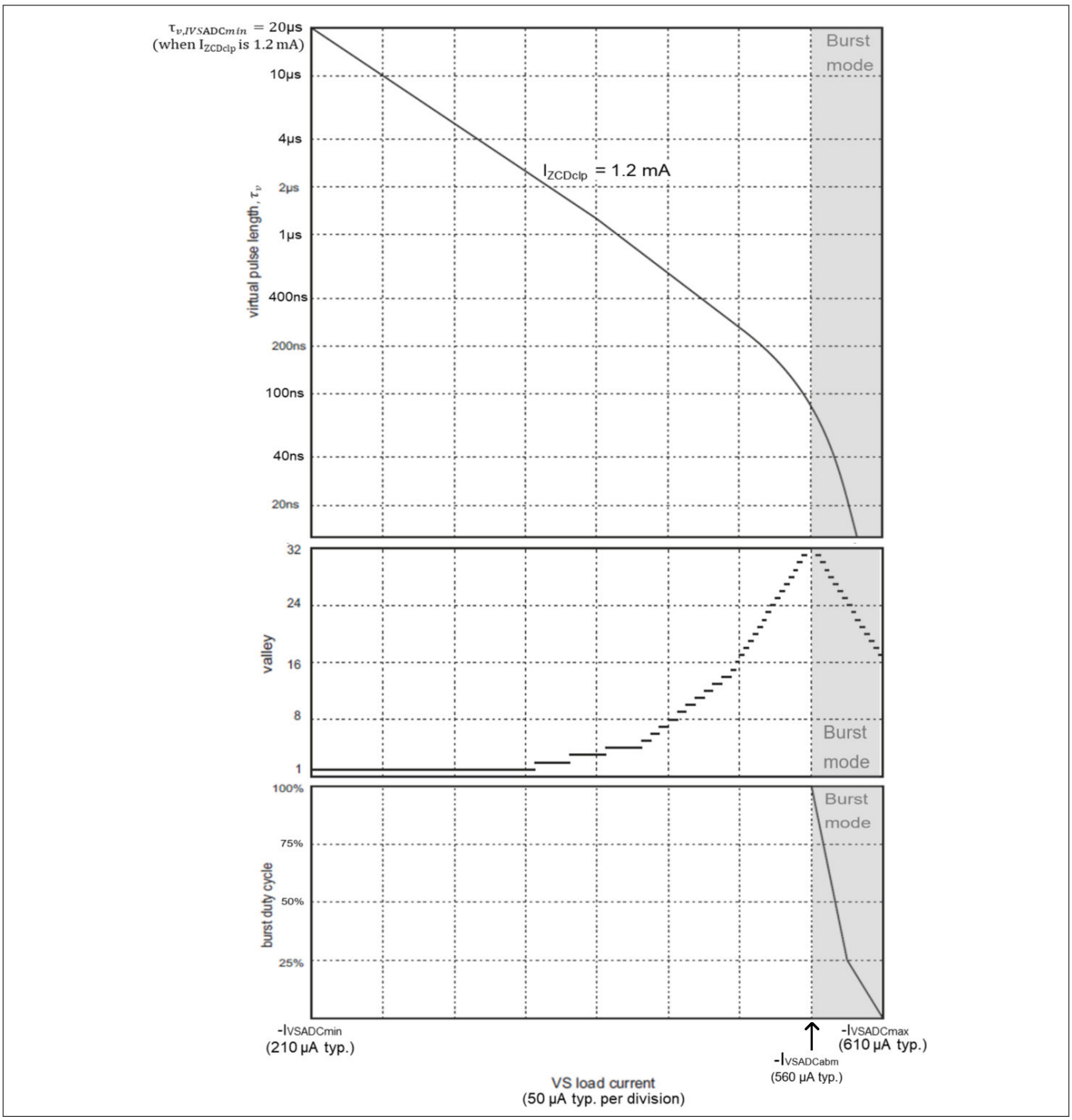


Figure 12 Virtual pulse length mapping (based on I_{ZCDclp} = 1.2 mA as an example), valley number mapping and burst mode mapping

Virtual pulse length mapping and its use case

The virtual pulse length mapping is an illustrative on-time mapping which excludes:

- the system-dependent on-time compensation effect for valley number change (see Figure 10)
- the on-time extension effect for THD correction (see Figure 8)
- the power limiting effect on the maximum on-time (to be explained in this chapter)
- the minimum gate pulse length limit by the pulse generation block

The virtual pulse length mapping shown in Figure 12 is not static.

It shifts vertically based on the *ZCD* pin peak to peak settled clamping current I_{ZCDclp}, which is dependent on the R_{ZCD}, transformer winding turns ratio, operating input and output voltages.

As shown in Figure 13, a different I_{ZCDclp} level leads to a change on the virtual pulse length at every valley-changing position, including the burst mode entry position. It means when the input voltage is lower or when R_{ZCD} value is increased for example, a decrease of I_{ZCDclp} leads to the relative on-time decrease at every valley-changing position, including the burst mode entry position. And vice-versa.

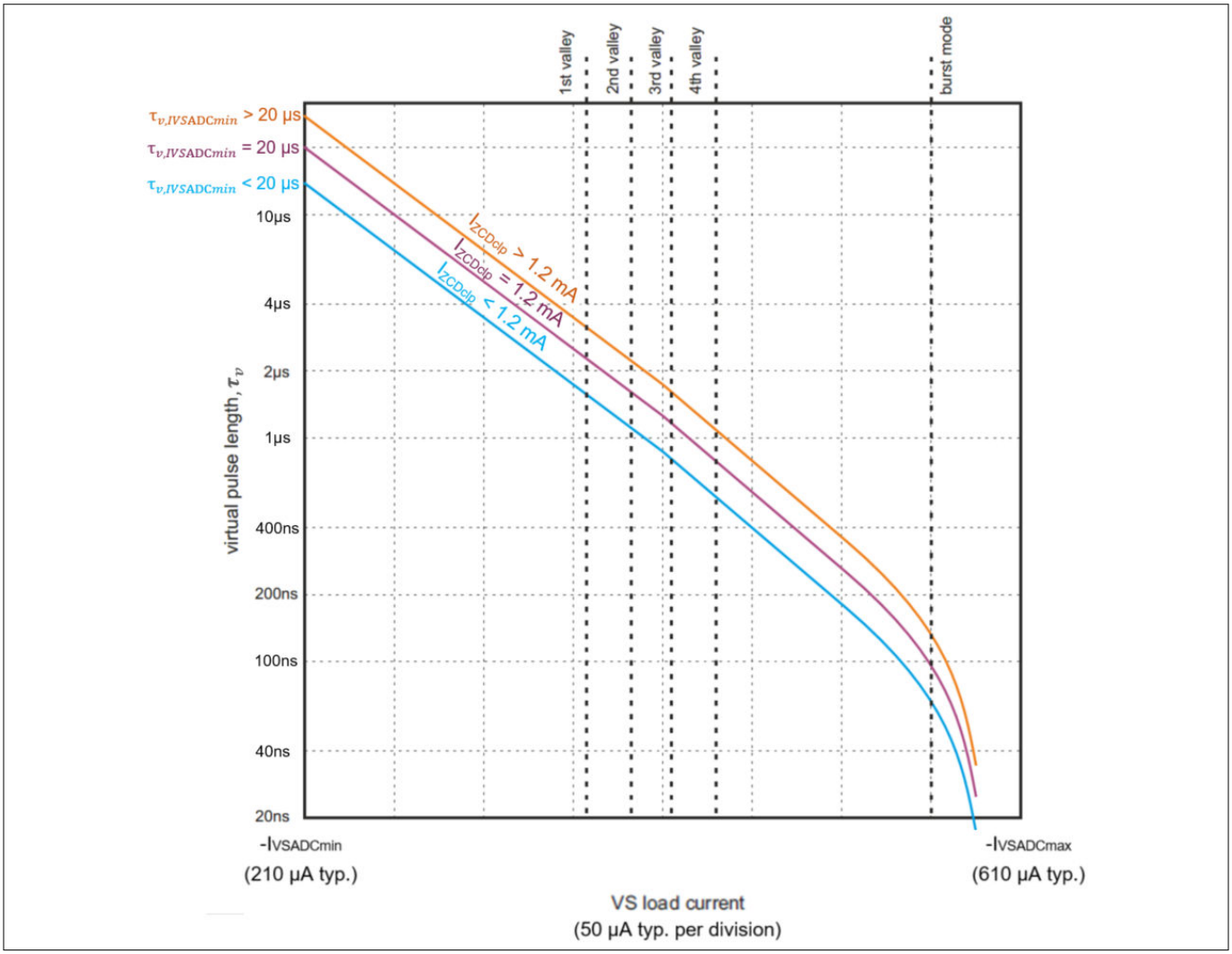


Figure 13 Effect of I_{ZCDclp} change on the virtual pulse length mapping

As an example, the virtual pulse length mapping based on I_{ZCDclp} = 1.2 mA in Figure 13 is derived based on the following steps:

1. Based on I_{ZCDclp} = 1.2 mA, obtain $\tau_{v,IVSADCmin}$ = 20 µs from Figure 14.
2. Mark $\tau_{v,IVSADCmin}$ = 20 µs on the y-axis, and take it as the starting point for the virtual pulse length mapping curve plot, which is relatively well exponential in the range from 20 µs to 1 µs, with a halving of the pulse length per 50 µA *VS* pin load current increase.

For example, another practical use case of the virtual pulse length mapping is to estimate the minimum on-time of the QRM 1st valley switching (approximately 10% of $\tau_{v,IVSADCmin}$), to estimate the system maximum switching frequency.

***Note**: When the valley number is higher than 1 in QRM, or when in burst mode, the virtual pulse length mapping value should not be taken directly as the estimated on-time, since it excludes the on-time compensation effect for valley number change.*

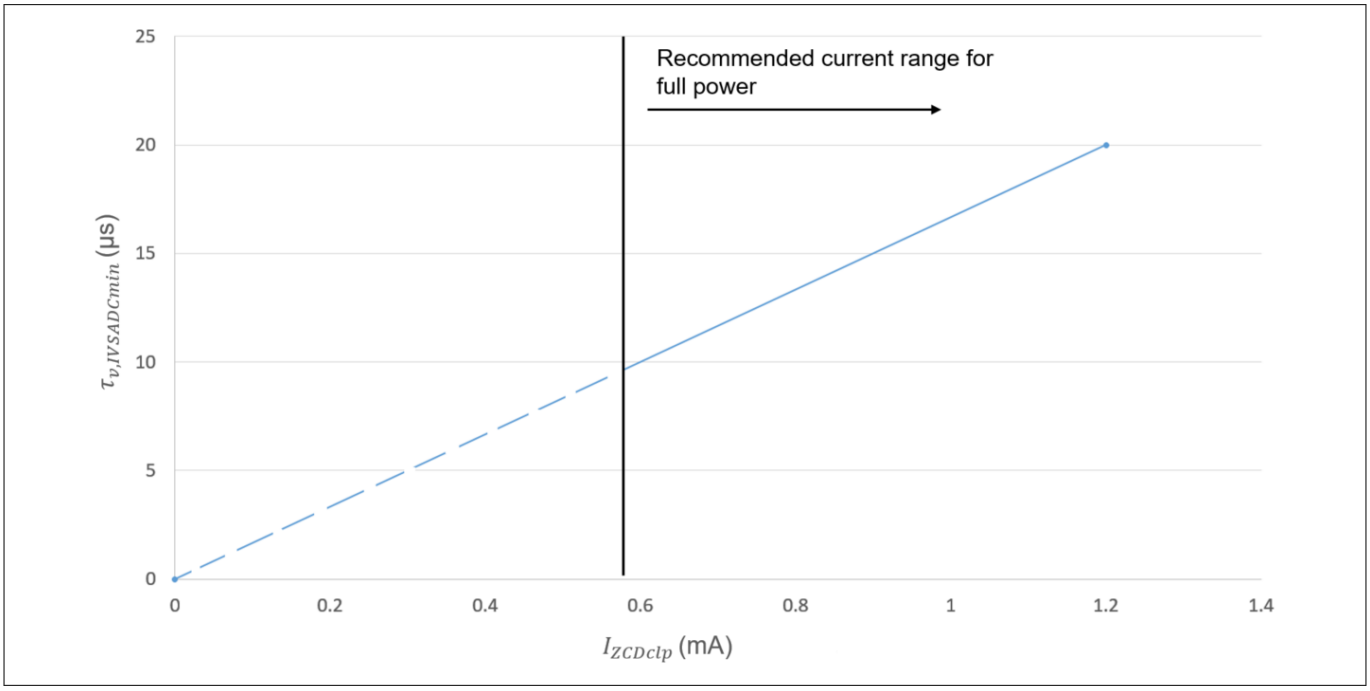


Figure 14 Virtual pulse length at $I_{VSADCmin}$, $\tau_{v,IVSADCmin}$ versus *ZCD* peak to peak settled clamping current, I_{ZCDclp}

Power-limitation and maximum on-time

The ICL8830 power limitation features limit the maximum on-time $t_{ON,max}$ based on:

$$t_{ON,\max} \approx \tau_{v,IVSADC\min} \cdot \min\left[1, \frac{1}{2^{3.058 \cdot \ln\left(\frac{V_{VIN,avg}}{0.4}\right) - 1.25}}\right] \quad (5)$$

For $t_{ON,max}$ estimation, it is important to note that $\tau_{v,IVSADCmin}$ changes with different $V_{VIN,avg}$ level, when the input voltage detection circuit in Figure 6 is applied. This is because $\tau_{v,IVSADCmin}$ is scaled depending on I_{ZCDclp} in Figure 14, while I_{ZCDclp} is dependent on the input voltage, as explained in ZCD pin signal sensing.

$t_{ON,max}$ is applied when the *VS* pin load current is $I_{VSton,sat}$ or lower, where $I_{VSton,sat}$ can be estimated based on:

$$-I_{VSton,sat} \approx -I_{VSADC\min} + \max\left[0,\ 152.9 \cdot \ln\left(\frac{V_{VIN,avg}}{0.4}\right) - 62.5\right] \cdot 10^{-6} \quad (6)$$

Figure 15 shows the virtual pulse length with the power limiting maximum on-time effect, when $V_{VIN,avg}$ is 0.65 V, 1.0 V, 1.5 V and 1.9 V, respectively.

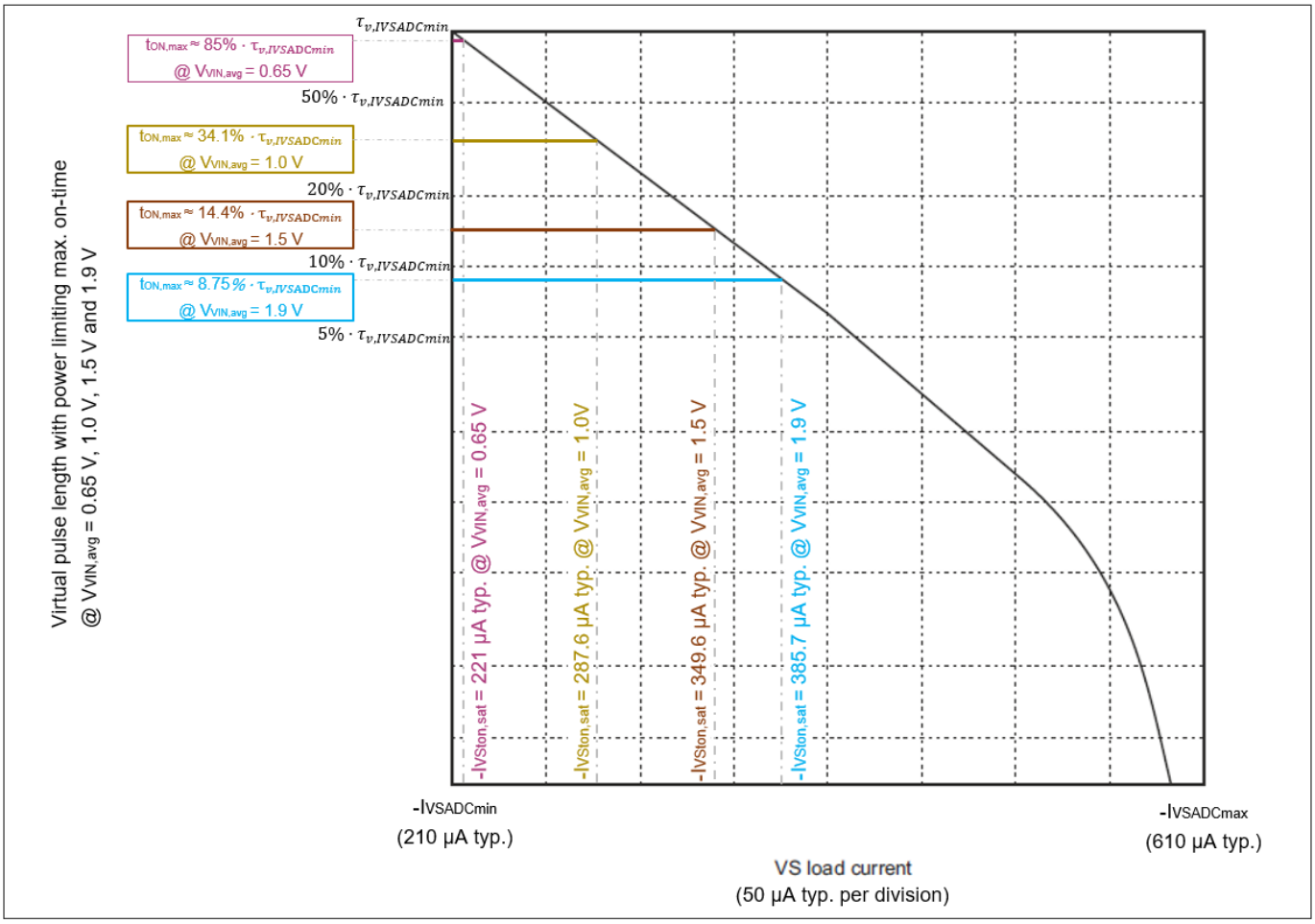


Figure 15 Virtual pulse length mapping with power limiting maximum on-time effect

When $V_{VIN,avg}$ is in the range from the brownout level (0.44 V typ.) to approximately 0.6 V, the power limitation is disabled, where $t_{ON,max} = \tau_{v,IVSADCmin}$.

When $V_{VIN,avg}$ is at the brownin level (V_{BI} = 0.65 V typ.), the power limitation is enabled with $t_{ON,max}$ = 85% of $\tau_{v,IVSADCmin}$, as shown in Figure 15. For example, if the desired $t_{ON,max}$ at brownin level is 17 µs typ., it is necessary to have $\tau_{v,IVSADCmin}$ = 17 µs / 85% = 20 µs. And, according to Figure 14, $\tau_{v,IVSADCmin}$ = 20 µs is obtained when I_{ZCDclp} =1.2 mA is applied. As a result, to achieve $t_{ON,max}$ = 17 us typ. at brownin level, R_{ZCD} should be dimensioned to produce I_{ZCDclp} = 1.2 mA typ. at brownin level.

Valley number and burst duty cycle

The valley number and burst duty cycle mappings based on *VS* pin load current are shown in Figure 12. The burst duty cycle refers to the ratio of the burst pulsing duration to burst cycle time. $-I_{VSADCabm}$ (560 µA typ.) marks the boundary between QRM and burst mode.

In QRM, the mapped valley number is not necessarily taken directly or immediately as the *ZCD* pin valley-count number, for the pulse generation. The update of the *ZCD* pin valley-count number is done based on the following valley selection hysteresis mechanism:

1. To minimize the multiple valley changes within one AC half cycle, ICL8830 updates the *ZCD* valley-count number once every AC half cycle, based on the lowest mapped valley number from the last AC half cycle, as shown in Figure 16. During each AC half cycle, the controller adjusts the on-time to stay in the selected valley number. In this way, the number of valley jumps is limited to a minimum.
2. When a load jump happens, if the valley number has to be decreased, it happens immediately. For the case of valley number increase, if the load jump results to a valley number increase by 10 or more, it happens immediately. Otherwise, the change happens only at the start of the next AC half cycle, as shown in Figure 16.

***Note**: If the selected ZCD valley-count number cannot happen before the maximum off-time t_{off} (47 µs typ.) is reached, the pulse generation will be based on t_{off}, instead of the selected ZCD valley counting number.*

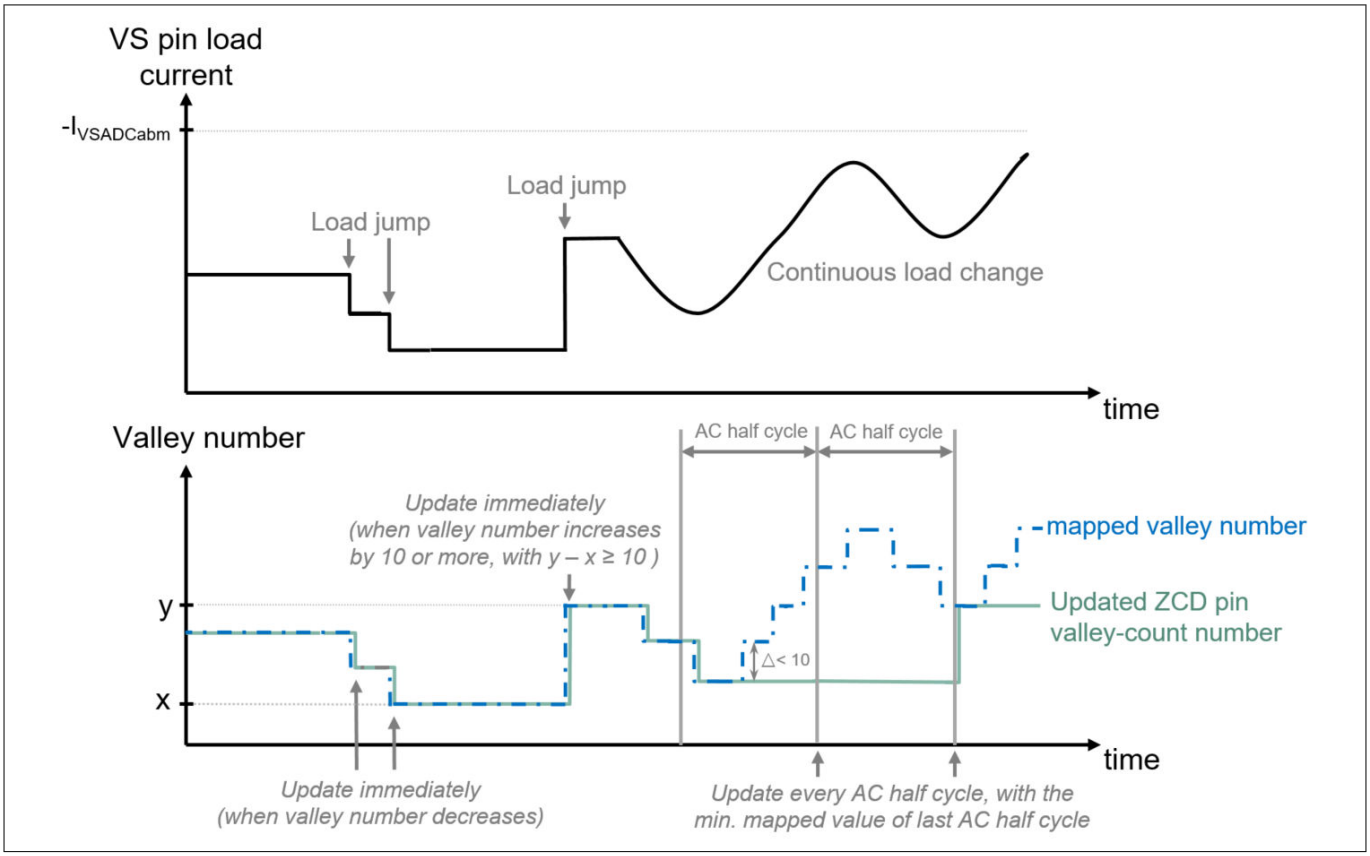


Figure 16 Illustrative example of the QRM valley selection hysteresis mechanism

***Note**: If the AC half cycle period cannot be synced, for example when the input voltage is DC, or when the VS pin load current ripple is very small , the regular valley update cycle will be based on either approximately 10 ms, or the last synced AC half cycle period.*

In burst mode, the controller measures the *VS* load current at a regular wake-up interval, and applies the mapped valley number immediately as the *ZCD* pin valley-count number for the burst switching pulse generation. Also, the mapped burst duty cycle is taken immediately to determine the burst pulsing duration, as shown in Figure 11. If the measured *VS* load current is $-I_{VSADCmin}$ (610 µs typ.) or more, the burst pulsing is skipped.

Instead of waking up based on the regular interval, a higher priority *VCC* wake-up threshold can trigger a burst start if V_{VCC} drops to $V_{VCCwake}$ (7.6 V typ.). In case of *VCC* wake-up burst being triggered, the burst pulsing duration depends on the time needed to charge the V_{VCC} from $V_{VCCwake}$ to $V_{VCCburst}$ (8.1 V typ.).

Attention**: **The VCC wake-up burst control mechanism is intended to work with the VCC voltage supply via the ZCD winding. In case of the VCC voltage is supplied via a winding voltage, which follows a certain ratio of the primary bus voltage, it is a must to ensure that the VCC voltage during burst mode is always higher than $V_{VCCburst}$ maximum value (9.1 V maximum) by a sufficient margin, especially when the input voltage is low and close to brownout level, so that the VCC wake-up burst mechanism can be avoided, to achieve a good output regulation.

Burst mode regular wake-up interval and burst cycle time

Refer to the burst mode section in the Operating modes chapter.

3.9 Primary side overcurrent protection

The primary side overcurrent protection level 1 (OCP1) is performed by means of the cycle-by-cycle peak current limitation. An internal leading edge blanking t_{LEB} (160 ns typ.) prevents false triggering of this protection due to a leading edge spike. If the measured *CS* pin voltage exceeds V_{OCP1} (0.61 V typ.) for more than t_{LEB} (160 ns typ.), the protection is triggered and the *GD* pin output is pulled low for that switching cycle.

The primary side overcurrent protection level 2 (OCP2) is meant for covering fault conditions like a short in the transformer primary winding or transformer core saturation. In this case, the OCP1 does not limit properly the peak current due to the very steep slope of the peak current. If the measured *CS* pin voltage with an initial level of at least V_{OCP1} reaches V_{OCP2} (1.21 V typ.) or more within the time window of t_{OCP2} (150 ns typ.), the OCP2 protection is triggered.

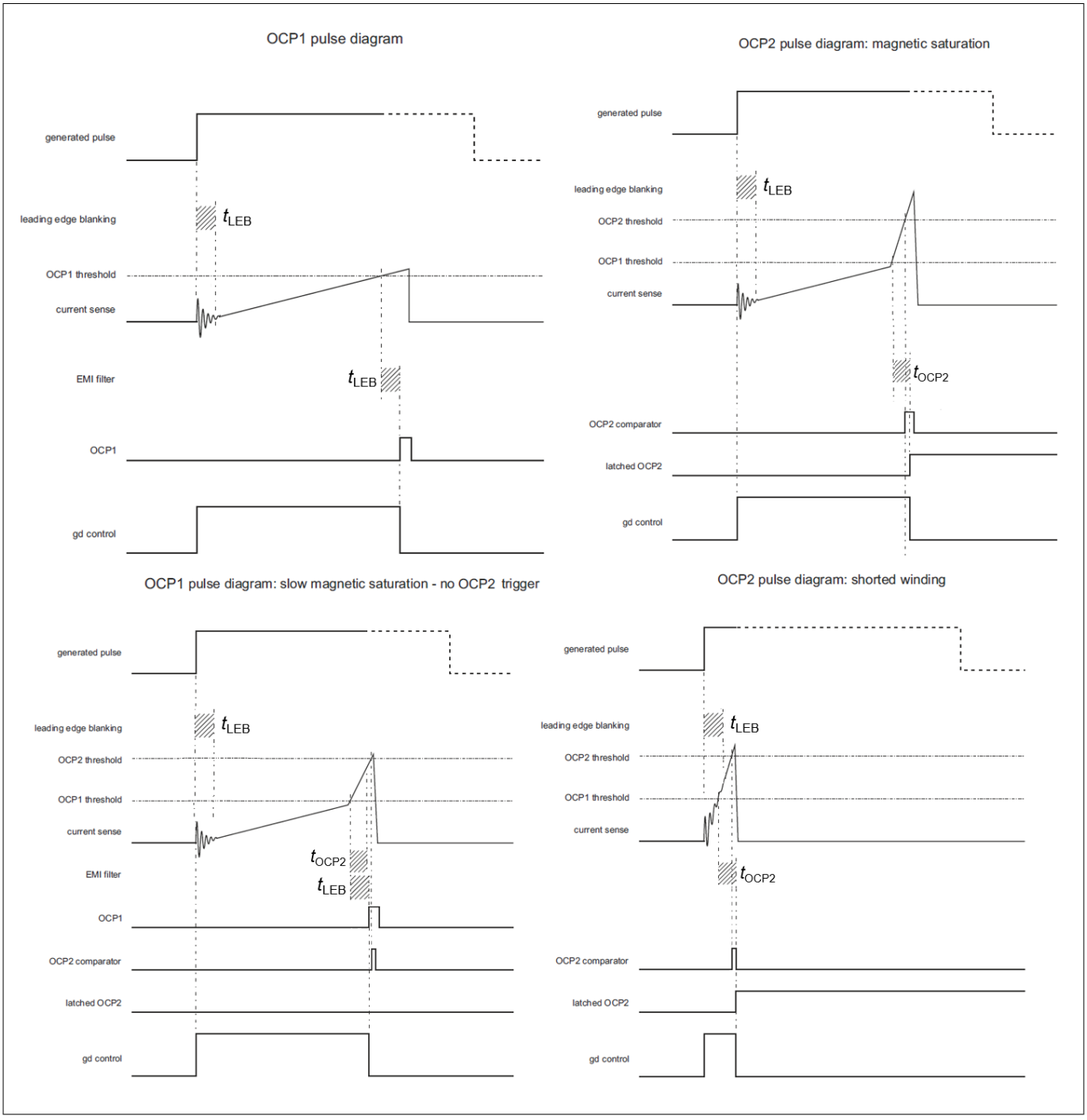


Figure 17 Timing overview of the OCP1 and OCP2

3.10 VCC voltage protections

An UVLO is implemented to activate and deactivate the controller depending on the supply voltage on the *VCC* pin. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} (12.5 V typ.) for activating the controller and V_{VCCmin} (6.6 V typ.) for deactivating the controller.

When the controller is not active, the current consumption is $I_{VCCstart}$ (30 µA typ.).

If the voltage on *VCC* pin reaches $V_{VCCclamp}$ (24.2 V typ.) during start-up, restart and in the burst pause, the controller is able to sink up to $I_{VCCclamp}$ (2.5 mA typ.). The *VCC* overvoltage protection is implemented based on a threshold of V_{VCCmax} (25 V typ.).

VCC wake-up burst

To maintain sufficient V_{VCC} in burst mode, the controller operates with the following two mechanisms:

- The *VCC* wake-up threshold can trigger a burst start if V_{VCC} drops to $V_{VCCwake}$ (7.6 V typ.). The controller continues the burst pulsing until $V_{VCC} = V_{VCCburst}$ (8.1 V typ.).
- The *TD* pin internal pull-up resistor is disabled when V_{VCC} drops to $V_{VCCwake}$, to allow an external start-up circuit to charge V_{VCC} to $V_{VCCburst}$.

Attention**: **The VCC wake-up burst control mechanism is intended to work with the VCC voltage supply via the ZCD winding. In case of the VCC voltage is supplied via a winding voltage, which follows a certain ratio of the primary bus voltage, it is a must to ensure that the VCC voltage during burst mode is always higher than $V_{VCCburst}$ maximum value (9.1 V maximum) by a sufficient margin, especially when the input voltage is low and close to brownout level, so that the VCC wake-up burst mechanism can be avoided, to achieve a good output regulation.

3.11 Flyback output overvoltage protection

During the transformer demagnetization time, the *ZCD* pin positive peak settled current $I_{ZCDpclp}$ is internally converted to a current flowing out of the *CS* pin with the conversion ratio n_{ZCDOVP}. The *CS* pin voltage level at this time is therefore approximately the multiplication of this out-flowing current and the *CS* pin resistance to ground. If this voltage level exceeds the V_{OCP1} threshold (0.61 V typ.) for more than a blanking time, the flyback OVP is triggered.

Since the *CS* pin series resistor value is very much greater than the primary MOSFET current shunt resistor value, the flyback output OVP level can be adjusted based on the *CS* pin series resistance.

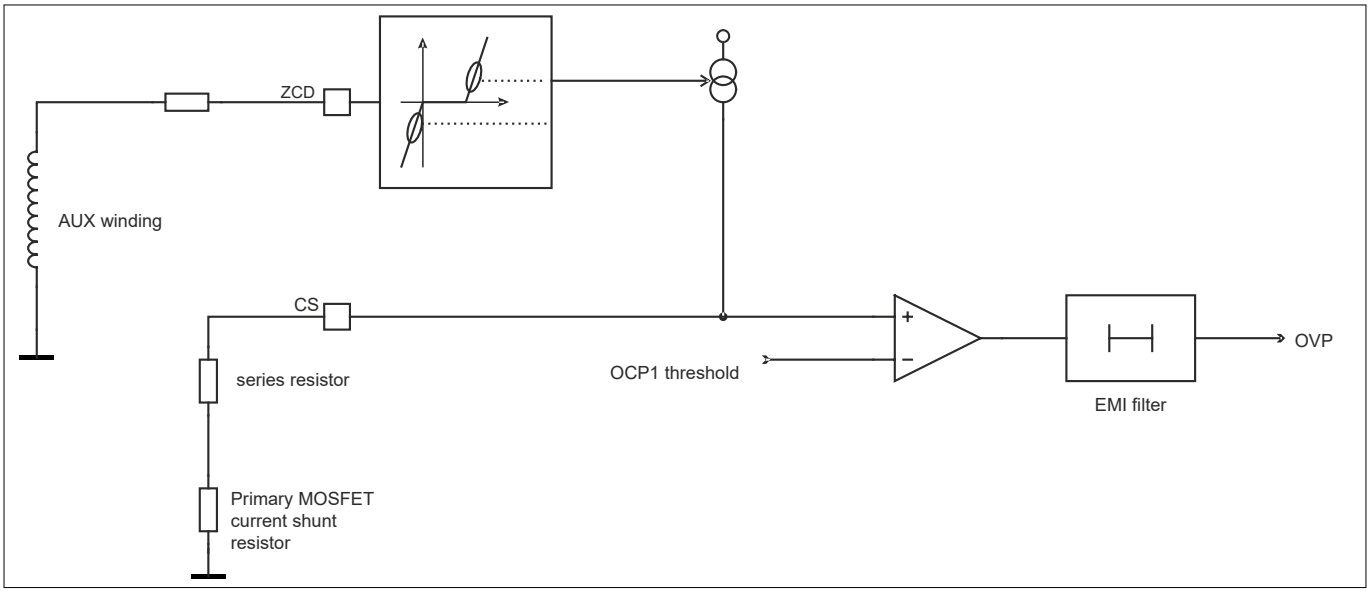


Figure 18 Flyback secondary output OVP

Due to this protection, the voltage on *CS* pin is not zero during the transformer demagnetization, but mirrors the reflected output voltage.

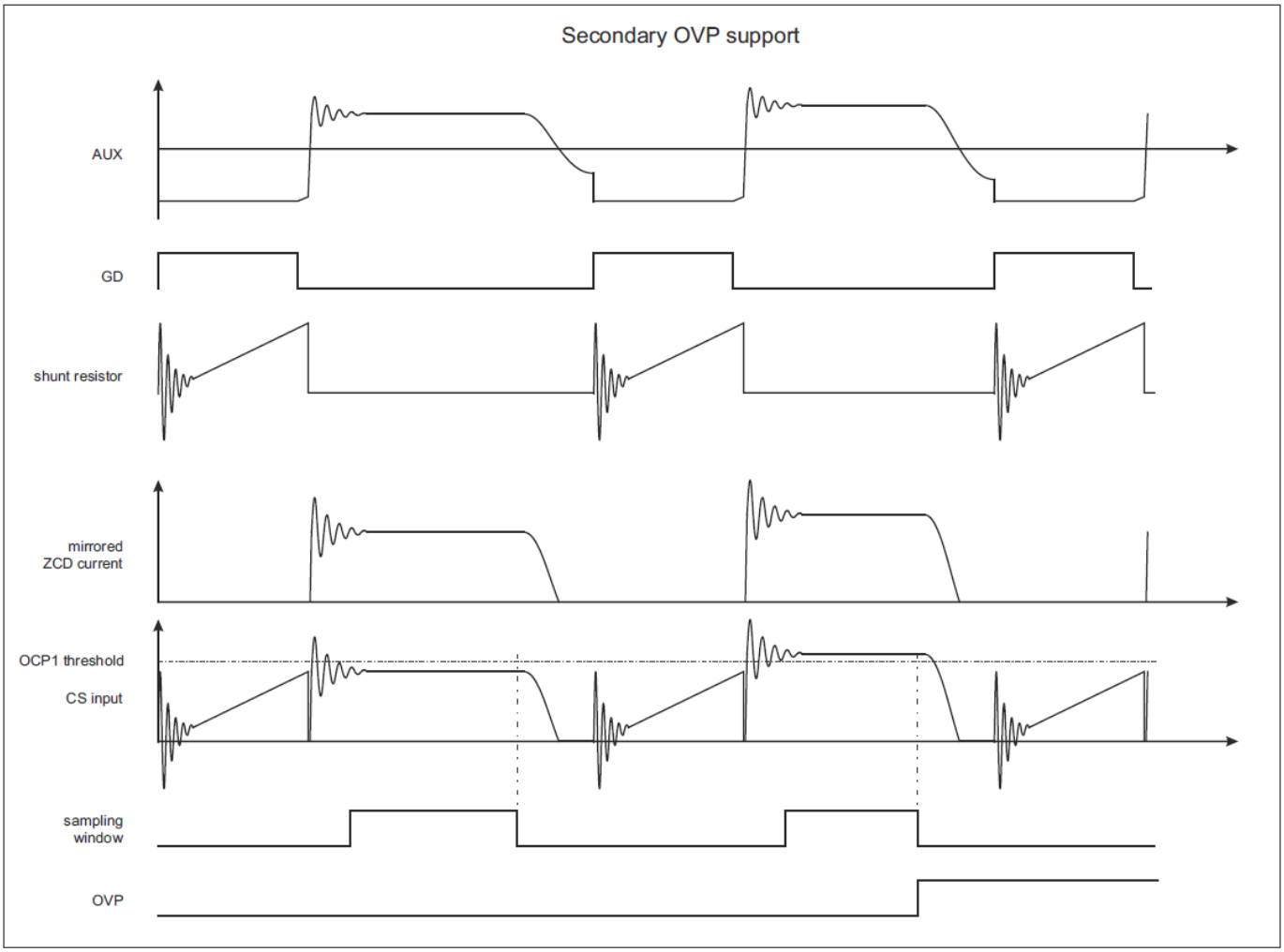


Figure 19 Flyback CS waveform

3.12 Overtemperature protection

ICL8830 offers an overtemperature protection using an internal temperature sensor. The overtemperature protection is triggered when internal junction temperature T_j reaches *T* (130°C typ.).

3.13 Open loop protection

An open feedback loop results in maximum power transfer after the soft start. The flyback output overvoltage protection can be triggered once the overvoltage threshold is exceeded for longer than the related blanking time. This causes an auto-restart.

In the case of an open *VS* pin, due to the *VS* pin sourcing a current of $-I_{VSBias}$ (1 µA typ.) out of the controller during normal operation, the *VS* pin voltage rises. The *VS* pin voltage is compared to the overvoltage comparator threshold $V_{VSOVOFFFB}$ (2.7 V typ.). If the voltage exceeds the threshold for longer than the related blanking time, the *VS* pin overvoltage protection blocks any switching. A reset may occur if the *VCC* voltage drops below V_{VCCmin}.

3.14 State flow chart and fault reaction

Flow chart

Figure 20 shows the different states of the IC and the conditions to change the state.

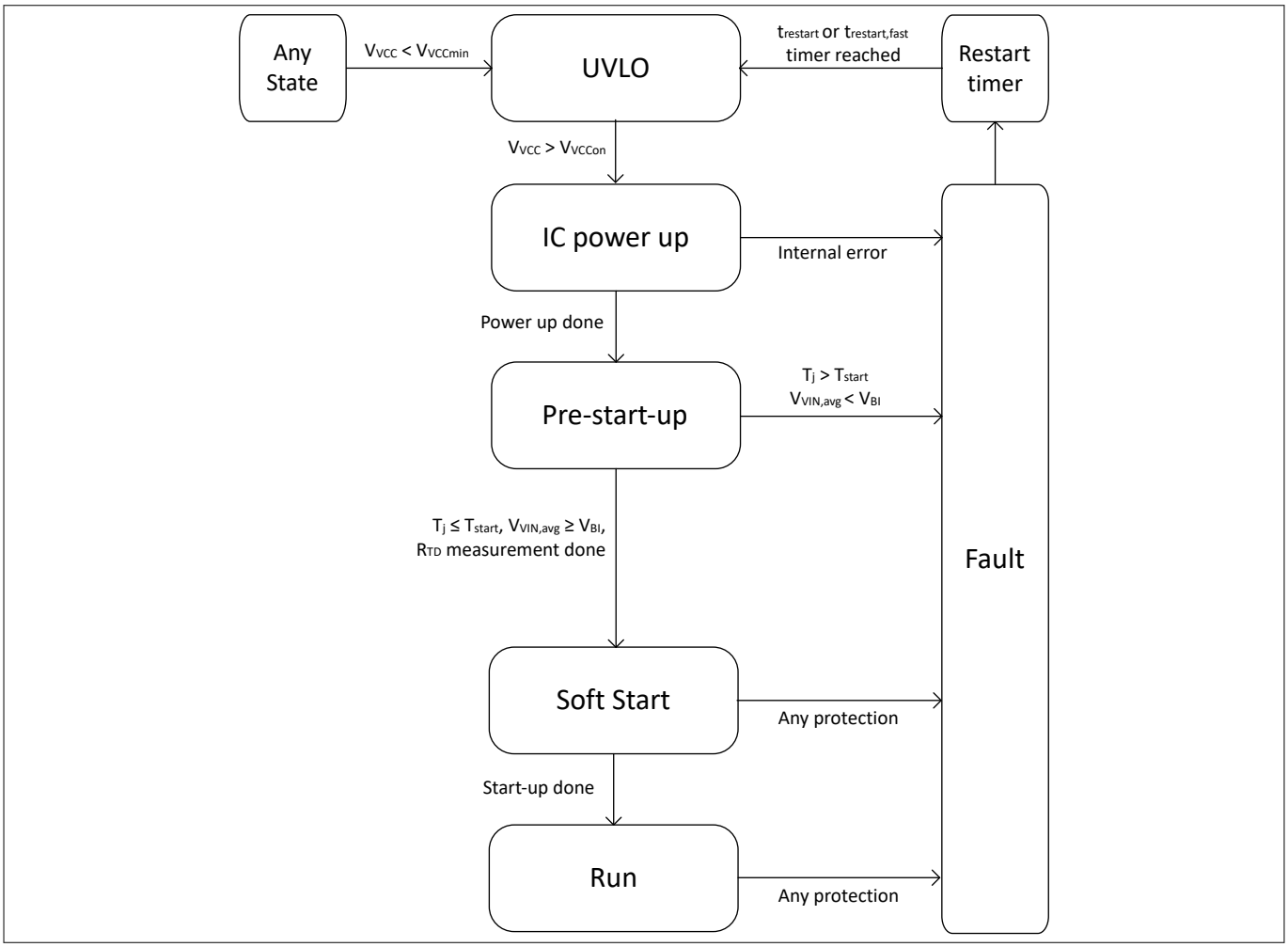


Figure 20 State flow chart

Fault reaction

The controller handles protections as listed in Table 2.

***Note**: Some blanking times vary slightly with the line frequency.*

Table 2 Fault matrix

Fault	Detection	Typical blanking time	State			Reaction
			Pre-start-up	Soft start	Run	
Insufficient supply	$V_{VCC} < V_{VCCon}$	1 µs	X	-	-	Wait in reset
Insufficient supply	$V_{VCC} < V_{VCCmin}$	1 µs	X	X	X	Reset
VCC overvoltage	$V_{VCC} > V_{VCCOVP}$	1 µs	-	X	X	Auto-restart after $t_{restart}$
VIN short protection	$V_{VIN} < V_{VINshort}$	1 µs	-	X	X	Auto-restart after $t_{restart}$
Brownin protection	$V_{VIN,avg} < V_{BI}$	2 ms	X	-	-	Fast auto-restart after $t_{restart,fast}$
Brownout protection	$V_{VIN,avg} < (V_{BI}\text{-}\Delta V_{BI\text{-}BO})$	2 ms	-	X	X	Auto-restart after $t_{restart}$
VIN overvoltage protection	$V_{VIN,avg} > V_{VINOV}$	2 ms	-	X	X	Auto-restart after $t_{restart}$
Overcurrent protection (OCP1)	$V_{CS} > V_{OCP1}$	t_{LEB}	-	X	X	Turn off gate driver for the on-going switching cycle
Overcurrent protection (OCP2)	$V_{CS} > V_{OCP2}$	t_{OCP2}	-	X	X	Auto-restart after $t_{restart}$
Flyback output overvoltage protection	$I_{ZCDpclp} * n_{ZCDOVP} > V_{OCP1}$	100 µs	-	X	X	Auto-restart after $t_{restart}$
Overtemperature	$T_j > T$ or $T_j > T_{start}$	18 µs	X	X	X	Auto-restart after $t_{restart}$
VS overvoltage	$V_{VS} > V_{VSOVOFFFB}$	20 µs	-	X	X	Turn off gate driver and restart if $V_{VS} < V_{VSOVONFB}$

3.15 Adjustable functions

Some features of the controller can be adjusted using external circuitry:

- The maximum power/on-time/operating point can be configured using the *ZCD* pin series resistance to the ZCD/auxiliary winding
- The flyback output overvoltage protection can be configured using the *CS* pin series resistance to the primary MOSFET current shunt resistor.
- Brownin and brownout protection and the related input overvoltage protection
- Primary side overcurrent protection

4 Electrical characteristics and parameters

All signals are measured with respect to the ground pin, *GND*. The voltage levels are valid provided that other ratings are not violated.

4.1 Absolute maximum ratings

***Note**: Absolute maximum ratings are defined as ratings, which if exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.*

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC voltage	V_{VCC}	-0.5	–	26	V	
Junction temperature	T_j	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	
Soldering temperature	T_S	–	–	260	°C	Wave soldering according to JESD22-A111 Rev A.
Thermal resistance junction to ambient	R_{ThJA}	–	–	185	K/W	
Power dissipation at 50°C	P_D	–	–	0.5	W	
ESD capability HBM	V_{ESD}	–	–	2	kV	ESD-HBM according to ANSI/ESDA/JEDEC JS-001.
ESD capability CDM	V_{ESD}	–	–	500	V	ESD-CDM according to ANSI/ESDA/JEDEC JS-002.
GD voltage	V_{GD}	-0.5	–	V_{VCC} + 0.3	V	
CS voltage	V_{CS}	-0.5	–	3.6	V	
CS current	I_{CS}	-2	–	2	mA	
ZCD voltage	V_{ZCD}	-1.2	–	3.6	V	
ZCD current	I_{ZCD}	-4	–	4	mA	
VS voltage	V_{VS}	-0.3	–	3.6	V	
VIN voltage	V_{VIN}	-0.3	–	3.6	V	
TD voltage	V_{TD}	-0.3	–	3.6	V	

4.2 Operating conditions

The recommended operating conditions are shown for which the DC electrical characteristics are valid.

Table 4 Operating characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Junction temperature	T_J	-40	–	T	°C	
Supply voltage	V_{VCC}	$V_{VCCburst}$	–	23	V	
External capacitance at the *TD* pin	C_{TD}	–	–	1	nF	

4.3 DC electrical characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range. Devices are tested in production at T_A = 25°C. Values have been verified either with simulation models or by device characterization up to 125°C. Typical values represent the median values related to T_A = 25°C.

All voltages refer to *GND*, and the assumed supply voltage is V_{VCC} = 15 V, if not otherwise specified.

4.3.1 Power supply

Table 5 Power supply characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC turn-on threshold	V_{VCCon}	12.0	12.5	13.1	V	
Start-up current	$I_{VCCstart}$	–	30	–	µA	
Supply current	I_{CC}	–	2.0	–	mA	IC self-supply excluding gate currents.
Supply current during burst pause	$I_{CCburst}$	–	220	–	µA	
Supply current in protection mode	$I_{CCrestart}$	–	40	–	µA	
VCC undervoltage threshold	V_{VCCmin}	6.0	6.6	7.6	V	
VCC wake-up threshold	$V_{VCCwake}$	6.6	7.6	8.8	V	
VCC burst threshold	$V_{VCCburst}$	7.1	8.1	9.1	V	
Difference between $V_{VCCwake}$ and $V_{Vccburst}$	V_{delta}	500	–	–	mV	
VCC overvoltage threshold	V_{VCCmax}	23.8	25	26.4	V	
VCC clamp voltage	$V_{VCCclamp}$	–	24.2	–	V	
VCC clamp current	$I_{VCCclamp}$	–	2.5	–	mA	

4.3.2 Zero crossing detection

Table 6 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Zero crossing threshold (falling edge)	$V_{ZCDDown}$	10	45	–	mV	
Zero crossing threshold (rising edge)	V_{ZCDUp}	–	55	90	mV	
Clamping of positive voltages	$V_{ZCDpclp}$	400	550	700	mV	$I_{ZCDSink}$ = 1 mA
Clamping of negative voltages	$V_{ZCDnclp}$	-600	-500	-400	mV	$I_{ZCDSource}$ = - 1 mA
ZCD ringing suppression time	$t_{Ringsup}$	350	700	1100	ns	
ZCD to GD delay	t_{ZCDGD}	–	270	–	ns	R_{TD} = 18 kΩ
ZCD to *CS* current ratio for flyback secondary side OVP	n_{ZCDOVP}	0.455	0.484	0.513		$I_{CSsource}$ / $I_{ZCDpclp}$ at 1.2 mA
ZCD to *CS* current ratio for flyback secondary side OVP	n_{ZCDOVP}	0.450	0.484	0.518		$I_{CSsource}$ / $I_{ZCDpclp}$ at 0.8 mA

4.3.3 Voltage sense

***Note**: R_{TD} limits from Table 9 apply for Table 7.*

Table 7 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VS bias current	- I_{VSBias}	0.5	1.0	1.5	µA	V_{VS} = V_{ref}.
Voltage source for optocoupler/ feedback supply	V_{VS}	1.56	1.6	1.63	V	Internal series resistance of 500 Ω.
VS current threshold for start up	- I_{VSsink}	102	130	154	µA	12 kΩ from VS to GND.
Open pin turn-off	$V_{VSOVOFFFB}$	2.64	2.7	2.76	V	
Voltage for restart after overvoltage turn-off	$V_{VSOVONFB}$	2.54	2.6	2.66	V	
ADC lower current limit	- $I_{VSADCmin}$	166	210	260	µA	For maximum on-time during operation.
ADC upper current limit	- $I_{VSADCmax}$	500	610	720	µA	For minimum on-time in burst mode.

4.3.4 Input voltage detection

Table 8 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VIN pin short to GND threshold	$V_{VINshort}$	150	200	250	mV	
VIN overvoltage threshold	V_{VINOV}	1.9	2.0	2.1	V	

4.3.5 TD configuration

Table 9 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Internal pull-up resistor for pre-start-up R_{TD} measurement	$R_{TD,flyback}$	32	40	48	kΩ	Internal voltage 3.3 V.
Internal pull-up resistor for RUN state and pre-start-up R_{TD} measurement	$R_{TD,RUN}$	8	10	12	kΩ	Internal voltage 3.3 V. Pull-up is disabled in burst mode if *VCC* wake-up is triggered from $V_{VCC} \leq V_{VCCwake}$, until V_{VCC} reaches $V_{VCCburst}$.
TD pin resistance to ground, for configuration and to activate *VS* pin load current sensing for output regulation	R_{TD}	18	–	68	kΩ	Internal voltage 3.3 V. Minimum value based on Internal pull-up resistor of $R_{TD,RUN}$. Maximum value based on internal pull-up resistor of $R_{TD,flyback}$. Measured in pre-start-up phase.

4.3.6 Current sense

Table 10 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
OCP1 turn-off threshold	V_{OCP1}	570	610	650	mV	
OCP1 leading-edge blanking time	t_{LEB}	–	160	–	ns	
OCP2 turn-off threshold	V_{OCP2}	1140	1210	1260	mV	
OCP2 trigger time	t_{OCP2}	–	150	–	ns	Pulse width when $V_{CS} > V_{OCP2}$
CS pull-up current	$-I_{CSPU}$	0.5	1	1.5	µA	

4.3.7 PWM generation

Table 11 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Repetition time	t_{Rep}	47	52	60	µs	V_{ZCD} = 0 V
Off-time	t_{Off}	42	47	52.5	µs	

4.3.8 Gate driver

Table 12 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
GD source current	$-I_{source}$	125	–	–	mA	
GD sink current	I_{sink}	250	–	–	mA	
GD peak voltage	V_{GDfull}	10.4	11.0	11.6	V	$V_{VCC} > (V_{GDfull} + 0.5\ V)$ and in QRM.
Reduced *GD* peak voltage	V_{GDred}	6.5	7.0	7.5	V	$V_{VCC} > (V_{GDred} + 0.7\ V)$, during start-up or burst mode.

4.3.9 Clock oscillators

Table 13 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Restart time	$t_{restart}$	–	200	–	ms	
Fast restart time	$t_{restart,fast}$	–	25	–	ms	Only for *VIN* under voltage (brownin protection) event

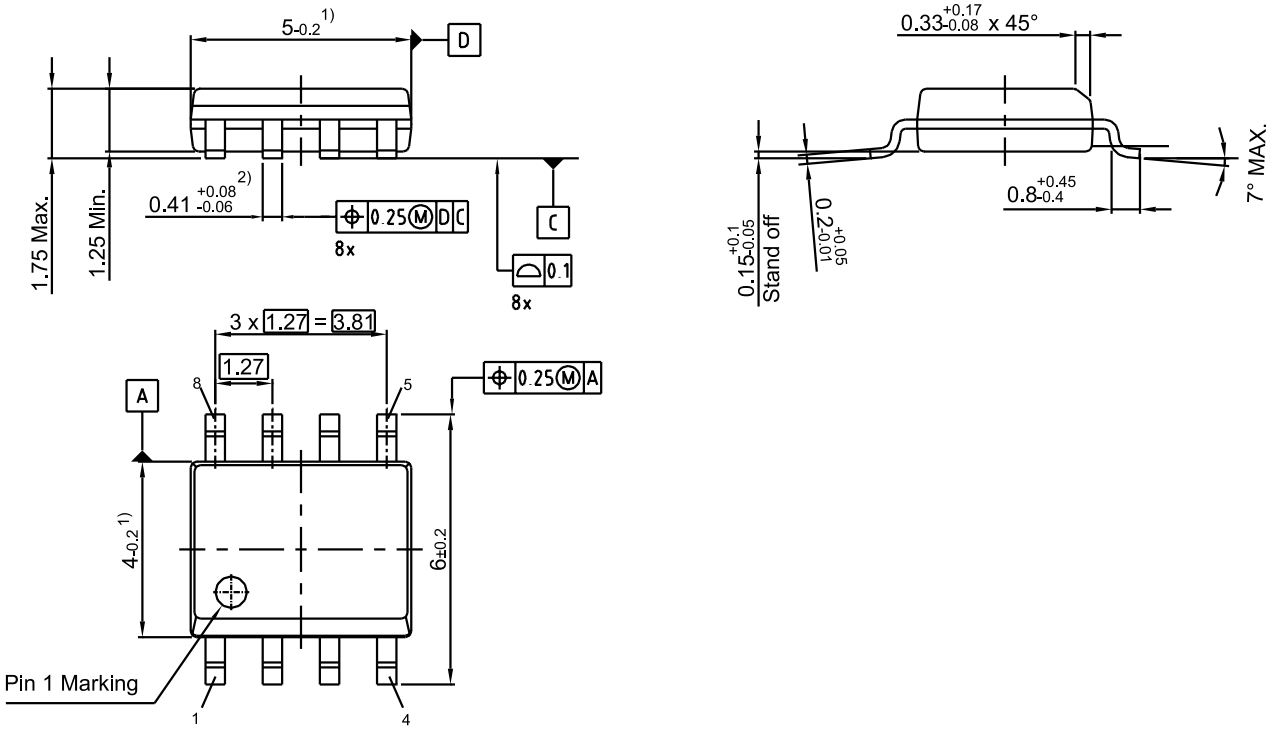
4.3.10 Temperature sensor

Table 14 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Relative accuracy of the temperature sensor	ΔT	-6	–	+6	°C	
Shutdown temperature	T	–	130	–	°C	

5 Package dimensions

The package dimensions of PG-DSO-8 are provided.



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 Max. in excess of the lead width dimension
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 21 Package dimensions for PG-DSO-8

5 Package dimensions

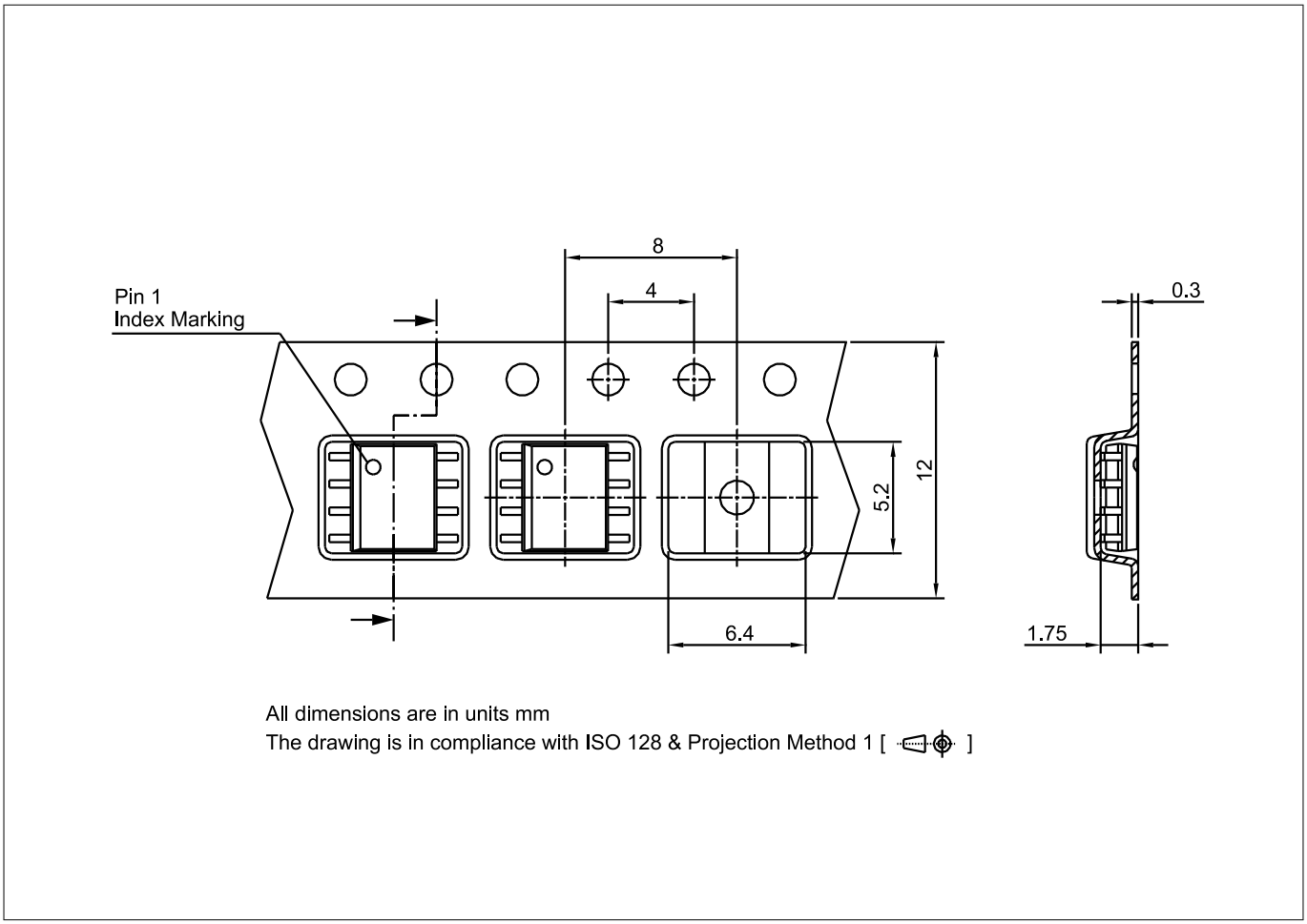


Figure 22 Tape and reel for PG-DSO-8

***Note**: You can find all of our packages, packing types and other package information on our Infineon Internet page "Products": http://www.infineon.com/products.*

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pbfree finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

6 Glossary

AC	Alternating current
ADC	Analog-to-digital converter
BM	Burst mode
CV	Constant voltage
CCM	Continuous conduction mode
DC	Direct current
EMI	Electromagnetic interference
ESD	Electrostatic discharge
OCP	Overcurrent protection
OTP	Overtemperature protection
OVP	Overvoltage protection
QR	Quasi-resonant
QRM	Quasi-resonant mode
SSR	Secondary side regulation
UVLO	Under voltage lockout unit

Revision history

Document version	Date of release	Description of changes
Rev. 1.0	2025-04-07	Initial release
Rev. 1.1	2025-04-28	Update Figure 1, Figure 2: PFC Flyback-SSR-CV with GaN FET, Si MOSFET

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