CoolSET™ 5th Generation Quasi Resonant Plus - in DSO-12 Package

Features

- Integrated 800 V avalanche rugged CoolMOS™
- Novel Quasi Resonant operation and proprietary implementation for low EMI
- Active Burst Mode with selectable entry and exit standby power to reach the lowest standby power <100 mW
- Fast startup achieved with cascode configuration
- Digital frequency reduction for higher system efficiency
- Minimum switching frequency difference between low & high line for higher system efficiency & low EMI
- Cycle-by-cycle peak current limitation
- Maximum on/off time limitation to avoid audible noise during start up and power down
- Auto restart mode protection for VCC Over Voltage, VCC Under Voltage, Over load/Open Loop, Line/Output Over Voltage, Brownout, Over Temperature
- Increased pin voltage rating for ease of system design
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

Potential applications

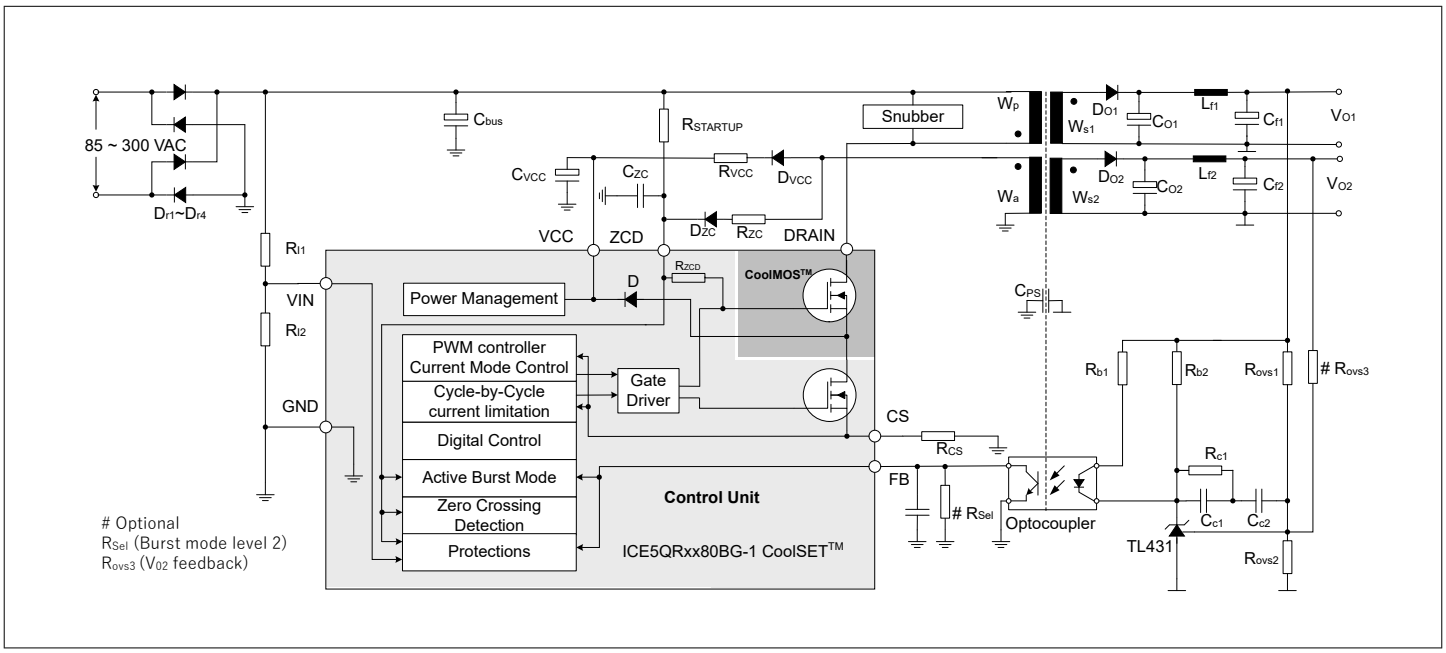
- Auxiliary power supply for home appliances/white goods, TV, PC & server
- Blu-ray player, set-top box & LCD/LED monitor

Product validation

Product validation according to JEDEC standard.

Description

The ICE5QRxx80BG-1 is the CoolSET™ 5th generation Quasi Resonant Plus of integrated power IC optimized for off-line switch power supply in cascode configuration. It is housed in single package with 2 separate chips: one is controller chip and other is HV MOSFET chips. The IC can achieve lower EMI and higher efficiency with improved digital frequency reduction through the proprietary novel Quasi-Resonant operation. The Active Burst Mode enables flexibility in standby power range selection. The product has a wide operation range (10 ~ 32V) of IC power supply and lower power consumption. The numerous protection functions including the robust line protection (both input OVP and brownout) to support the protections of the power supply system in failure situations. All of these make the CoolSET™ 5th generation Quasi Resonant Plus series an outstanding integrated power device in Quasi Resonant flyback converter in the market.



Typical application in isolated flyback using TL431 and optocoupler

Table 1 Output power of CoolSET™ 5th Generation Quasi Resonant Plus in flyback design

Type	Package	Marking	VDS	$R_{DS(on)}$ [1]	220 V AC ±20% [2]	85-300 V AC [2]
ICE5QR4780BG-1	PG-DSO-12	5QR4780BG-1	800 V	4.13 Ω	28 W	15 W
ICE5QR2280BG-1	PG-DSO-12	5QR2280BG-1	800 V	2.13 Ω	42 W	23 W
ICE5QR1680BG-1	PG-DSO-12	5QR1680BG-1	800 V	1.53 Ω	50 W	27 W
ICE5QR0680BG-1	PG-DSO-12	5QR0680BG-1	800 V	0.71 Ω	77 W	42 W

1. Typically at T_j = 25°C (inclusive of low side MOSFET).

2. Calculated maximum output power rating in an open frame design at T_a = 50°C, T_j = 125°C (integrated high voltage MOSFET) and using minimum drain pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purpose only. The actual power can vary depending on the designs. Contact a technical expert from Infineon® for more information.

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1 Pin configuration and functionality

The pin configuration is shown below and the functions are described in Table 2.

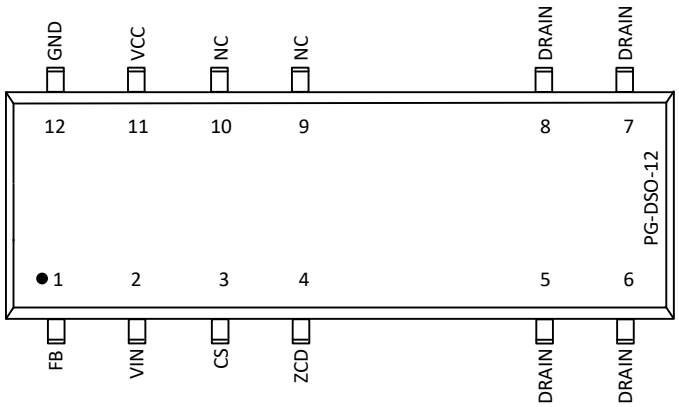


Figure 1 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	FB	Feedback & Burst entry/exit control FB pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
2	VIN	Input Line OVP & BrownIn/Out VIN pin is connected to the bus via resistor divider (see typical application circuit) to sense the line voltage. This pin combines the functions of input Line OVP, Brown in/out and minimum and maximum ZC count setting for low and high line.
3	CS	Current Sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
4	ZCD	Zero Crossing Detection ZCD pin combines the functions of start up, zero crossing detection and output over voltage protection. During the start up, it is used to provide a voltage level to the gate of power switch CoolMOS™ to charge VCC capacitor.
5,6,7,8	DRAIN	Drain The DRAIN pin is connected to the drain of the integrated CoolMOS™.
9,10	NC	Not Connected
11	VCC	VCC(Positive Voltage Supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
12	GND	Ground The GND pin is the common ground of the controller.

2 Representative block diagram

***Note**: Junction temperature of the controller chip is sensed for over temperature protection. The CoolMOS™ is a separate chip from the controller chip in the same package. Please refer to the design guide and/or consult a technical expert for the proper thermal design*

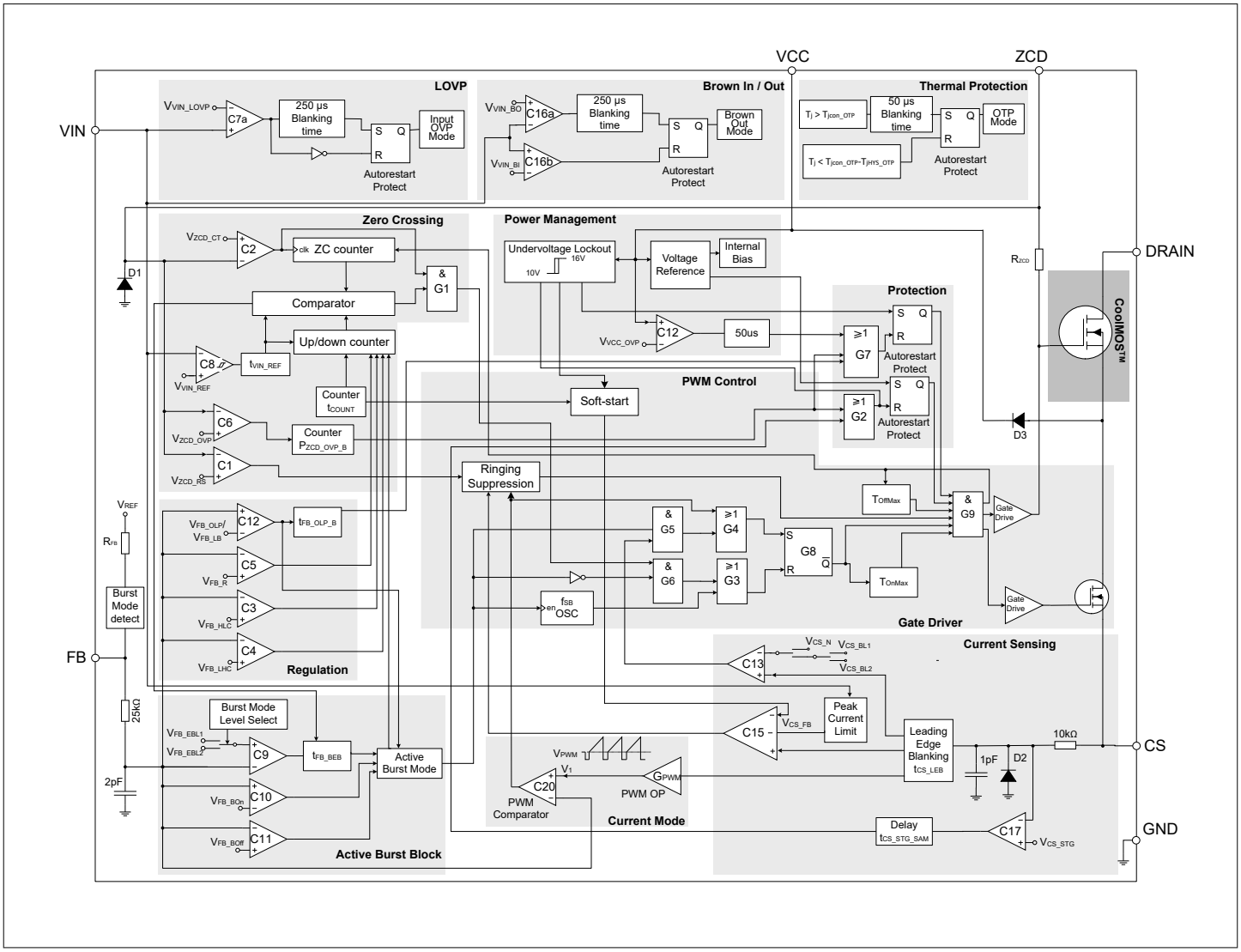


Figure 2 Representative block diagram

3 Functional description

3.1 VCC pre-charging and typical VCC voltage during start-up

As shown in the typical application circuits in page 1, once the line input voltage is applied, a rectified voltage appears across the capacitor C_{BUS}. The pull-up resistor $R_{STARTUP}$ provides a current to charge the C_{ISS} (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over C_{ISS} is high enough, CoolMOS™ and the VCC capacitor are charged through the primary inductance of a transformer L_P, CoolMOS™ and the internal diode D3 with the two steps constant current source $I_{VCC\_Charge1}$[1)] and $I_{VCC\_Charge3}$[1)]. A very small constant current source ($I_{VCC\_Charge1}$) is charged to the VCC capacitor until VCC reaches V_{CC_SCP} to protect the controller from the VCC pin short to ground during the startup. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the VCC capacitor further, until the VCC voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 3, the VCC voltage increases almost linearly with two steps.

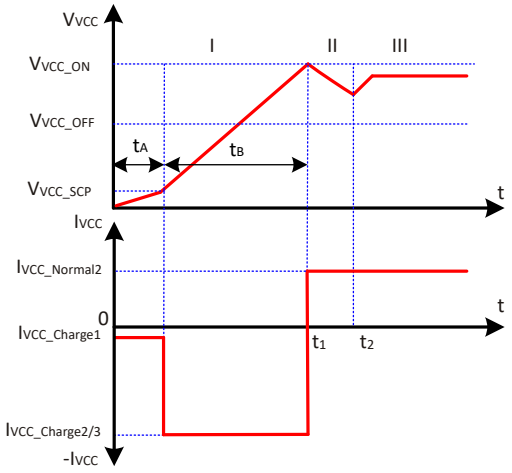


Figure 3 VCC voltage and current at startup

The time for the V_{CC} pre-charging can then be calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \times C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \times C_{VCC}}{I_{VCC\_Charge3}} \quad (1)$$

When the V_{CC} voltage exceeds the V_{CC} turn on threshold V_{VCC_ON} at time t_1, the IC starts to operate with soft start. Due to the power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t_2 onward and delivering the $I_{VCC\_Normal2}$[2] to the CoolSET™. V_{CC} then reaches a constant value depending on the output load.

1) $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during startup.

2) $I_{VCC\_Normal2}$ is supply current from VCC capacitor or auxiliary winding to the CoolSET™ during normal operation with active gate.

3.2 Soft-start

As shown in Figure 4 below, the IC begins to operate with a soft-start at time t_{on}. The switching stresses on the power MOSFET, diode and transformer are minimized during soft-start. The soft-start implemented in ICE5QRXX80BG-1 is a digital time-based function. The preset soft-start time is t_{SS} (12ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3V to V_{CS_N} finally. The normal feedback loop will take over

the control when the output voltage reaches its regulated value. During the first 3 ms of soft start, the ringing suppression time is set to t_{ZCD_RS2} to avoid irregular switching due to switch off oscillation noise.
The zero-crossing counter (ZC counter) is set to 1 during soft-start.

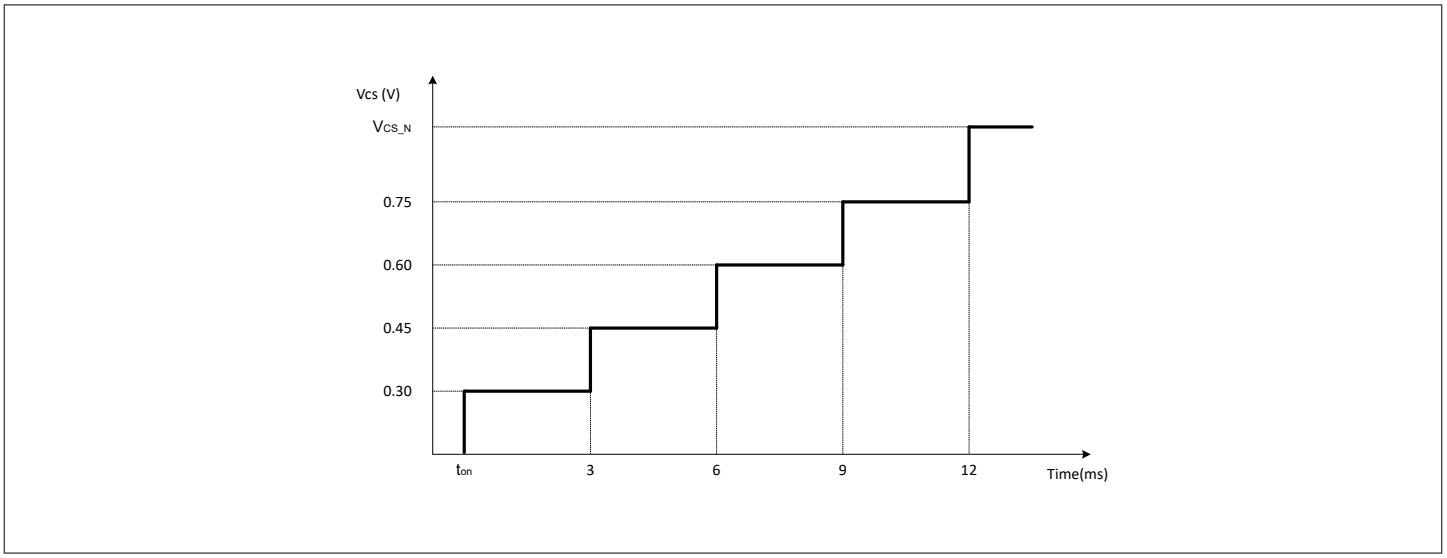


Figure 4 Current Sense Voltage during Soft Start

3.3 Normal operation

During normal operation, ICE5QRxx80BG-1 work with a digital signal processing circuit comprising an up/down counter, a zero-crossing counter (ZC counter) a zero count comparator and an analog circuit comprising a current measurement unit and a current limit comparator. The switch-on and switch-off time points are each determined by the digital circuit and the analog circuit, respectively. The input information of the zero-crossing signal and the value of the up/down counter are needed to determine the switch-on while the feedback signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the full operation of the CoolSET™ in normal operation are illustrated in the following paragraphs.

3.3.1 Digital Frequency Reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are key to implement digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mis-triggering by the high frequency oscillation when the output voltage is very low under conditions such as soft-start or output short circuit. Functionality of these parts is described in the following sub-sections.

3.3.1.1 Minimum ZC Count Determination

To reduce the switching frequency difference between low and high line, minimum ZC count determination is implemented. Minimum ZC count is set to 1 if VIN less than V_{VIN_REF} which represents for low line. For high line, minimum ZC count is set to 3 after VIN higher than V_{VIN_REF}. There is also a hysteresis V_{VIN_REF} with certain blanking time t_{VIN_REF} for stable AC line selection between low and high line.

3.3.1.2 Up/Down Counter

The up/down counter stores the number of the zero crossings which determines valley numbers to switch-on the CoolMOS™ after demagnetization of the transformer. This value is determined by the feedback voltage V_{FB} which contains information about the output power. In a typical peak current mode control, a high output power results in a high feedback voltage and vice-versa. The V_{FB} determines the value of the up/down counter. As a consequence the off-time of the CoolMOS™ varies according to the output power.

The feedback voltage V_{FB} is checked every 48ms and compared with three threshold voltages V_{FB_LHC}, V_{FB_HLC} and V_{FB_R} .The up/down counter can either increase ,decrease or be constant depending on the value of V_{FB} as shown in Table 3.

Table 3 Operation of Up/Down Counter

V_{FB}	Counter Action
Always lower than V_{FB_LHC}	Count upwards till n=8/10[1]
Once higher than V_{FB_LHC}, but always lower than V_{FB_HLC}	Stop counting, no value changing
Once higher than V_{FB_HLC}, but always lower than V_{FB_R}	Count downwards till n=1/3[2]
Once higher than V_{FB_R}	Set up/down counter to n=1/3[2]

[1] *n=8 (for low line) and n=10 (for high line)*

[2] *n=1 (for low line) and n=3 (for high line)*

The number of zero crossings is limited .The counter varies from 1 to 8 (for low line) or from 3 to 10 (for high line) and any attempt beyond this range is ignored. The up/down counter value is reset to 1 during soft-start to ensure an efficient start-up. After blanking time t_{VIN_REF} , the up/down counter is initially 1(for low line) and 3(for high line).The counter is then updated as per the sampled value of V_{FB} at the rising edge of the clock .If V_{FB} exceeds V_{FB_R} voltage due to sudden load increase, the IC resets the up/down counter to 1 (low line) and 3 (high line) without waiting for the next clock pulse in order to allow the system to react rapidly. Figure 5 shows some examples on how up/down counter is changed according to the feedback voltage over time. The use of two different thresholds V_{FB_LHC} and V_{FB_HLC} to count upward or downward is to prevent frequency jittering when the feedback voltage is close to the threshold point.

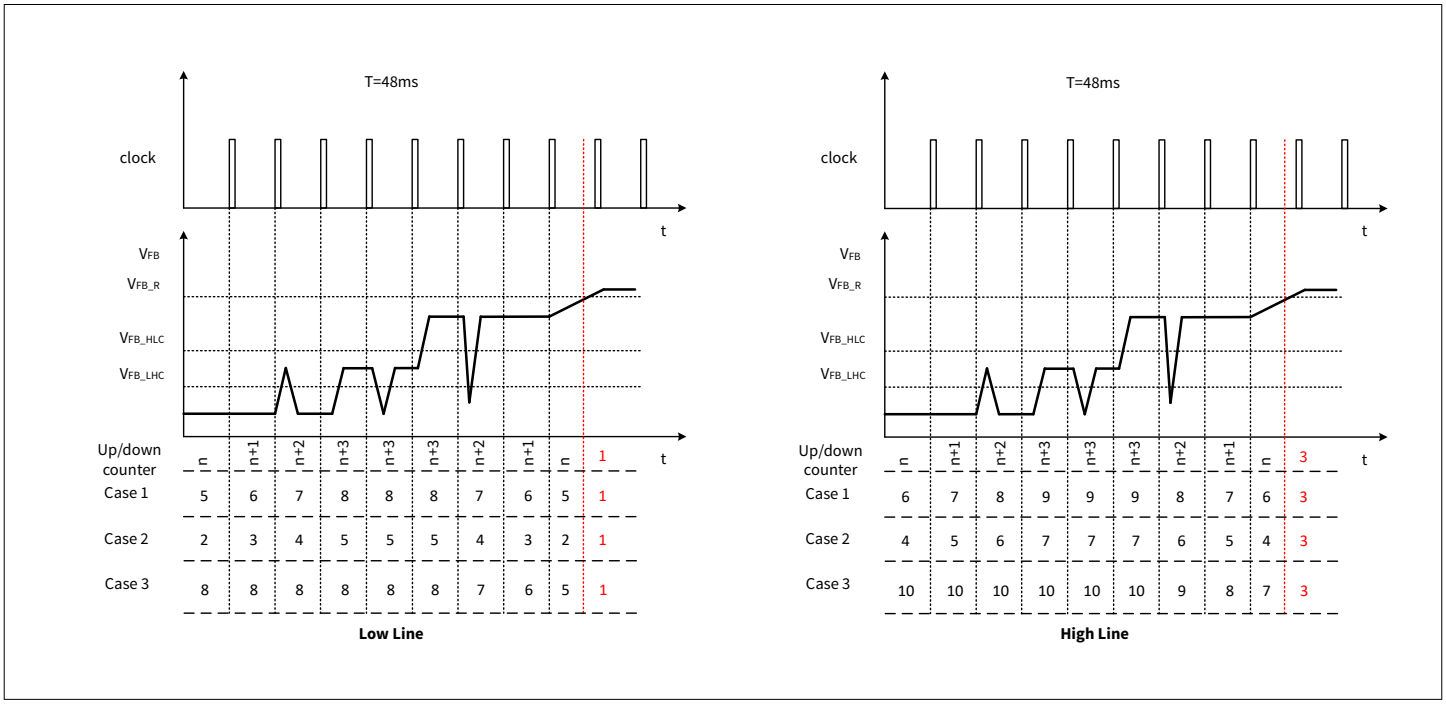


Figure 5 Up/Down counter operation

3.3.1.3 Zero Crossing (ZC Counter)

In the system, the voltage from the auxiliary winding is applied to the ZCD pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally this pin is connected to a negative clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller. During on-state of the power switch, a positive gate drive voltage is applied to the ZCD pin due to R_{ZCD} resistor, hence external diode D_{ZC} (see typical application circuit) is added to block the negative voltage from the auxiliary winding. The ZC counter has a minimum value of 1 (for low line) or 3 (for high line) and maximum value of 8 (for low line) or 10 (for high line). After

the internal high voltage CoolMOS™ is turned off, every time when the falling voltage ramp of ZCD pin crosses the V_{ZCD_CT} threshold, a zero crossing is detected and ZC counter will increase by 1. It is reset every time after the DRIVER output is changed to high. To achieve the switch on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of R_{ZC} and C_{ZC} as shown in typical application circuit) before it is applied to the zero-crossing detector through the ZCD pin. The needed time delay to the main oscillation signal Δt should be approximately one fourth of the oscillation period, T_{OSC} (by transformer primary inductor and drain-source capacitor) minus the propagation delay from the detected zero-crossing to the switch-on of the main switch t_{delay}, theoretically:

$$\Delta t = \frac{T_{osc}}{4} - t_{delay} \tag{2}$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{ZC} \times \frac{R_{ZC} \times R_{ZCD}}{R_{ZC} + R_{ZCD}} \tag{3}$$

3.3.2 Ringing Suppression Time

When the CoolMOS™ turns off, there will be voltage oscillation on the drain due to leakage inductance and MOSFET parasitic capacitance, which will be reflected on ZCD voltage, V_{ZCD}. To avoid mis-triggering of the CoolMOS™ due to such oscillations, a ringing suppression timer is implemented. This suppression time is dependent on V_{ZCD}. If V_{ZCD} is lower than threshold V_{ZCD_RS}, a longer time t_{ZCD_RS2} is applied. However, if V_{ZCD} is higher than the threshold, a shorter time t_{ZCD_RS1} is set.

3.3.2.1 Switch on determination

After the gate drive goes to low, it cannot be changed to high during ringing suppression time. After ringing suppression time, the gate drive can be turned on when the ZC counter value is equal to up/down counter value. However, it is also possible that the oscillation between primary inductor and MOSFET parasitic capacitance damps very fast and IC cannot detect zero crossings event. In this case, a maximum off time is implemented. After gate drive has been remained off for the period of t_{OffMax}, the gate drive will be turned on again regardless of the ZC counter values and V_{ZCD}. This function can effectively prevent the switching frequency from going lower than 20 kHz. Otherwise it will cause audible noise.

3.3.2.2 Switch off determination

In the converter system, the primary current is sensed by an external shunt resistor which is connected between the internal low side MOSFET and the common ground. The sensed voltage across the shunt resistor ,V_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the feedback voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB} ,the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the V_{CS} is described by (see Figure 2):

$$V_{CS} = I_D \times R_{CS} \tag{4}$$

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} \tag{5}$$

where

I_D : power MOSFET drain current
V_{CS} : CS pin voltage
R_{CS} : current sense resistance
V1 : voltage compared to V_{FB}

G_{PWM} : PWM-OP gain
V_{PWM} : offset for voltage ramp

To avoid mis-triggering caused by the voltage spike across the shunt resistor at the turn on of the main power switch, a leading edge blanking time, t_{CS_LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on time of the gate drive is the leading edge blanking time. In addition, there is a maximum on time, t_{OnMax} implemented in the IC. Once the gate drive has been in high state longer than the maximum on time, it will be turned off to prevent the switching frequency from going too low because of long on time. Also, if the voltage at the current sense pin is lower than the preset threshold V_{CS_STG} after the time $t_{CS\_STG\_SAM}$ for three consecutive pulses during on-time of the power switch, this abnormal V_{CS} will trigger IC into auto restart mode.

3.3.3 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. There is a slope control of the rising edge at the output of driver (see Figure 6). Thus the leading switch spike during turn on is minimized.

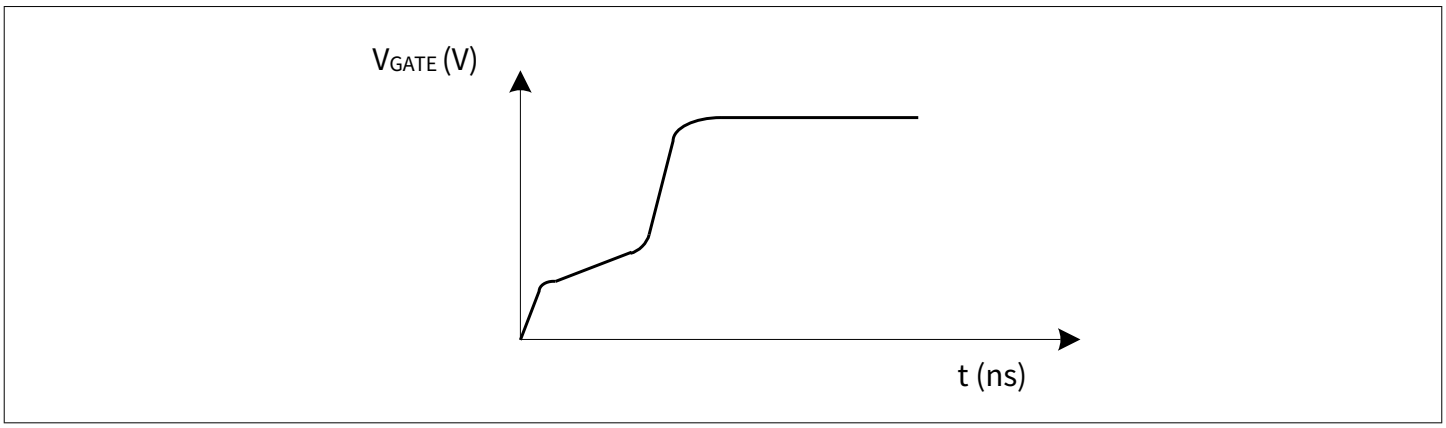


Figure 6 Modulated gate drive

3.3.4 Current Limitation

There is a cycle-by-cycle current limitation realized by the current limit comparator to provide over-current detection. The source current of the CoolMOS™ is sensed via a sense resistor R_{CS}. By means of R_{CS} the source current is transformed to a sense voltage V_{CS} which is fed into the pin CS. If V_{CS} exceeds an internal voltage limit, adjusted according to the Line voltage, the comparator immediately turns off the gate drive. When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased which is beyond the converter design limit. To compensate such effect, both the internal peak current limit circuit (V_{CS}) and the ZC count varies with the bus voltage according to Figure 7.

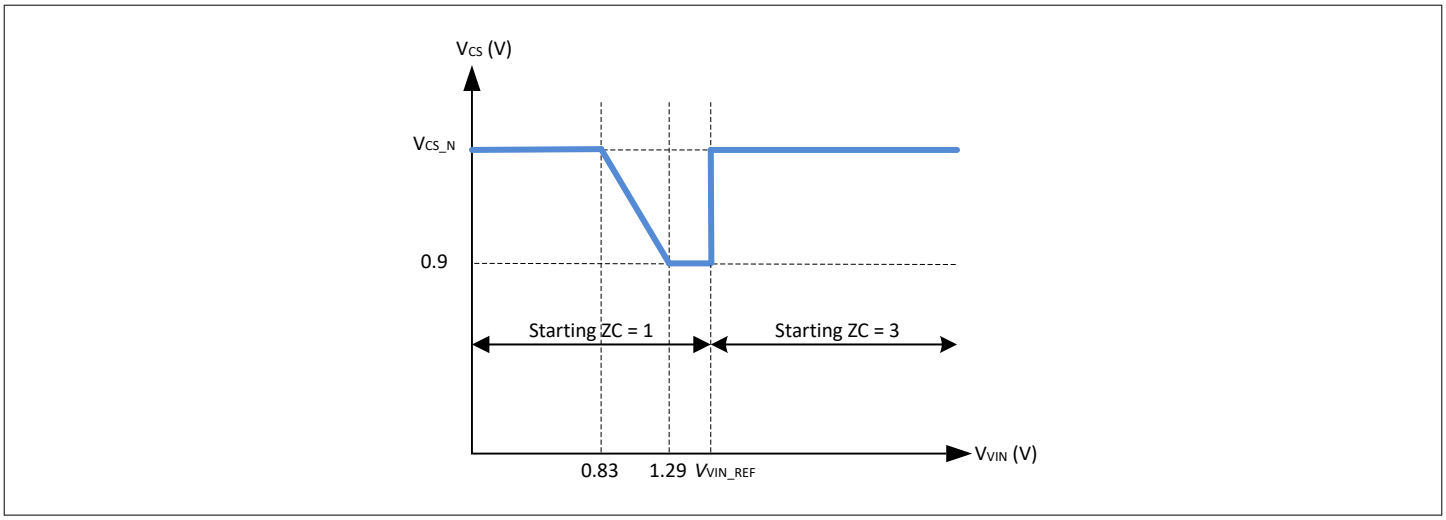


Figure 7 Variation of V_{CS} limit voltage according to V_{IN} voltage

3.4 Active Burst Mode (ABM) with selectable power level

At light load condition, the IC enters Active Burst Mode operation to minimize the power consumption. Details about Active Burst Mode operation are explained in the following paragraphs. The burst mode entry level can be selected by changing the different resistor R_{Sel} at FB pin. There are 2 levels to be selected with different resistor which are targeted for low range of Active Burst Mode power (Level 1) and high range of Active Burst Mode power (Level 2). The following table shows the control logic for the entry and exit level with the FB voltage.

Table 4 Two Levels for Entry and Exit of Active Burst Mode

Level	V_{FB}	V_{CS}	Entry Level (V_{FB_EBLX})	Exit Level (V_{FB_LB})
1	$V_{FB} > V_{REF\_B}$	V_{CS_BL1} = 0.31 V	0.9	2.75
2	$V_{FB} < V_{REF\_B}$	V_{CS_BL2} = 0.35 V	1.05	2.75

During IC first startup, the internal Ref_{GOOD} signal is logic low when VCC < 4 V. It will reset the Burst Mode level Detection latch. When the Burst Mode Level Detection latch is low and IC is in OFF state, the IC internal R_{FB} resistor is disconnected from the FB pin and a current source I_{sel} is turned on instead. From VCC = 4.44 V to the VCC on threshold, the FB pin will source current I_{Sel} through R_{Sel} and external FB network. When VCC reaches VCC on threshold, the FB voltage is sensed. The burst mode threshold is then chosen according to the FB voltage level. The Burst Mode Level Detection latch is then set to high. Once the detection latch is set high, any change of the FB level will not change the threshold selection. The current source I_{sel} is turned off in 2 µs after VCC reaches VCC on threshold and the R_{FB} resistor is re-connected to FB pin (see Figure 8).

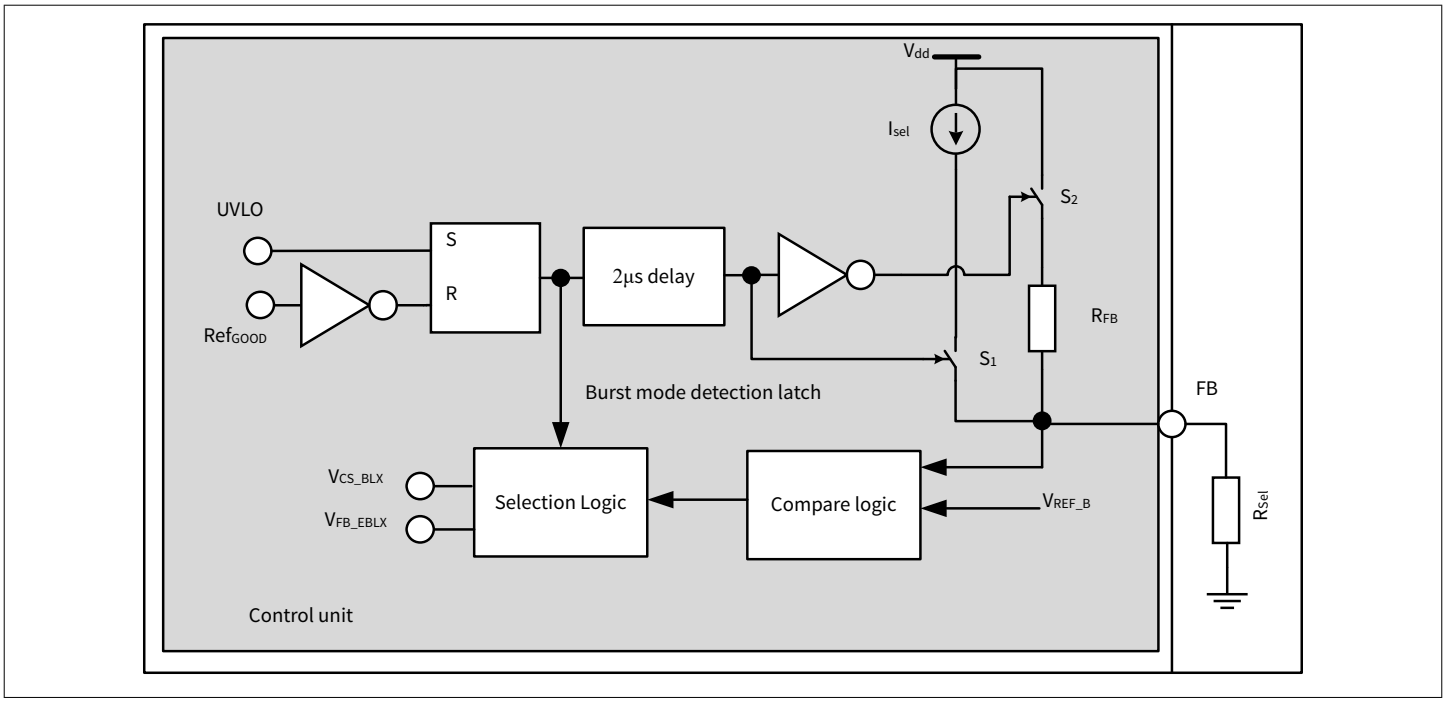


Figure 8 Detection for Burst Mode Level

3.4.1 Entering Burst Mode Operation

For determination of entering Active Burst Mode operation, three conditions apply:

- The feedback voltage is lower than the threshold of V_{FB_EBLX}
- The up/down counter has reached its maximum value depending on the line voltage (8 for low line or 10 for high line)
- The above two conditions remain after a certain blanking time t_{FB_BEB} (20 ms)

Once all the above conditions are fulfilled, the Active Burst Mode flip-flop is set and the IC enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

3.4.2 During ABM operation

After entering the Active Burst Mode, the feedback voltage V_{FB} rises as V_O (output voltage) starts to decrease due to the inactive PWM section. Switching resumes when V_{FB} reaches V_{FB_BOn}. The turn-on time is limited solely by the voltage at the CS pin. When the V_{CS} reaches V_{CS_BLX} the CoolMOS™ turns off. The ZC counter value is maximum (8 for low line and 10 for high line) before the CoolMOS™ turns on.If the output load is still low,V_{FB} decreases as the PWM section is operating. When V_{FB} reaches the threshold V_{FB_BOff} , the internal circuit is reset again and the PWM section is disabled till V_{FB} increases to V_{FB_BOn} .In Active Burst Mode, V_{FB} is changing like a saw tooth between V_{FB_BOff} and V_{FB_BOn} (see Figure 9).

3.4.3 Leaving ABM operation

The feedback voltage immediately increases if there is a high load jump. This is observed by a comparator with threshold of V_{FB_LB}. As the current limit is V_{CS_BLX} (31% or 35%) during Active Burst Mode, a certain load is needed so that feedback voltage can exceed V_{FB_LB}. After leaving Active Burst Mode, Gate will only turn on if zero crossing is detected (V_{ZCD}<V_{ZCD_LB}) to ensure full transformer demagnetization. This eases synchronous rectification implementation by ensuring DCM operation upon exit of burst mode. Then, normal peak current control through V_{FB} is re-activated. In addition, the up/down counter will be set to 1 (low line) or 3 (high line) immediately after leaving Active Burst Mode. This is helpful to minimize the output voltage undershoot.

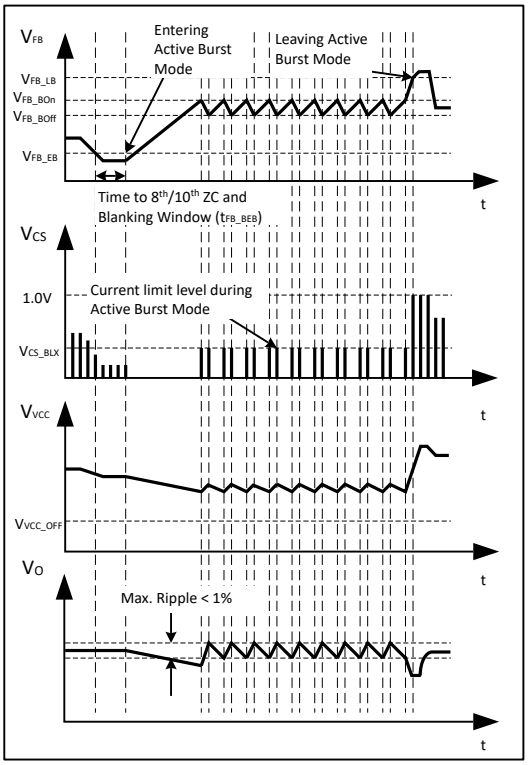


Figure 9 Signals in Active Burst Mode

3.5 Protection functions

The ICE5QRxx80BG-1 provide numerous protection functions which considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions. There are 3 different kinds of protection mode; non-switch auto restart, auto-restart and odd cycle skip auto-restart. The details can refer to the Figure 10, Figure 11 and Figure 12.

Table 5 Protection Functions

Fault Type	Normal Mode	Burst Mode		Protection Mode
		Burst On	Burst Off	
Line Over Voltage	✓	✓	✓	Non-Switch Auto Restart
Brownout	✓	✓	✓	Non-Switch Auto Restart
VCC over voltage	✓	✓	Not Applicable	Odd Cycle Skip Auto Restart
VCC under voltage	✓	✓	Not Applicable	Auto Restart
Over Load	✓	Not Applicable	Not Applicable	Odd Cycle Skip Auto Restart
Output Over Voltage	✓	✓	Not Applicable	Odd Cycle Skip Auto Restart
Over Temperature	✓	✓	✓	Non-Switch Auto Restart

3.5.1 Line Over Voltage

The AC line over voltage protection is detected by sensing bus capacitor voltage through VIN pin via 2 potential divider resistors, R_{l1} and R_{l2} (see typical application circuit). Once V_{VIN} voltage is higher than the line over voltage threshold V_{VIN_LOVP}, the IC enters Line Over Voltage Protection and it releases the protection mode after V_{VIN} is lower than V_{VIN_LOVP}.

3.5.2 Brownout

The brownout protection is observed by VIN pin similar to line over voltage protection method with a different voltage threshold level. When V_{VIN} voltage is lower than the brownout threshold (V_{VIN_BO}), the controller enters Brownout Protection and it releases the protection mode after V_{VIN} higher than brownin threshold (V_{VIN_BI}).

3.5.3 VCC over voltage or VCC under voltage

During operation, the VCC voltage is continuously monitored.

If VCC voltage falls below V_{VCC_OFF} for a blanking time of $t_{VCC\_OFF\_B}$, MOSFET will be switched off and auto restart will be initiated.

If VCC voltage exceeds V_{VCC_OVP} for a blanking time of $t_{VCC\_OVP\_B}$, MOSFET will be switched off and odd cycle skip auto restart will be initiated.

3.5.4 Over Load

In case of open control loop or output over Load, the feedback voltage will be pulled up and exceed V_{FB_OLP}. After a blanking time of $t_{FB\_OLP\_B}$, the IC enters auto restart mode. The blanking time here enables the converter to operate for a certain time during a sudden load jump.

3.5.5 Output Over Voltage

The voltage at the ZCD pin is sampled for output over voltage detection at t_{ZCD_RS1} after CoolMOS™ is turned off. If the voltage is higher than the preset threshold V_{ZCD_OVP} for 10 consecutive pulses, the IC enters Output Over Voltage Protection.

3.5.6 Over Temperature

If the junction temperature of controller exceeds T_{jCon_OTP}, the IC enters into Over Temperature Protection (OTP) auto restart mode. The IC has also implemented with a 40 °C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature is dropped 40 °C lower than the over temperature trigger point.

3.5.7 VCC short to GND

To limit the power dissipation of the startup circuit at V_{CC} short to GND condition, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_Charge1}$. With such low current, the power loss of the IC is limited to prevent overheating.

3.5.8 Signals in different protection modes

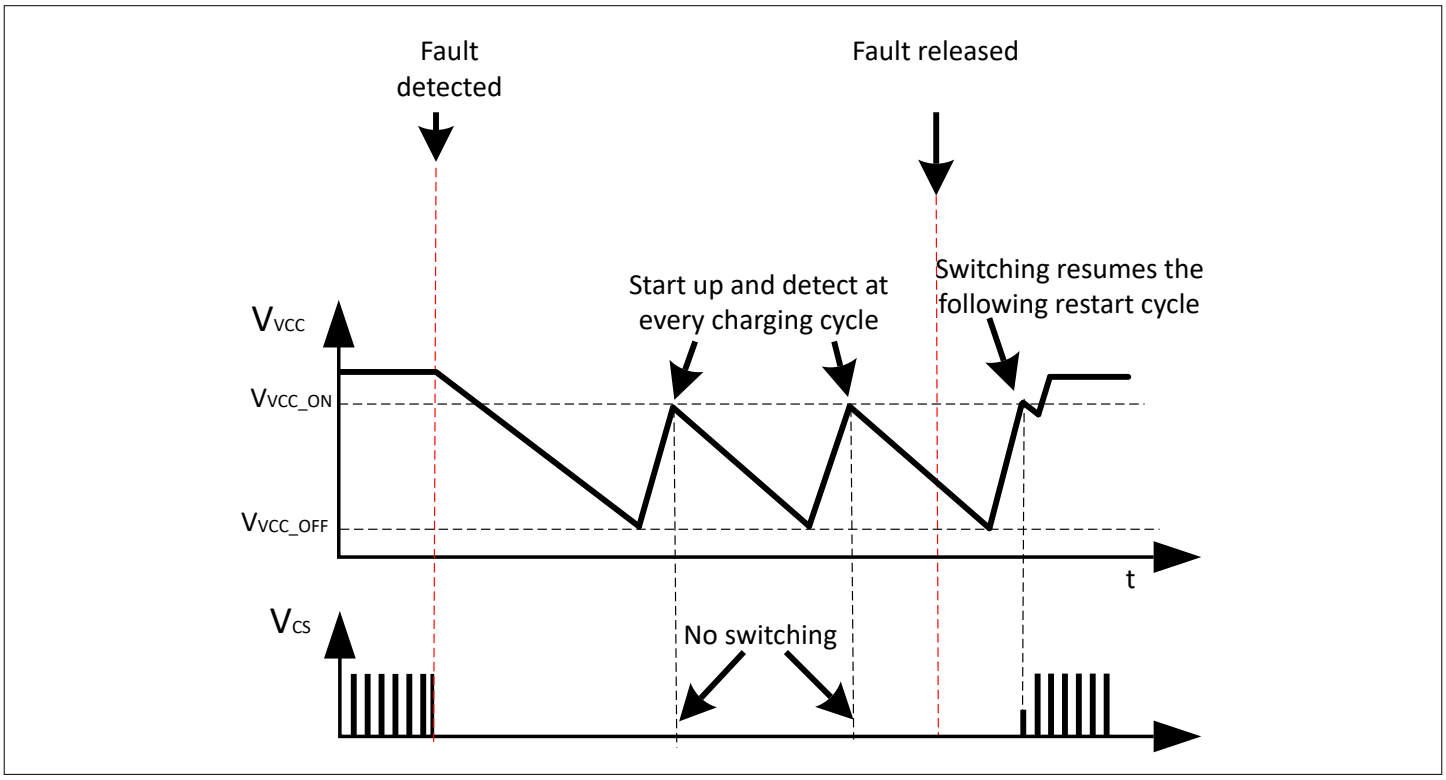


Figure 10 Non Switch Auto Restart

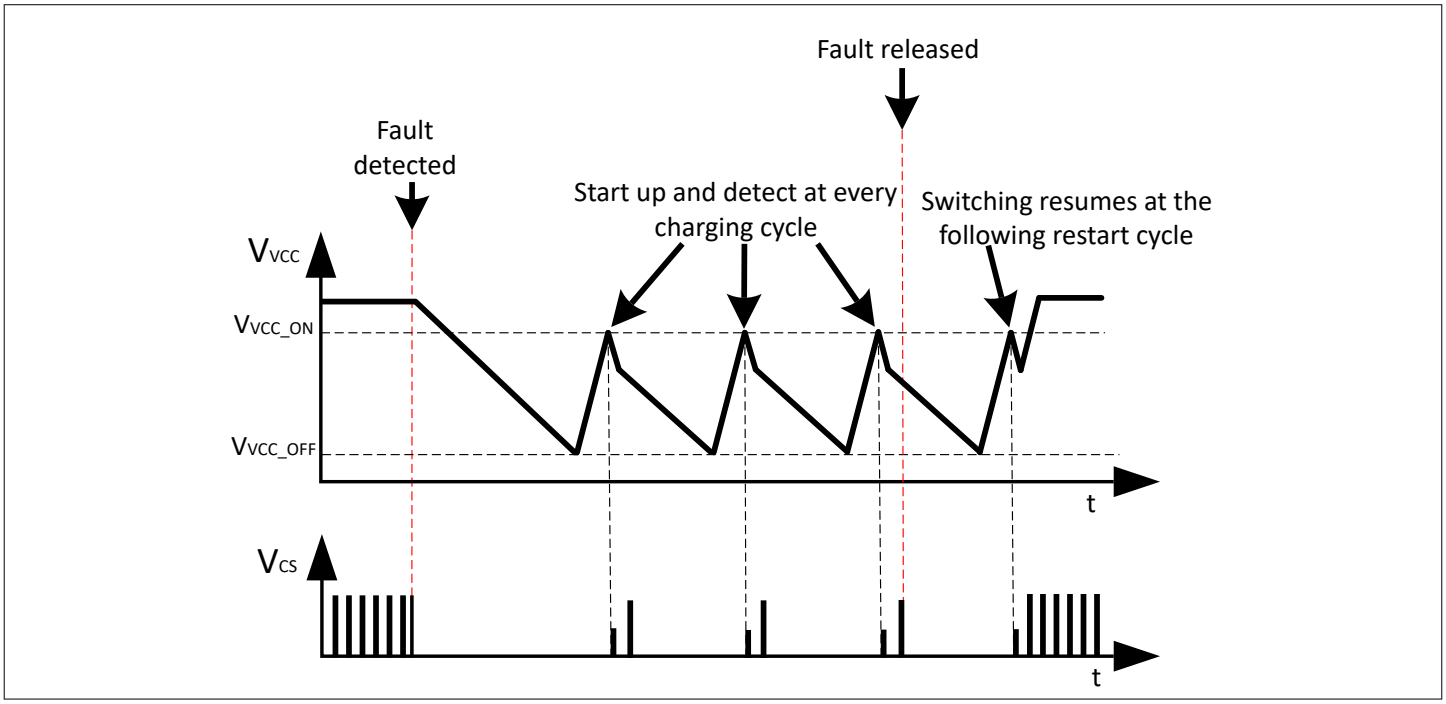


Figure 11 Auto Restart

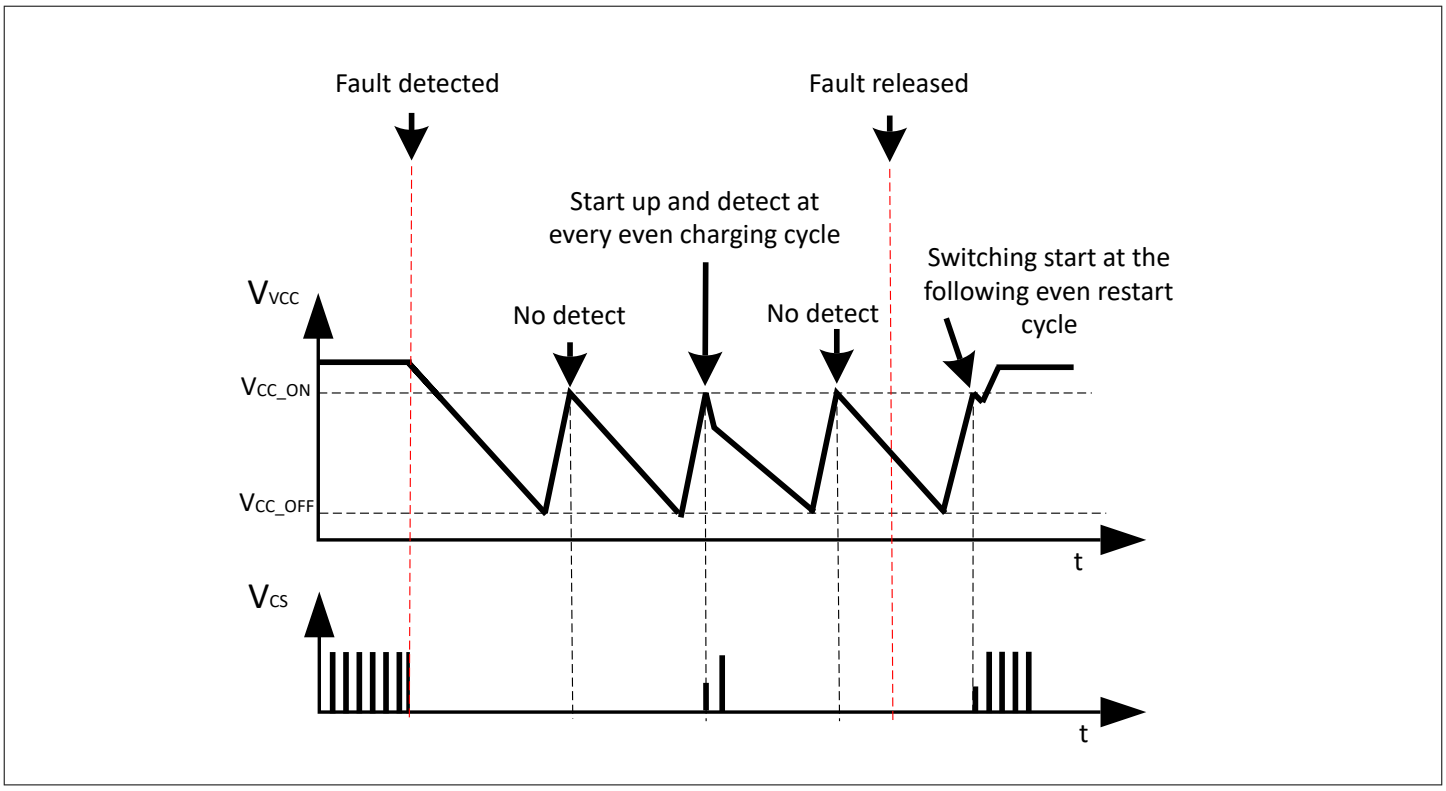


Figure 12 Odd Cycle Skip Auto Restart Mode

4 Electrical characteristics

Attention: ***All voltages are measured with respect to ground (pin 12). The voltage levels are valid if other ratings are not violated.***

4.1 Absolute maximum ratings

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that will be connected to pin 11 (VCC) is discharged before assembling the application circuit. T_a=25 °C unless otherwise specified.***

Table 6 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain voltage						
ICE5QRXX80BG-1	V_{DRAIN}	-	-	800	V	T_j = 25 °C
Pulse drain current						
ICE5QR4780BG-1	I_{D_PULSE}	-	-	2.6	A	Pulse width t_P limited by T_{j_max}
ICE5QR2280BG-1	I_{D_PULSE}	-	-	5.8	A	Pulse width t_P=20 µs and limited by T_{j_max}
ICE5QR1680BG-1	I_{D_PULSE}	-	-	5.8	A	Pulse width t_P=20 µs and limited by T_{j_max}
ICE5QR0680BG-1	I_{D_PULSE}	-	-	5.8	A	Pulse width t_P=20 µs and limited by T_{j_max}
Pin rating						
VCC Supply Voltage	V_{VCC}	-0.3	-	35	V	
FB Voltage	V_{FB}	-0.3	-	5.5	V	
ZCD Voltage	V_{ZCD}	-0.3	-	27	V	
CS Voltage	V_{CS}	-0.3	-	3.6	V	
VIN Voltage	V_{VIN}	-0.3	-	5.5	V	
Maximum DC current on any pin		-10		10	mA	Except DRAIN and CS pin
ESD robustness HBM	V_{ESD_HBM}	-	-	2000	V	According to EIA/JESD22
ESD robustness CDM	V_{ESD_CDM}	-	-	500	V	According to EIA/JESD22
Junction temperature range	T_j	-40	-	150	°C	Controller & CoolMOS
Storage Temperature	T_{STORE}	-55	-	150	°C	

(table continues...)

Table 6 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance (junction-ambient)						
ICE5QR4780BG-1	R_{thJA}	-	-	105	K/W	1)
ICE5QR2280BG-1	R_{thJA}	-	-	98	K/W	1)
ICE5QR1680BG-1	R_{thJA}	-	-	95	K/W	1)
ICE5QR0680BG-1	R_{thJA}	-	-	94	K/W	1)
Avalanche current, repetitive, t_{AR} limited by maximal T_j = 150°C and T_{j_Start} = 25°C						
ICE5QR4780BG-1	I_{AR}	-	-	0.2	A	
ICE5QR2280BG-1	I_{AR}	-	-	0.4	A	
ICE5QR1680BG-1	I_{AR}	-	-	0.6	A	
ICE5QR0680BG-1	I_{AR}	-	-	1.8	A	
Avalanche energy, repetitive, tAR limited by maximal Tj = 150°C and T_{j_Start} = 25°C						
ICE5QR4780BG-1	E_{AR}	-	-	0.02	mJ	I_D=0.2A,V_{DD}=50V
ICE5QR2280BG-1	E_{AR}	-	-	0.05	mJ	I_D=0.4A,V_{DD}=50V
ICE5QR1680BG-1	E_{AR}	-	-	0.07	mJ	I_D=0.6A,V_{DD}=50V
ICE5QR0680BG-1	E_{AR}	-	-	0.22	mJ	I_D=1.8A,V_{DD}=50V

1) Setup according to the JEDEC standard JESD51 and using minimum drain pin copper area in a 2 oz copper single sided PCB

4.2 Operating range

***Note**: Within the operating range, the IC operates as described in the functional description.*

Table 7 Operating range

Within the operating range, the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC Supply Voltage	V_{VCC}	V_{VCC_OFF}	-	V_{VCC_OVP}	V	
Junction Temperature of controller	T_{jCon_op}	-40	-	T_{jCon_OTP}	°C	Max value limited due to OTP of controller chip.
Junction Temperature of CoolMOS	$T_{jCoolMOS\_op}$	-40	-	150	°C	

4.3 Operating conditions

***Note**: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_j from – 40°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of VCC = 18 V is assumed.*

Table 8 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC Charge Current	$I_{VCC\_Charge1}$	-0.35	-0.20	-0.09	mA	V_{VCC}=0V,$R_{StartUp}$=50MΩ and V_{DRAIN}=90V
VCC Charge Current	$I_{VCC\_Charge2}$	-	-3.2	-	mA	V_{VCC}=3V,$R_{StartUp}$=50MΩ and V_{DRAIN}=90 V
VCC Charge Current	$I_{VCC\_Charge3}$	-5	-3	-1	mA	V_{VCC}=15V,$R_{StartUp}$=50MΩ and V_{DRAIN}=90 V
Current Consumption, Startup Current	$I_{VCC\_Startup}$	-	0.22	-	mA	V_{VCC}=15 V
Current Consumption, Normal	I_{VCC_Normal}	-	0.9	-	mA	I_{FB}=0A (No Gate Switching)
Current Consumption, Auto Restart	I_{VCC_AR}	-	380	-	µA	
Current Consumption, Burst Mode	$I_{VCC\_Burst\ Mode}$	-	0.5	-	mA	V_{FB}=1.8V
VCC Turn-on Threshold Voltage	V_{VCC_ON}	15.3	16.0	16.5	V	
VCC Turn-off Threshold Voltage	V_{VCC_OFF}	9.5	10	10.5	V	
VCC Short Circuit Protection	V_{VCC_SCP}	-	1.1	1.9	V	
VCC Turn-off blanking	$t_{VCC\_OFF\_B}$	-	50	-	µs	

4.4 Internal voltage reference

Table 9 Internal voltage reference

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Internal reference voltage	V_{REF}	3.20	3.30	3.39	V	Measured at FB pin I_{FB}=0 A

4.5 PWM section

Table 10 PWM section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Feedback pull-up resistor	R_{FB}	11	15	20	kΩ	
PWM-OP gain	G_{PWM}	1.95	2.05	2.15	-	

(table continues...)

Table 10 (continued) PWM section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Offset for voltage ramp	V_{PWM}	0.42	0.5	0.58	V	
Maximum on time in normal operation	t_{OnMax}	28	35	42	µs	
Maximum off time in normal operation	t_{OffMax}	34	42.5	51	µs	

4.6 Current sense

Table 11 Current sense

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.94	1.00	1.06	V	
Leading edge-blanking time	t_{CS_LEB}	118	220	462	ns	
Peak Current Limitation in Active Burst Mode – Level 1	V_{CS_BL1}	0.26	0.31	0.36	V	
Peak Current Limitation in Active Burst Mode - Level 2	V_{CS_BL2}	0.3	0.35	0.4	V	
Abnormal CS voltage threshold	V_{CS_STG}	0.06	0.10	0.15	V	
Abnormal CS voltage consecutive trigger	P_{CS_STG}	-	3	-	cycle	
Abnormal CS voltage sample period	$t_{CS\_STG\_SAM}$	2.3	5	-	µs	

4.7 Soft start

Table 12 Soft start

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Soft start time	t_{SS}	8.5	12.0	-	ms	
Soft start time step	t_{SS_S} [1)]	-	3	-	ms	
Internal regulation voltage at first step	V_{SS1} [1)]	-	0.30	-	V	CS peak voltage
Internal regulation voltage step at soft start	V_{SS_S} [1)]	-	0.15	-	V	

1) This parameter is not subjected to production test - verified by design/characterization

4.8 Digital Zero Crossing

Table 13 Digital Zero Crossing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Zero crossing threshold voltage	V_{ZCD_CT}	60	100	150	mV	
Zero crossing ringing suppression threshold	V_{ZCD_RS}	-	0.45	-	V	
Minimum ringing suppression time	t_{ZCD_RS1}	2	2.5	3	µs	$V_{ZCD}>V_{ZCD\_RS}$
Maximum ringing suppression time	t_{ZCD_RS2}	-	25	-	µs	$V_{ZCD}<V_{ZCD\_RS}$
Threshold to reset Up/Down Counter	V_{FB_R}	-	2.75	-	V	
Threshold for downward counting	V_{FB_HLC}	-	2.05	-	V	
Threshold for upward counting	V_{FB_LHC}	-	1.55	-	V	
Counter time	t_{COUNT}	-	48	-	ms	
ZCD resistance	R_{ZCD}	2.5	3.0	3.5	kΩ	Internal resistor at ZCD pin
VIN voltage threshold for line selection	V_{VIN_REF}	1.48	1.52	1.58	V	
Blanking time for VIN voltage threshold for line selection	t_{VIN_REF}	-	16	-	ms	

4.9 Active burst mode

Table 14 Active Burst Mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Charging current to select burst mode	I_{sel}	2.5	3.0	3.5	µA	
Burst mode selection reference voltage threshold	V_{REF_B}	2.65	2.75	2.85	V	
Feedback voltage for entering Active Burst Mode for level 1	V_{FB_EBL1}	0.86	0.90	0.94	V	
Feedback voltage for entering Active Burst Mode for level 2	V_{FB_EBL2}	1.0	1.05	1.1	V	
Blanking Time for entering Active Burst Mode	t_{FB_BEB}	-	20	-	ms	

(table continues...)

Table 14 (continued) Active Burst Mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Feedback voltage for leaving Active Burst Mode	V_{FB_LB}	2.65	2.75	2.85	V	
ZCD voltage threshold for first pulse after leaving Active Burst Mode	V_{ZCD_LB}	60	100	150	mV	
Feedback voltage for burst-on	V_{FB_BOn}	2.30	2.40	2.50	V	
Feedback voltage for burst-off	V_{FB_BOff}	1.90	2.0	2.10	V	

4.10 Line overvoltage protection

Table 15 Line overvoltage protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Line overvoltage threshold	V_{VIN_LOVP}	2.80	2.90	3.00	V	
Line overvoltage blanking	$t_{VIN\_LOVP\_B}$	-	250	-	µs	

4.11 Brown In/Out Protection

Table 16 Brown In/Out Protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
BrownIn threshold	V_{VIN_BI}	0.63	0.66	0.69	V	
BrownIn Blanking	$t_{VIN\_BI\_B}$	-	250	-	µs	
BrownOut threshold	V_{VIN_BO}	0.37	0.40	0.43	V	
BrownOut Blanking	$t_{VIN\_BO\_B}$	-	250	-	µs	

4.12 VCC overvoltage protection

Table 17 VCC over voltage protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCC_OVP}	29.0	30.5	32.0	V	
VCC overvoltage blanking	$t_{VCC\_OVP\_B}$	-	55	-	µs	

4.13 Overload protection

Table 18 Overload protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overload detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.65	2.75	2.85	V	
Overload protection blanking time	$t_{FB\_OLP\_B}$	-	30	-	ms	

4.14 Output Over Voltage Protection

Table 19 Output OVP

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output Over Voltage threshold	V_{ZCD_OVP}	1.90	2.00	2.10	V	
Output Over Voltage Blanking Pulse	$P_{ZCD\_OVP\_B}$	-	10	-	Pulse	Consecutive pulses

4.15 Thermal protection

Table 20 Thermal protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Over temperature protection	T_{jCon_OTP} [1)]	129	140	150	°C	Junction temperature of the controller chip (not the CoolMOS™ chip).
Over temperature hysteresis	T_{jHYS_OTP}	-	40	-	°C	
Over temperature blanking time	$T_{jCon\_OTP\_B}$	-	50	-	µs	

1) This parameter is not subjected to production test, verified by design/characterization

4.16 CoolMOS™ section

Table 21 CoolMOS™ section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain Source Breakdown Voltage						
ICE5QRXX80BG-1	$V_{(BR)DSS}$	800	-	-	V	T_j = 25°C

(table continues...)

Table 21 (continued) CoolMOS™ section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain Source On-Resistance (inclusive of low side MOSFET)						
ICE5QR4780BG-1	R_{DSon}	-	4.13	4.85	Ω	T_j=25°C at I_D = 0.4A
ICE5QR4780BG-1	R_{DSon}	-	8.69[1)]	-	Ω	T_j=125°C at I_D = 0.4A
ICE5QR2280BG-1	R_{DSon}	-	2.13	2.35	Ω	T_j = 25°C at I_D = 1A
ICE5QR2280BG-1	R_{DSon}	-	4.31[1)]	-		T_j = 125°C at I_D = 1A
ICE5QR1680BG-1	R_{DSon}	-	1.53	1.75	Ω	T_j = 25°C at I_D = 1.4A
ICE5QR1680BG-1	R_{DSon}	-	3.01[1)]	-	Ω	T_j = 125°C at I_D = 1.4A
ICE5QR0680BG-1	R_{DSon}	-	0.71	0.80	Ω	T_j=25°C at I_D = 2A
ICE5QR0680BG-1	R_{DSon}	-	1.27[1)]	-	Ω	T_j=125°C at I_D = 2A
Dynamic characteristics						
Rise time	t_{rise}[2)]	-	30	-	ns	
Fall time	t_{fall}[2)]	-	30	-	ns	
Effective output capacitance, energy related						
ICE5QR4780BG-1	$C_{o(er)}$	-	3[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V
ICE5QR2280BG-1	$C_{o(er)}$	-	7[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V
ICE5QR1680BG-1	$C_{o(er)}$	-	8[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V
ICE5QR0680BG-1	$C_{o(er)}$	-	24[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V

1) Not subject to production test, specified by design.
2) Measured in a typical flyback application.

5 CoolMOS™ performance characteristics

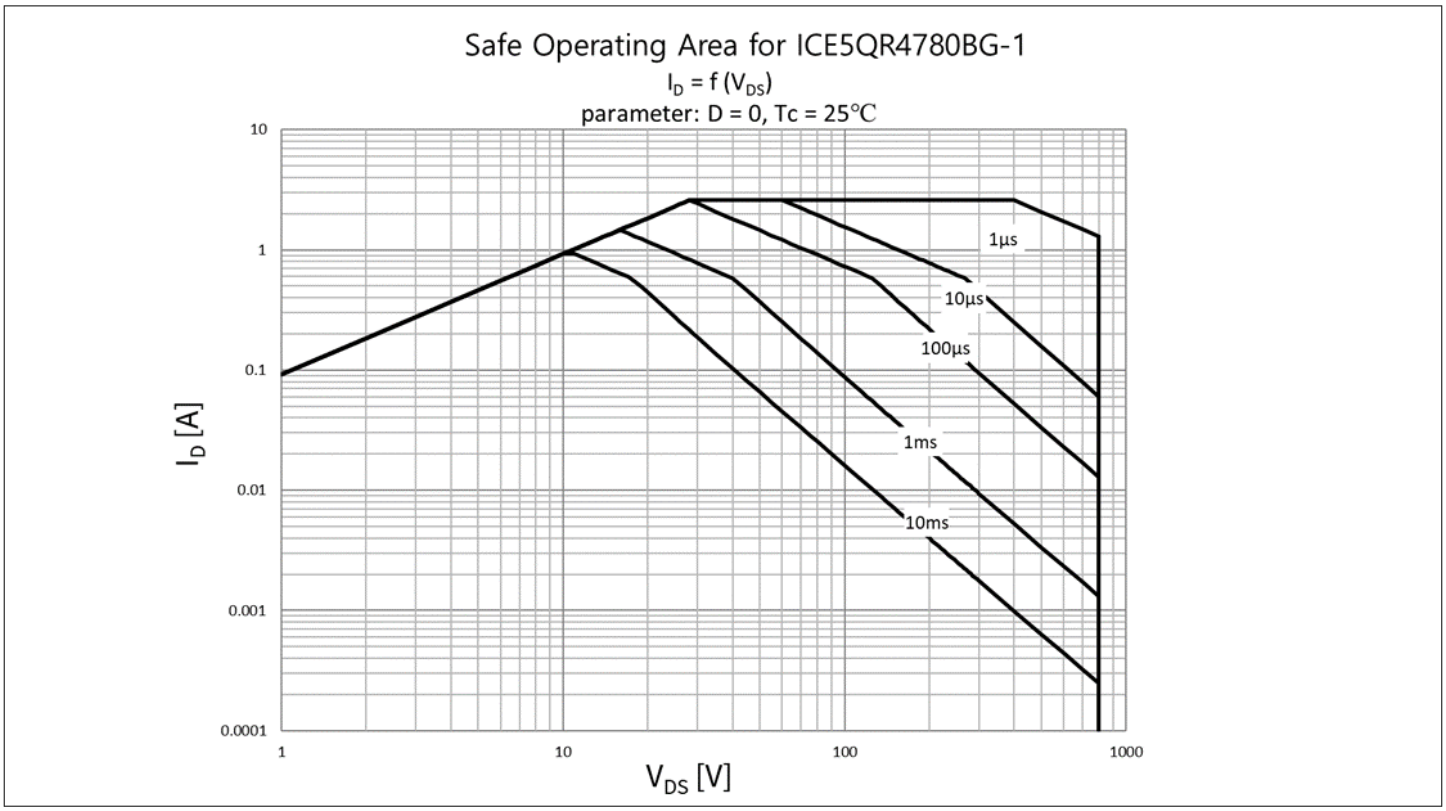


Figure 13 SOA for ICE5QR4780BG-1

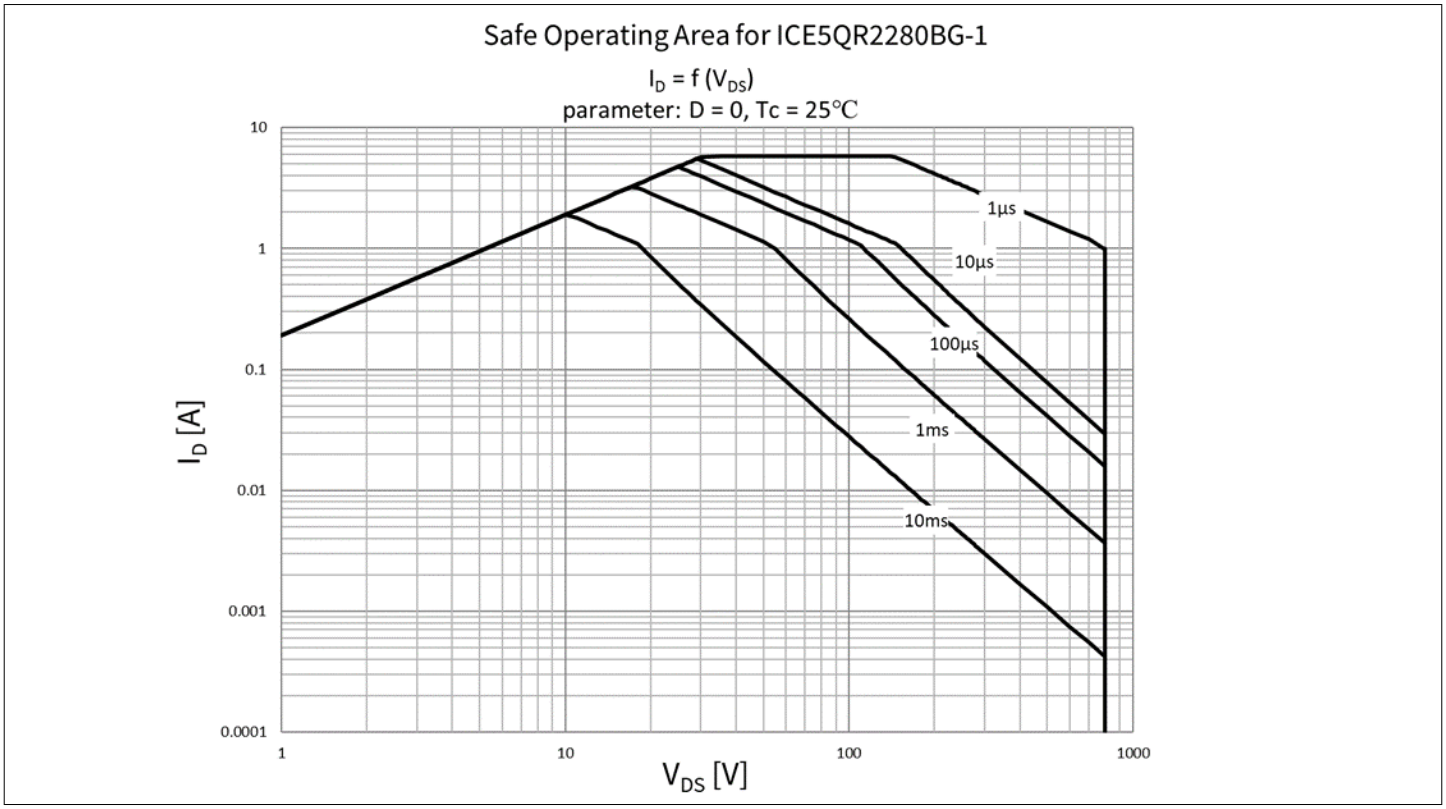


Figure 14 SOA for ICE5QR2280BG-1

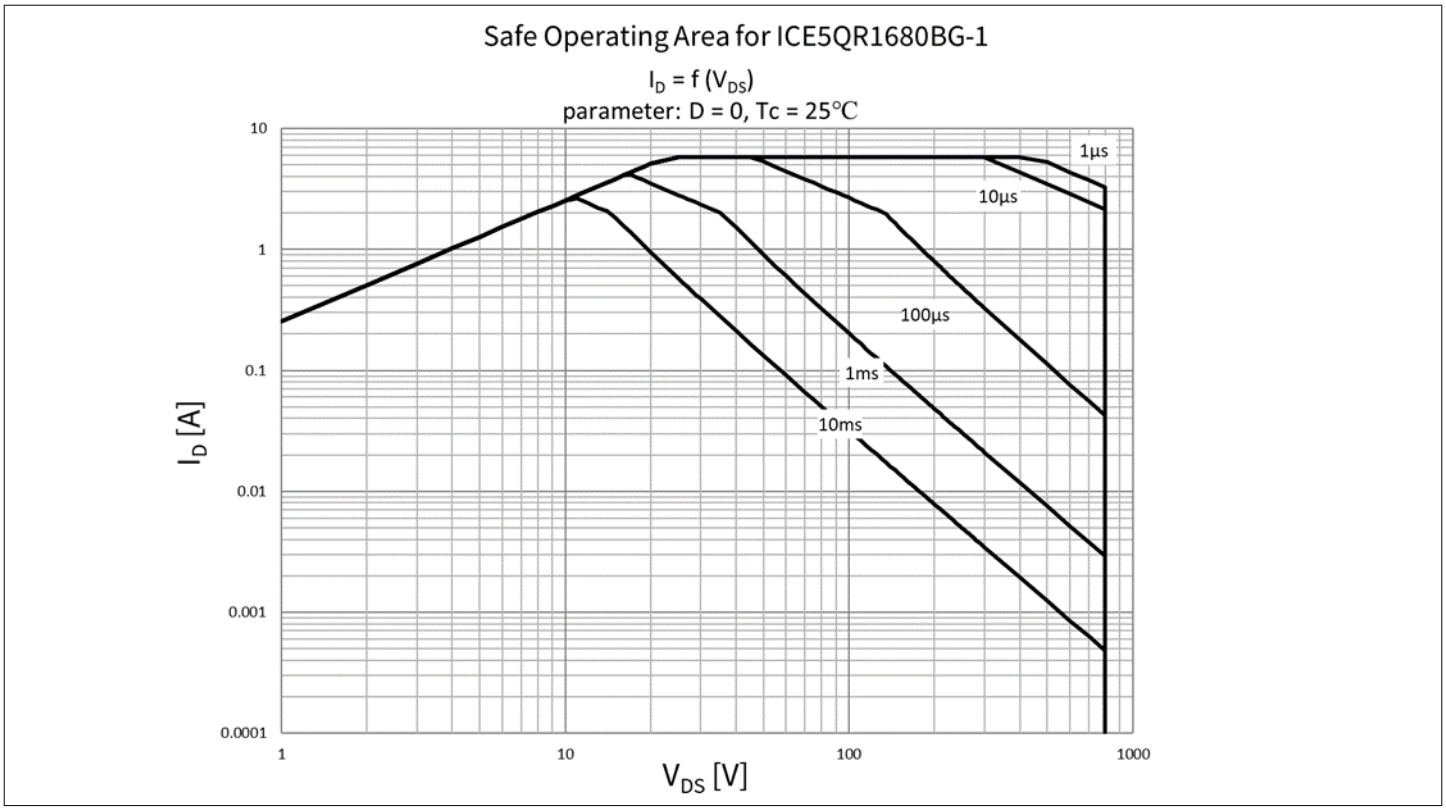


Figure 15 SOA for ICE5QR1680BG-1

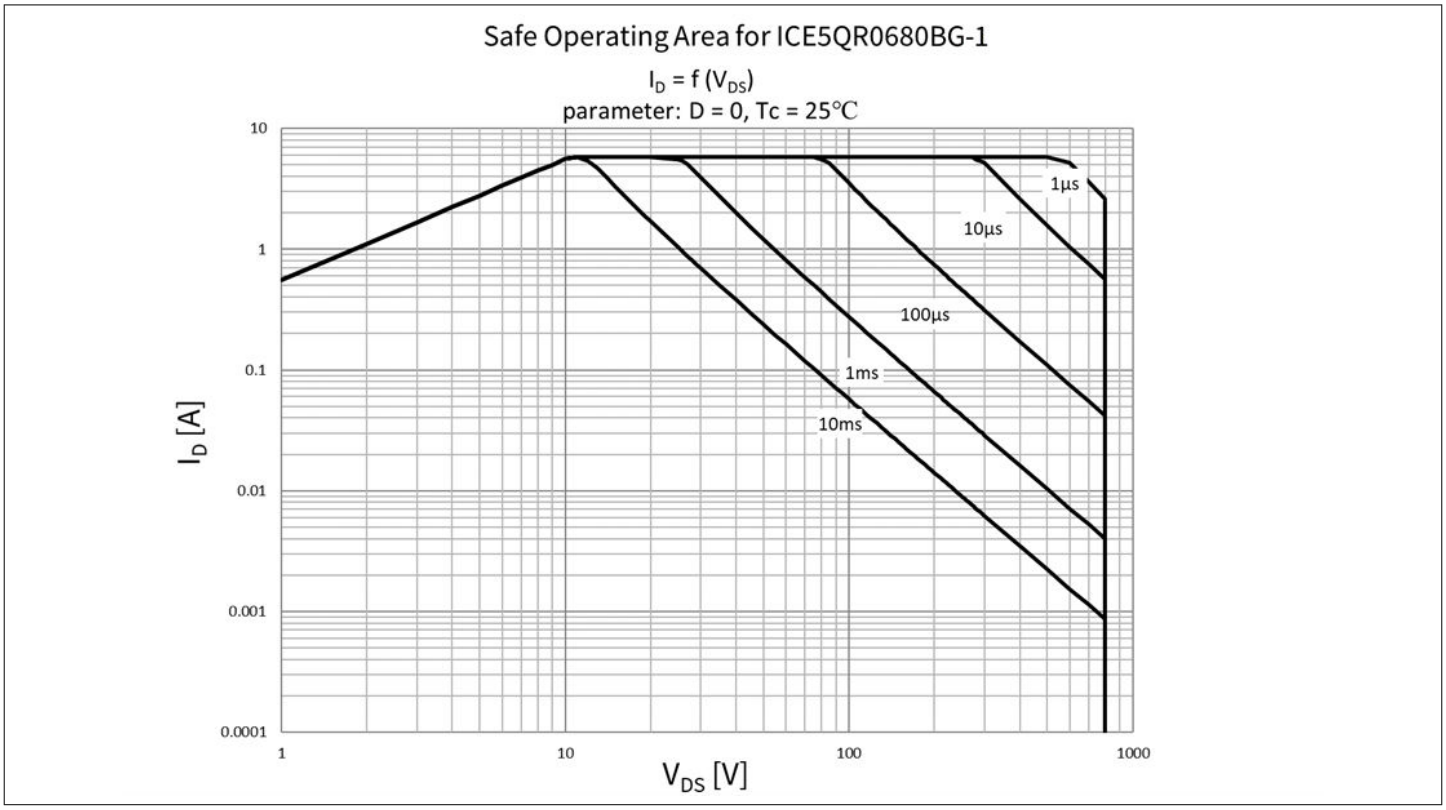


Figure 16 SOA for ICE5QR0680BG-1

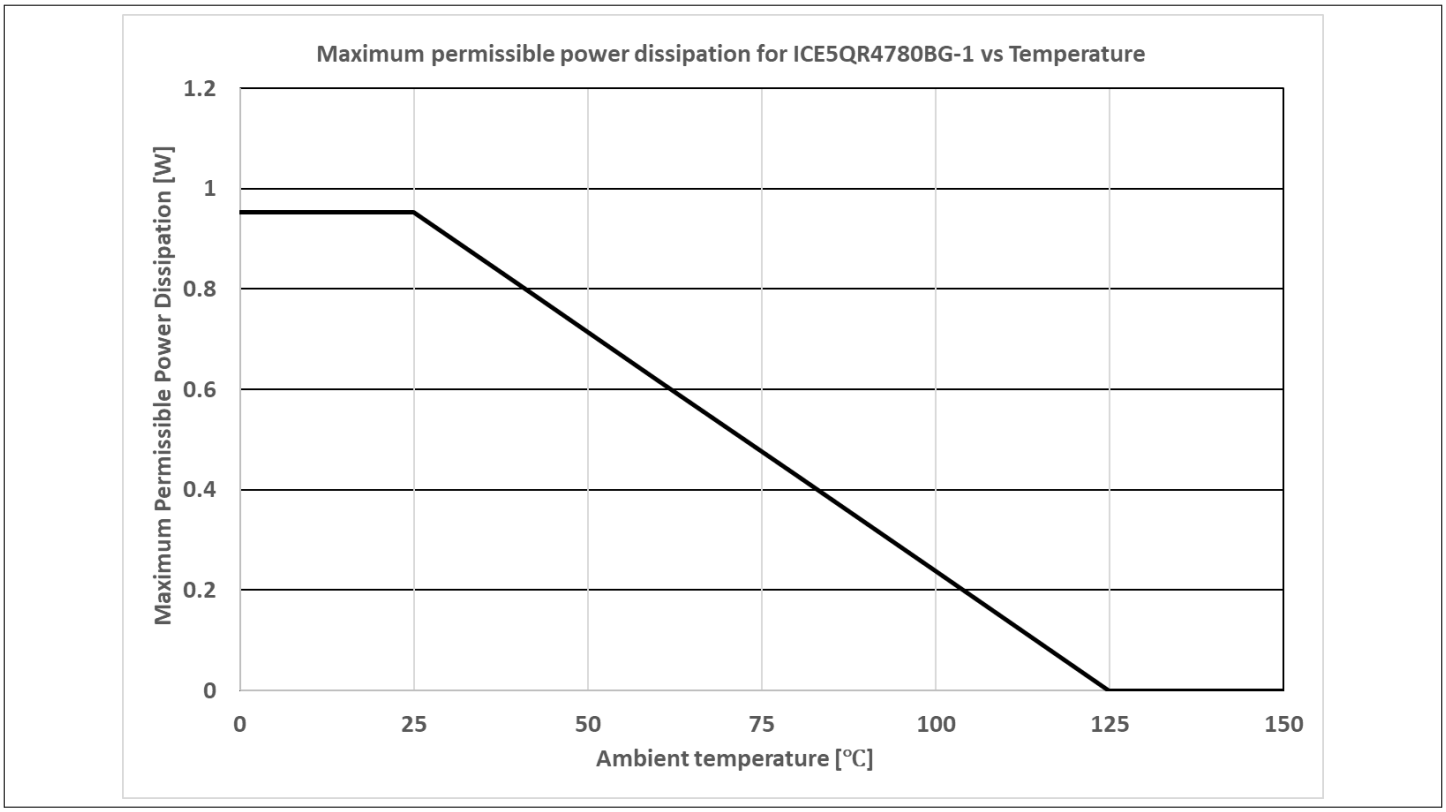


Figure 17 **Power dissipation of ICE5QR4780BG-1; $P_{tot}=f(T_a)$, (Maximum ratings as given in section 6 must not be exceeded)**

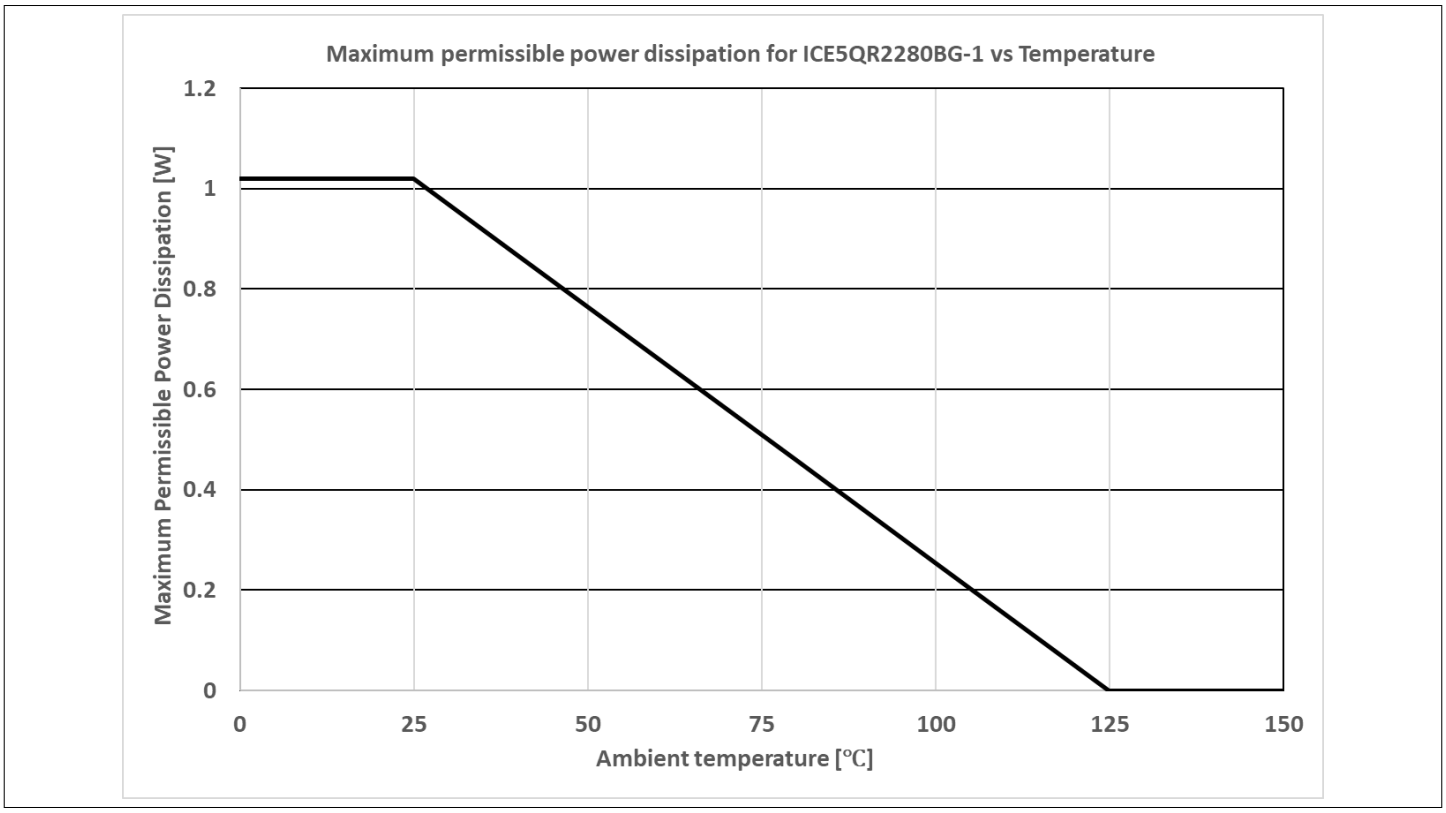


Figure 18 **Power dissipation of ICE5QR2280BG-1; $P_{tot}=f(T_a)$, (Maximum ratings as given in section 6 must not be exceeded)**

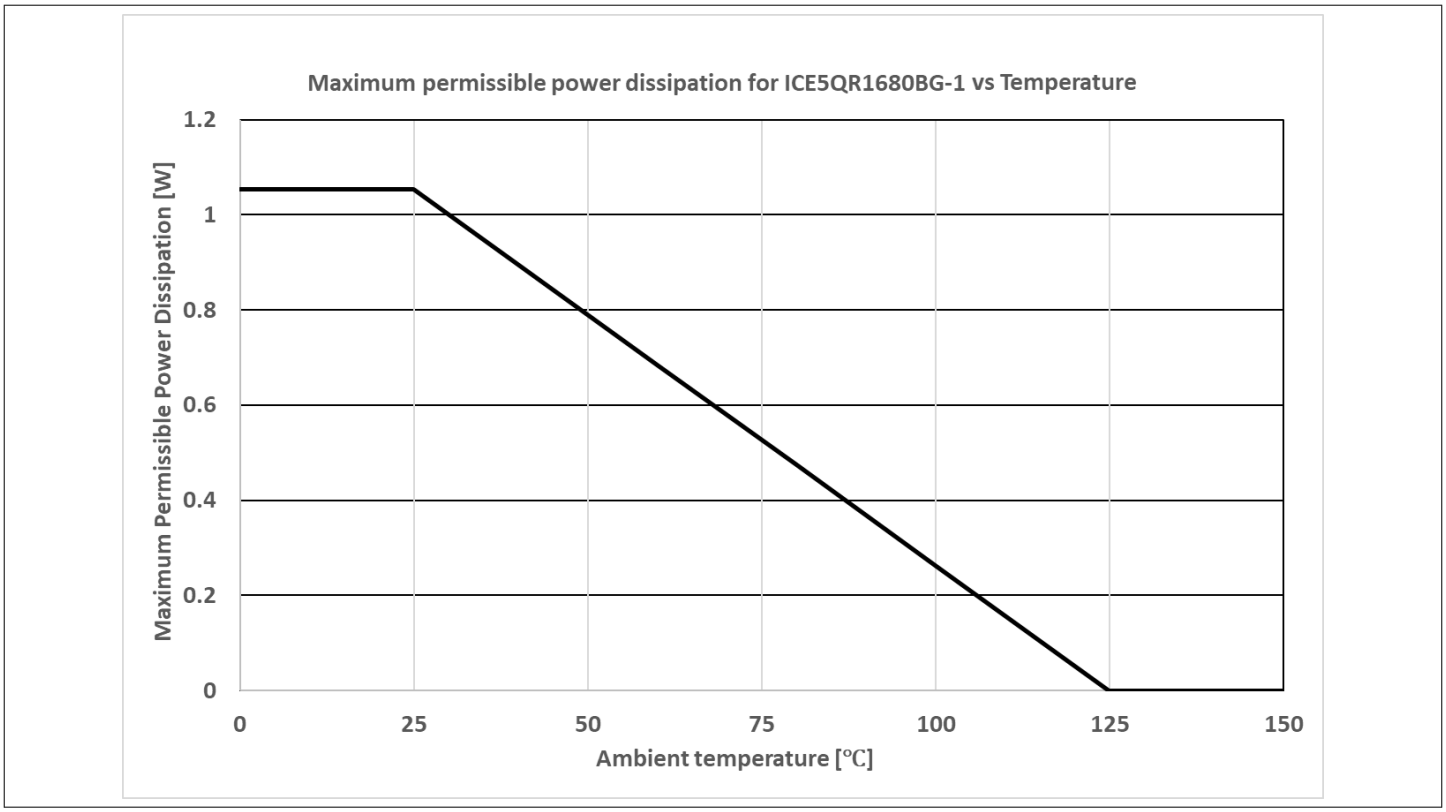


Figure 19 **Power dissipation of ICE5QR1680BG-1; $P_{tot}=f(T_a)$, (Maximum ratings as given in section 6 must not be exceeded)**

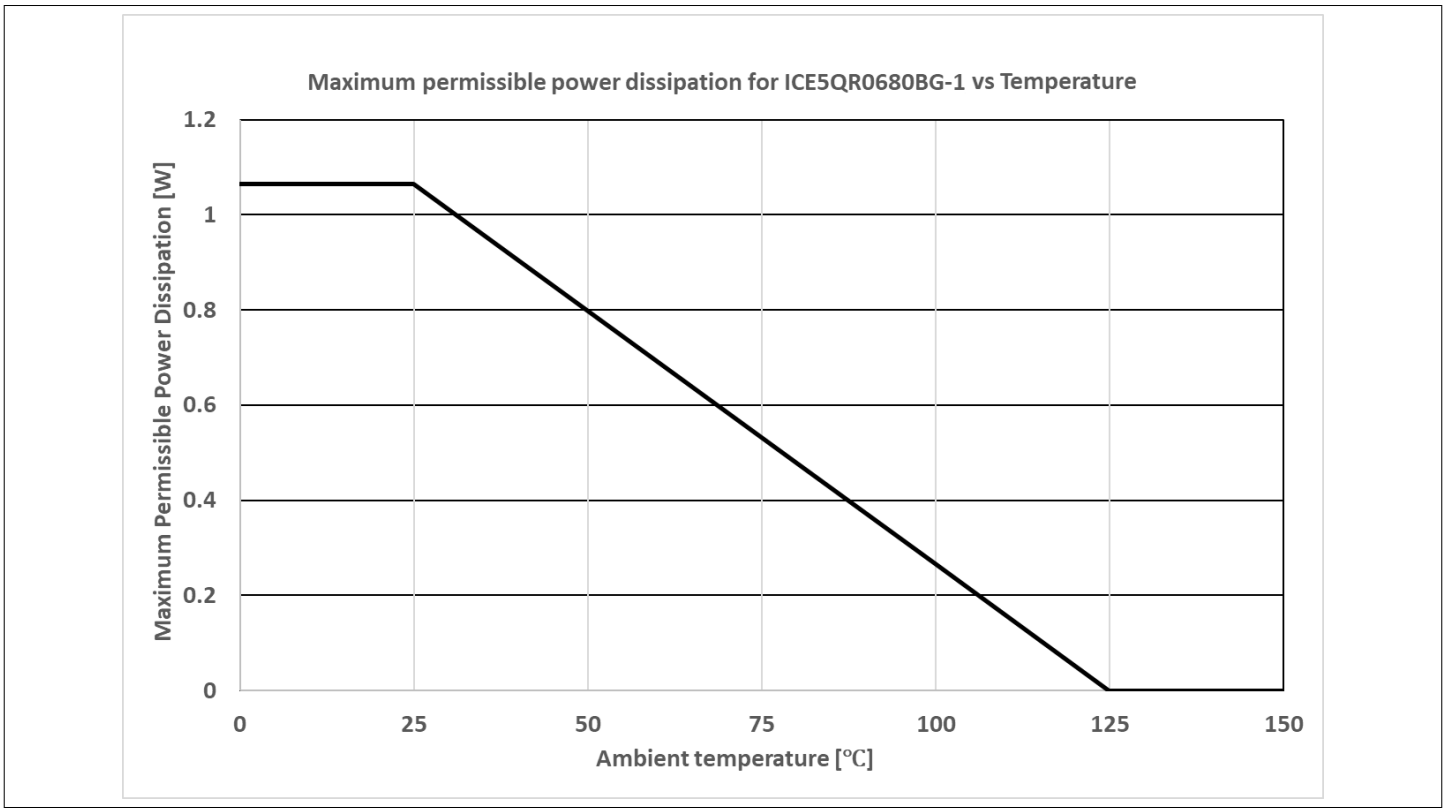


Figure 20 **Power dissipation of ICE5QR0680BG-1, $P_{tot}=f(T_a)$, (Maximum ratings as given in section 6 must not be exceeded)**

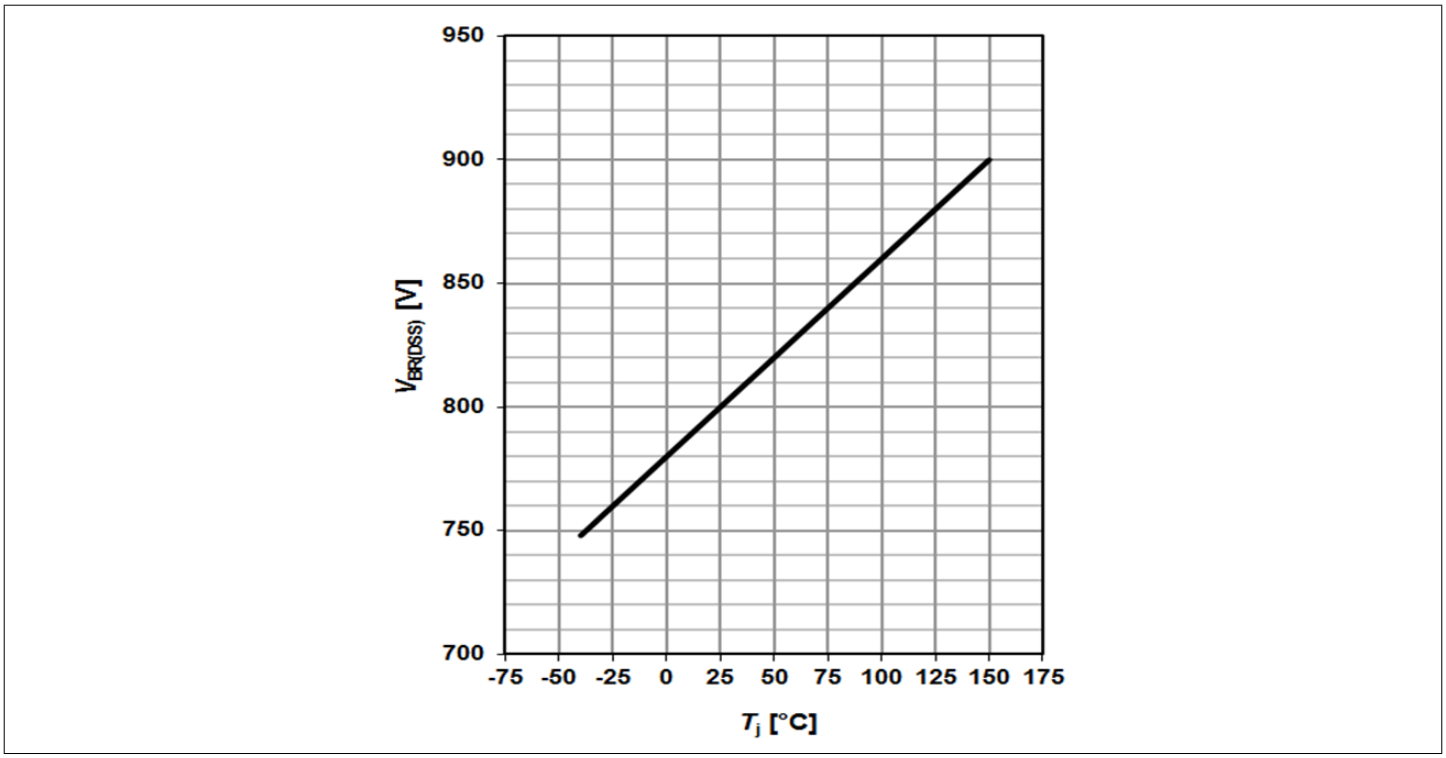


Figure 21 **Drain-source breakdown voltage ICE5QRxx80BG-1; $V_{BR(DSS)}=f(T_j)$, I_D=1 mA**

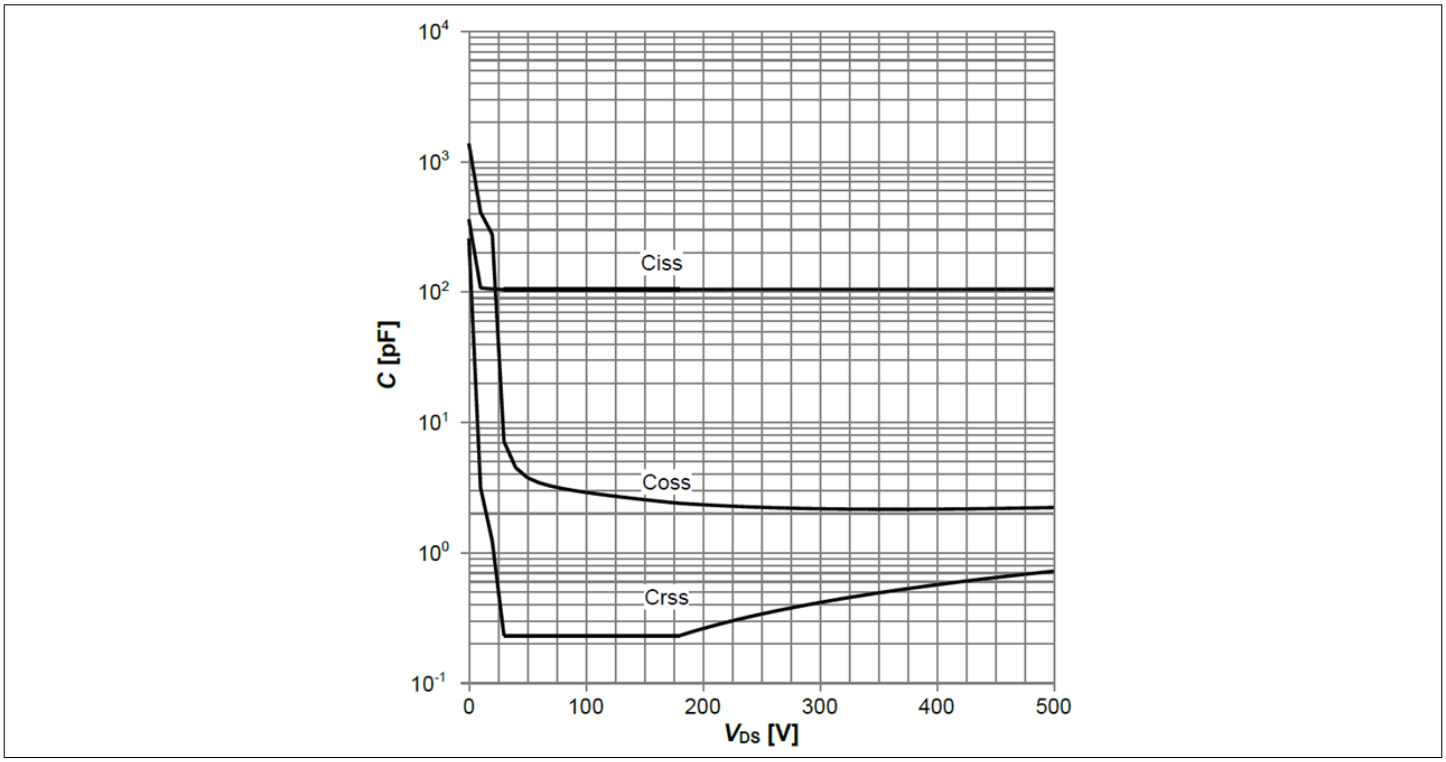


Figure 22 **Typical CoolMOS™ capacitances of ICE5QR4780BG-1; $C=f(V_{DS})$, (V_{GS}=0V; f=250 kHz)**

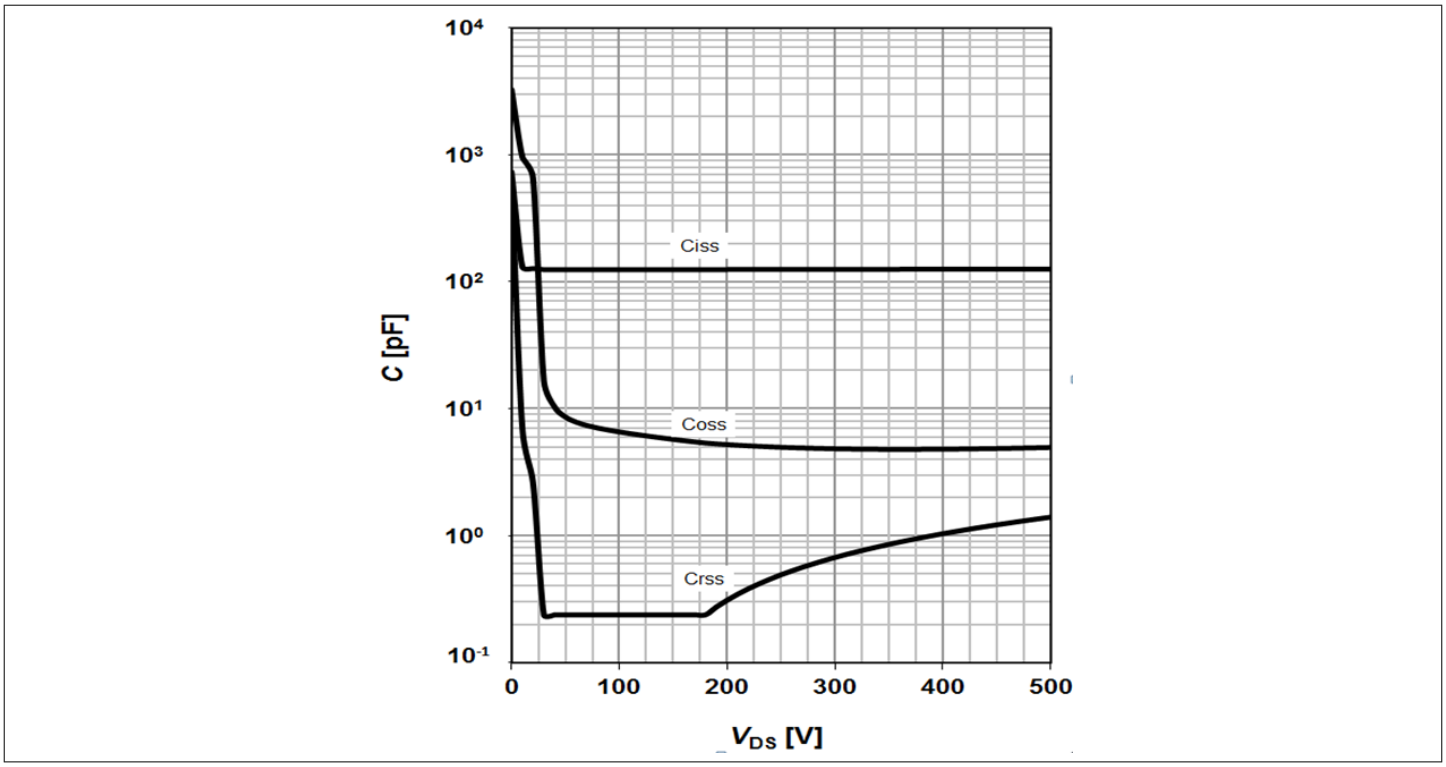


Figure 23 **Typical CoolMOS™ capacitances of ICE5QR2280BG-1; C=f(V_{DS}), (V_{GS}=0V; f=250 kHz)**

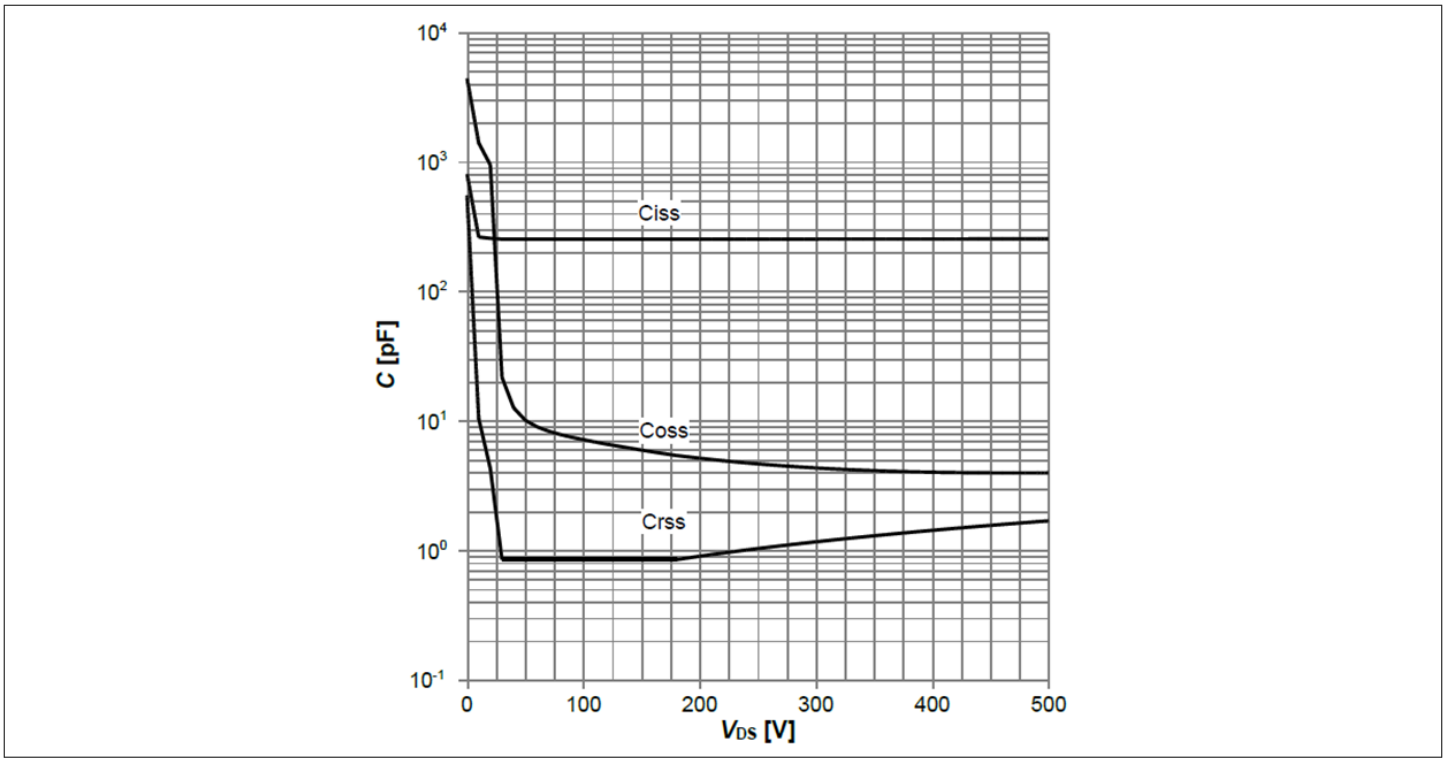


Figure 24 **Typical CoolMOS™ capacitances of ICE5QR1680BG-1; C=f(V_{DS}), (V_{GS}=0V; f=250 kHz)**

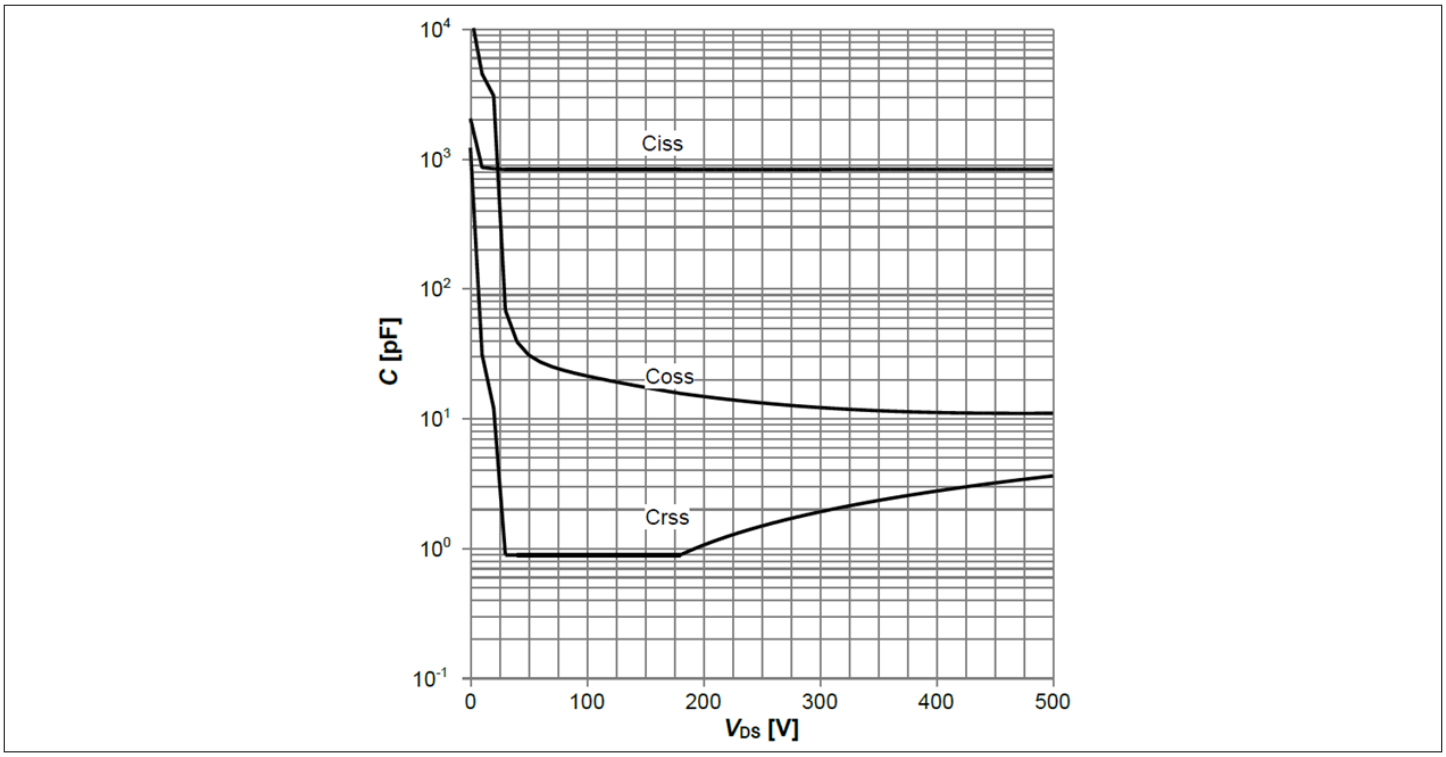


Figure 25 Typical CoolMOS™ capacitances of ICE5QR0680BG-1; C=f(V_{DS}), (V_{GS}=0V; f=250 kHz)

6 Maximum Output Power curve vs Temperature

The calculated output power curves giving the typical output power versus ambient temperature are shown below. The curves are derived based on a typical discontinuous mode flyback in an open frame design at T_a=50°C, T_j=125°C (integrated high voltage MOSFET), using minimum drain pin copper area in a 2 oz copper single sided PCB and steady state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purpose only. The actual power can vary depending on particular designs. In a power supply system, appropriate thermal design margins must be applied to make sure that the maximum ratings given in section 4.1 are respected at all times.

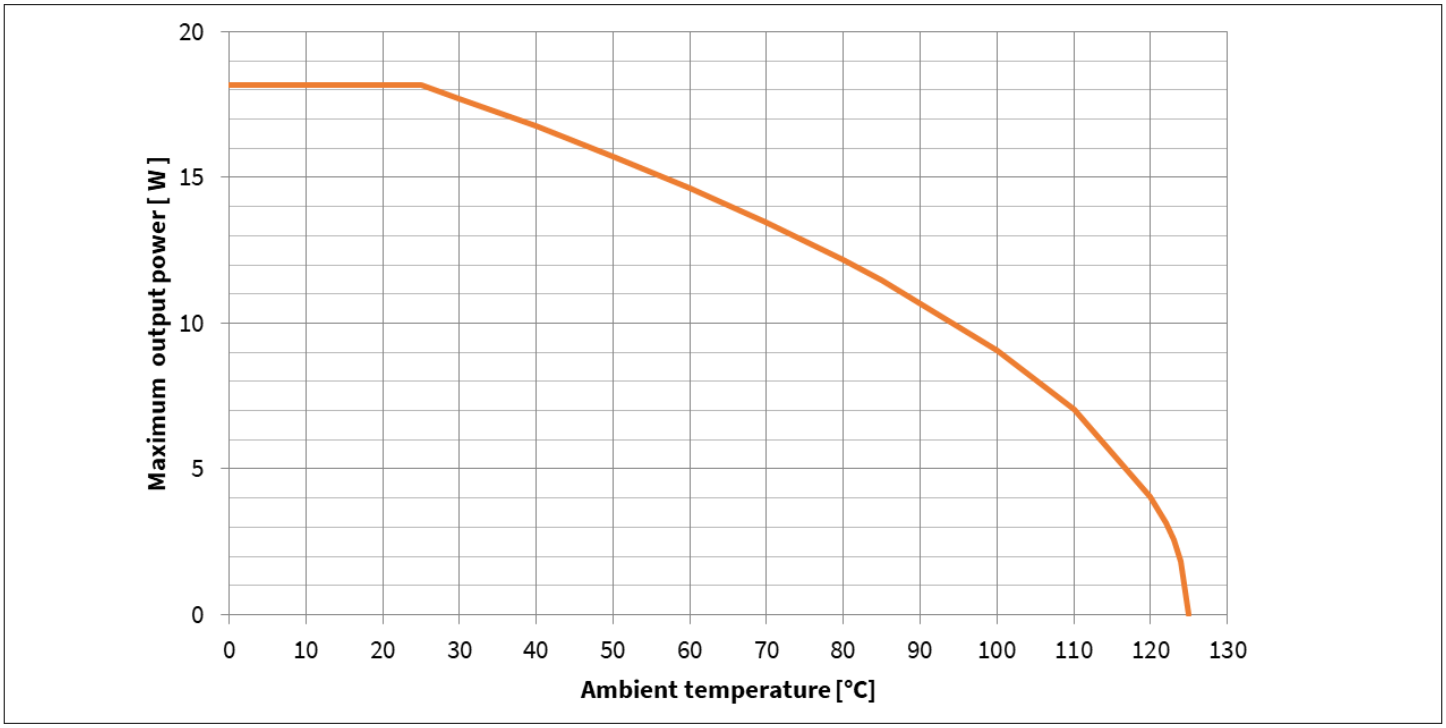


Figure 26 Maximum output power vs Temperature for ICE5QR4780BG-1 (AC mains voltage: 85~300 VAC)

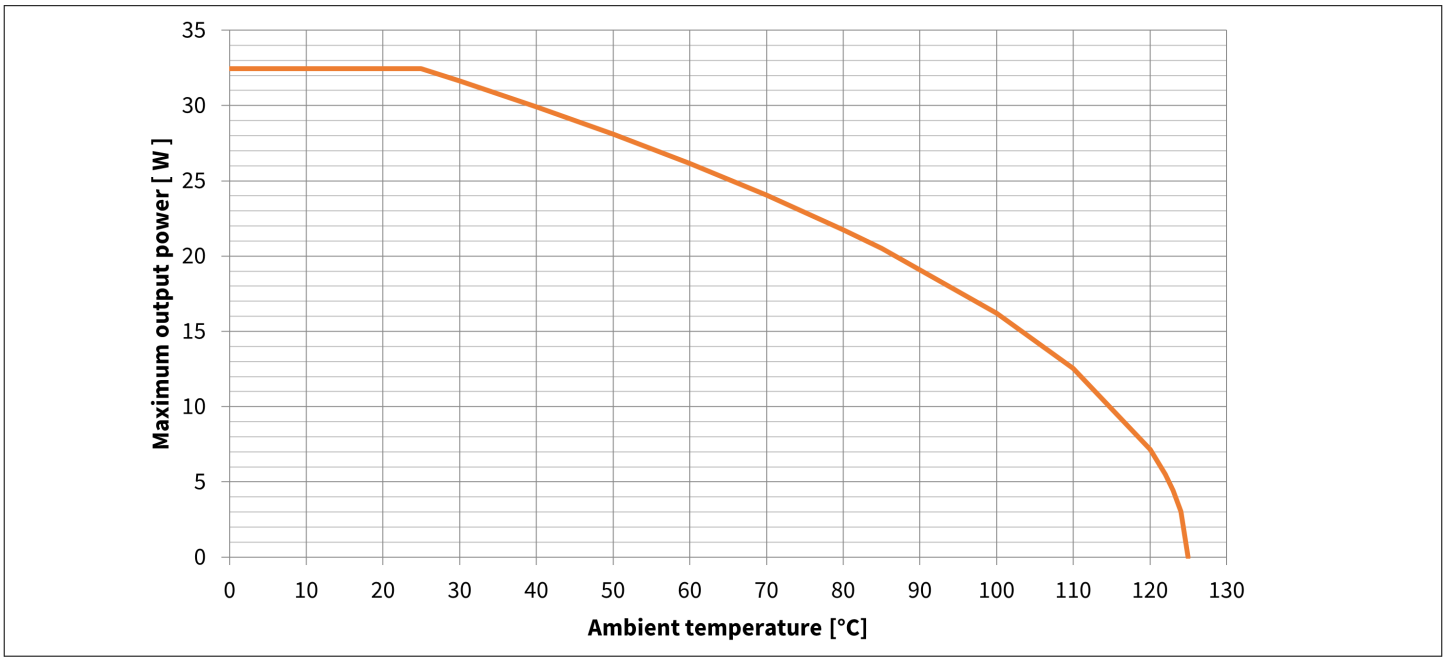


Figure 27 Maximum output power vs Temperature for ICE5QR4780BG-1 (AC mains voltage: 220 VAC)

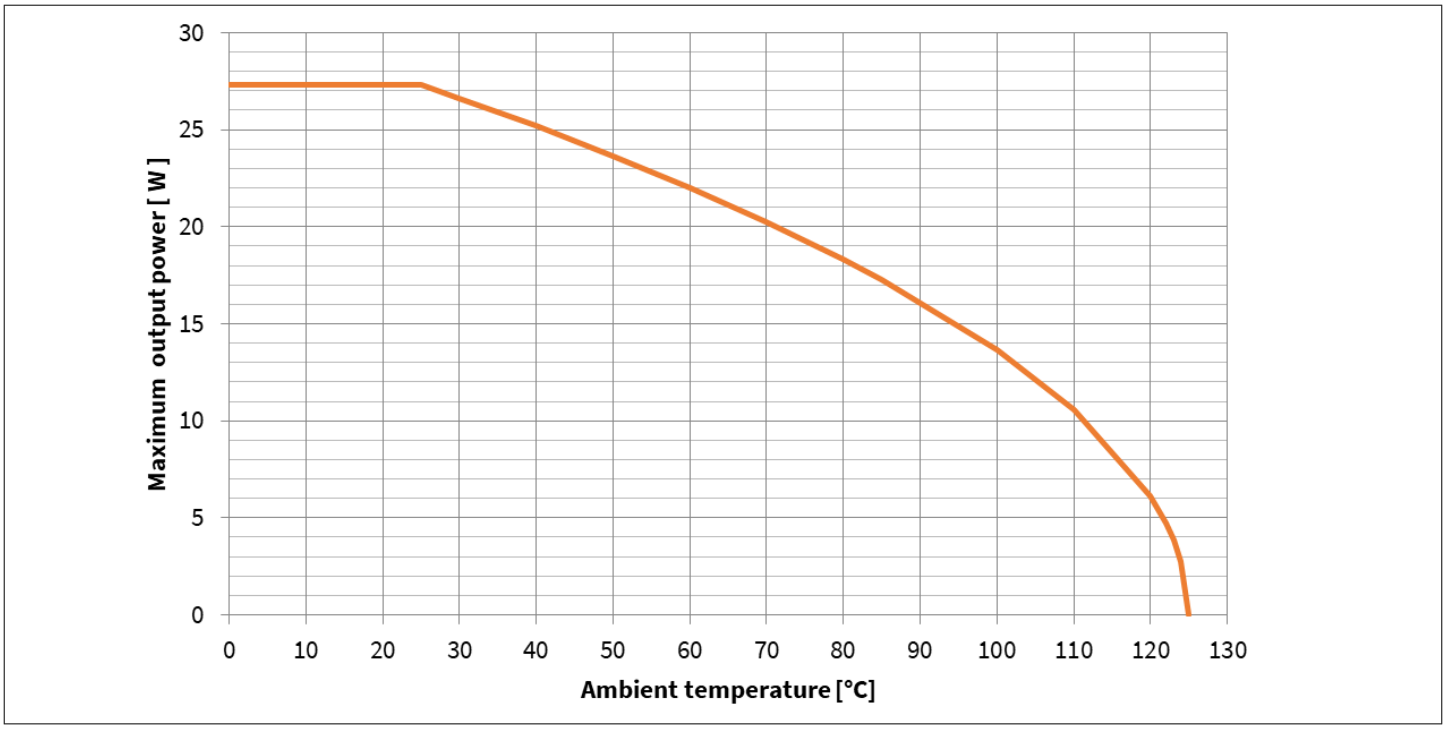


Figure 28 **Maximum output power vs Temperature for ICE5QR2280BG-1 (AC mains voltage: 85~300 VAC)**

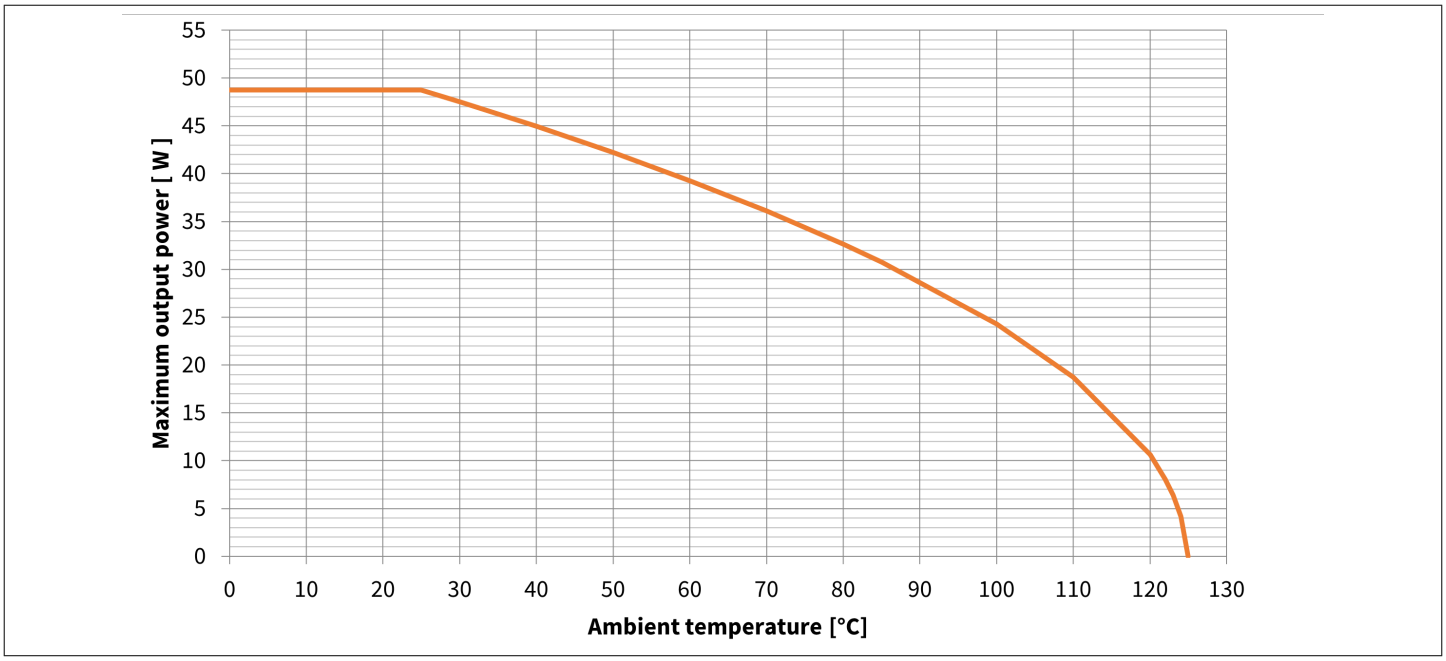


Figure 29 **Maximum output power vs Temperature for ICE5QR2280BG-1 (AC mains voltage: 220 VAC)**

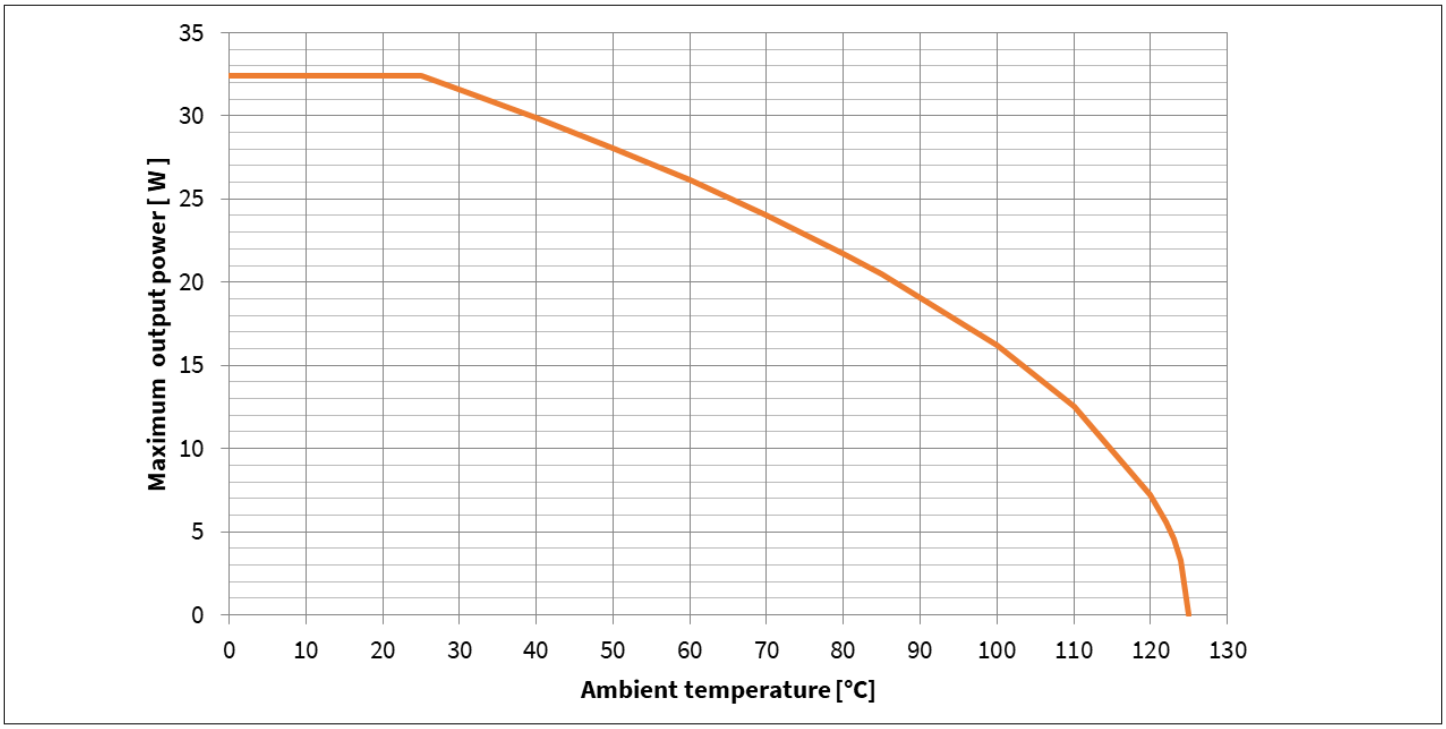


Figure 30 **Maximum output power vs Temperature for ICE5QR1680BG-1 (AC mains voltage: 85~300 VAC)**

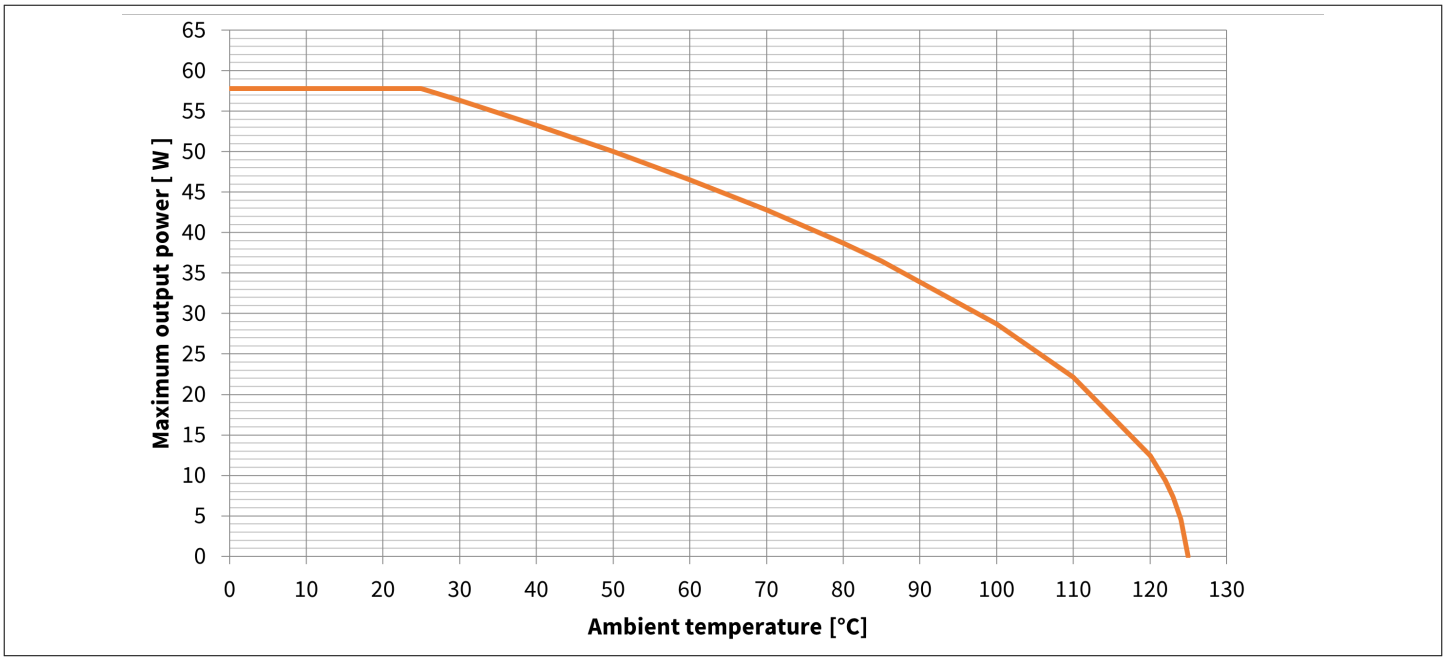


Figure 31 **Maximum output power vs Temperature for ICE5QR1680BG-1(AC mains voltage: 220 VAC)**

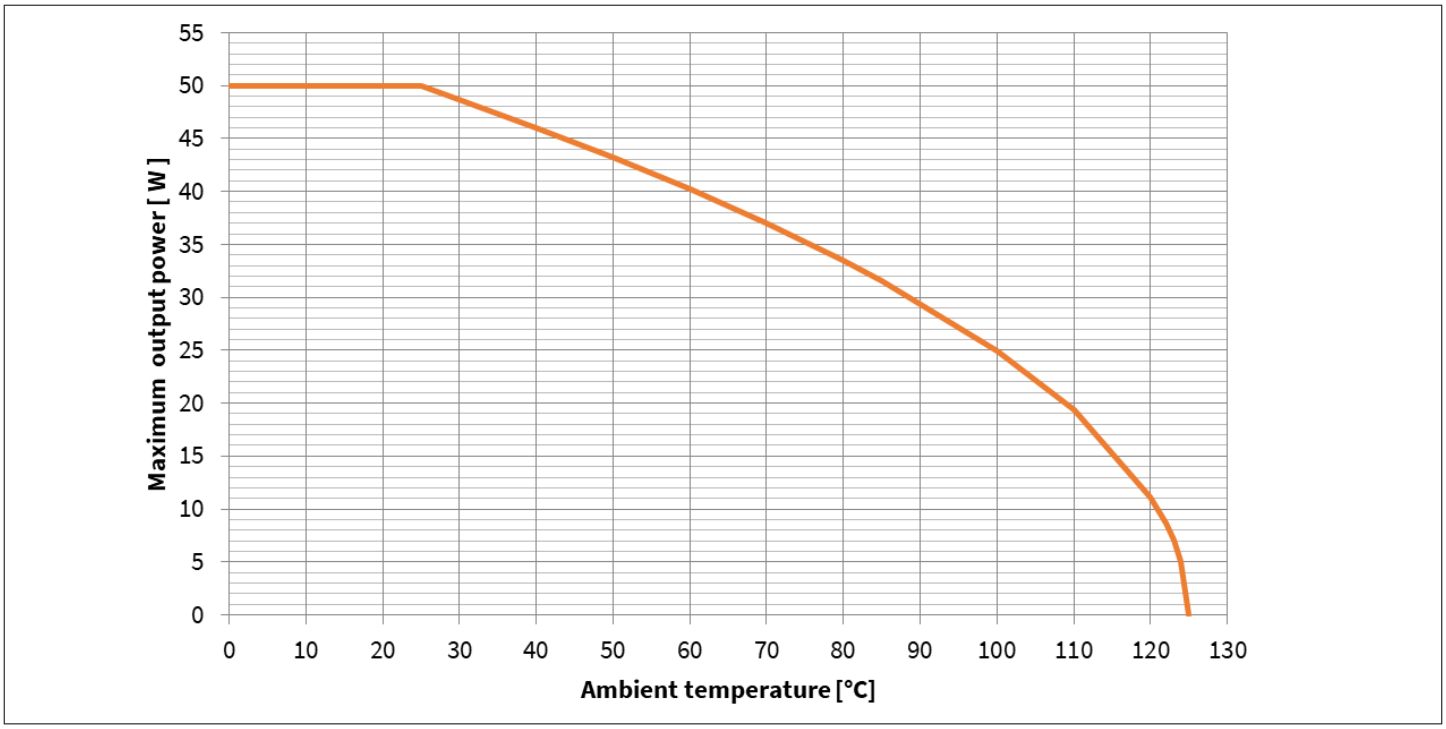


Figure 32 **Maximum output power vs Temperature for ICE5QR0680BG-1 (AC mains voltage: 85~300 VAC)**

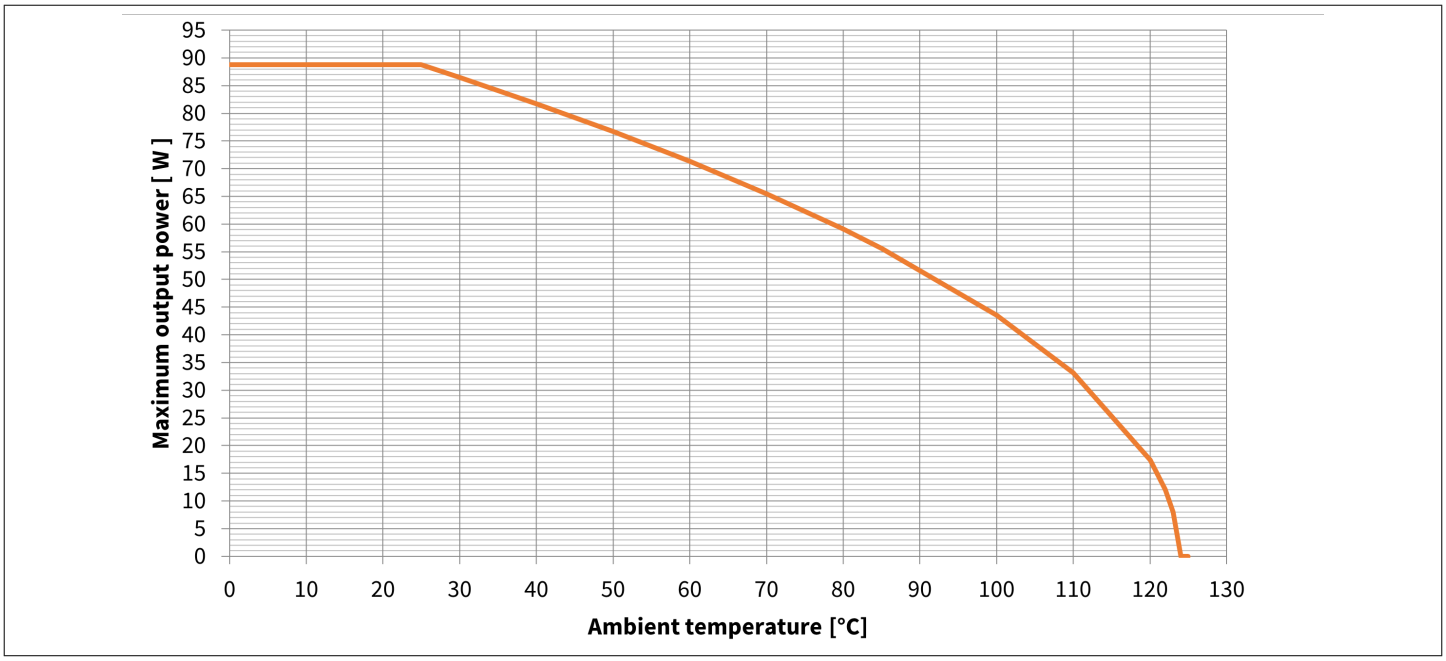
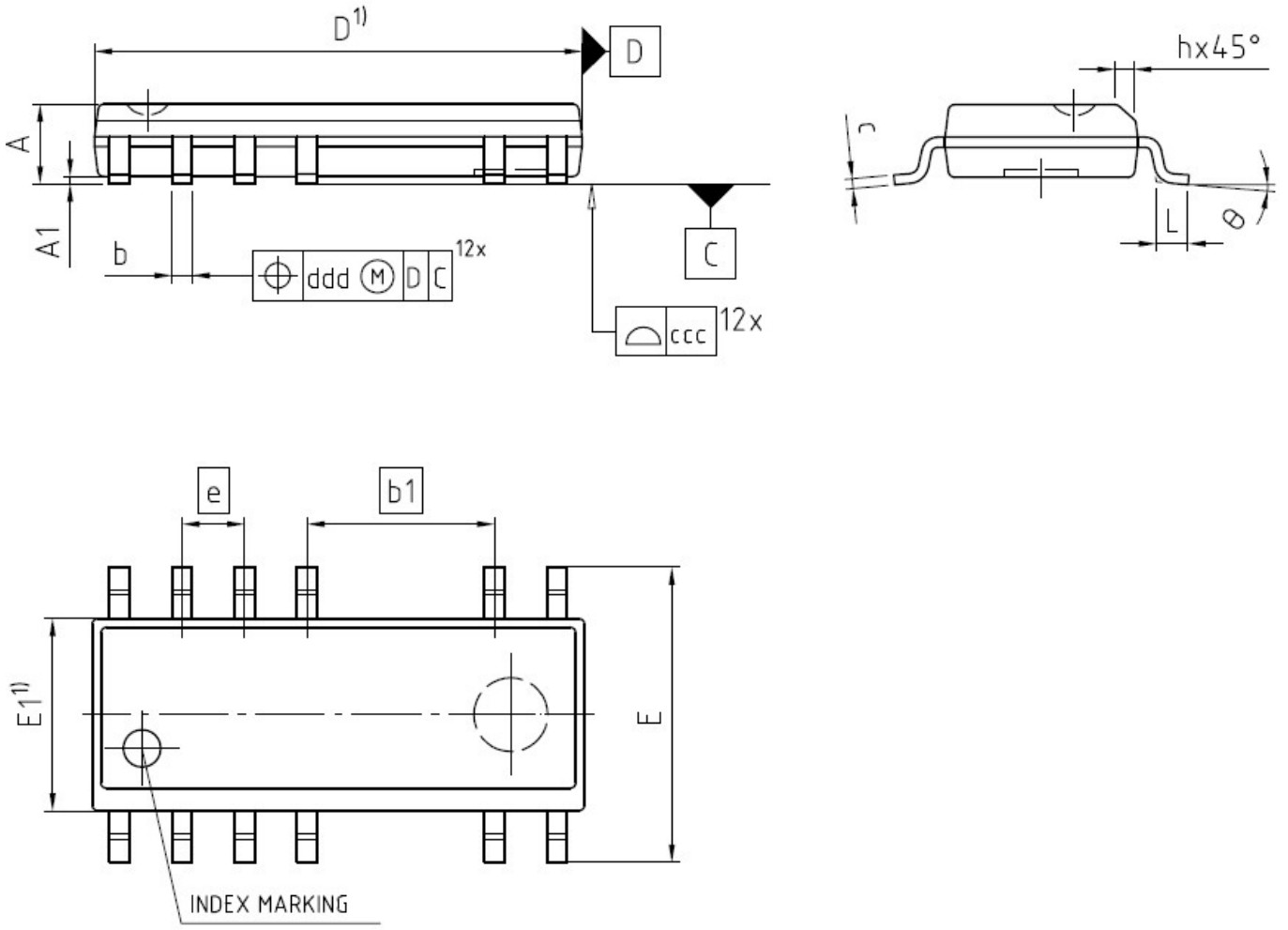


Figure 33 **Maximum output power vs Temperature for ICE5QR0680BG-1 (AC mains voltage: 220 VAC)**

7 Package information



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
b	0.35	0.51	0.014	0.020
b1	3.81 (BSC)		0.150 (BSC)	
c	0.19	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 (BSC)		0.050 (BSC)	
N	12		12	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
θ	-	8°	-	8°
ccc	0.10		0.004	
ddd	0.20		0.008	

DOCUMENT NO.
Z8B00168485

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

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REVISION
02

Figure 34 Package information

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e., Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

7.1 Marking

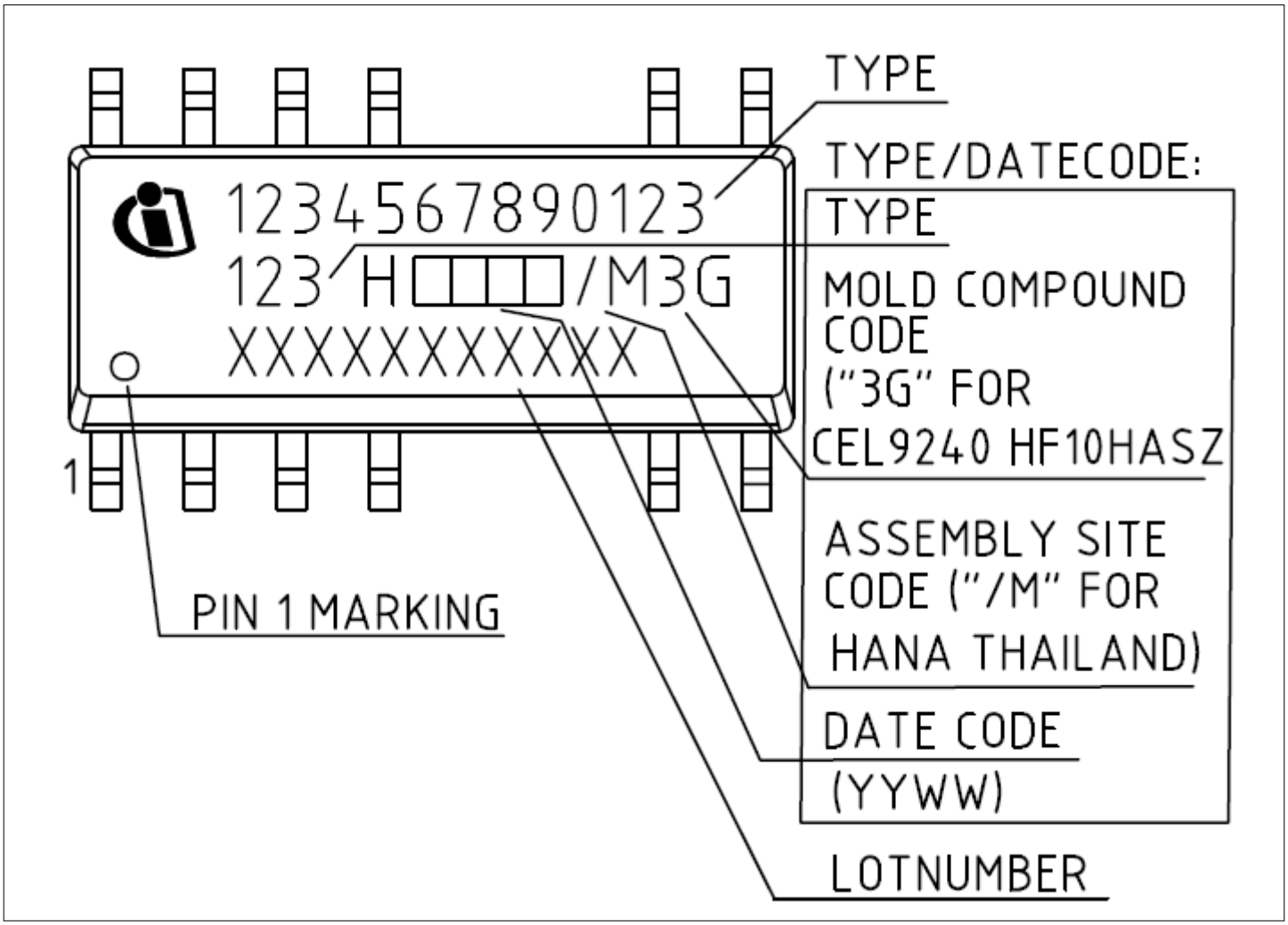

Figure 35 Marking on package PG-DSO-12-24

8 Revision history

Revision	Date	Changes
Rev 1.0	2024-09-02	Initial release

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