CoolSET™ 5th Generation Fixed Frequency Plus - in DIP-7 Package

Features

- Integrated 700 V/ 800 V/ 950 V avalanche rugged CoolMOS™
- Active Burst Mode with selectable entry and exit standby power to reach the lowest standby power <100 mW
- Frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- Frequency jitter and soft gate driving for low EMI
- Integrated error amplifier to support direct feedback in non-isolated flyback and buck topologies
- Increased pin voltage rating for ease of system design
- Comprehensive protection and most protections are in auto restart mode
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

Potential applications

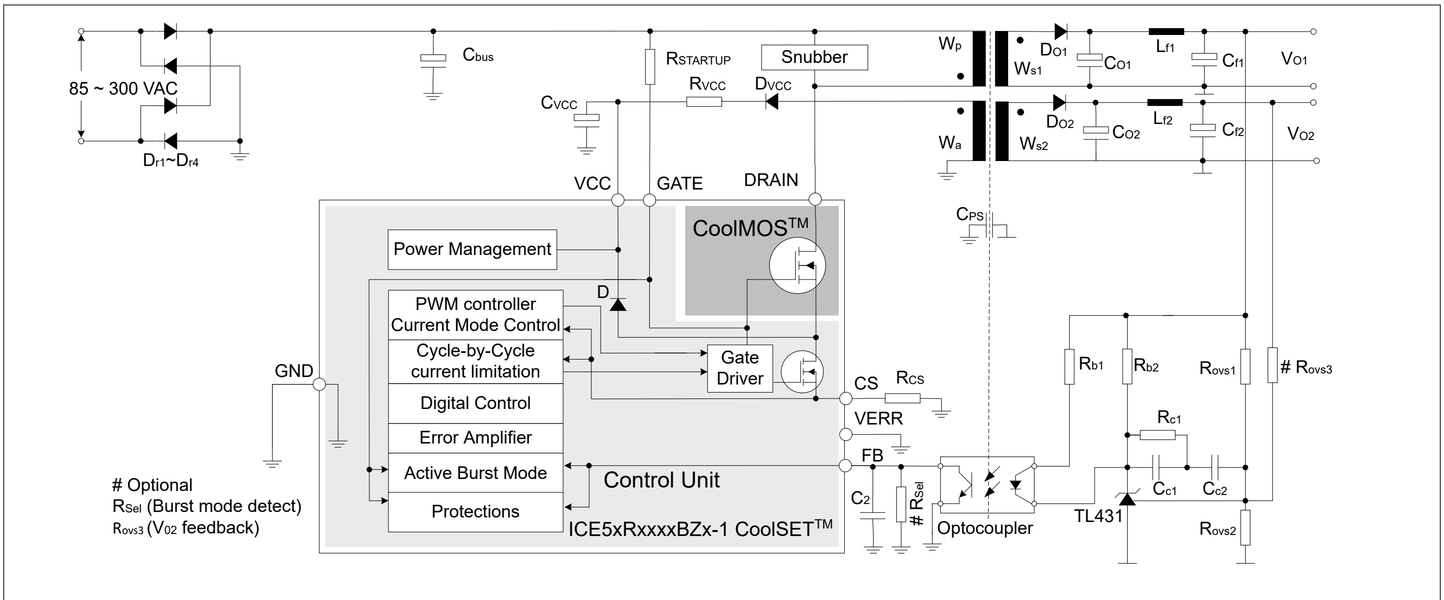
- Auxiliary power supply for home appliances/white goods, TV, PC & server, smart metering
- Blu-ray player, set-top box & LCD/LED monitor

Product validation

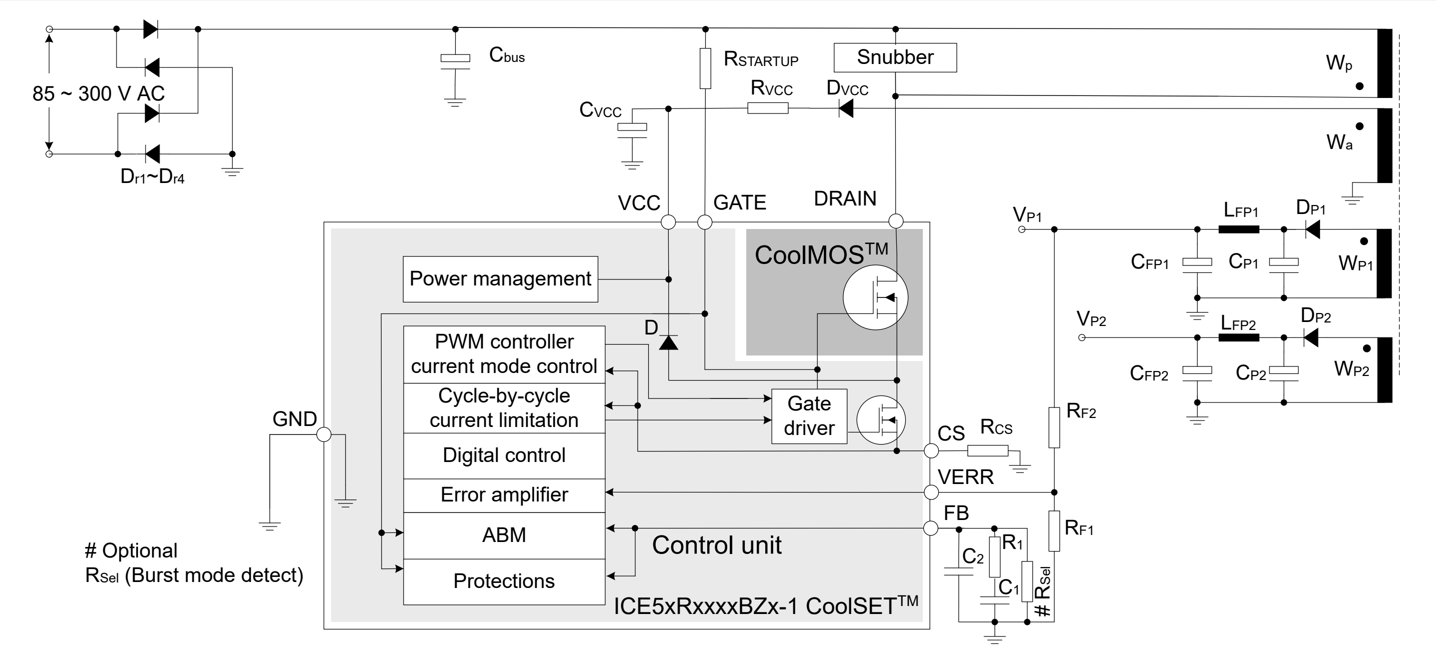
Product validation according to JEDEC standard.

Description

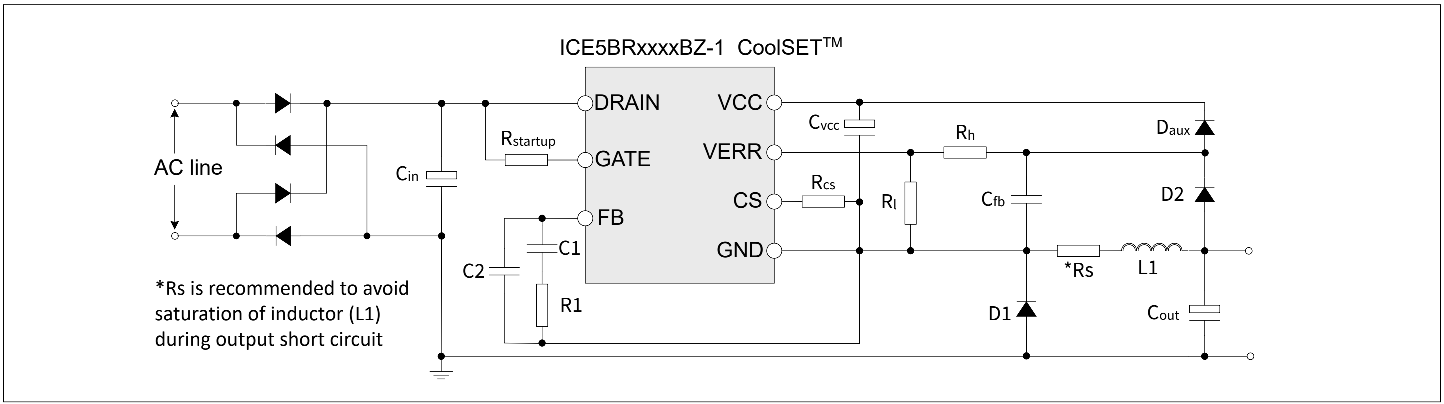
The ICE5xRxxxxBZx-1 is the CoolSET™ 5th Generation Fixed Frequency Plus of integrated power IC optimized for off-line switch mode power supply in cascode configuration. The CoolSET™ package has 2 separate chips inside; one is controller chip and the other is a 700 V/ 800 V/ 950 V CoolMOS™ chip. The cascode configuration helps achieve fast startup. The frequency reduction with soft gate driving and frequency jitter operation offer lower EMI and better efficiency. The selectable entry and exit standby power ABM enables flexibility and ultra-low power consumption at standby mode with small and controllable output voltage ripple. The product has a wide operating range (10.0 ~ 32.0 V) of IC power supply and lower power consumption. The numerous protection functions support the power supply system in failure situations. All these make the CoolSET™ 5th Generation Fixed Frequency Plus series an outstanding integrated power stage fixed frequency flyback and buck converter in the market.



Typical application in an isolated fixed frequency flyback converter using TL431 and an optocoupler



Typical application in a non-isolated flyback converter using an integrated error amplifier



Typical application in non-isolated buck

Table 1 **Output power of CoolSET™ 5th Generation Fixed Frequency Plus in flyback design**

Type	Package	Marking	VDS	Fsw	R_{DSon}[1]	220 V AC ±20%[2] at DCM	85-300 V AC[2] at DCM	85-300 V AC[2] at CCM
ICE5AR4770BZS-1	PG-DIP-7	5AR4770BZS-1	700 V	100 kHz	4.73 Ω	26.5 W	14.5 W	16 W
ICE5AR4780BZS-1	PG-DIP-7	5AR4780BZS-1	800 V	100 kHz	4.13 Ω	27.5 W	15 W	16.5 W
ICE5BR4780BZ-1	PG-DIP-7	5BR4780BZ-1	800 V	65 kHz	4.13 Ω	27.5 W	15 W	16.5 W
ICE5AR3995BZ-1	PG-DIP-7	5AR3995BZ-1	950 V	100 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR3995BZ-1	PG-DIP-7	5BR3995BZ-1	950 V	65 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR2280BZ-1	PG-DIP-7	5BR2280BZ-1	800 V	65 kHz	2.13 Ω	40 W	22 W	24 W
ICE5AR0680BZS-1	PG-DIP-7	5AR0680BZS-1	800 V	100 kHz	0.71 Ω	66 W	39 W	41 W

1) Typically at T_j = 25°C (inclusive of low side MOSFET).

2) Calculated maximum output power rating in an open frame design at T_a = 50°C, T_j = 125°C (integrated high voltage MOSFET) and using minimum drain pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purpose only. The actual power can vary depending on the designs. Contact a technical expert from Infineon® for more information.

Table 2 **Output current of CoolSET™ 5th Generation Fixed Frequency Plus in non-isolated buck design**

Type	Package	Marking	V_{DS}	Fsw	R_{DSon}[1]	85-265 V AC[3] at DCM	Typical output voltage
ICE5BR4780BZ-1	PG-DIP-7	5BR4780BZ-1	800 V	65 kHz	4.13 Ω	450 mA	15 V
ICE5BR3995BZ-1	PG-DIP-7	5BR3995BZ-1	950 V	65 kHz	3.46 Ω	550 mA	
ICE5BR2280BZ-1	PG-DIP-7	5BR2280BZ-1	800 V	65 kHz	2.13 Ω	700 mA	

Infineon® recommends the 65 kHz variant for a non-isolated Buck converter.

1) Typically at T_j = 25°C (inclusive of low side MOSFET).

3) Calculated maximum output current rating in an open frame design at T_a = 50°C, T_j = 125°C (integrated high voltage MOSFET) and using minimum $100mm^2$ drain pin copper area in a 2 oz copper single-sided PCB. The output current figure is for selection purpose only. The actual current can vary depending on the designs. Contact a technical expert from Infineon® for more information.

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1 Pin configuration and functionality

The pin configuration is shown below and the functions are described in Table 3.

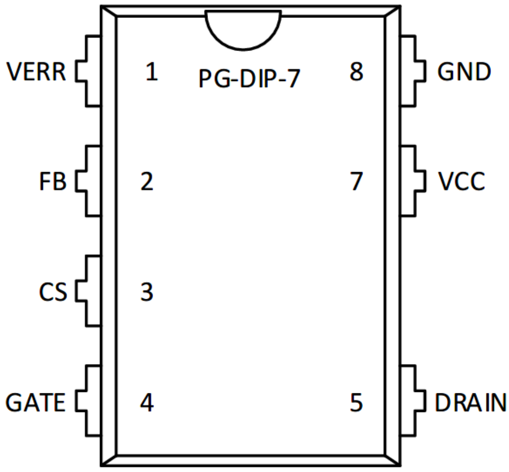


Figure 1 **Pin configuration**

Table 3 **Pin definitions and functions**

Pin	Symbol	Function
1	VERR	Error amplifier VERR pin is internally connected to the transconductance error amplifier for non-isolated flyback application. Connect this pin to GND for isolated flyback application.
2	FB	Feedback and ABM entry/exit control FB pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
3	CS	Current sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
4	GATE	Gate driver output The GATE pin is connected to the Gate of the internal CoolMOS™ and additionally, a pull up resistor is connected from bus voltage to turn on the internal CoolMOS™ for charging up the VCC capacitor during startup.
5	DRAIN	DRAIN(Drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™.
7	VCC	VCC(Positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	Ground The GND pin is the common ground of the controller.

2 Representative block diagram

***Note**: Junction temperature of the controller chip is sensed for over temperature protection. The CoolMOS™ is a separate chip from the controller chip in the same package. Please refer to the design guide and/or consult a technical expert for the proper thermal design*

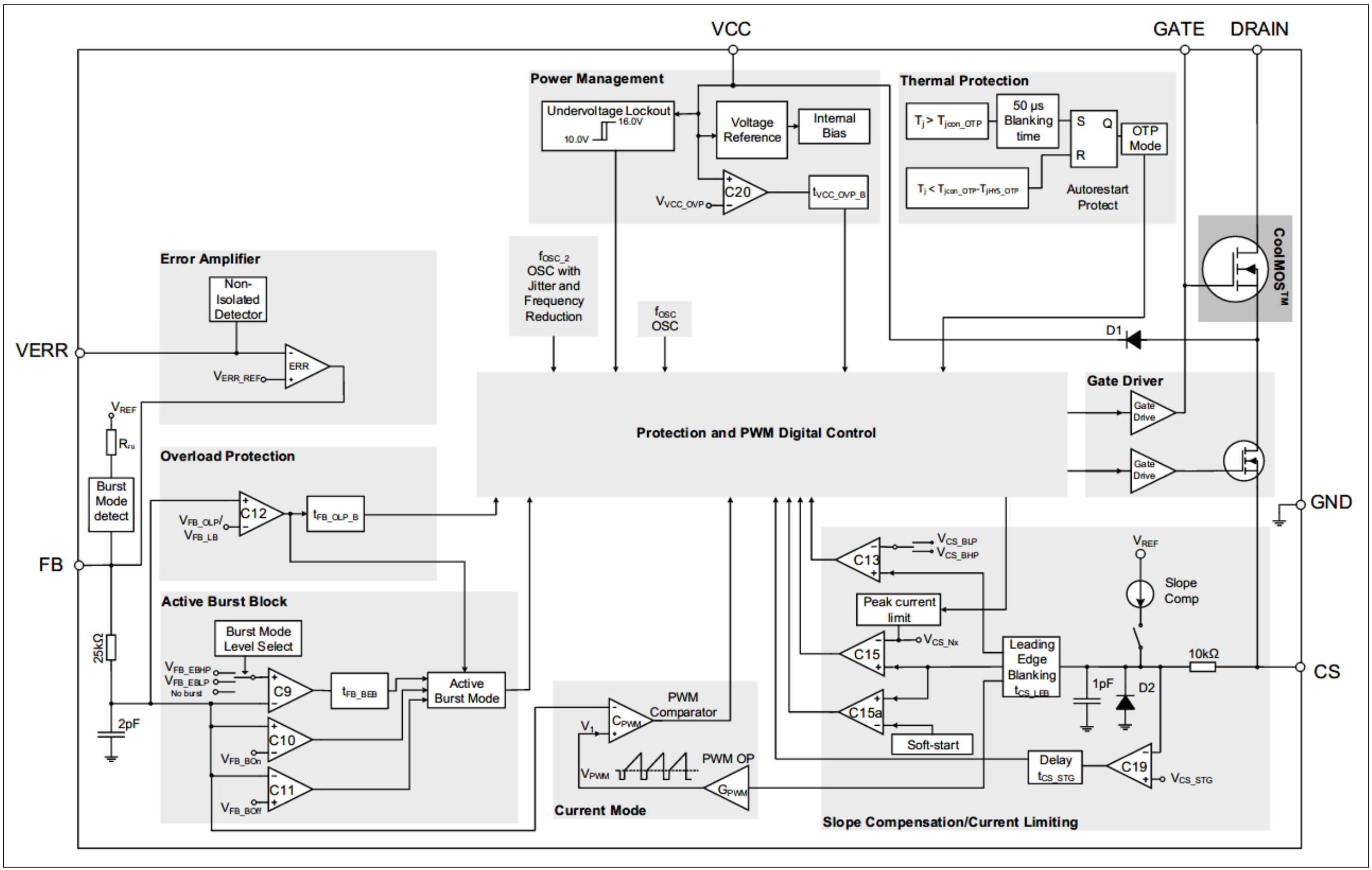


Figure 2 Representative block diagram

3 Functional description

3.1 VCC pre-charging and typical VCC voltage during start-up

As shown in the figures typical application circuits, once the line input voltage is applied, a rectified voltage appears across the capacitor C_{BUS}. The pull-up resistor $R_{STARTUP}$ provides a current to charge the Ciss (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over Ciss is high enough, CoolMOS™ and the V_{CC} capacitor are charged through the primary inductance of a transformer L_P, CoolMOS™ and the internal diode D1 with the two steps constant current source $I_{VCC\_Charge1}$[1)] and $I_{VCC\_Charge3}$[1)].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the V_{CC} capacitor until V_{CC} reaches V_{CC_SCP} to protect the controller from the V_{CC} pin short to ground during the startup. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the V_{CC} capacitor further, until the V_{CC} voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 3, the V_{CC} voltage increases almost linearly with two steps.

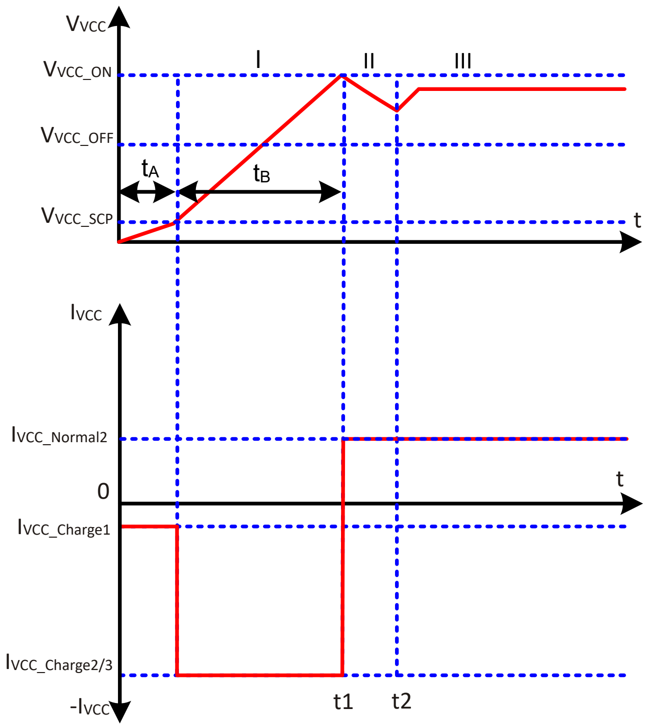


Figure 3 V_{CC} voltage and current at startup

The time for the V_{CC} pre-charging can then be calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \times C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \times C_{VCC}}{I_{VCC\_Charge3}} \tag{1}$$

When the V_{CC} voltage exceeds the V_{CC} turn on threshold V_{VCC_ON} at time t1, the IC starts to operate with soft start. Due to the power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t2 onward and delivering the $I_{VCC\_Normal2}$[2)] to the CoolSET™. V_{CC} then reaches a constant value depending on the output load.

1) $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during startup.

2) $I_{VCC\_Normal2}$ is supply current from VCC capacitor or auxiliary winding to the CoolSET™ during normal operation.

3.2 Soft-start

As shown in the figure below, the IC begins to operate with a soft-start at time ton. The switching stresses on the power MOSFET, diode and transformer are minimized during soft-start. The soft-start implemented in ICE5xRxxxxBZx-1 is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to V_{CS_N} (0.8 V) finally. The normal feedback loop will take over the control when the output voltage reaches its regulated value.

The frequency for the first 3ms is $f_{OSC2\_MIN}/f_{OSC4\_MIN}$ in order to minimize current spikes due to CCM during start-up. After the first 3ms,the switching frequency changes to f_{OSC2}/f_{OSC4} for the remaining duration of soft start.

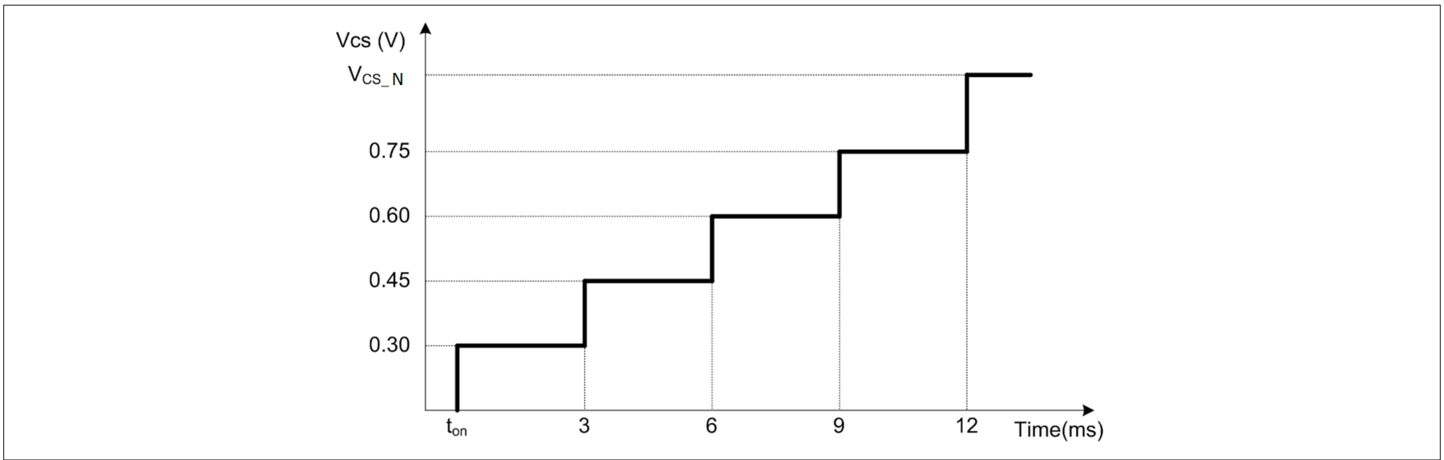


Figure 4 **Maximum current sense voltage during soft start**

3.3 Normal operation

The PWM controller during normal operation consists of a digital signal processing circuit including regulation control and an analog circuit including a current measurement unit and a comparator. Details about the full operation of the CoolSET™ in normal operation are illustrated in the following paragraphs.

3.3.1 PWM operation and peak current mode control

3.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator with a switching frequency f_{SW} that corresponds to the voltage level V_{FB} (see Figure 6).

3.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V1 (see Figure 2) which is the representation of the instantaneous current of the power MOSFET. When V1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the GATE of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the feedback voltage V_{FB} (see Figure 5).

At switch on transient of the power MOSFET, a voltage spike across R_{CS} can cause V1 to increase and exceed V_{FB}. To avoid a false switch off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn on time of the power MOSFET is t_{CS_LEB}.

For some reason that the voltage level at V1 takes long time to exceed V_{FB}, the IC has implemented a maximum duty cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75 is reached.

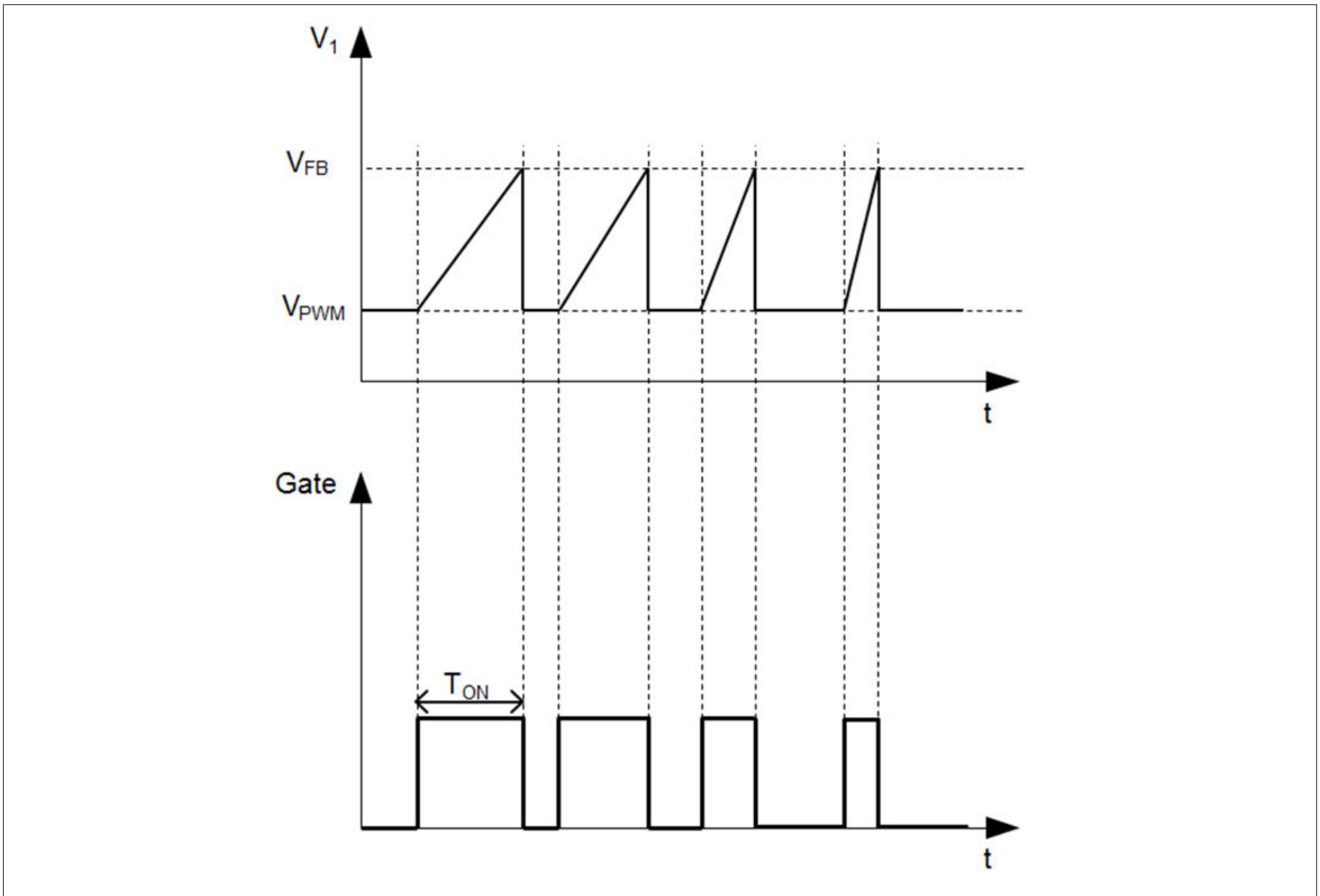


Figure 5 **Pulse width modulation**

3.3.2 Current sense

The power MOSFET current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then, added with an offset V_{PWM} to become V1 as described in below equation.

$$V_{CS} = I_D \times R_{CS} \tag{2}$$

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} \tag{3}$$

where,

I_D : power MOSFET current
V_{CS} : CS pin voltage
R_{CS} : resistance of the current sense resistor
V1 : voltage level compared to V_{FB} as described
G_{PWM} : PWM-OP gain
V_{PWM} : offset for voltage ramp

If the voltage at the current sense pin is lower than the preset threshold V_{CS_STG} after the time $t_{CS\_STG\_SAM}$ for three consecutive pulses during on-time of the power switch, this abnormal V_{CS} will trigger IC into auto restart mode.

3.3.3 Frequency reduction

Frequency reduction is implemented in ICE5xRxxxxBZx-1 to achieve a better efficiency during the light load.

At light load, the reduced switching frequency F_{SW} improves efficiency by reducing the switching loses.

When the load decreases, V_{FB} decreases as well. F_{SW} is dependent on the V_{FB} as shown in Figure 6. Therefore, F_{SW} decreases as the load decreases.

For example, F_{SW} at high load is 65 kHz and starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reached the f_{OSC2_MIN} even the load is further reduced.

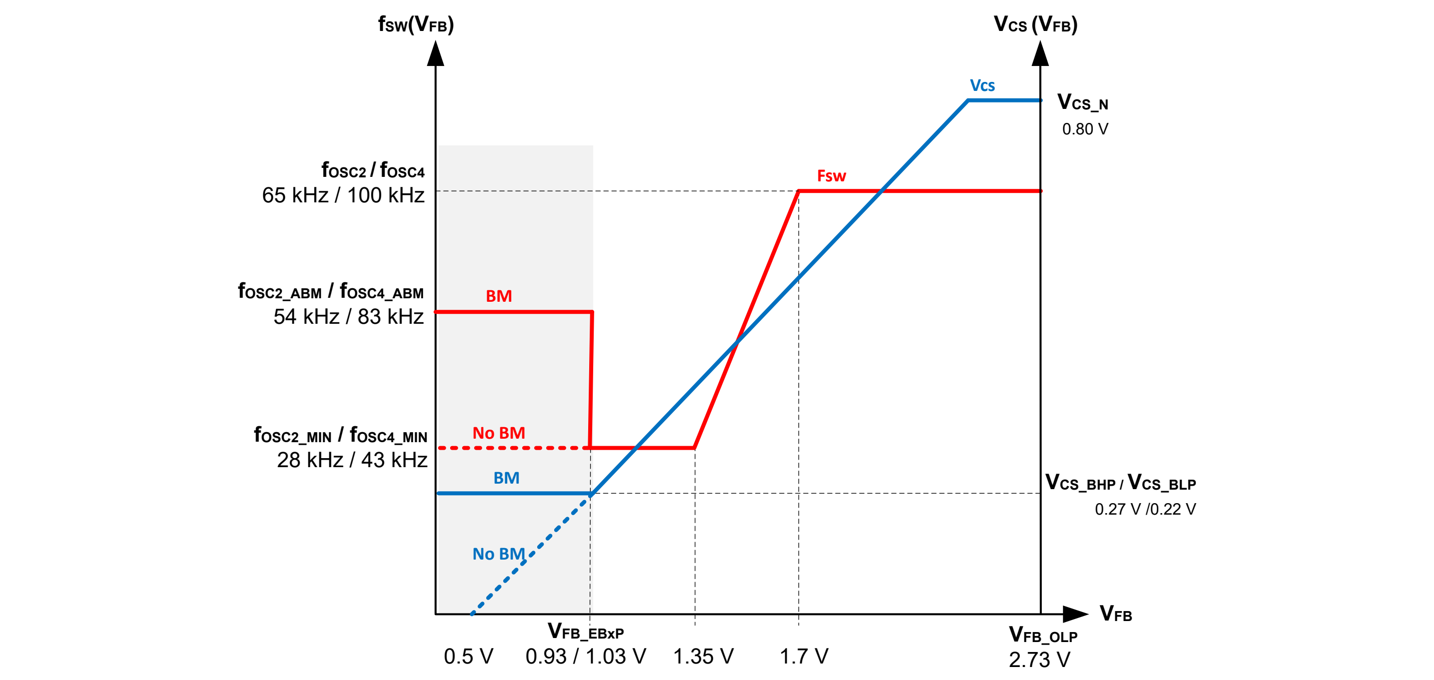


Figure 6 **Frequency reduction curve**

3.3.4 Slope compensation

ICE5xRxxxxBZx-1 can operate at Continuous Conduction Mode (CCM). At CCM operation, duty cycle greater than 50% may generate a sub-harmonic oscillation. To avoid the sub-harmonic oscillation, slope compensation is added to V_{CS} pin when the gate of the power MOSFET is turned on for more than 40% of the switching cycle period. The relationship between V_1 and the V_{CS} for CCM operation is described in below equation:

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} + M_{COMP} \times (T_{ON} - 40\,\% \times T_{PERIOD}) \tag{4}$$

where,

M_{COMP} : slope compensation rate

T_{ON} : gate turn on time of the power MOSFET

T_{PERIOD} : switching cycle period

Slope compensation circuit is disabled and no slope compensation is added into the V_{CS} pin during active burst mode to save the power consumption.

3.3.5 Oscillator and frequency jittering

The oscillator generates a frequency f_{OSC} with frequency jittering of ±4% at a jittering period of T_{JITTER} (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

3.3.6 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of driver (see Figure 7). Thus the leading switch spike during turn on is minimized.

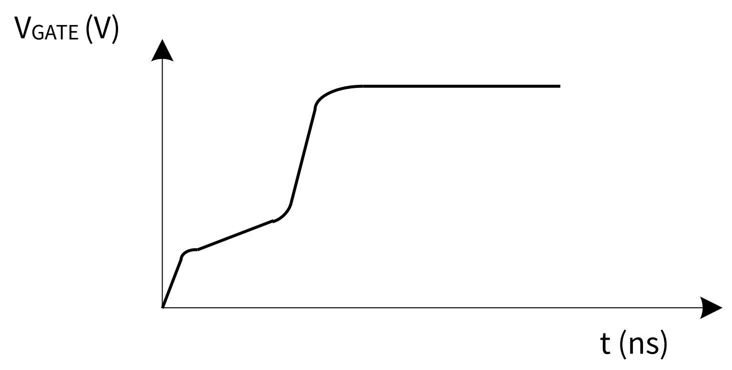


Figure 7 **Modulated gate drive**

3.4 Peak current limitation

There is a cycle by cycle peak current limitation realized by the current limit comparator to provide primary over-current protection. The primary current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{PEAK\_PRI} = V_{CS\_N}/R_{CS} \tag{5}$$

To avoid mistriggering caused by MOSFET switch on transient voltage spikes, a leading edge blanking time (t_{CS_LEB}) is integrated in the current sensing path.

3.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching the power MOSFET off. An overshoot on the peak current Ipeak caused by the delay depends on the ratio of dI/dt of the primary current.

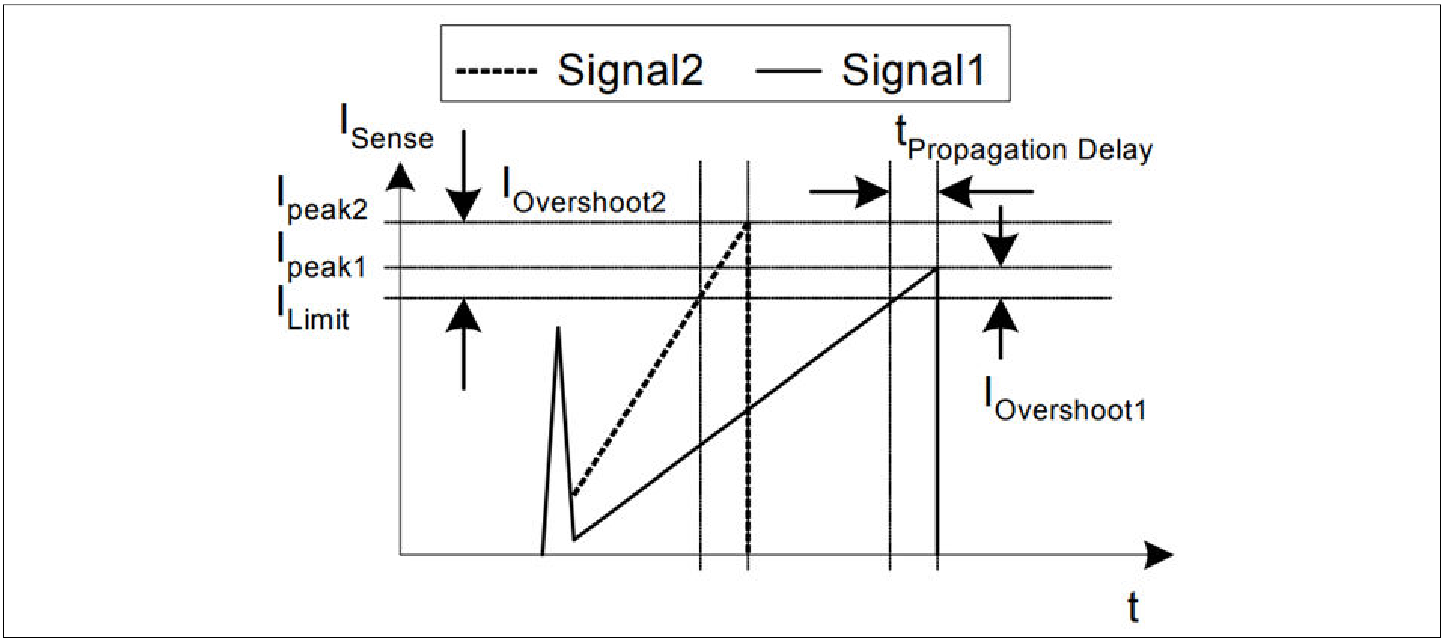


Figure 8 **Current limiting**

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{CS_N} and the switching off of the power MOSFET is compensated over wide bus voltage range. Current limiting becomes more accurate which will result in a minimum difference of overload protection triggering power between low and high AC line input voltage.

Under CCM operation, the same V_{CS} do not result in the same power. In order to achieve a close overload triggering level for CCM, ICE5xRxxxxBZx-1 has implemented a 2 compensation curve as shown Figure 9. One of the curve is used for T_{ON} greater than 0.40 duty cycle and the other is for lower than 0.40 duty cycle.

Similarly, the same concept of propagation delay compensation is also implemented in ABM with reduced level. With this implementation, the entry and exit burst mode power can be close between low and high AC line input voltage.

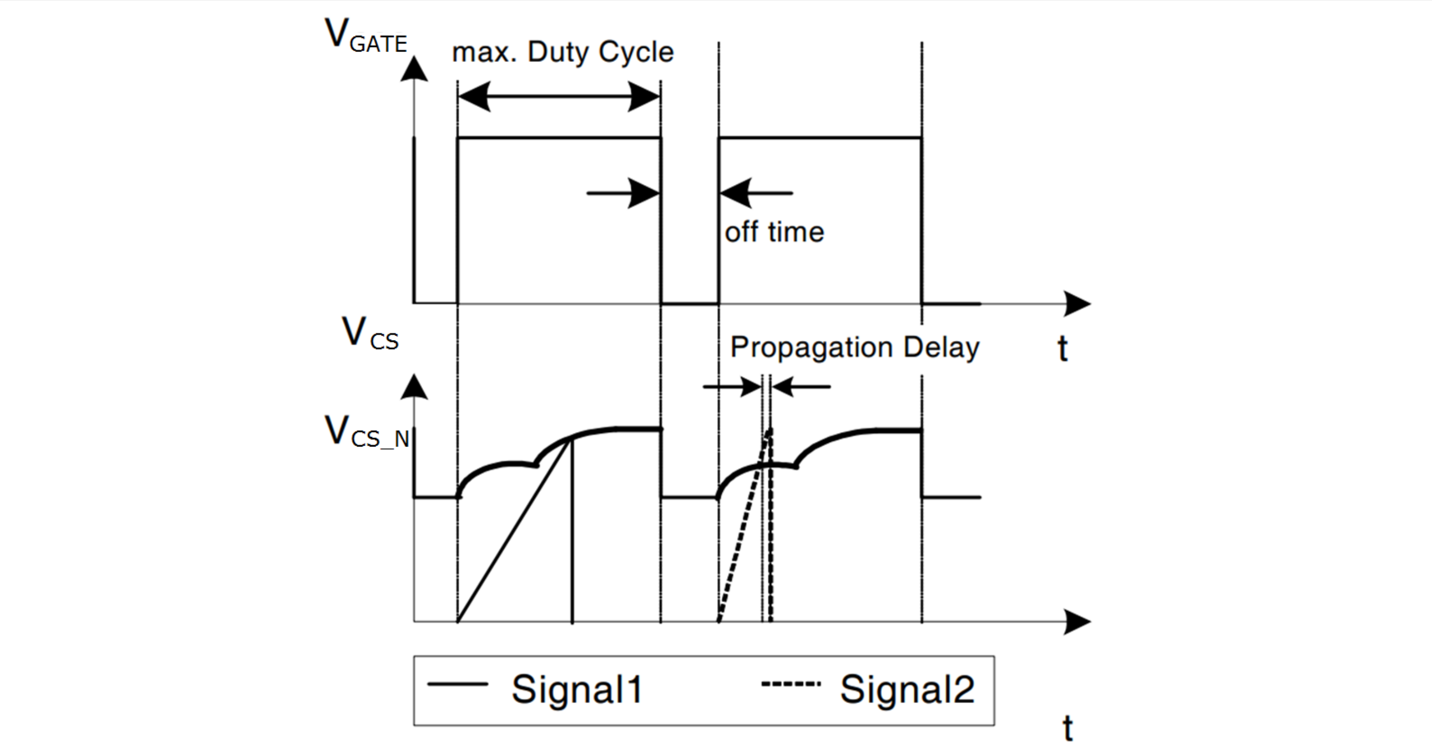


Figure 9 **Dynamic voltage threshold V_{CS_N}**

3.5 Active Burst Mode (ABM) with selectable power level

At light load condition, the IC enters ABM operation to minimize the power consumption. Details about ABM operation are explained in the following paragraphs.

3.5.1 Entering ABM operation

The sytem will enter into ABM operation when two conditions below are met:

- the FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP} depending on burst configuration option setup
- and a certain blanking time t_{FB_BEB}

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of entering ABM operation, so that the controller enters ABM operation only when the output power is really low.

3.5.2 During ABM operation

After entering ABM, the PWM section will be inactive making the V_{OUT} start to decrease. As the V_{OUT} decreases, V_{FB} rises. Once V_{FB} exceeds V_{FB_BOn}, the internal circuit is again activated by the internal bias to start with the switching.

If the PWM is still operating and the output load is still low, V_{OUT} increases and V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled with no switching until V_{FB} increases back to exceed V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn} shown in Figure 10.

During ABM, the switching frequency is f_{OSC2_ABM} or f_{OSC4_ABM}. The peak current I_{PEAK_ABM} of the power MOSFET is defined by:

$$I_{PEAK\_ABM} = \frac{V_{CS\_BxP}}{R_{CS}} \tag{6}$$

where V_{CS_BxP} is the peak current limitation in ABM.

3.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds V_{FB_LB}, it will leave ABM and the peak current limitation threshold voltage will return back to V_{CS_N} immediately.

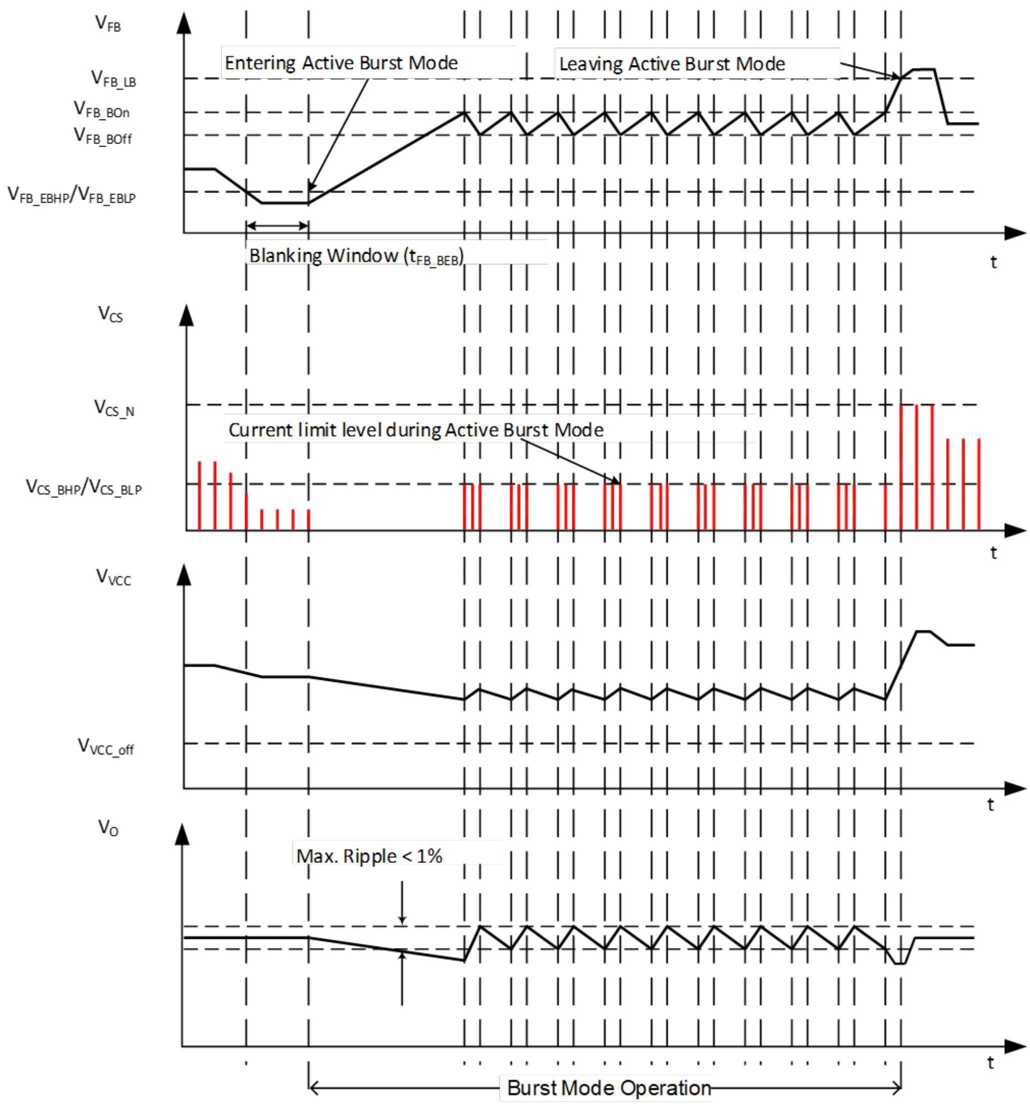


Figure 10 **Signals in ABM**

3.5.4 ABM configuration

The burst mode entry level can be selected by changing the different resistance R_{Sel} at FB pin. There are 3 configuration options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit level with the FB voltage.

Table 4 ABM configuration option setup

Option	V_{FB}	V_{CS_BxP}	Entry level	Exit level
			V_{FB_EBxP}	V_{FB_LB}
1	$V_{FB} < V_{FB\_P\_BIAS1}$	-	No ABM	No ABM
2	$V_{FB\_P\_BIAS1} < V_{FB} < V_{FB\_P\_BIAS2}$	0.22 V	0.93 V	2.73 V
3	$V_{FB} > V_{FB\_P\_BIAS2}$	0.27 V	1.03 V	2.73 V

During IC first startup, the controller preset the ABM selection to Option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see Figure 11)and a current source I_{sel} is turned on instead.From VCC = 4.44 V to the VCC on threshold, the FB pin will source current I_{Sel} through R_{Sel} and external FB network. When V_{CC} reaches V_{CC} on threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option and the current source (I_{sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit.

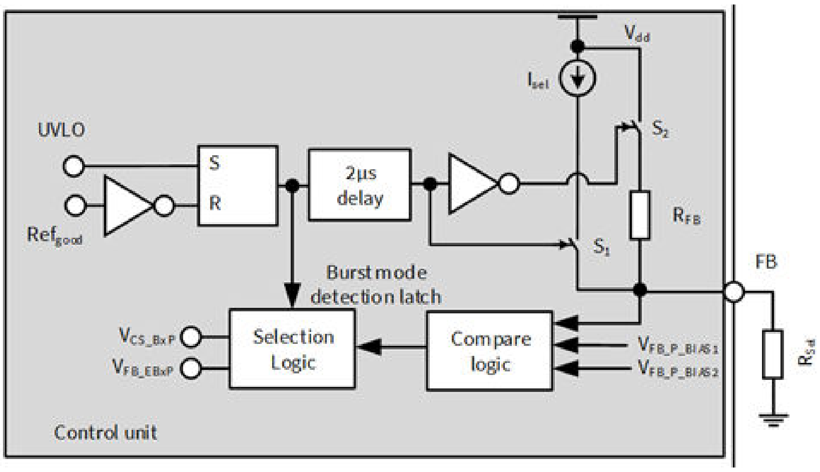


Figure 11 ABM detect and adjust

3.6 Non-isolated/isolated configuration

ICE5xRxxxxBZx-1 has a VERR Pin, which is connected to the input of an integrated error amplifier to support non-isolated converter (see the figures typical application circuits). When V_{CC} is charging and before reaching the V_{CC} on threshold, a current source $I_{ERR\_P\_BIAS}$ from VERR pin together with R_{F1} and R_{F2} will generate a voltage across it. If VERR voltage is more than $V_{ERR\_P\_BIAS}$ (0.2 V), non-isolated configuration is selected, otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

In case of non-isolated configuration, the voltage divider R_{F1} and R_{F2} is used to sense the output voltage and compared with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

3.7 Protection functions

The ICE5xRxxxxxZx-1 provides numerous protection functions that considerably improve the power supply system robustness, safety, and reliability. The following table summarizes these protection functions and the corresponding protection mode whether as a non-switch auto restart, auto restart or extended cycle skip auto restart mode. Refer to Figure 12, Figure 13 and Figure 14 for the waveform illustration of protection modes.

Table 5 Protection functions

Protections functions	Normal mode	Burst mode		Protection mode
		Burst ON	Burst OFF	
VCC overvoltage	√	√	Not applicable	Extended cycle skip auto restart
VCC undervoltage	√	√	√	Auto restart
Overload or open loop	√	Not applicable	Not applicable	Extended cycle skip auto restart
Overtemperature	√	√	√	Non-switch auto restart
VCC short to GND	√	√	√	No start-up

3.7.1 VCC overvoltage and undervoltage

During operation, the VCC voltage is continuously monitored.

If VCC voltage falls below V_{VCC_OFF} for a blanking time of $t_{VCC\_OFF\_B}$, MOSFET will be switched off and auto restart will be initiated.

If VCC voltage exceeds V_{VCC_OVP} for a blanking time of $t_{VCC\_OVP\_B}$, MOSFET will be switched off and extended cycle skip auto restart will be initiated.

3.7.2 Overload or open loop

In case of open control loop or output overload, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters extended cycle skip auto restart mode. The blanking time enables the converter to provide a peak power in case the increase in V_{FB} is due to a sudden load increase.

3.7.3 Over temperature

If the junction temperature of controller exceeds T_{jCon_OTP}, the IC enters into Over Temperature Protection (OTP) auto restart mode. The IC has also implemented with a 40 °C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature is dropped 40 °C lower than the over temperature trigger point.

3.7.4 VCC short to GND

To limit the power dissipation of the startup circuit at V_{CC} short to GND condition, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_ Charge1}$. With such low current, the power loss of the IC is limited to prevent overheating.

3.7.5 Signals in different protection modes

All the protections are in auto restart mode with a new soft start sequence. The three auto restart modes are illustrated in the following figures.

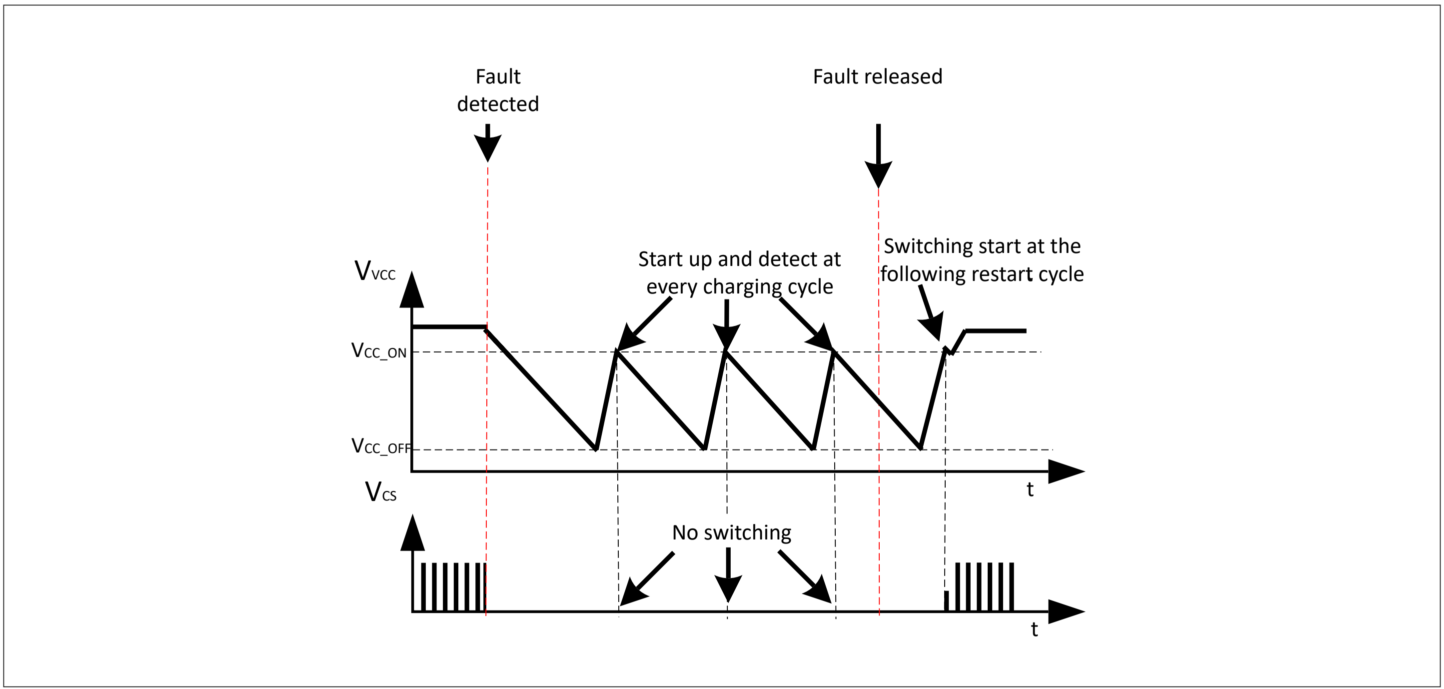


Figure 12 **Non-switch auto restart mode**

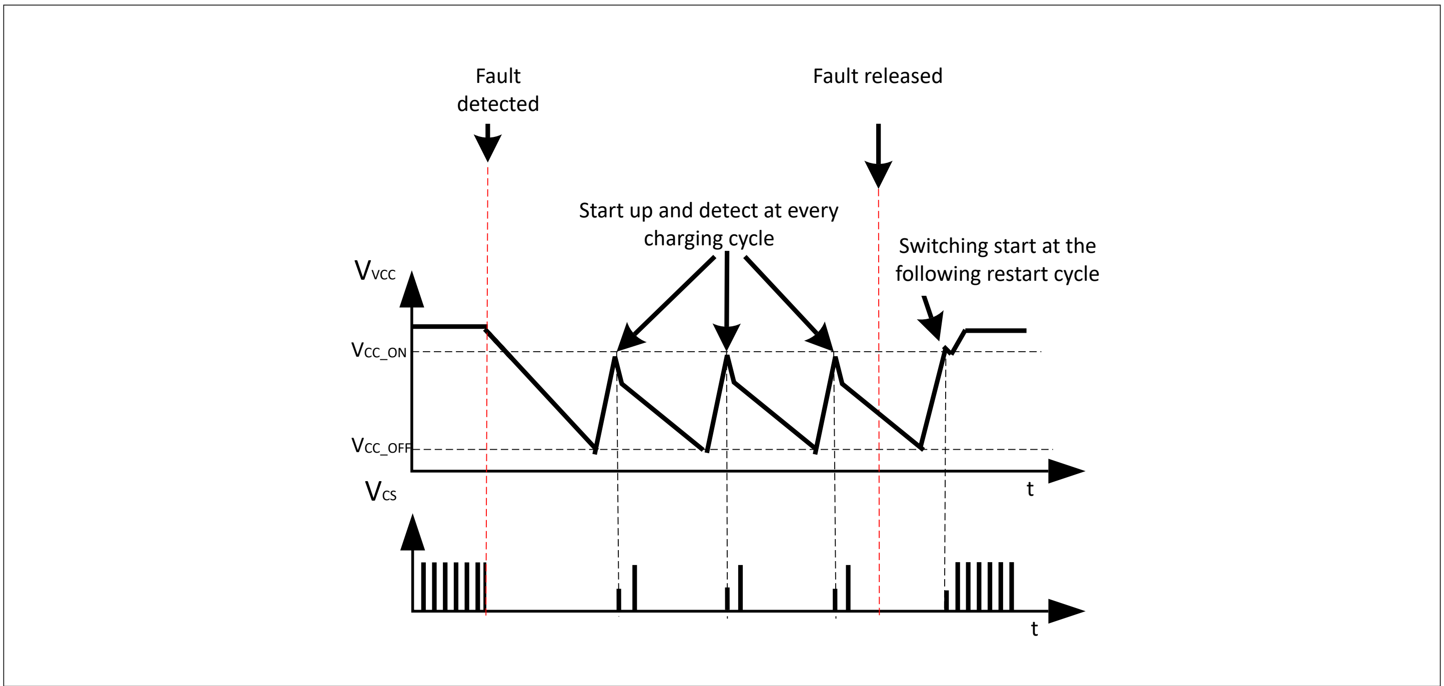


Figure 13 **Auto restart mode**

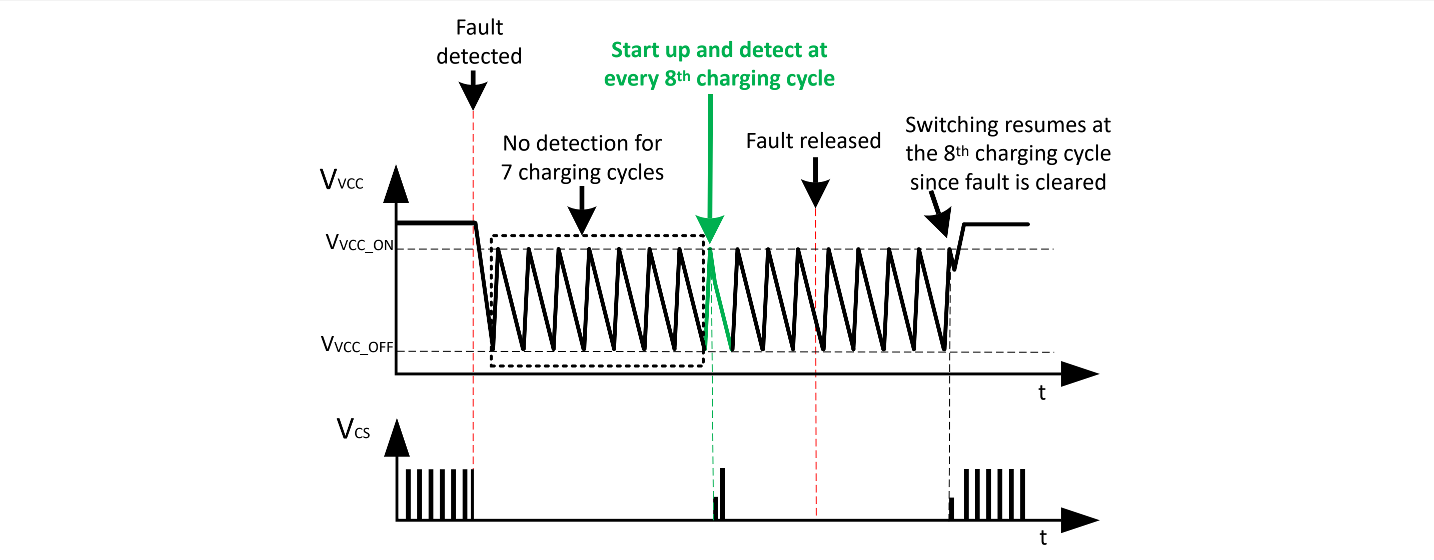


Figure 14 Extended cycle skip auto restart

4 Electrical characteristics

Attention: All voltages are measured with respect to ground (pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute maximum ratings

Attention: Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit. T_a=25 °C unless otherwise specified.

Table 6 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain voltage						
ICE5AR4770BZS-1	V_{DRAIN}	-	-	700	V	T_j = 25 °C
ICE5xRxx80BZx-1	V_{DRAIN}	-	-	800	V	T_j = 25 °C
ICE5xR3995BZ-1	V_{DRAIN}	-	-	950	V	T_j = 25°C
Pulse drain current						
ICE5AR4770BZS-1	I_{D_Pulse}	-	-	2.2	A	Pulse width t_P limited by T_{j_max}
ICE5xR4780BZx-1	I_{D_Pulse}	-	-	2.6	A	Pulse width t_P limited by T_{j_max}
ICE5xR3995BZ-1	I_{D_Pulse}	-	-	5.0	A	Pulse width t_P limited by T_{j_max}
ICE5BR2280BZ-1	I_{D_Pulse}	-	-	5.8	A	Pulse width t_P = 20 µs and limited by T_{j_max}
ICE5AR0680BZS-1	I_{D_Pulse}	-	-	5.8	A	Pulse width t_P limited by T_{j_max}
Pin rating						
VCC Supply Voltage	V_{CC}	-0.3	-	35	V	
GATE Voltage	V_{GATE}	-0.3	-	27	V	
FB Voltage	V_{FB}	-0.3	-	5.5	V	
VERR Voltage	V_{ERR}	-0.3	-	5.5	V	
CS Voltage	V_{CS}	-0.3	-	3.6	V	
Maximum DC current on any pin		-10	-	10	mA	Except DRAIN and CS pin
ESD robustness HBM	V_{ESD_HBM}	-	-	2000	V	According to EIA/JESD22
ESD robustness CDM	V_{ESD_CDM}	-	-	500	V	According to EIA/JESD22

(table continues...)

Table 6 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction temperature range	T_j	-40	-	150	°C	Controller & CoolMOS
Storage Temperature	T_{STORE}	-55	-	150	°C	
Thermal resistance (junction-ambient)						
ICE5AR4770BZS-1	R_{thJA}	-	-	106	K/W	1)
ICE5xR4780BZx-1	R_{thJA}	-	-	107	K/W	1)
ICE5xR3995BZ-1	R_{thJA}	-	-	106	K/W	1)
ICE5BR2280BZ-1	R_{thJA}	-	-	104	K/W	1)
ICE5AR0680BZS-1	R_{thJA}	-	-	100	K/W	1)
Avalanche energy, repetitive, t_{AR} limited by maximal T_j = 150°C and T_{j_Start} = 25°C						
ICE5AR4770BZS-1	E_{AR}	-	-	0.02	mJ	I_D = 0.14 A, V_{DD} = 50 V
ICE5xR4780BZx-1	E_{AR}	-	-	0.02	mJ	I_D = 0.20 A, V_{DD} = 50 V
ICE5BR2280BZ-1	E_{AR}	-	-	0.05	mJ	I_D = 0.40 A, V_{DD} = 50 V
ICE5xR3995BZ-1	E_{AR}	-	-	0.04	mJ	I_D = 0.20 A, V_{DD} = 50 V
ICE5AR0680BZS-1	E_{AR}	-	-	0.22	mJ	I_D = 1.80 A, V_{DD} = 50 V
Avalanche current, repetitive, t_{AR} limited by maximal T_j = 150°C and T_{j_Start} = 25°C						
ICE5AR4770BZS-1	I_{AR}	-	-	0.14	A	
ICE5xR4780BZx-1	I_{AR}	-	-	0.20	A	
ICE5xR3995BZ-1	I_{AR}	-	-	0.20	A	
ICE5BR2280BZ-1	I_{AR}	-	-	0.40	A	
ICE5AR0680BZS-1	I_{AR}	-	-	1.80	A	

1) Setup according to the JEDEC standard JESD51 and using minimum drain pin copper area in a 2 oz copper single sided PCB

4.2 Operating range

***Note**: Within the operating range, the IC operates as described in the functional description.*

Table 7 Operating range

Within the operating range, the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC Supply Voltage	V_{VCC}	V_{VCC_OFF}	-	V_{VCC_OVP}		
Junction Temperature of controller	T_{jCon_op}	-40	-	T_{jCon_OTP}	°C	Max value limited due to OTP of controller chip

(table continues...)

Table 7 (continued) Operating range

Within the operating range, the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction Temperature of CoolMOS	$T_{jCoolMOS\_op}$	-40	-	150	˚C	

4.3 Operating conditions

Note: *The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_j from – 40°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of VCC = 18 V is assumed.*

Table 8 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC Charge Current	$I_{VCC\_Charge1}$	-0.35	-0.20	-0.09	mA	V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
VCC Charge Current	$I_{VCC\_Charge2}$	-	-3.2	-	mA	V_{VCC}=3 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
VCC Charge Current	$I_{VCC\_Charge3}$	-5	-3	-1	mA	V_{VCC}=15 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
VCC Turn-on Threshold Voltage	V_{VCC_ON}	15.3	16	16.5	V	
VCC Turn-off Threshold Voltage	V_{VCC_OFF}	9.4	10	10.4	V	
VCC Short Circuit Protection	V_{VCC_SCP}	-	1.1	1.9	V	
VCC Turn-off blanking	$t_{VCC\_OFF\_B}$	-	50	-	µs	
Current Consumption, Startup Current	$I_{VCC\_Startup}$	-	0.25	-	mA	V_{VCC}=15 V
Current Consumption, Auto Restart	I_{VCC_AR}	-	410	-	µA	
Current Consumption, Burst Mode – Isolated	$I_{VCC\_Burst Mode\_ISO}$	-	0.54	-	mA	
Current Consumption, Burst Mode – Non-Isolated	$I_{VCC\_Burst Mode\_NISO}$	-	0.61	-	mA	
Current Consumption, Normal with Inactive Gate	I_{VCC_Normal}	-	1.1	-	mA	I_{FB}=0 A (No gate switching)
Current consumption, normal with Active Gate						
ICE5AR4770BZS-1	$I_{VCC\_Normal2}$	-	-	2.20	mA	

(table continues...)

Table 8 (continued) Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ICE5AR4780BZS-1	$I_{VCC\_Normal2}$	-	-	2.20	mA	
ICE5AR3995BZ-1	$I_{VCC\_Normal2}$	-	-	2.36	mA	
ICE5AR0680BZS-1	$I_{VCC\_Normal2}$	-	-	4.18	mA	
ICE5BR4780BZ-1	$I_{VCC\_Normal2}$	-	-	1.84	mA	
ICE5BR3995BZ-1	$I_{VCC\_Normal2}$	-	-	1.97	mA	
ICE5BR2280BZ-1	$I_{VCC\_Normal2}$	-	-	2.04	mA	

4.4 Internal voltage reference

Table 9 Internal voltage reference

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Internal reference voltage	V_{REF}	3.2	3.3	3.39	V	Measured at FB pin I_{FB} = 0 A

4.5 PWM section

Table 10 PWM section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fixed Oscillator Frequency – 100 kHz	f_{OSC4}	94	100	106	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 100 kHz	f_{OSC3}	92	100	108	kHz	Operating temperature range
Fixed Oscillator Frequency – 100 kHz (ABM)	f_{OSC4_ABM}	71	83	94	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 100 kHz (minimum Fsw)	f_{OSC4_MIN}	36	43	51	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 65 kHz	f_{OSC1}	59.8	65	70.2	kHz	Operating temperature range
Fixed Oscillator Frequency – 65 kHz	f_{OSC2}	61.1	65	68.9	kHz	T_j = 25°C
Fixed Oscillator Frequency – 65 kHz (ABM)	f_{OSC2_ABM}	46.2	54	61.1	kHz	T_j = 25°C
Fixed Oscillator Frequency – 65kHz (minimum Fsw)	f_{OSC2_MIN}	23.4	28	33.2	kHz	T_j = 25°C

(table continues...)

Table 10 **(continued) PWM section**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Frequency jittering range	f_{JITTER}	-	± 4	-	%	$T_j = 25°C$
Frequency jittering period	T_{JITTER}	-	4	-	ms	$T_j = 25°C$
Maximum duty cycle	D_{MAX}	70	75	80	%	
Feedback pull-up resistor	R_{FB}	11	15	20	kΩ	
PWM-OP gain	G_{PWM}	1.91	2.03	2.16		
Offset for voltage ramp	V_{PWM}	0.42	0.5	0.58	V	
Slope compensation rate - 100 kHz	M_{COMP}	41	50	58	mV/µs	Vcs = 0 V
Slope compensation rate - 65 kHz	M_{COMP}	26.5	32.5	38	mV/µs	Vcs = 0 V
Feedback Cutoff Voltage	$V_{FB,Cutoff}$	-	0.41	-	V	When $V_{FB} < V_{FB,Cutoff}$, no PWM switching.

4.6 Error amplifier

Table 11 **Error amplifier**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transconductance	G_{ERR_M}	2.14	2.80	3.44	mA/V	
Transconductance – Burst mode	G_{ERR_BM}	6.9	9.2	11.6	mA/V	
Error amplifier source current	I_{ERR_SOURCE}	85	150	223	µA	
Error amplifier sink current	I_{ERR_SINK}	85	150	223	µA	
Error amplifier reference voltage	V_{ERR_REF}	1.76	1.80	1.84	V	
Error amplifier output dynamic range of transconductance	V_{ERR_DYN}	0.05	-	3.15	V	
Error amplifier mode bias current	$I_{ERR\_P\_BIAS}$	9.5	14.0	18.5	µA	
Error amplifier mode threshold	$V_{ERR\_P\_BIAS}$	0.16	0.20	0.24	V	

4.7 Current sense

Table 12 Current sense

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.72	0.80	0.88	V	$dV_{sense}/dt = 0.41$ V/µs
Peak current limitation in normal operation, 15% Duty Cycle	V_{CS_N15}	0.74	0.79	0.84	V	
Leading edge-blanking time	t_{CS_LEB}	70	220	365	ns	
Peak current limitation in ABM - high power	V_{CS_BHP}	0.23	0.27	0.31	V	
Peak current limitation in ABM - low power	V_{CS_BLP}	0.18	0.22	0.26	V	
Abnormal CS voltage threshold	V_{CS_STG}	0.06	0.10	0.15	V	
Abnormal CS voltage consecutive trigger	P_{CS_STG}	-	3	-	cycle	
Abnormal CS voltage sample period	$t_{CS\_STG\_SAM}$	$t_{PERIOD} \times 0.36$	$t_{PERIOD} \times 0.4$	$t_{PERIOD} \times 0.44$	µs	

4.8 Soft start

Table 13 Soft start

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Soft start time	t_{SS}	7.3	12.0	-	ms	
Soft start time step	t_{SS_S}	-	3	-	ms	1)
CS peak voltage at first step of soft start	V_{SS1}	-	0.30	-	V	1)
Step increment of CS peak voltage in soft start	V_{SS_S}	-	0.15	-	V	1)

1) Not subject to production test, specified by design.

4.9 Active burst mode

Table 14 Active Burst Mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Charging current to select burst mode	I_{sel}	2.5	3.0	3.5	μA	
Burst mode selection reference voltage threshold	$V_{FB\_P\_BIAS1}$	1.65	1.73	1.80	V	
Burst mode selection reference voltage threshold	$V_{FB\_P\_BIAS2}$	2.76	2.89	3.01	V	
Feedback voltage for entering ABM for high power	V_{FB_EBHP}	0.98	1.03	1.08	V	
Feedback voltage for entering ABM for low power	V_{FB_EBLP}	0.88	0.93	0.98	V	
Blanking time for entering ABM	t_{FB_BEB}	-	36	-	ms	
Feedback voltage for leaving ABM	V_{FB_LB}	2.63	2.73	2.83	V	
Feedback voltage for burst-on – isolated case	$V_{FB\_Bon\_ISO}$	2.26	2.35	2.45	V	
Feedback voltage for burst-off – isolated case	$V_{FB\_BOff\_ISO}$	1.88	2.00	2.05	V	
Feedback voltage for burst-on – non-isolated case	$V_{FB\_Bon\_NISO}$	1.88	1.95	2.05	V	
Feedback voltage for burst-off – non-isolated case	$V_{FB\_BOff\_NISO}$	1.50	1.55	1.64	V	

4.10 VCC overvoltage protection

Table 15 VCC over voltage protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCC_OVP}	29	30.5	32	V	
VCC overvoltage blanking	$t_{VCC\_OVP\_B}$	-	55	-	μs	

4.11 Overload protection

Table 16 Overload protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overload detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.63	2.73	2.83	V	
Overload protection blanking time	$t_{FB\_OLP\_B}$	30	54	-	ms	

4.12 Thermal protection

Table 17 Thermal protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature protection	T_{jcon_OTP} [1)]	129	140	150	°C	Junction temperature of the controller chip (not the CoolMOS™ chip).
Overtemperature hysteresis	T_{jHYS_OTP}	-	40	-	°C	
Overtemperature blanking time	$T_{jcon\_OTP\_B}$	-	50	-	µs	

1) Not subject to production test, specified by design.

4.13 CoolMOS™ section

Table 18 CoolMOS™ section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain Source Breakdown Voltage						
ICE5AR4770BZS-1	$V_{(BR)DSS}$	700	-	-	V	T_j = 25°C
ICE5xRxx80BZx-1	$V_{(BR)DSS}$	800	-	-	V	T_j = 25°C
ICE5xR3995BZ-1	$V_{(BR)DSS}$	950	-	-	V	T_j = 25°C
Drain Source On-Resistance (inclusive of low side MOSFET)						
ICE5AR0680BZS-1	R_{DSon}	-	0.71	0.80	Ω	T_j=25°C at I_D=2A
ICE5AR0680BZS-1	R_{DSon}	-	1.27 [1)]	-	Ω	T_j=125°C at I_D=2A
ICE5BR2280BZ-1	R_{DSon}	-	2.13	2.35	Ω	T_j=25°C at I_D=1A
ICE5BR2280BZ-1	R_{DSon}	-	4.31 [1)]	-		T_j=125°C at I_D=1 A
ICE5xR3995BZ-1	R_{DSon}	-	3.46	4.05	Ω	T_j=25° at I_D=0.8A

(table continues...)

Table 18 (continued) CoolMOS™ section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ICE5xR3995BZ-1	R_{DSon}	-	7.69[1)]	-	Ω	T_j=125°C at I_D=0.8 A
ICE5xR4780BZx-1	R_{DSon}	-	4.13	4.85	Ω	T_j=25°C at I_D=0.4A
ICE5xR4780BZx-1	R_{DSon}	-	8.69[1)]	-	Ω	T_j=125°C at I_D=0.4A
ICE5AR4770BZS-1	R_{DSon}	-	4.73	5.18	Ω	T_j=25°C at I_D=0.4A
ICE5AR4770BZS-1	R_{DSon}	-	8.73[1)]	-	Ω	T_j=125°C at I_D=0.4A
Dynamic characteristics						
Rise time	t_{rise}[2)]	-	30	-	ns	
Fall time	t_{fall}[2)]	-	30	-	ns	
Effective output capacitance, energy related						
ICE5AR4770BZS-1	$C_{o(er)}$	-	3.4[1)]	-	pF	V_{GS}=0V, V_{DS}=0~480V
ICE5xR4780BZx-1	$C_{o(er)}$	-	3[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V
ICE5BR2280BZ-1	$C_{o(er)}$	-	7[1)]	-	pF	V_{GS} = 0 V, V_{DS} = 0 ~ 500 V
ICE5xR3995xZ-1	$C_{o(er)}$	-	5[1)]	-	pF	V_{GS} = 0 V, V_{DS} = 0 ~ 400 V
ICE5AR0680BZS-1	$C_{o(er)}$	-	24[1)]	-	pF	V_{GS}=0V, V_{DS}=0~500V

1) Not subject to production test, specified by design.
2) Measured in a typical flyback / buck converter application.

5 CoolMOS™ performance characteristics

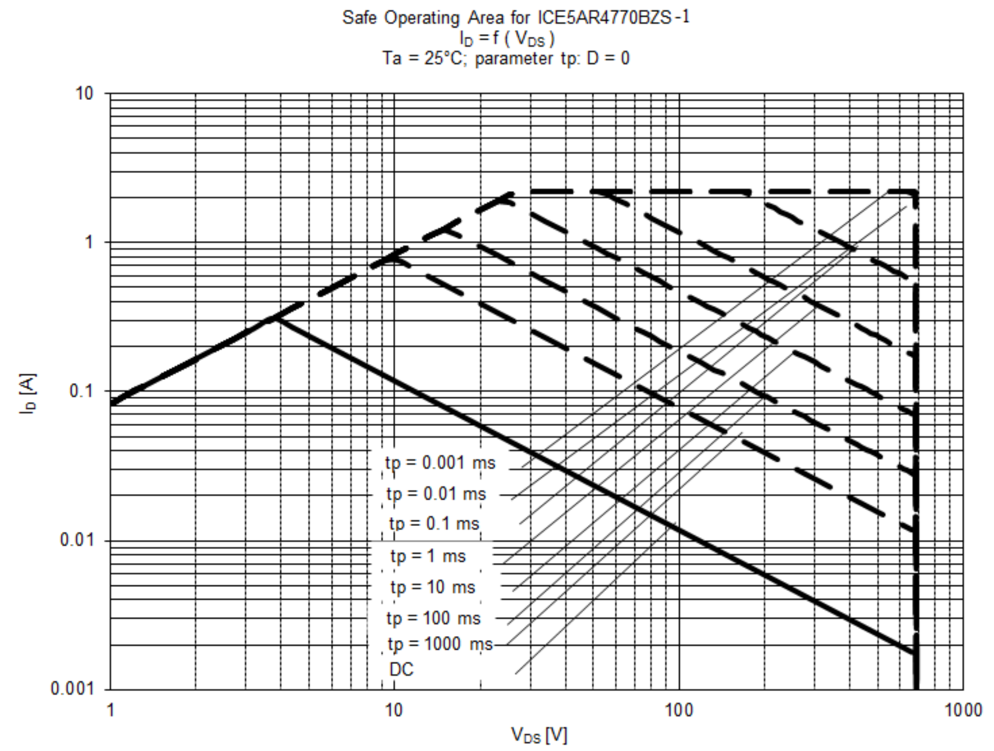


Figure 15 Safe Operating Area (SOA) curve for ICE5AR4770BZS-1

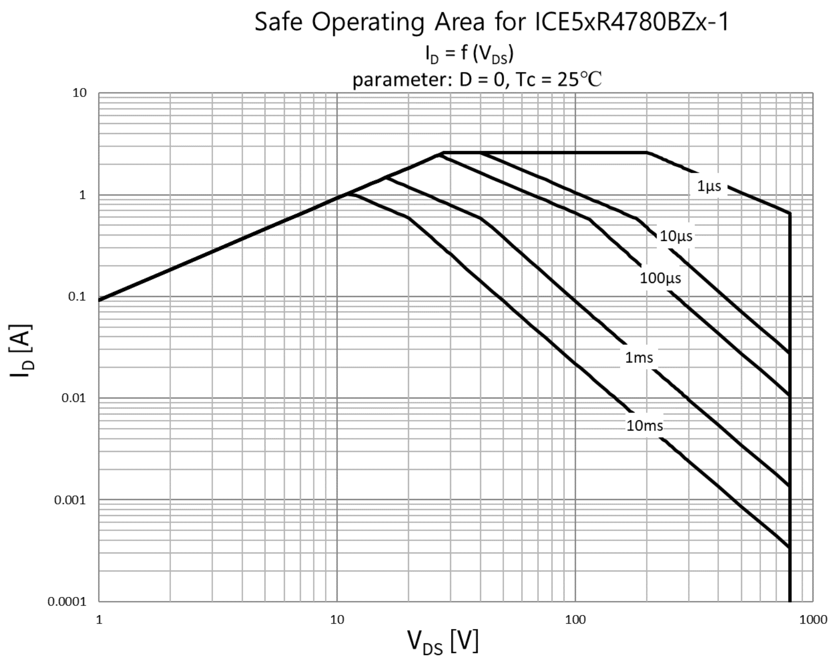


Figure 16 Safe Operating Area (SOA) curve for ICE5xR4780BZx-1

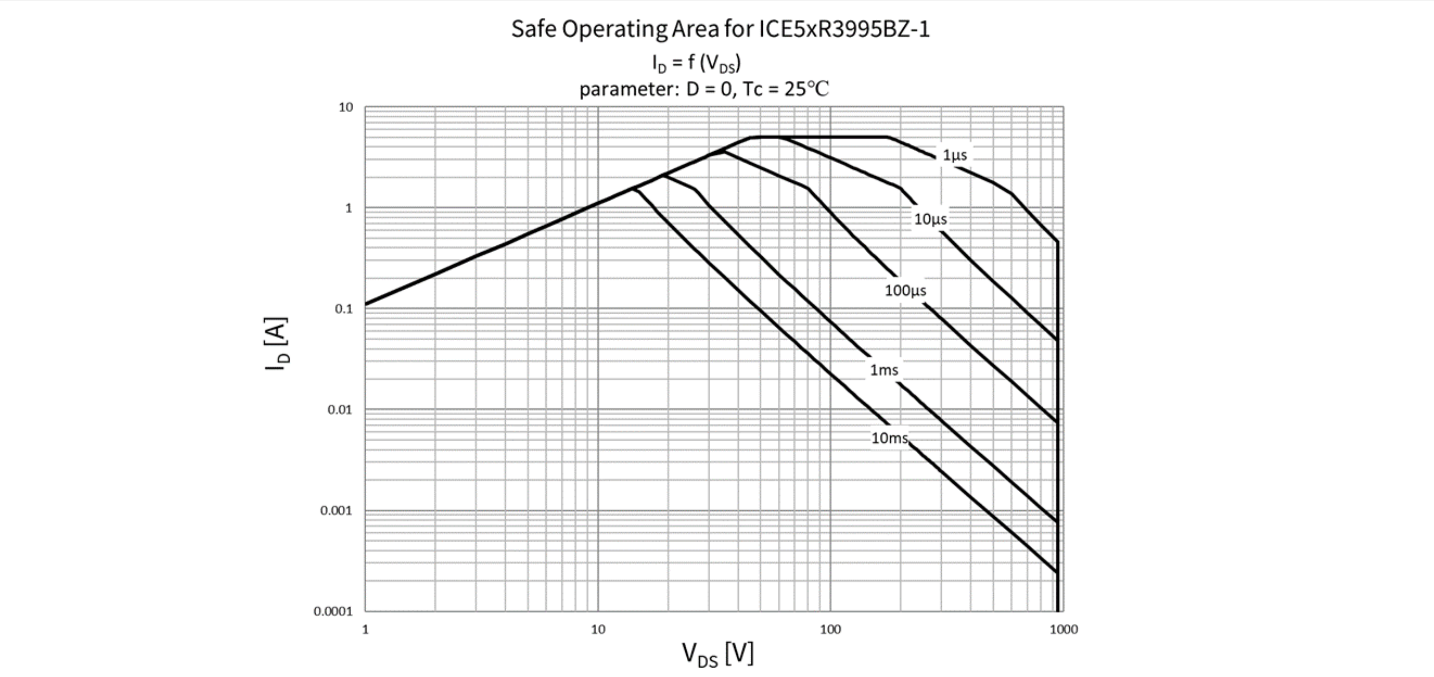


Figure 17 **Safe operating area (SOA) curve for ICE5xR3995BZ-1**

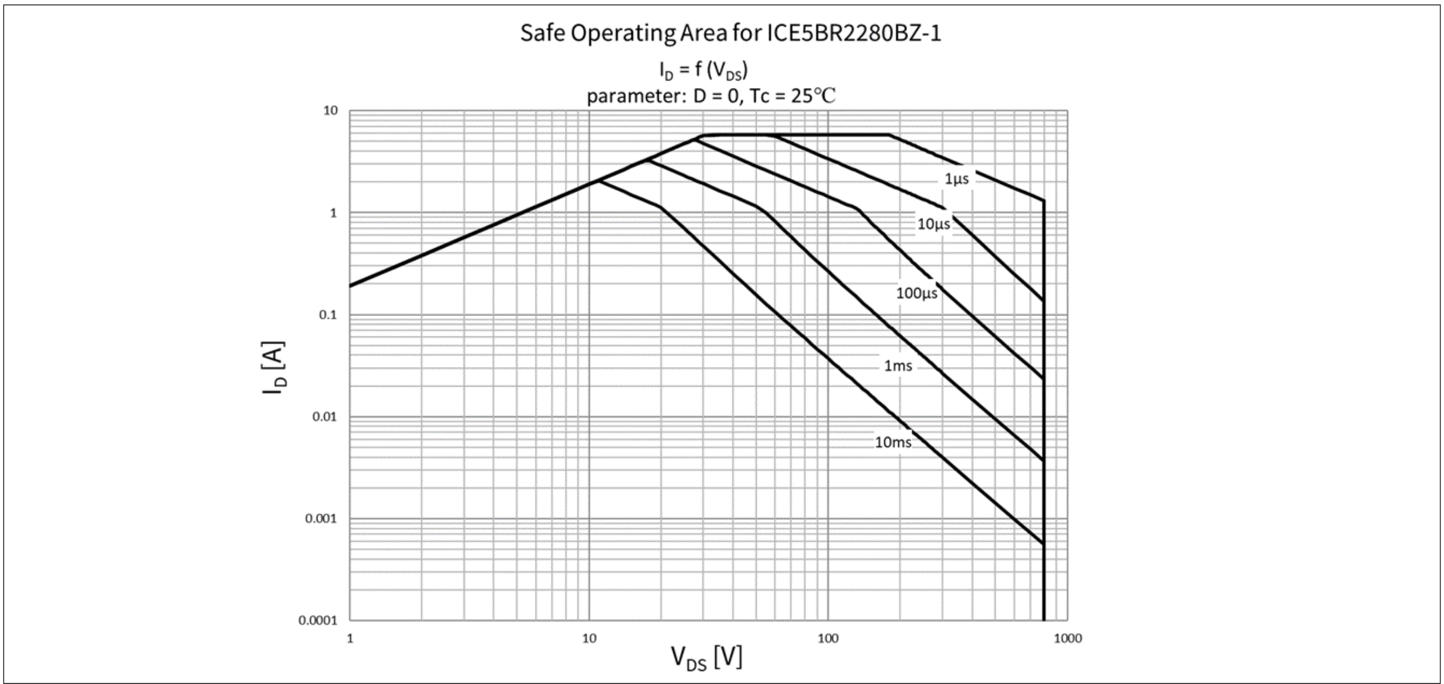


Figure 18 **Safe Operating Area (SOA) curve for ICE5BR2280BZ-1**

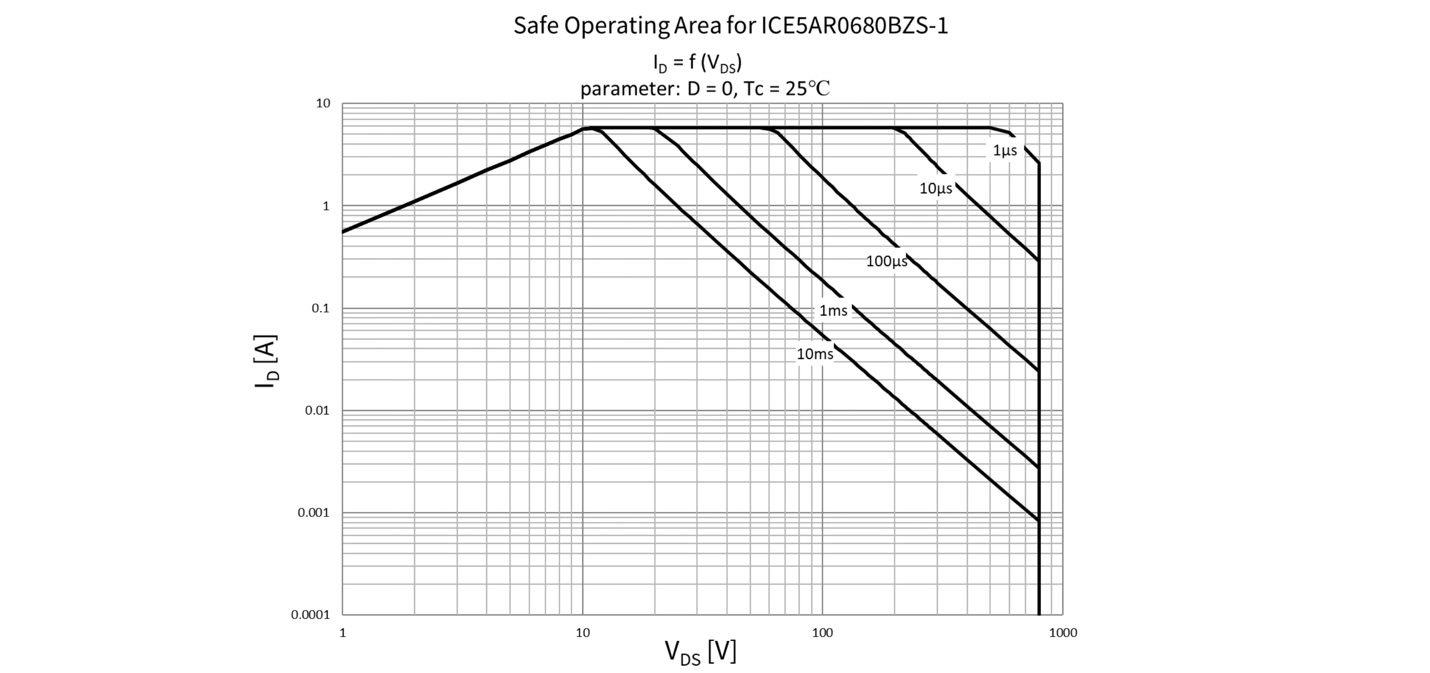


Figure 19 Safe Operating Area (SOA) curve for ICE5AR0680BZS-1

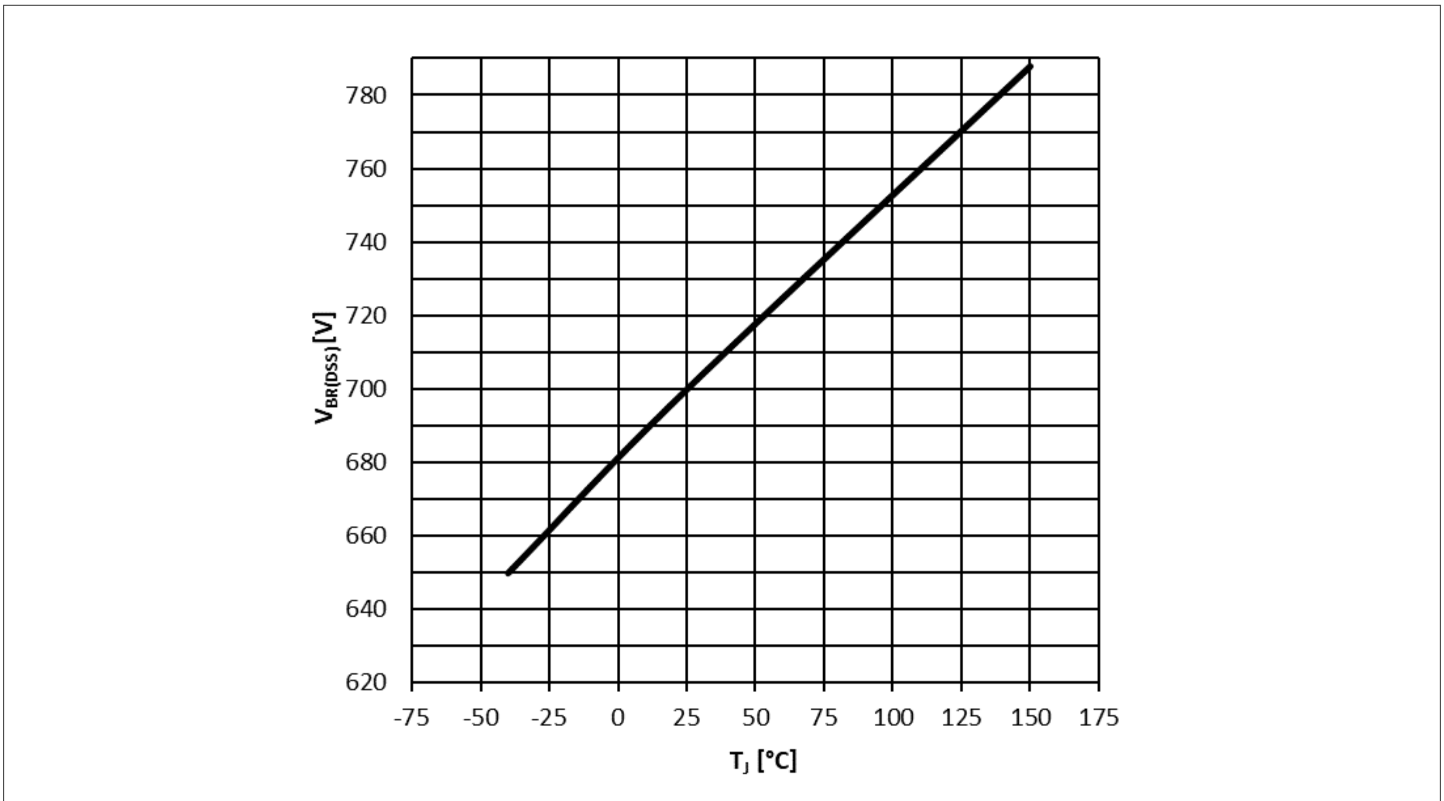


Figure 20 Drain-source breakdown voltage ICE5AR4770BZS-1; $V_{BR(DSS)}$=f(T_j), I_D=1 mA

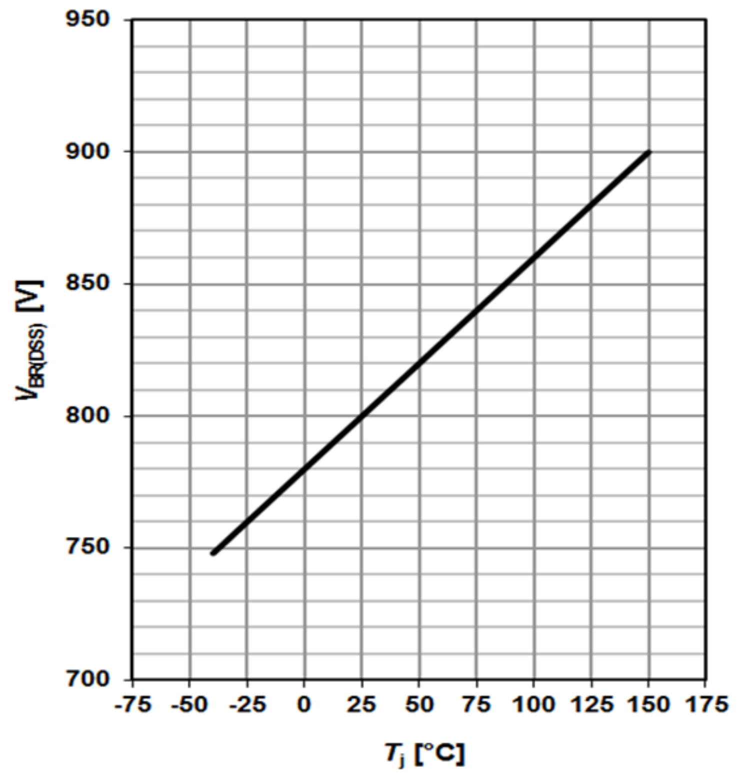


Figure 21 Drain-source breakdown voltage ICE5xRxx80BZ-1; $V_{BR(DSS)} = f(T_j)$, $I_D = 1$ mA

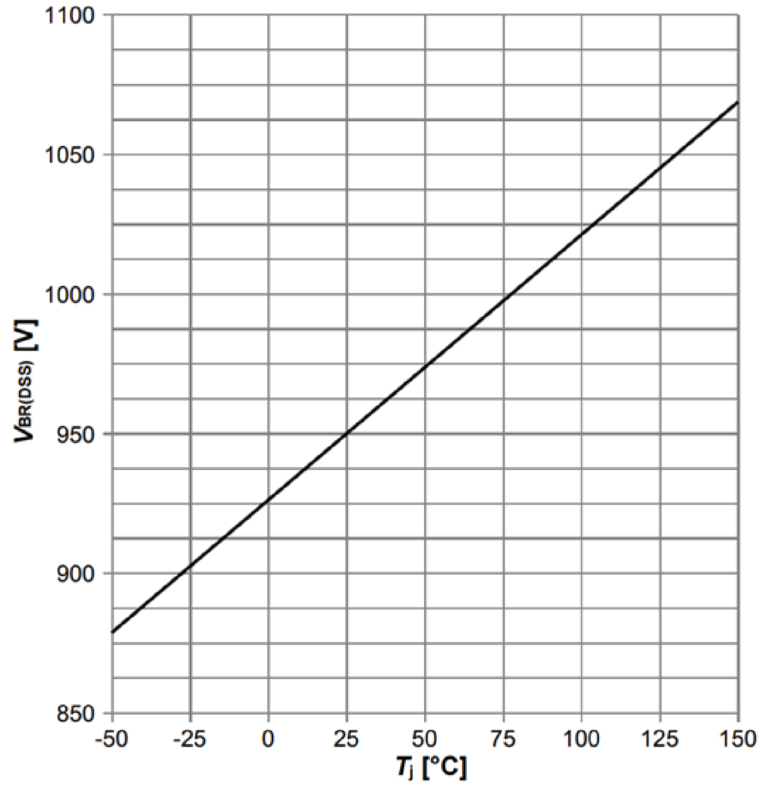


Figure 22 Drain-source breakdown voltage ICE5xR3995BZ-1; $V_{BR(DSS)} = f(T_j)$, $I_D = 1$ mA

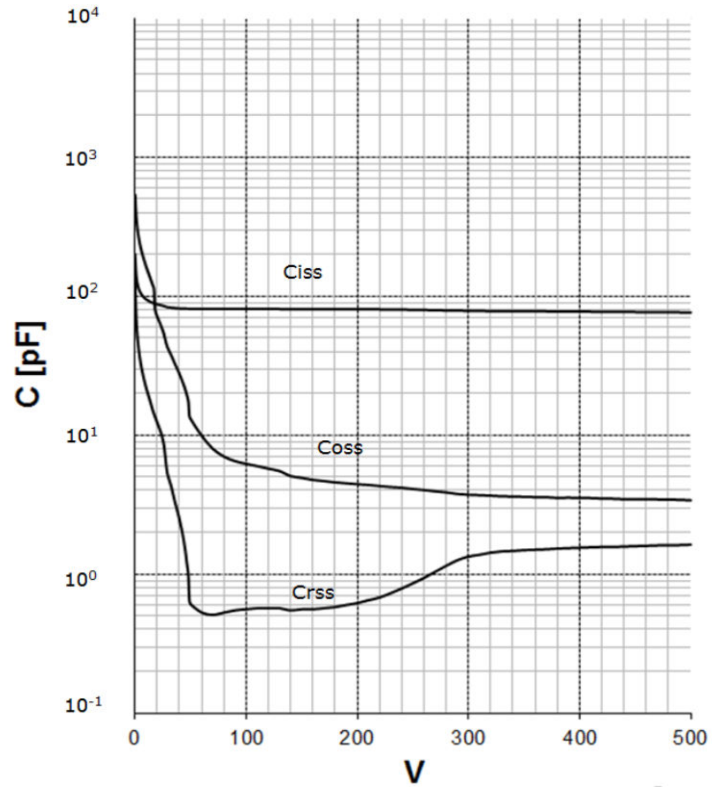


Figure 23 Typical CoolMOS™ capacitances of ICE5AR4770BZS-1; C = f(V_{DS}), (V_{GS} = 0 V; f = 1 MHz)

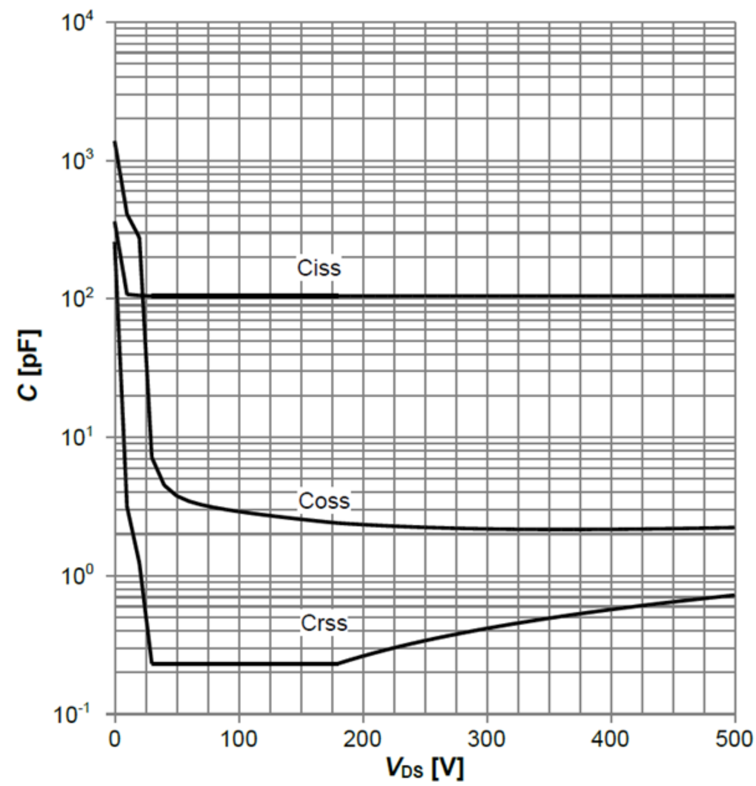


Figure 24 Typical CoolMOS™ capacitances of ICE5xR4780BZ-1; C = f(V_{DS}), (V_{GS} = 0 V; f = 250kHz)

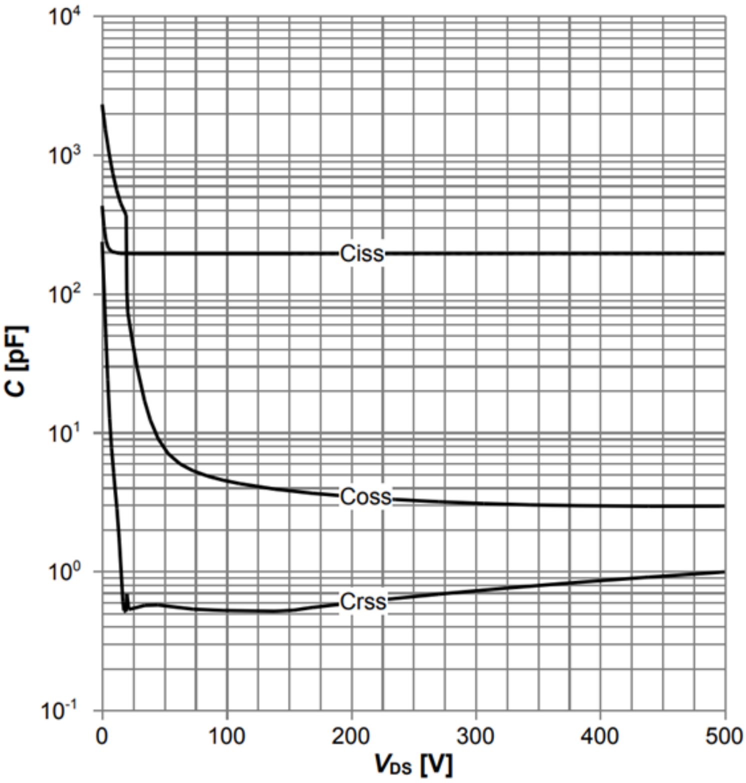


Figure 25 Typical CoolMOS™ capacitances of ICE5xR3995BZ-1; $C = f(V_{DS})$, (V_{GS} = 0 V; f = 250kHz)

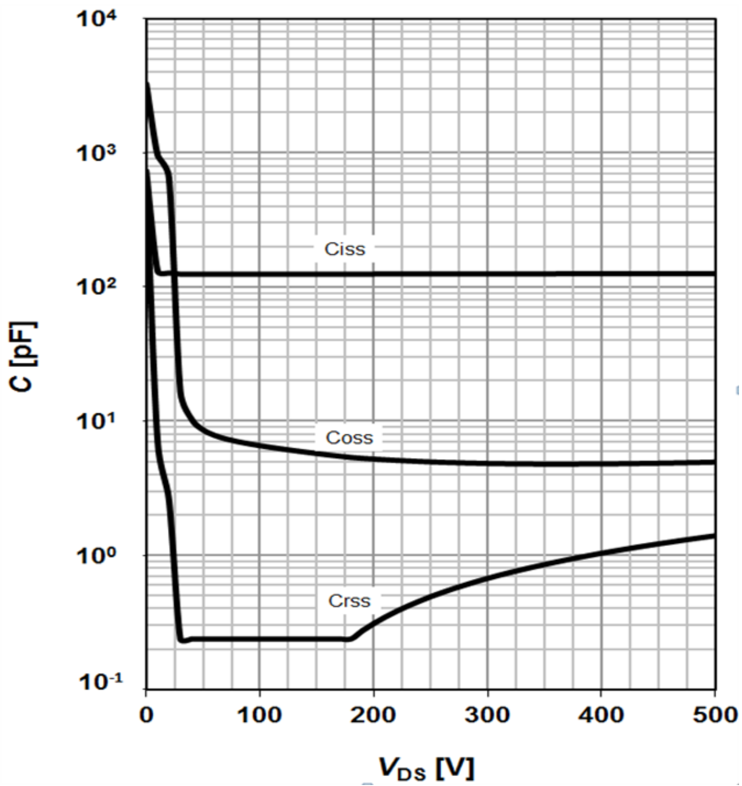


Figure 26 Typical CoolMOS™ capacitances of ICE5BR2280BZ-1; $C = f(V_{DS})$, (V_{GS} = 0 V; f = 250kHz)

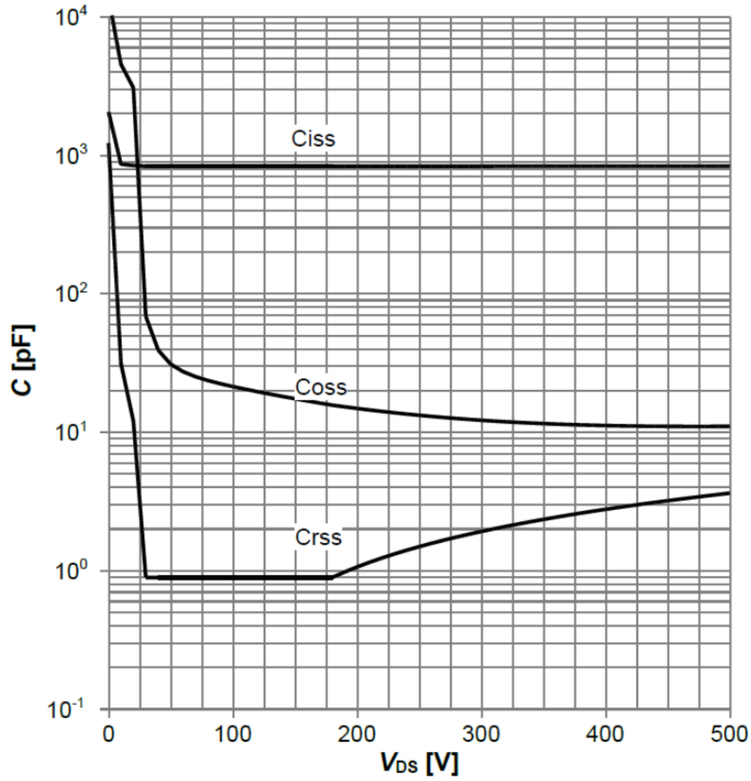


Figure 27 Typical CoolMOS™ capacitances of ICE5AR0680BZS-1; C = f(V_{DS}), (V_{GS} = 0 V; f = 250kHz)

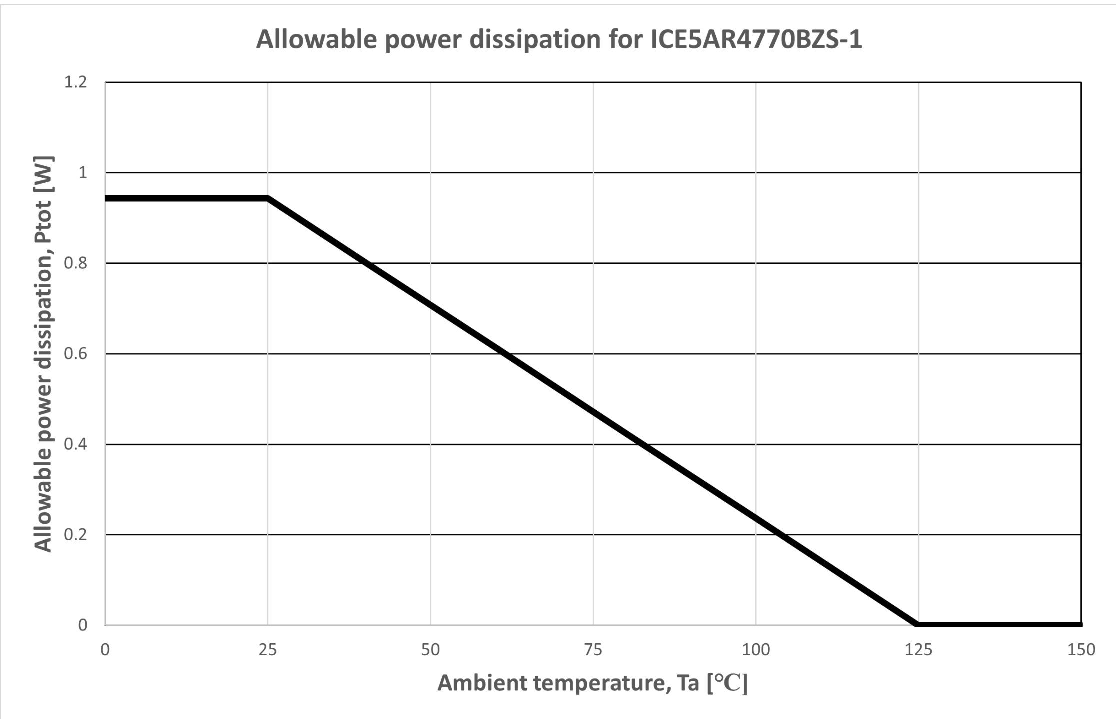


Figure 28 Power dissipation of ICE5AR4770BZS-1; P_{tot}=f(T_a), (Maximum ratings as given in section 6 must not be exceeded)

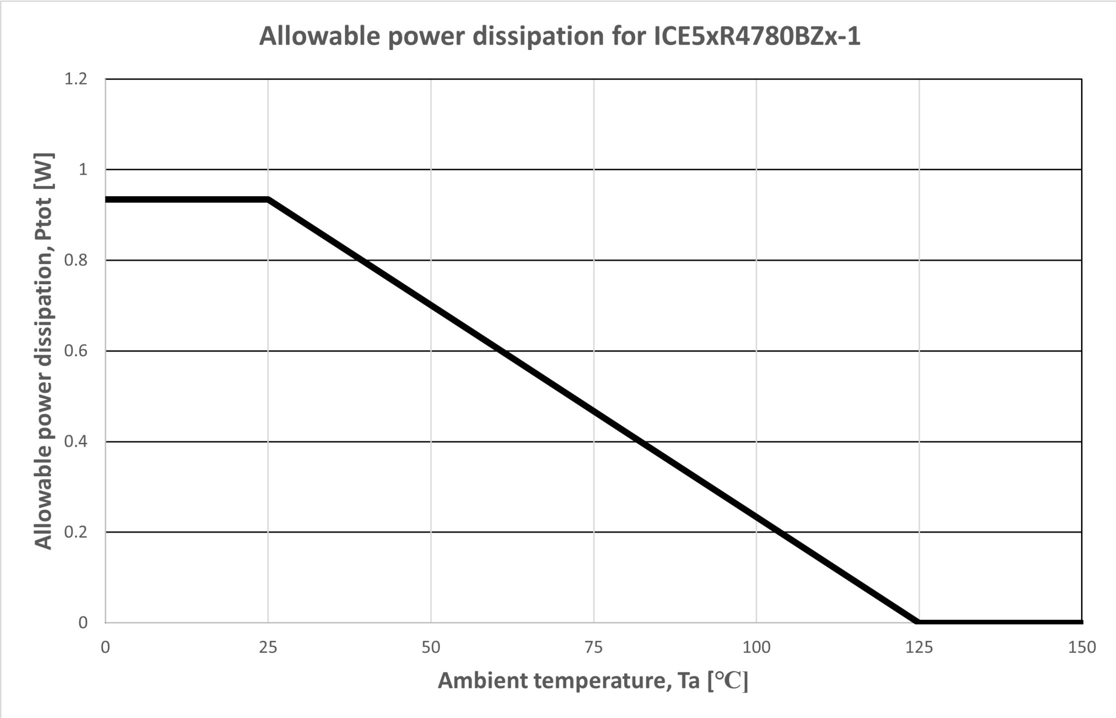


Figure 29 **Power dissipation of ICE5xR4780BZx-1; $P_{tot} = f(T_a)$ (Maximum ratings as given in chapter 6 must not be exceeded)**

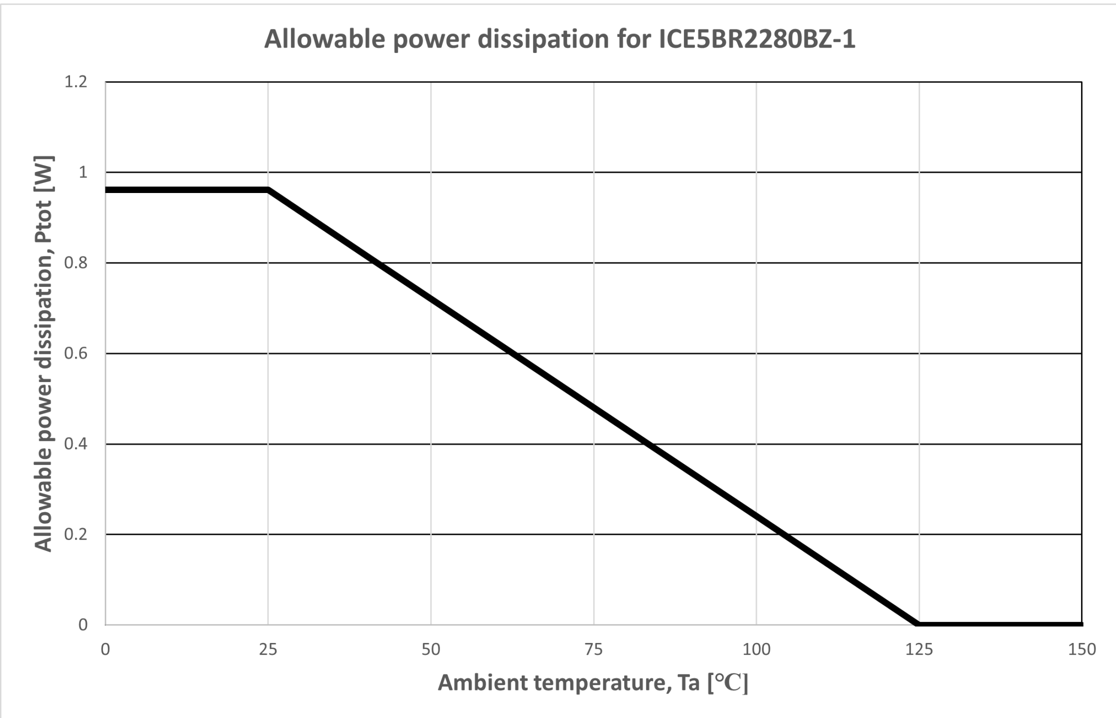


Figure 30 **Power dissipation of ICE5BR2280BZ-1; $P_{tot} = f(T_a)$ (Maximum ratings as given in chapter 6 must not be exceeded)**

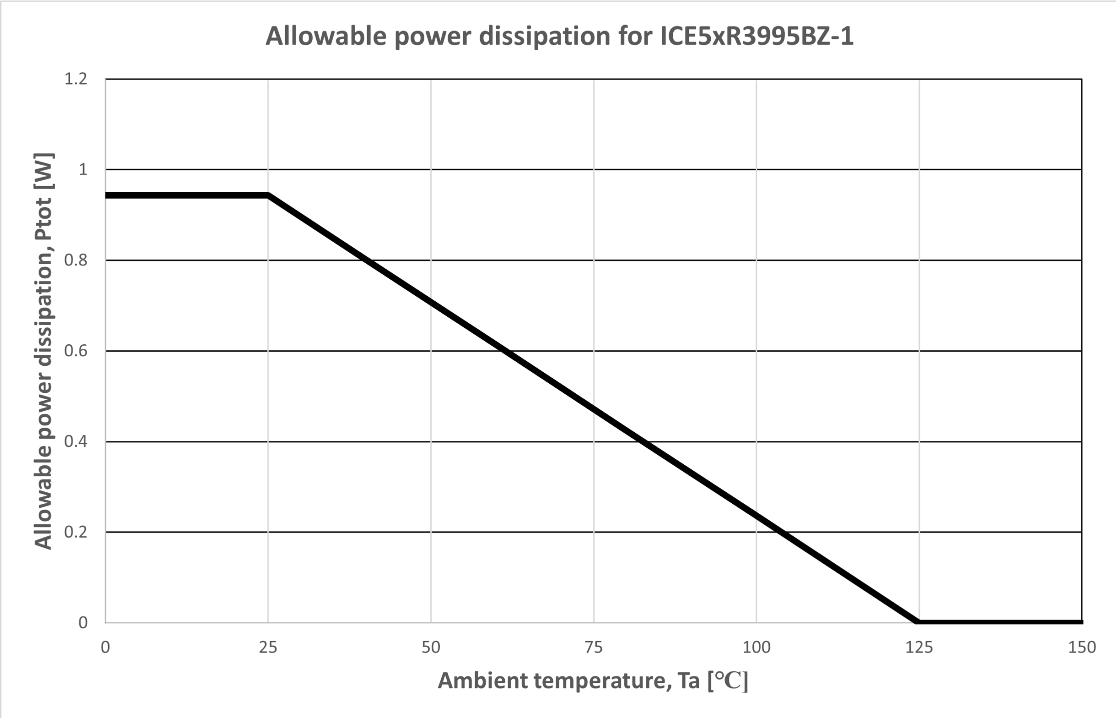


Figure 31 Power dissipation of ICE5xR3995BZ-1; $P_{tot} = f(T_a)$ (Maximum ratings as given in chapter 6 must not be exceeded)

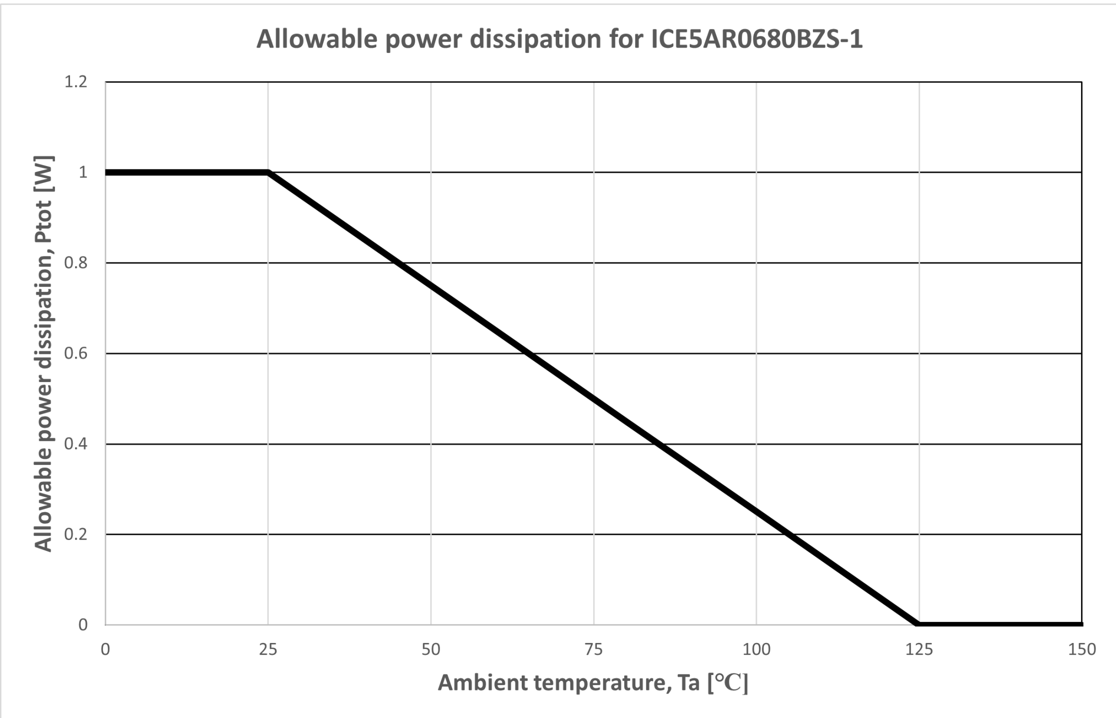


Figure 32 Power dissipation of ICE5AR0680BZS-1; $P_{tot} = f(T_a)$ (Maximum ratings as given in chapter 6 must not be exceeded)

6 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM/CCM flyback in an open frame design setting the maximum T_j of the integrated CoolMOS™ at 125°C, using minimum drain pin copper area in a 2 oz copper single-sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for selection purpose only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in chapter 4.1.

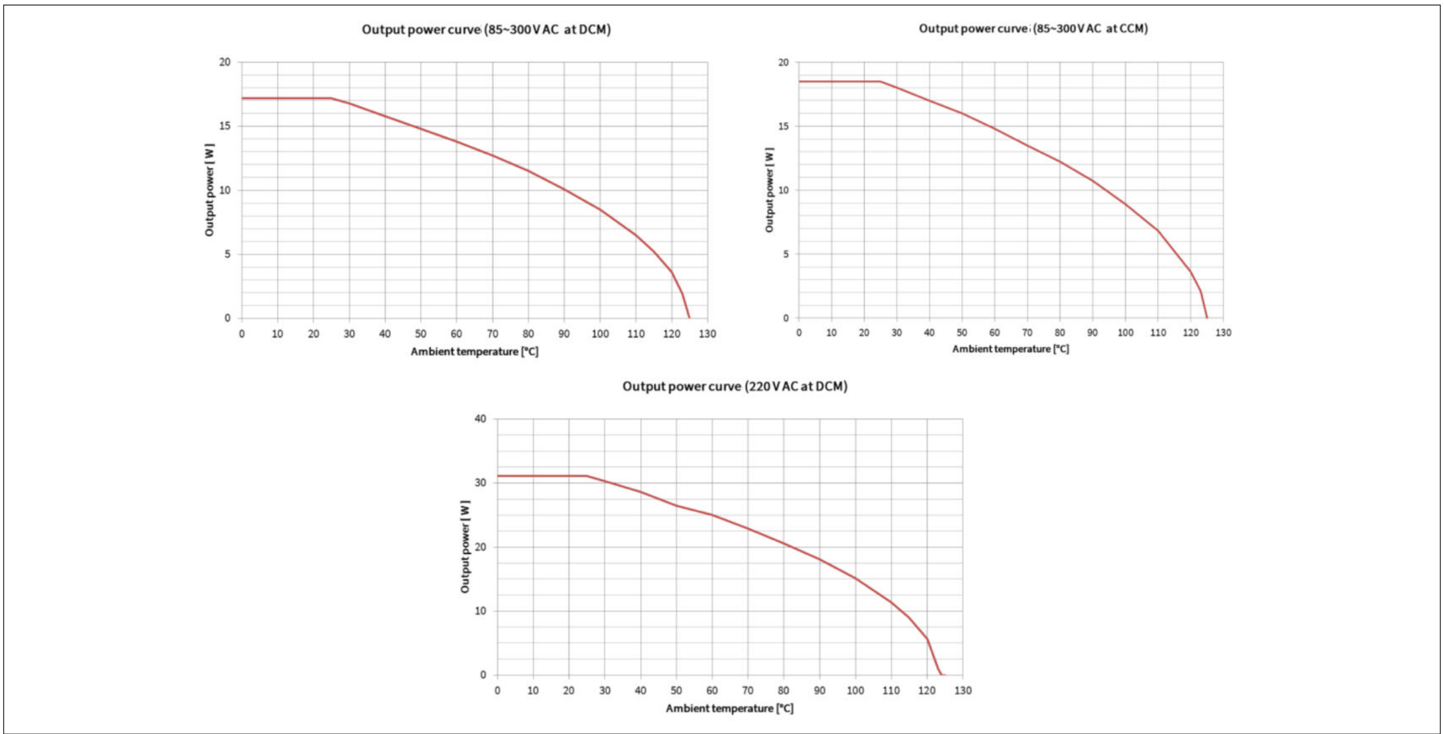


Figure 33 Output power curve of ICE5AR4770BZS-1

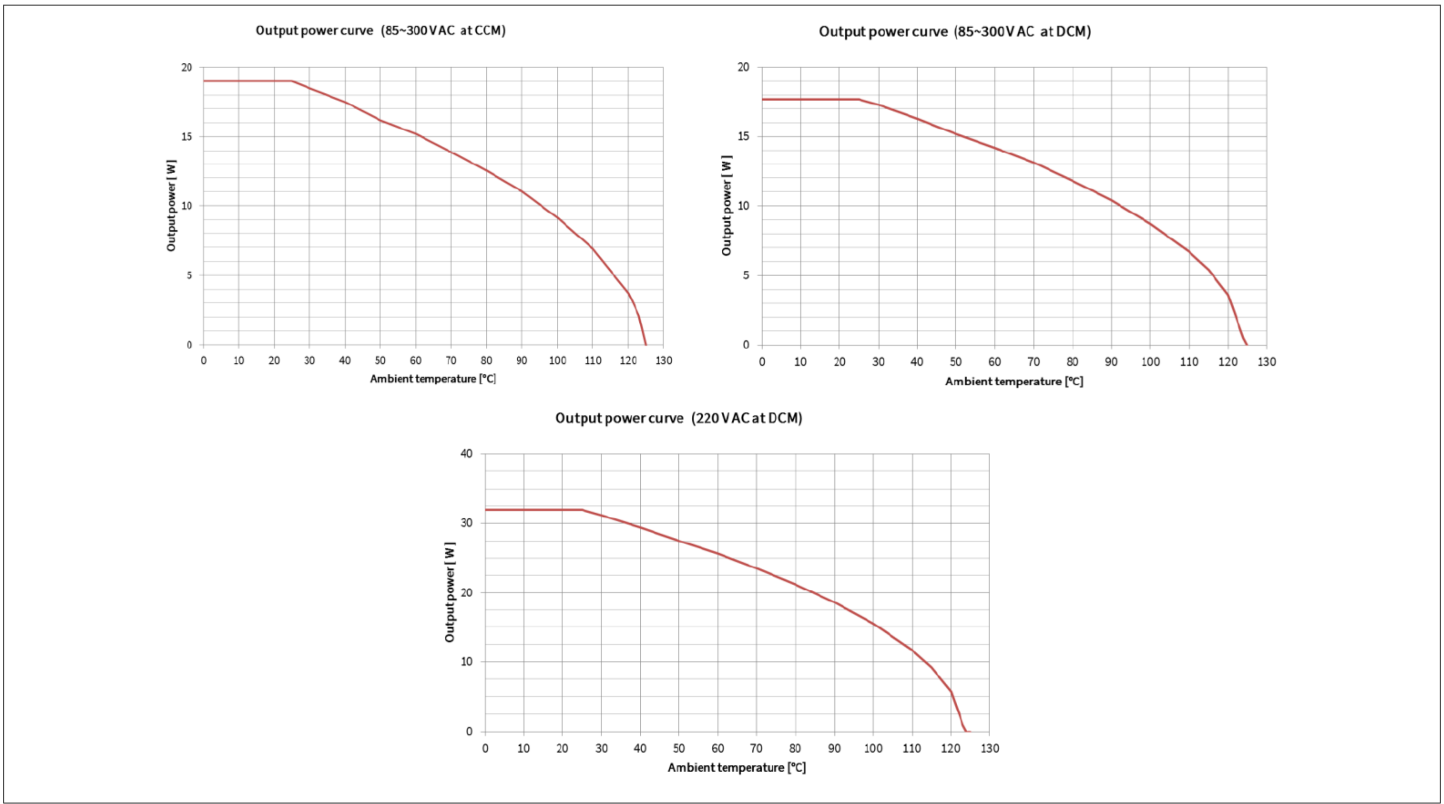


Figure 34 **Output power curve of ICE5xR4780BZx-1**

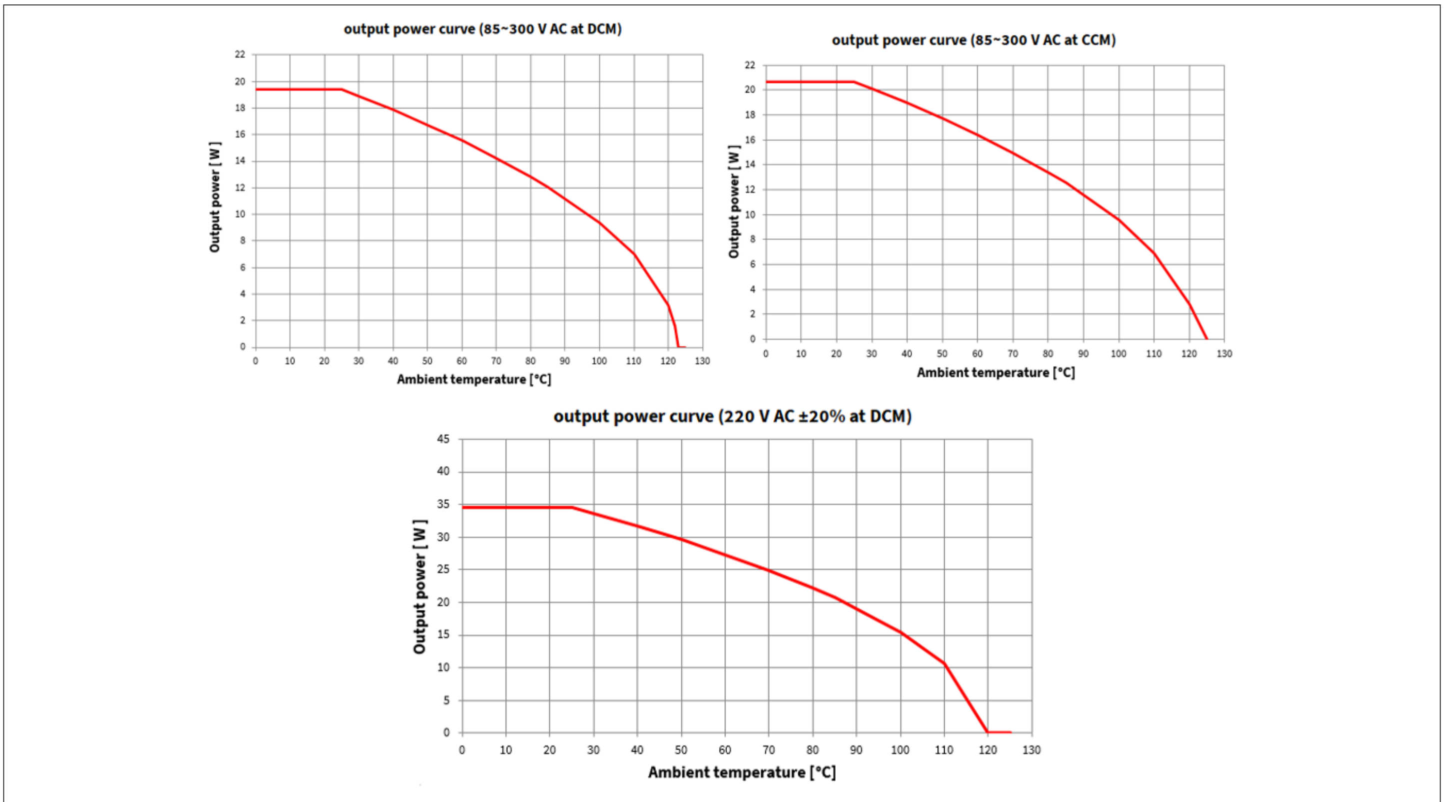


Figure 35 **Output power curve of ICE5xR3995BZ-1**

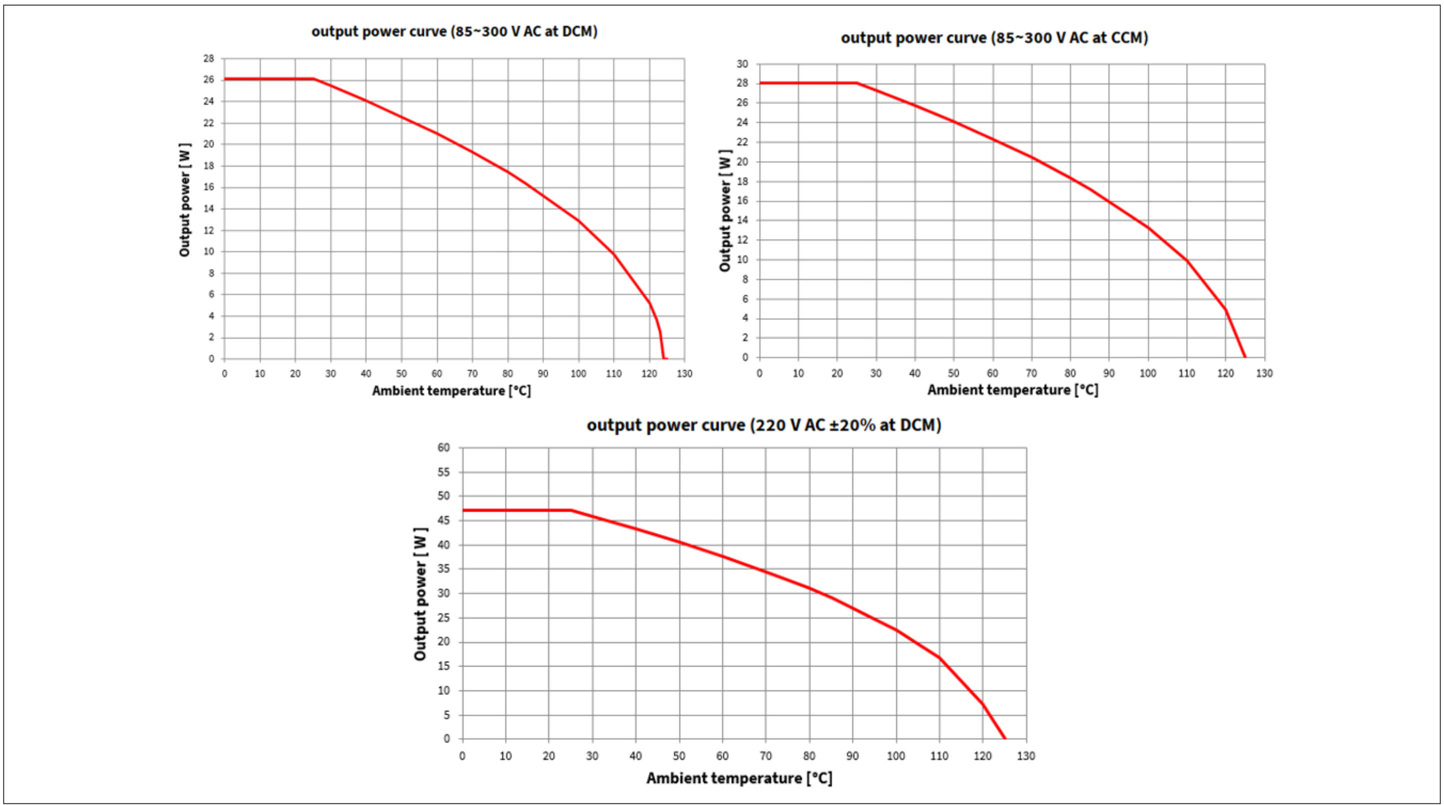


Figure 36 Output power curve of ICE5BR2280BZ-1

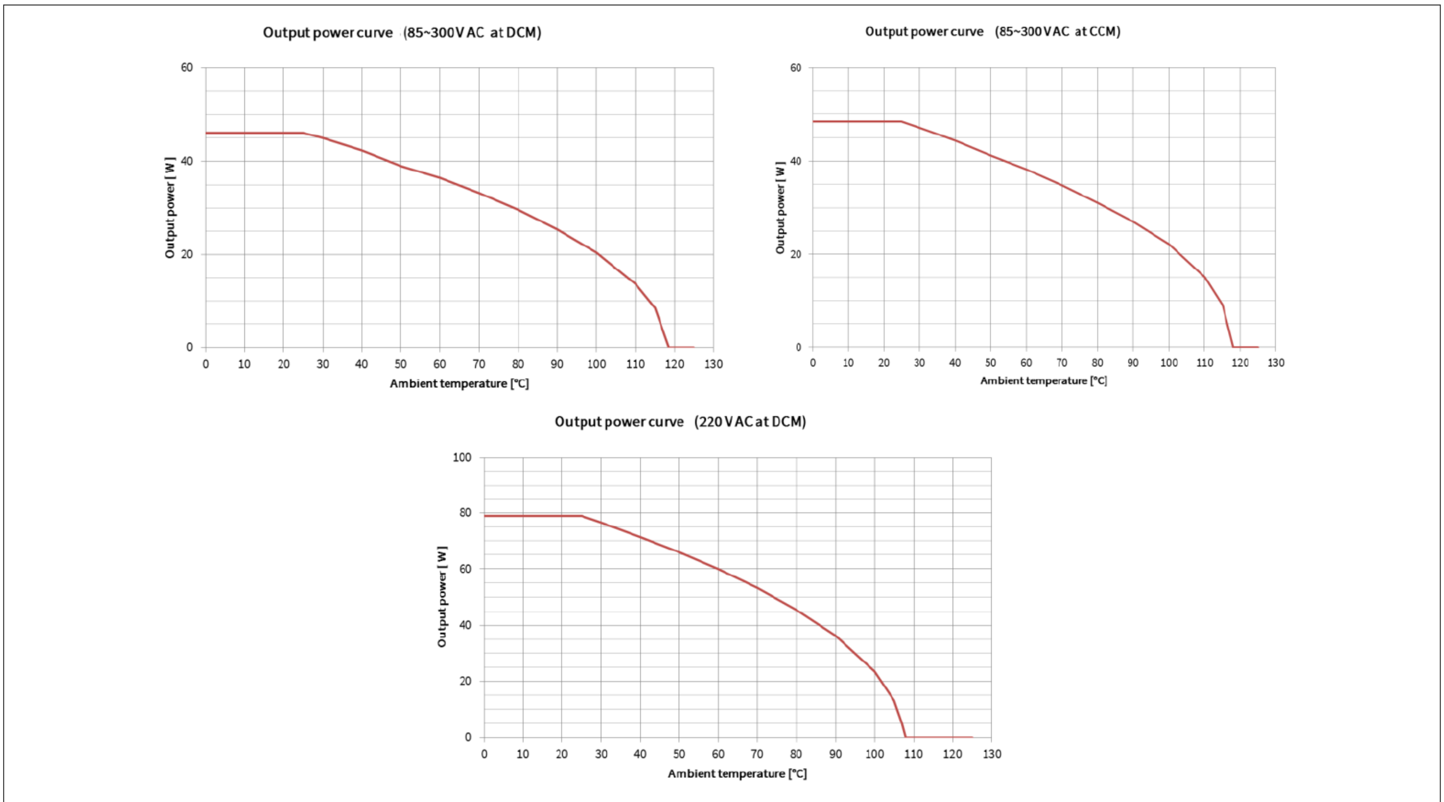


Figure 37 Output power curve of ICE5AR0680BZS-1

7 Output current curve

The calculated output current curves versus ambient temperature are shown below. The curves are derived based on an open-frame design at T_a = 50°C, T_j = 125°C (integrated HV MOSFET for CoolSET™), using the minimum 100 mm^2 drain pin copper area in a 2 oz copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output current figure is for selection purposes only. The actual current can vary depending on the specific design.

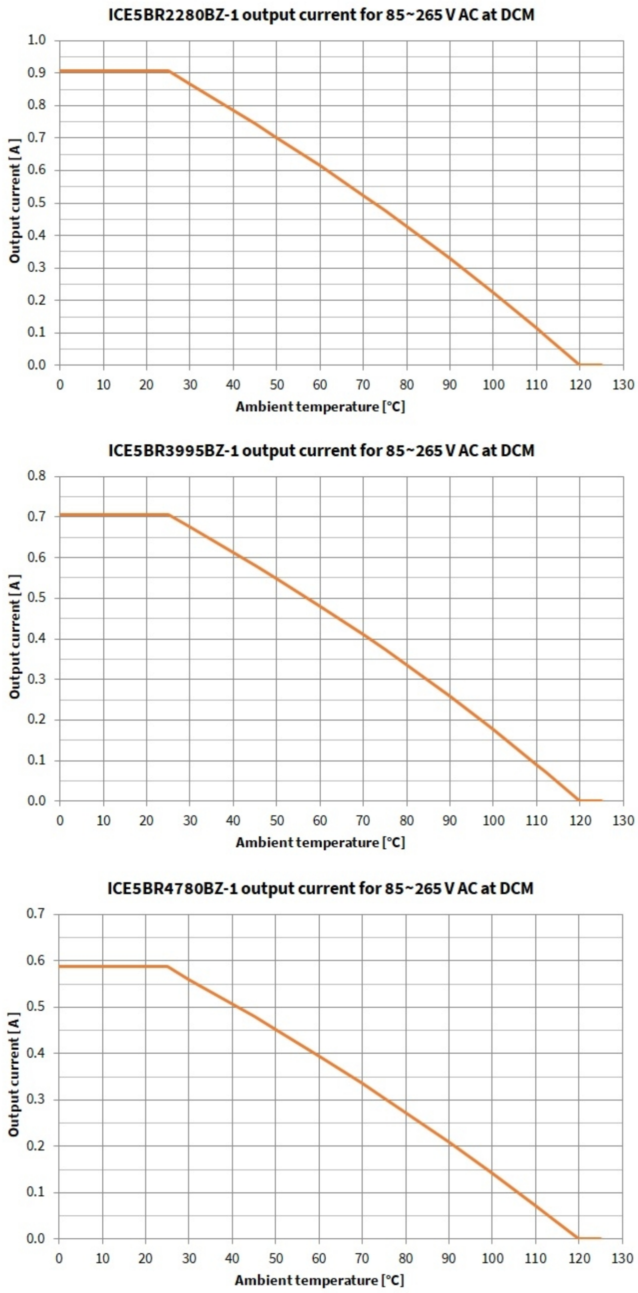
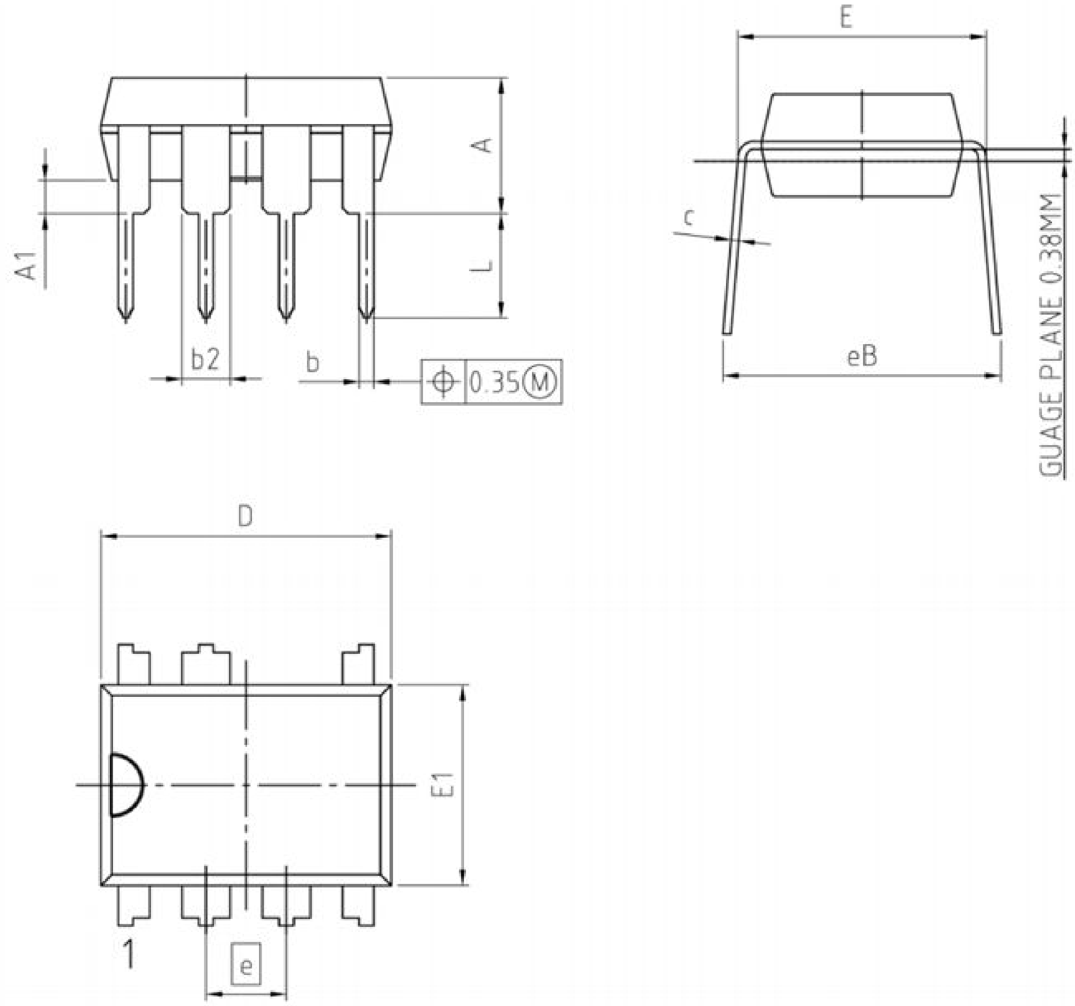


Figure 38 Output current curve

8 Package information



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.57	-	0.180
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.70	-	0.067
c	0.20	0.36	0.008	0.014
D	9.10	9.77	0.358	0.385
E	7.49	8.26	0.295	0.325
E1	6.10	6.60	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	7		7	
eB	7.90	10.90	0.311	0.429
L	2.92	-	0.115	-

DOCUMENT NO.
Z8B00155542

SCALE
0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
22.07.2011

REVISION
02

Figure 39 **Package information**

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e., Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

8.1 Marking

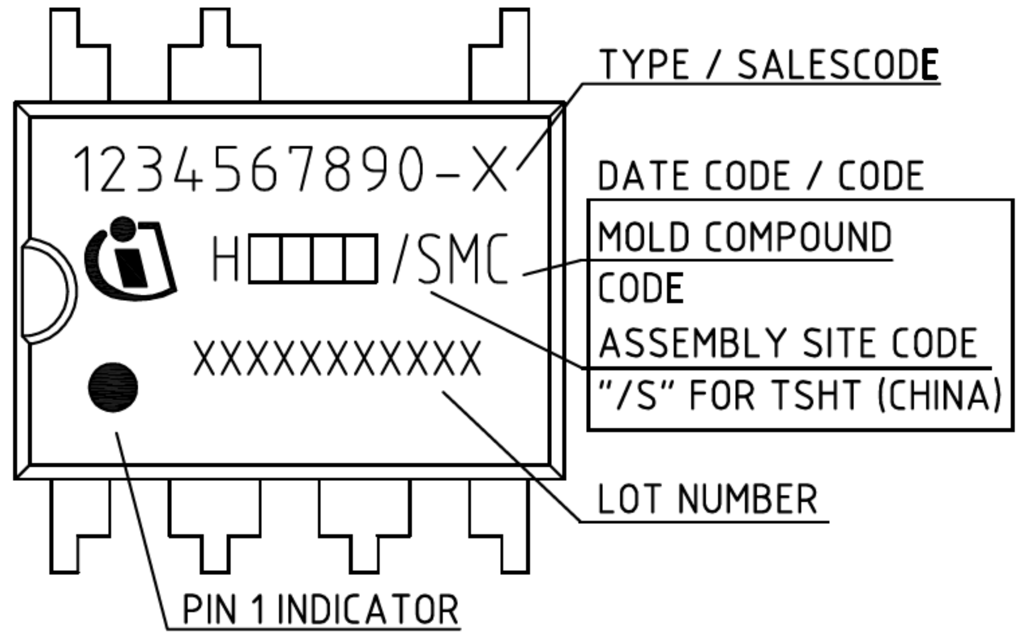


Figure 40 **Marking on package PG-DIP-7-10**

9 Revision history

Revision	Date	Changes
Rev 1.0	12 Aug 2024	First release

Trademarks

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Edition 2024-08-12

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-drl1687448856163