

Automotive MOSFET

OptiMOS™ 7 Power-Transistor



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL2 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential Applications

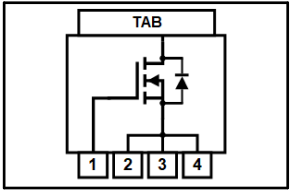
General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	40	V
$R_{DS(on)}$	1.14	mΩ
I_D (chip limited)	270	A



Type	Package	Marking
IAUMN04S7N011G	PG-HSOG-4-1	7N04N011



Table of Contents

Description	1
Maximum ratings	3
Thermal characteristics.....	4
Electrical characteristics.....	4
Electrical characteristics diagrams.....	6
Package outline & footprint	10
Revision history.....	11
Disclaimer.....	12

Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS} = 10\text{ V}$, Chip limitation ^{1,2)}	270	A
		$V_{GS} = 10\text{ V}$, DC current	150	
		$T_a = 100^\circ\text{C}$, $V_{GS} = 10\text{ V}$, R_{thJA} on 2s2p ^{2,3)}	38	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C = 25^\circ\text{C}$, $t_p = 100\text{ }\mu\text{s}$	750	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D = 65\text{ A}$	133	mJ
Avalanche current, single pulse	I_{AS}	–	130	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	124	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	$^\circ\text{C}$

Thermal Characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	1.21	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}	–	–	23.7	–	

Electrical Characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static Characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	2.2	2.6	3.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$	–	–	1	μA
		$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 100^\circ\text{C}^{2)}$	–	–	13	
Gate-source leakage current	I_{GSS}	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 7\text{ V}$, $I_D = 38\text{ A}$	–	1.10	1.27	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 75\text{ A}$	–	0.95	1.14	
Gate resistance ²⁾	R_G	–	–	1.56	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics ²⁾						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	–	3580	4654	pF
Output capacitance	C _{oss}		–	2091	2719	
Reverse transfer capacitance	C _{rss}		–	89	134	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, V _{GS} = 10 V, I _D = 75 A, R _G = 3.5 Ω	–	7	–	ns
Rise time	t _r		–	6	–	
Turn-off delay time	t _{d(off)}		–	19	–	
Fall time	t _f		–	12	–	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD} = 20\text{ V}, I_D = 75\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$	–	15	20	nC
Gate to drain charge	Q_{gd}		–	11	17	
Gate charge total	Q_g		–	52	68	
Gate plateau voltage	$V_{plateau}$		–	4.2	–	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C = 25^\circ\text{C}$	–	–	150	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C = 25^\circ\text{C}, t_p = 100\ \mu\text{s}$	–	–	750	
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = \text{None A}, T_J = 25^\circ\text{C}$	–	0.8	0.95	V
Reverse recovery time ²⁾	t_{rr}	$V_R = 20\text{ V}, I_F = 50\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$	–	37	55	ns
Reverse recovery charge ²⁾	Q_{rr}		–	20	41	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

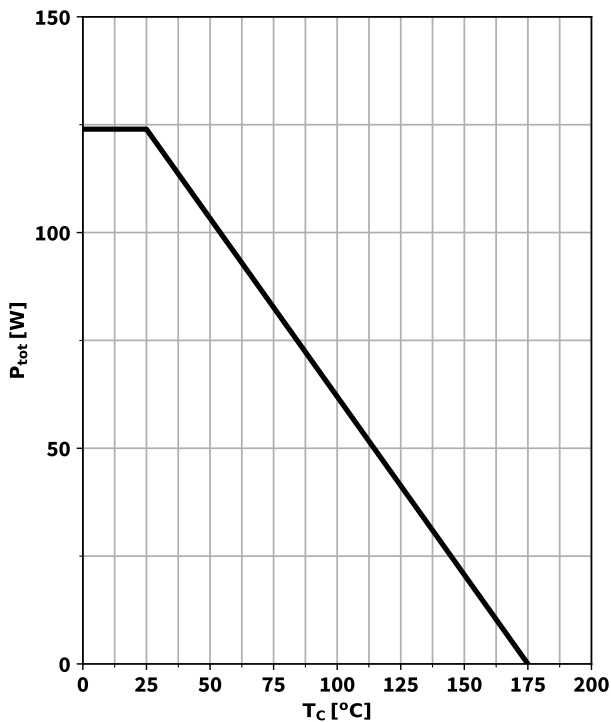
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

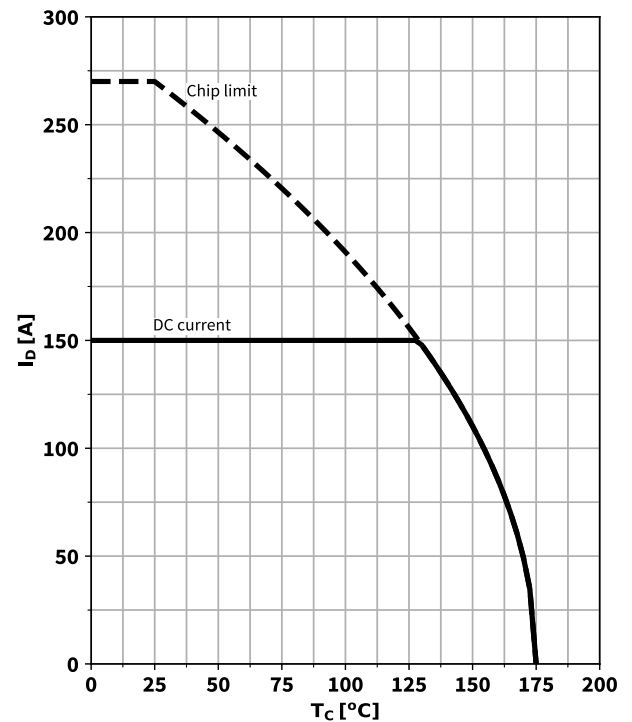
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



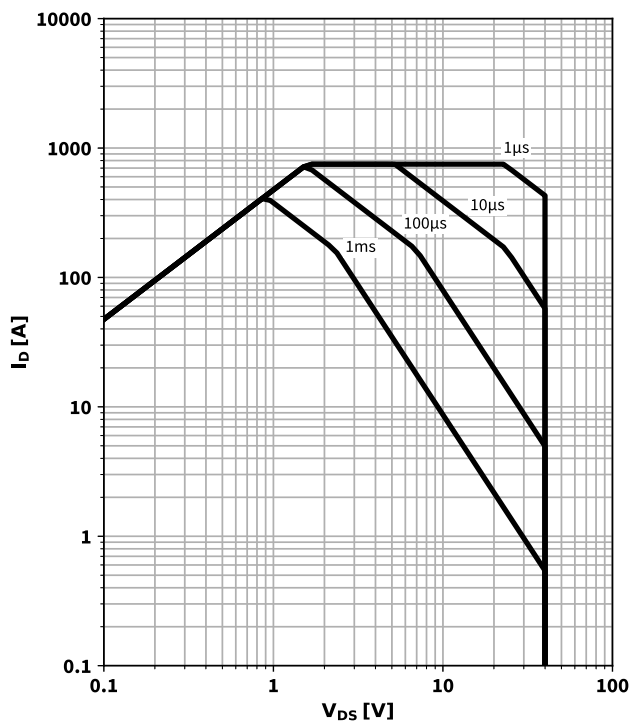
2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



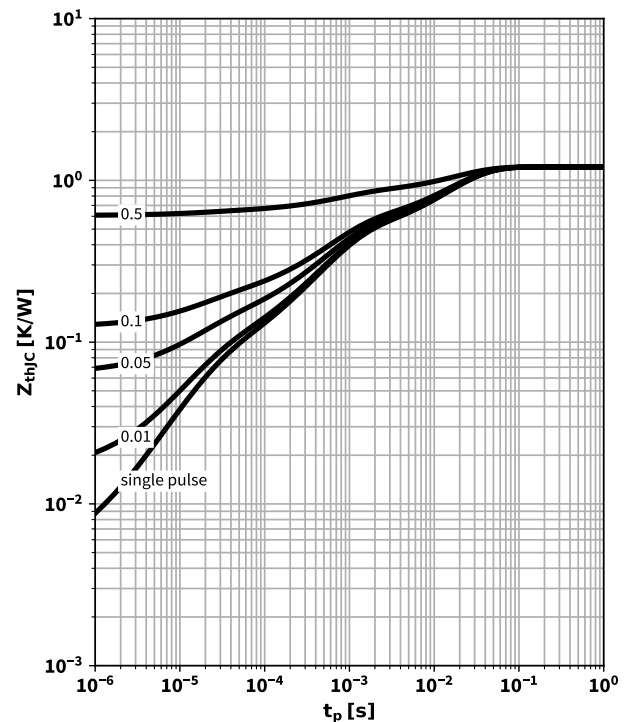
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^{\circ}\text{C}; D = 0; \text{parameter: } t_p$$



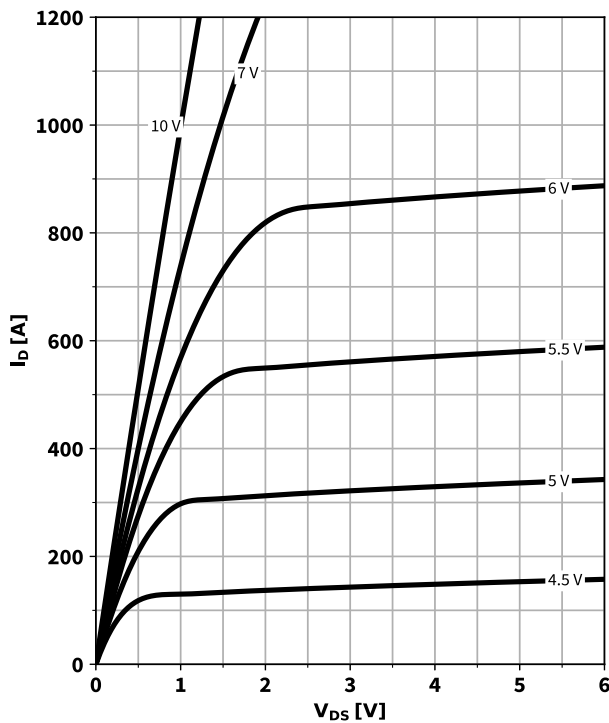
4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



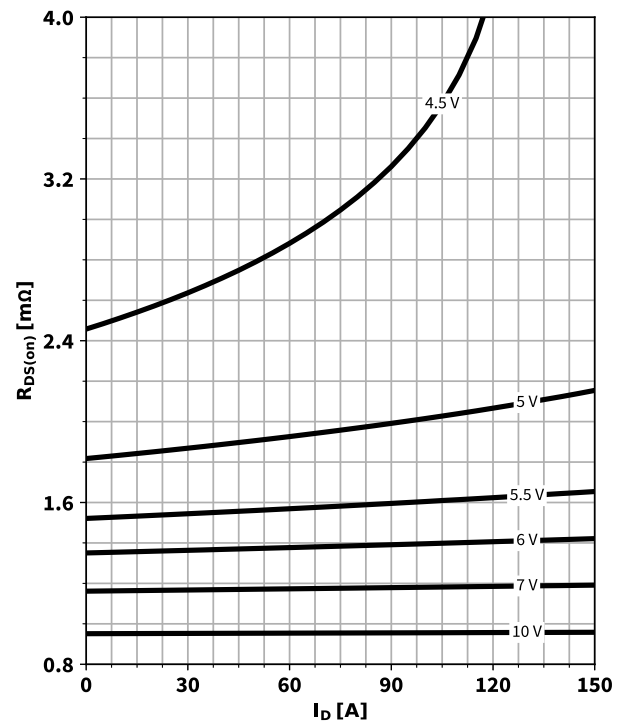
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



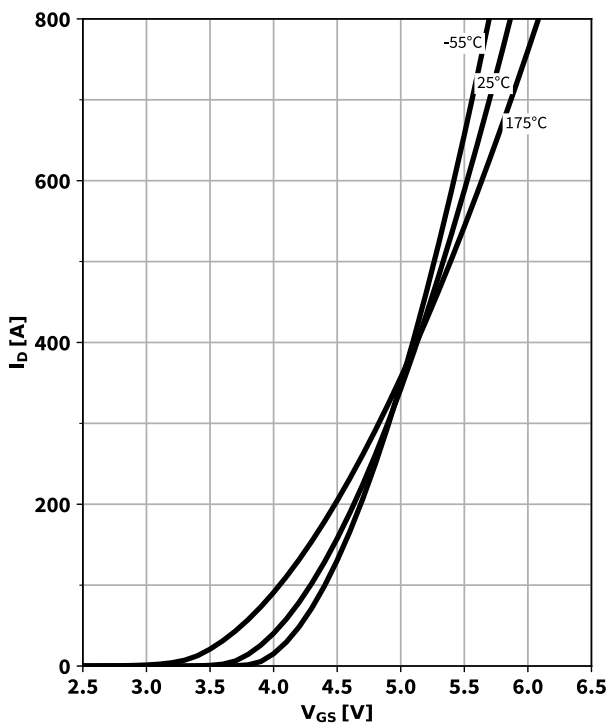
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



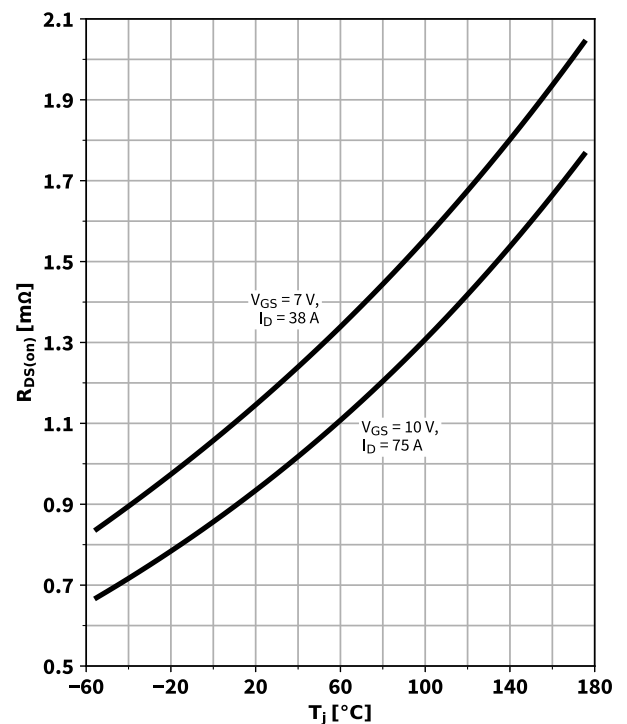
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$



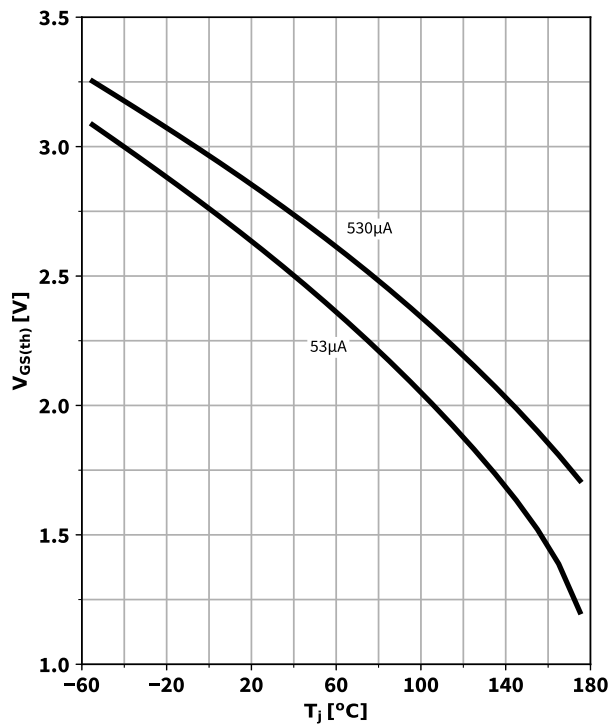
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



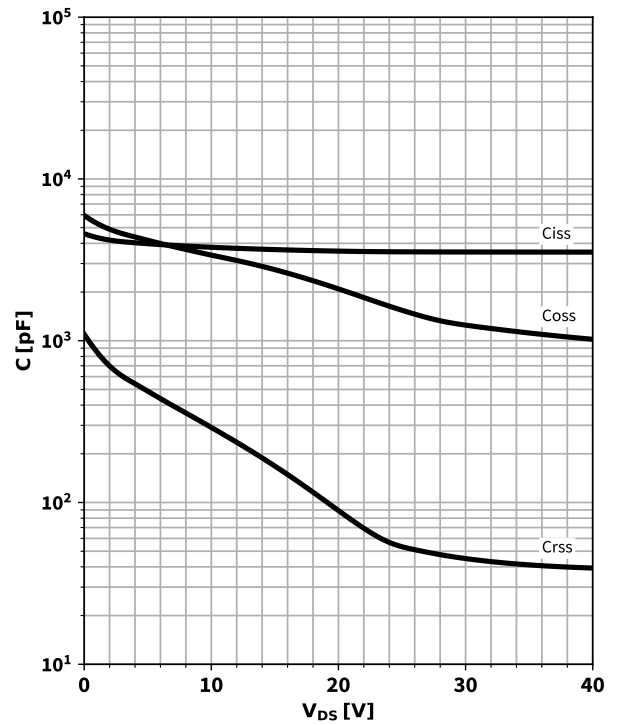
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



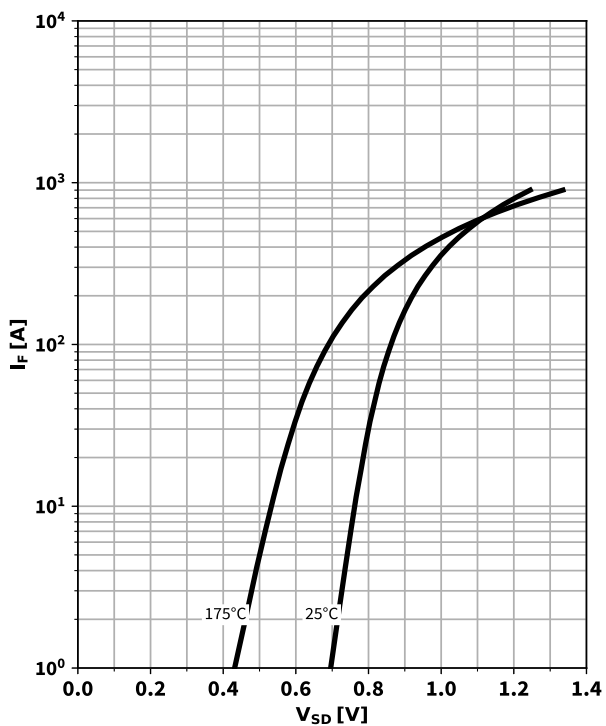
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0 V$; $f = 1 MHz$



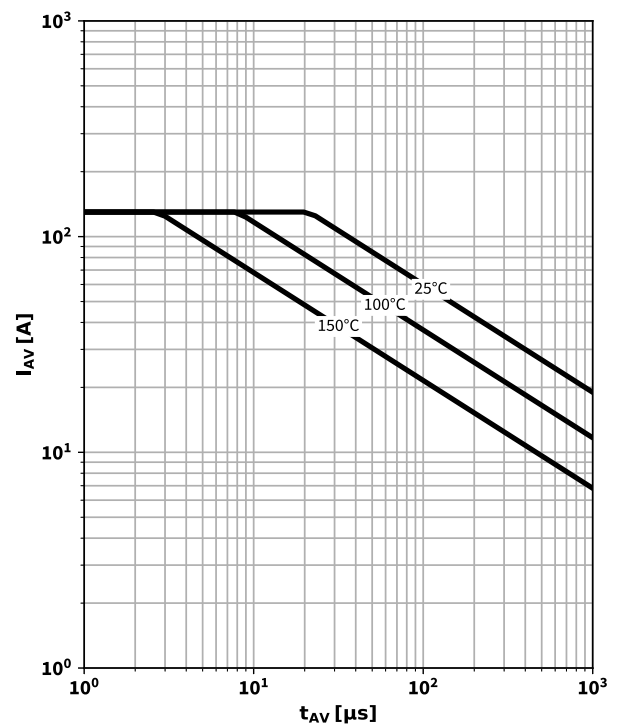
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



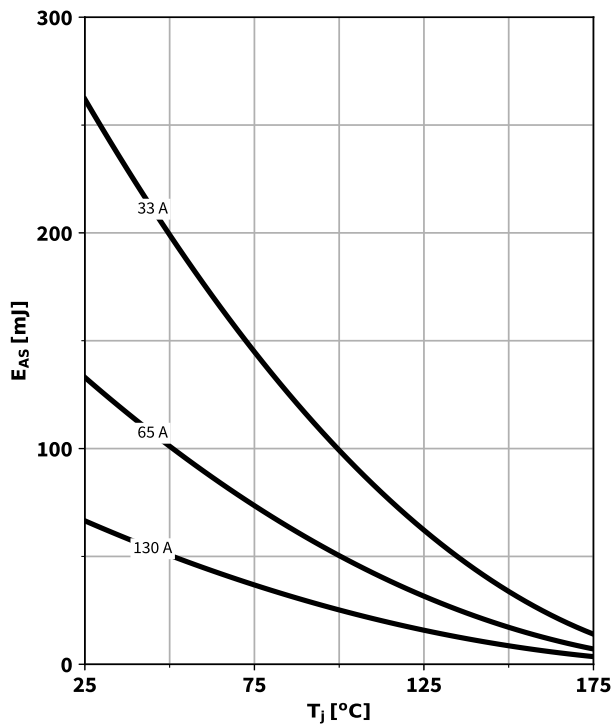
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



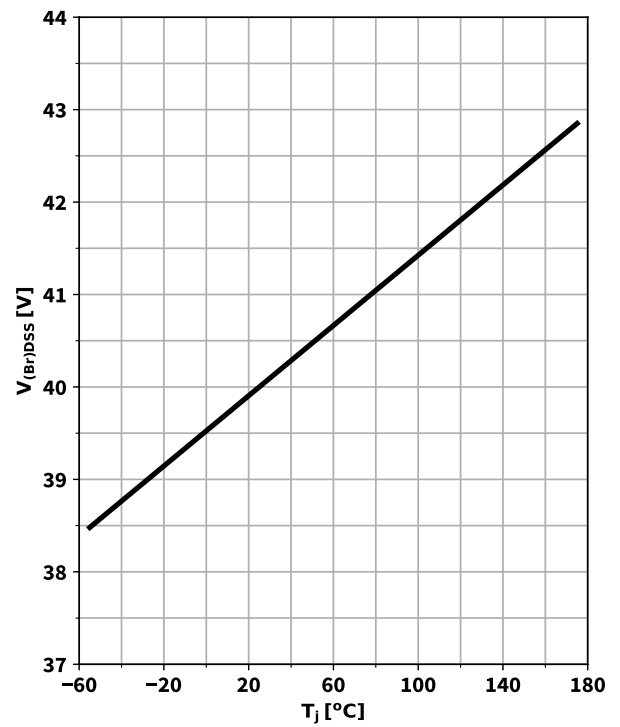
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



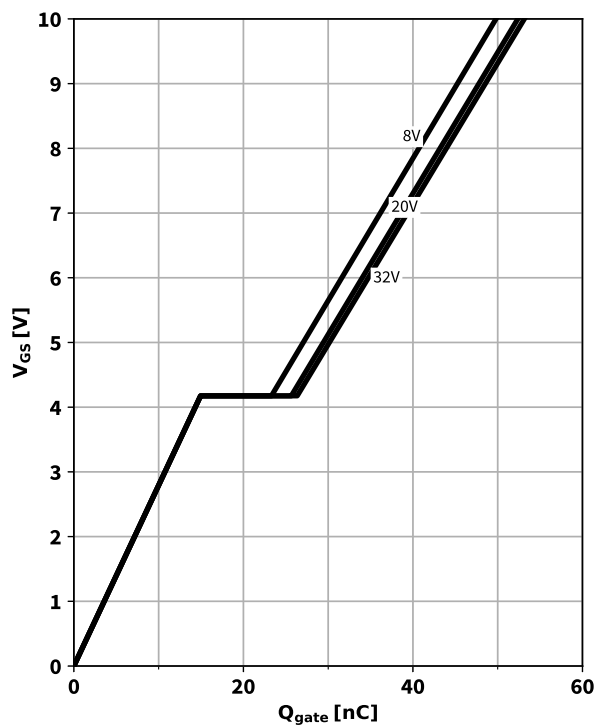
14 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$; $I_D = 1$ mA



15 Typ. gate charge

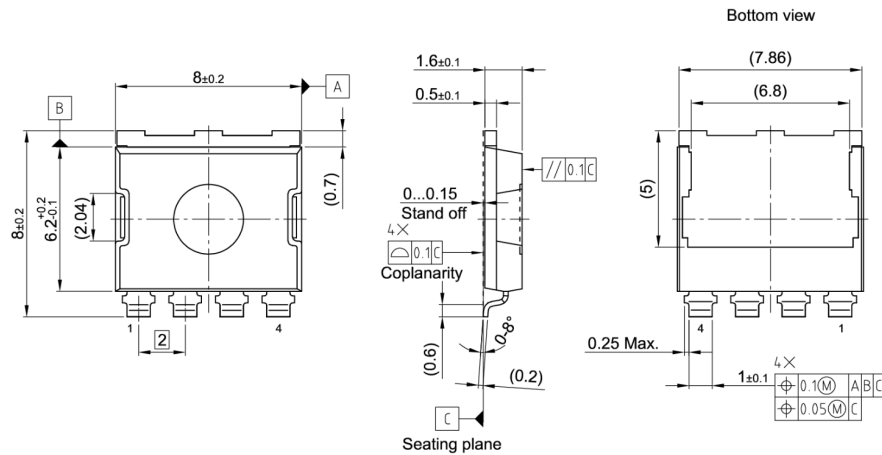
$V_{GS} = f(Q_{gate})$; $I_D = 75$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

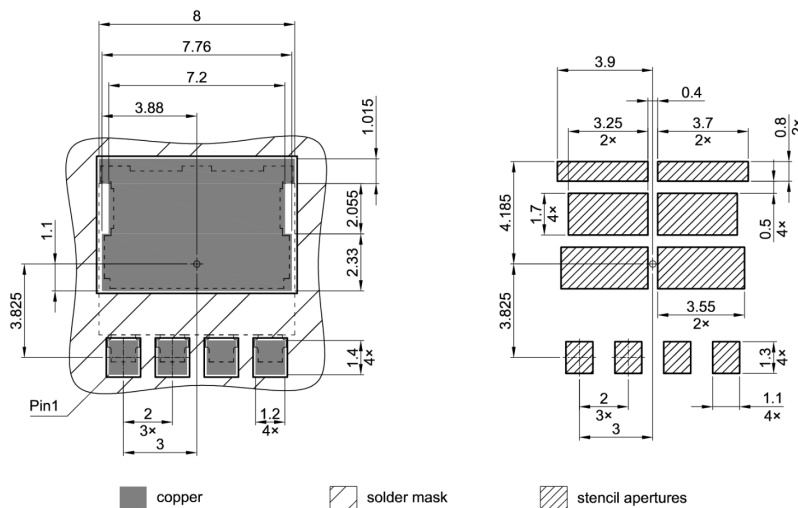


Package Outline



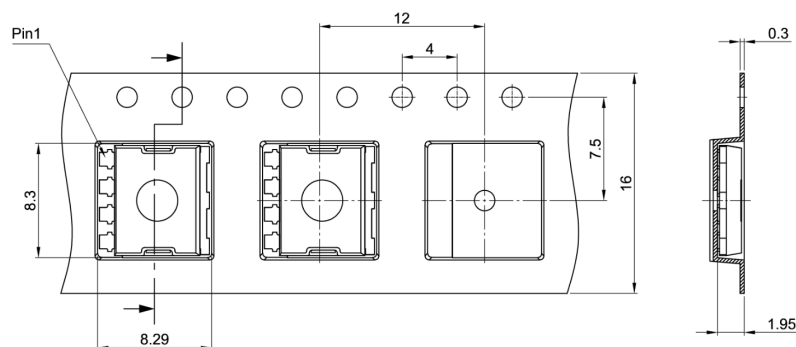
All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥] [⊙]
 Drawing according to ISO 8015, general tolerances ISO 2768-mK

Footprint



All dimensions are in units mm
 All pads are non-solder mask defined

Packaging



All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥] [⊙]



Revision History

Revision	Date	Changes
Revision 1.0	2024-04-05	Final Data Sheet

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Edition 2024-04-05

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

IAUMN04S7N011G-Data-Sheet-10-Infineon

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